PITHA 94/45

SCAN-9508264

CERN LIBRARIES, GENEVA

SCW 9535

DC and Noise Performance of C-HFET Transistors at Low Drain Current Densities

W. Karpinski, K. Lübelmeyer , G. Pierschel,
C. Rente, F. Tenbusch

PHYSIKALISCHE INSTITUTE
RWTH AACHEN
Sommerfeldstr.
52056 AACHEN, GERMANY

DC and Noise Performance of C-HFET Transistors at Low Drain Current Densities**

W. Karpinski, K. Lübelmeyer*, G. Pierschel, C. Rente, F. Tenbusch

I. Physikalisches Institut RWTH Aachen, 52056 Aachen Germany

ABSTRACT

The results of measurements of Complementary Heterostructure Field Effect Transistors (C-HFET) are reported. We have investigated the DC, AC and noise parameters of the devices as a function of the operating conditions. In particular, we analysed their behaviour in the low power region at drain current densities less than 2 mA/mm and drain bias voltages less than 2 V. It is shown that the transistors have excellent amplification in this region. We found that the dominant $1/f$ noise, if measured as an equivalent noise charge on the input gate, is independent of the drain current and the drain bias voltage. Furthermore, the data show that the white serial noise increases with decreasing drain current density and becomes a significant noise source at peaking times less than 25 ns and drain current densities less than 1 mA/mm only. An extrapolation of the measurements shows that the total ENC of a C-HFET input transistor with 25 μm gate-width and 3 μW power dissipation will be about 25 electrons at zero detector capacitance with a slope $\Delta(\text{ENC})/\Delta C_{\text{det}}$ around 440 electrons/pF.

1. INTRODUCTION

The excellent radiation hardness of C-HFET devices [1], [2] has prompted us to further investigate their behaviour at low drain currents and low drain bias voltages, these being the conditions appropriate for low power amplifiers. To this purpose we ordered from Honeywell Technology Centre (HTC) 40 bare dice, each containing one C-HFET operational amplifier with 330 μm gate-width input transistors and discrete n-type FETs with gate-widths of 10, 100, and 330 (2x) μm . All 40 dice came from the same process lot, #5379-1. The dice were split into two groups each consisting of 20 pieces. The 20 dice labelled „A“ came from wafer #12 and the 20 dice labelled „T“ came from wafer #7.

There are the following differences between the wafers:

- The p-channel FET threshold voltage on wafer „T“ is -0.3V and on wafer „A“ -0.7V.
- Wafer „A“ has a new type of buffer between the heterostructure and the substrate.
- The nominal transistor gate length on wafer „T“ is 0.65 μm and on wafer „A“ 0.85 μm .

For purposes of identification we labelled each transistor by the wafer type, followed by the serial number of the die and the width of the gate of the transistor.

2. TRANSISTOR DC PARAMETERS

The architecture and the operation of the C-HFET have been discussed elsewhere [3], [4], [5]. We measured the DC transistor

*Corresponding author.

**Supported by The German Bundesministerium für Forschung und Technologie under contract number 056AC11P.

parameters (at room temperature) using a semiconductor parameter analyser HP4145A. The following measurements were carried out:

- drain current vs. drain-source and gate-source voltage: (i_d - V_{ds}), (i_d - V_{gs}) characteristics and
- gate current vs. gate-source voltage: (i_g - V_{gs}) characteristics.

We measured the devices over the whole operating region of i_d up to 200 mA/mm but we present the results only at low drain current densities (<4 mA/mm) appropriate for low power preamplifiers. Fig. 1 shows the i_d vs. V_{ds} characteristics and demonstrates that the transistors have an excellent behaviour in this operating region, free from „kink“ effects and other anomalies. We observe also that the drain current saturates at quite small values ($V_{ds} \sim 0.2$ V) of the drain-source voltage. The (i_d - V_{gs}) characteristics are shown in Fig. 2. We notice that in the threshold region (0.1V - 0.3V) the drain current density varies approximately exponentially with the gate voltage: $i_d \sim \exp(V_{gs}/V_a)$. The constant V_a depends only on the ratio of the change of channel potential to the change in gate-source voltage and can be expressed

Fig. 1. i_d - V_{ds} characteristics at different gate-source voltages of n-type C-HFET A15.330(2); WxL= 330 μ m x 0.85 μ m.

Fig. 2. i_d - V_{gs} characteristics of n-type C-HFET A15.330(2); WxL= 330 μ m x 0.85 μ m.

as $V_a = nkT/q$. (q : elementary charge) [6]. We found that the factor n is close to 1.5. Above threshold (0.4V - 0.5V) the current is approximately proportional to the square of the gate voltage. This is demonstrated by plotting the curve $\sqrt{i_d}$ vs. V_{gs} , also shown in Fig. 2.

To be able to compare different devices („A“ and „T“ transistors) with different threshold voltages and different gate-widths, we extracted from the measurements the gate current density i_g , the transconductance g_m , and the voltage amplification g_m/g_{ds} as a function of the drain current density i_d and we normalised all values to 1 mm gate-width. Fig. 3 shows g_m vs. i_d and g_m/g_{ds} vs. i_d for a representative „A“ transistor. The figure demonstrates that in the region of interest (0.1 mA/mm - 2 mA/mm) the transconductance is almost proportional to the drain current density $g_m \sim i_d^n$, where n is close to 0.75. The voltage amplification factor g_m/g_{ds} increases with decreasing drain current density which is advantageous for a low power preamplifier. Typical values for the gate current as a function of i_d are shown in Fig. 4. As seen in this figure the gate current is small, less than 30 nA/mm. The noise caused by the gate current contributions decreases with decreasing i_d (see section 4.4). In Table 1 the DC

Fig. 3. Measured values of transconductance g_m and voltage amplification g_m/g_{ds} for transistor type „A“; A15.330(2).

Fig. 4. Measured gate current i_g as a function of drain current density i_d for transistor A15.330(2).

parameters for all measured transistors are compared for a drain current density of 0.5 mA/mm and a drain-source voltage of 1V. The data in Table 1 show that all investigated transistors have a comparable transconductance, but the voltage amplification

Table 1

Basic DC parameters for all investigated transistors for $i_d = 0.5$ mA/mm and $V_{ds} = 1.0$ V.

Transistor	g_m [mS/mm]	g_m/g_{ds}	i_g [A/mm]
A15.10	9.5	200	3.5E-08
A15.100	11	175	7.1E-09
A15.330(1)	9.7	250	7.8E-09
A15.330(2)	9.9	250	7.4E-09
A16.100	9.6	218	4.1E-09
A16.330(1)	9.7	268	6.1E-09
A16.330(2)	9.6	193	5.9E-09
A17.100	10	185	-8.0E-10
A17.330(1)	9.5	250	-7.9E-10
A17.330(2)	9.7	248	-6.7E-10
A18.100	9.8	165	1.9E-09
A18.330(1)	9.6	258	8.7E-10
A18.330(2)	9.5	149	1.2E-09
A19.100	10	179	2.6E-09
A19.330(1)	9.8	200	1.3E-09
A19.330(2)	9.8	204	1.0E-09
T11.10	10	35	-4.4E-09
T11.100	12	30	-1.2E-09
T11.330(1)	11	44	3.0E-09
T11.330(2)	11	44	3.4E-09
T17.10	10.8	53	-2.3E-09
T17.100	12	50	-1.3E-09
T17.330(1)	11	74	3.6E-10
T17.330(2)	11	78	2.2E-10
T23.100	9.0	40	-2.0E-09
T23.330(1)	10.4	66	1.1E-09
T23.330(2)	10.2	65	8.9E-10

g_m/g_{ds} for the transistors from wafer „A“ is higher than that for wafer „T“, reaching an excellent value of about 200. In comparison to the transistors described in [1,2] the voltage amplification of the transistors of type „A“ is higher by a factor of ~ 3. Furthermore, the gate current is one order of magnitude smaller. (The gate current density for the transistors described in [1, 2] is of the order of 100 nA/mm at $i_d = 0.5$ mA/mm and $V_{ds} = 1$ V). The data in this table demonstrate also that the measured DC values scale well with the gate width.

3. NOISE BEHAVIOUR

The main purpose of the study was to investigate the dependence of the noise behaviour of the C-HFET on its biasing, in

order to find the best operating conditions for the input transistor of a low power consumption, low noise preamplifier. We investigated the noise of the transistors using a computer controlled system that automatically performs equivalent noise charge measurements of a preamplifier for peaking times ranging from 10 ns to 1 μ s. The detailed setup and operation of the measurement configuration, consisting of a preamplifier and shaper is described in [1], [7]. The transistor under investigation is the input transistor of a cascode charge preamplifier. The shaper is an unipolar filter of type CR-RC². The transfer function of the filter is:

$$H = \frac{\tau s}{(1 + \tau s)^3} \quad (1)$$

As shown in ref. [1], [7] by measuring the equivalent noise charge, *ENC*, for various peaking time constants t_p (in this case $t_p = 2\tau$), one can extract the power densities of the white serial noise (A_n), the white parallel noise (D_n), and of the $1/f$ serial noise (A_f) sources of the transistors. In this respect, we have carried out two analyses:

- ENC* measurements at various drain current densities in the range from 0.25 mA/mm to 2 mA/mm at constant drain-source voltage $V_{ds} = 1V$
- ENC* measurements for different V_{ds} in the range from 0.6V to 2 V at a constant drain current density $i_d = 0.5$ mA/mm.

The FETs were operated under saturation conditions as commonly employed in amplifier applications.

3.1 ENC vs. drain current density

In Fig. 5 the *ENC* measured for various values of the drain current for a transistor with 330 μ m gate-width is plotted as a function of peaking time. The

extracted power densities of each contribution to the *ENC* are listed in Table 2 (transistors A15.330(1); A15.330(2), T11.330(2)). These values indicate, that in the operating region under investigation the $1/f$ noise is almost independent of i_d . However, white serial noise (A_n) and white parallel noise (D_n) show a clear dependence on the drain current density. The white serial noise increases and white parallel noise decreases with decreasing drain current density. To illustrate the significance of each noise source in a readout system for semiconductor detectors, the noise densities have been converted to the equivalent number of electrons, also listed in Table 2, computed for a total input capacitance of 11 pF and 20ns peaking time. The data in Table 2 and in Fig. 5 show that in general the $1/f$ noise dominates, but at short peaking times, ≤ 25 ns, and low drain current densities, below 1 mA/mm, the white serial noise provides the most significant contribution to the total noise. This suggests that, at short peaking times and in case no restrictions are imposed on the power consumption, the amplifier noise can be minimised by keeping the current density of the input transistor higher than 1 mA/mm.

Fig. 5. *ENC* measurement at various drain current densities and constant drain voltage $V_{ds} = 1V$ for transistor A15.330(2) with total input capacity $C_{tot} = 11$ pF.

Table 2

Spectral noise density parameters obtained by fits to the *ENC* measurements for various biasing conditions and calculated contributions of each noise source to the total *ENC* for an input capacitance of 11 pF and 20ns peaking time, (errors are obtained from the fit).

Device	Biasing		D_n	A_n	A_r	ENC [electrons]		
	V_{ds} [V]	i_d [A/m]	$[10^{-27} \text{A}^2/\text{Hz}]$	$[10^{-19} \text{V}^2/\text{Hz}]$	$[10^{-10} \text{V}^2]$	(D_n)	(A_n)	(A_r)
A15.330(1)	1	0.25	4 ± 2	49 ± 2	0.34 ± 0.02	45	986	745
A15.330(1)	1	0.5	7 ± 2	30 ± 2	0.34 ± 0.02	59	772	745
A15.330(1)	1	1	9 ± 2	19 ± 2	0.35 ± 0.02	67	614	752
A15.330(1)	1	2	12 ± 2	11 ± 3	0.38 ± 0.02	78	467	784
A15.330(2)	1	0.25	4 ± 2	45 ± 1	0.31 ± 0.01	45	945	708
A15.330(2)	1	0.5	6 ± 2	25 ± 1	0.32 ± 0.01	55	704	716
A15.330(2)	1	1	7 ± 2	16 ± 2	0.33 ± 0.01	59	564	730
A15.330(2)	1	2	8 ± 2	10 ± 1	0.35 ± 0.01	63	446	752
T11.330(2)	1	0.25	6 ± 3	65 ± 3	0.42 ± 0.02	55	1136	824
T11.330(2)	1	0.5	6 ± 3	24 ± 2	0.42 ± 0.02	55	690	824
T11.330(2)	1	1	5 ± 3	11 ± 1	0.41 ± 0.02	50	467	813
T11.330(2)	1	2	7 ± 3	13 ± 1	0.42 ± 0.02	59	508	824
A16.330(1)	0.6	0.5	3.1 ± 2	30 ± 1.6	0.30 ± 0.01	41	772	696
A16.330(1)	1.0	0.5	4.1 ± 2	30 ± 1.6	0.32 ± 0.01	47	772	719
A16.330(1)	1.5	0.5	5.1 ± 2	30 ± 1.6	0.32 ± 0.01	51	772	719
A16.330(1)	2.0	0.5	5.9 ± 2	30 ± 1.6	0.32 ± 0.01	55	772	719
T17.330(2)	0.6	0.5	1.3 ± 1.7	25 ± 1.3	0.28 ± 0.01	27	704	673
T17.330(2)	1.0	0.5	2.9 ± 1.7	25 ± 1.3	0.27 ± 0.01	38	704	661
T17.330(2)	1.5	0.5	1.3 ± 1.7	25 ± 1.3	0.30 ± 0.01	27	704	696
T17.330(2)	2.0	0.5	1.3 ± 1.7	24 ± 1.3	0.32 ± 0.01	27	690	719

4.2 *ENC* versus drain-source voltage

Fig. 6 shows the *ENC* data for transistor A16.331 as a function of peaking time for various V_{ds} values. The noise power densities, as obtained from a fit to the measurements, and the corresponding equivalent numbers of electrons of each noise contribution, are shown in Table 2. The measurements demonstrate that parallel noise is only slightly affected by drain voltage due to the larger drain-gate reverse current at higher drain voltages. Furthermore, no dependence of any other noise source on V_{ds} is seen

4.3 Serial noise contribution

In the next two paragraphs we show that the noise parameters extracted by various

noise measurements are consistent with calculations of the noise parameters based on DC measurements.

White serial noise is caused by thermal fluctuations of the velocity of the current carriers in the channel. The noise of the drain thermal current is effectively reflected back to the gate as an equivalent noise voltage. Its density A_n can be expressed in the following manner [9]:

$$A_n = \frac{4kTP}{G_m} \quad (2)$$

where k is the Boltzmann constant, T the absolute temperature, and P is a numerical

Fig. 6. *ENC* measurement at various drain voltages and constant drain current density $i_d = 0.5 \text{ mA/mm}$ for transistor A16.330(1) with total input capacity $C_{tot} = 11 \text{ pF}$.

factor ranging approximately from 0.6 to 1.1. Table 3 shows the measured values of the transconductance G_m as a function of i_d and a comparison of the corresponding values of the parameter A_n : (a) as calculated according to equation (2) with a coefficient $P = 0.6$ and (b) as extracted from the *ENC* measurements. The two values are in good agreement.

4.4 Parallel noise contribution

The parallel white noise is generated by the gate current. Fig. 7 illustrates schematically the transistor structure and the current flow. The diodes in this figure represent the gate-drain and the gate-source barrier junctions. There are three contributions to the gate current:

- gate-source forward current I_{gsf}
- gate-source reverse current I_{gsr}
- drain-gate reverse current I_{dgr} .

Each of these shows shot noise (density D_n). Hence,

$$|I_g| = |I_{gsf} + I_{gsr} + I_{dgr}| \quad (3)$$

Table 3

Measured values of the transconductance G_m together with calculated (Eq. 2) and measured (see Table 2) values of the serial white noise density A_n .

Device	i_d	G_m	calc. A_n	meas. A_n
	[mA/mm]	[mS]	[$10^{-19} \text{ V}^2/\text{Hz}$]	
A15.330(1)	0.25	2.0	50	49
A15.330(1)	0.5	3.2	31	30
A15.330(1)	1.0	5.0	20	19
A15.330(1)	2.0	9.8	10	11
A15.330(2)	0.25	1.9	52	45
A15.330(2)	0.5	3.3	30	25
A15.330(2)	1.0	5.7	18	16
A15.330(2)	2.0	9.2	11	10
T11.330(2)	0.25	1.9	51	65
T11.330(2)	0.5	3.6	28	24
T11.330(2)	1.0	6.0	17	11
T11.330(2)	2.0	10.2	10	13

$$D_n = 2q(|I_{gsf}| + |I_{gsr}| + |I_{dgr}|) \quad (4)$$

The measured contributions to the gate current and the sum of their absolute values (Eq. 4) are illustrated in Fig. 8. The gate-source reverse current I_{gsr} is small in compa-

Fig. 7. C-HFET Model.

Table 4

Measured values of gate-source forward current I_{gsf} , drain-gate reverse current I_{dgr} and calculated (Eq. 4) and measured values (see Tables 2) of parallel white noise density D_n .

Device	i_d [mA/mm]	V_{ds} [V]	I_g [nA]	I_{gsf} [nA]	I_{dgr} [nA]	calc. D_n $10^{-27}A^2/Hz$	meas. D_n $10^{-27}A^2/Hz$
A15.330(2)	0.25	1.0	0.7	5.9	-5.2	3.5	4 ± 2
A15.330(2)	0.5	1.0	2.5	7.2	-4.8	3.8	6 ± 2
A15.330(2)	1.0	1.0	5.5	10	-4.2	4.5	7 ± 2
A15.330(2)	2.0	1.0	10.3	14	-3.5	5.8	8 ± 2
A16.330(1)	0.5	0.6	4.8	4.7	-0.1	1.5	3 ± 2
A16.330(1)	0.5	1.0	1.9	4.7	-2.4	2.4	4 ± 2
A16.330(1)	0.5	1.5	-1.0	4.7	-5.7	3.2	5 ± 2
A16.330(1)	0.5	2.0	-4.0	4.7	-8.7	4.5	6 ± 2

risson to the other two and has been omitted in these investigations. The measured values of I_g , I_{gsf} , I_{dgr} for transistors operated at different drain current densities, (A15.330(2)), and different drain voltages, (A16.330(1)), are listed in Table 4 together with the calculated values of the parameter D_n (Eq. 4). Fair agreement is obtained between measured and calculated values of D_n . The data in Tables 2 and 4 show that the shot noise decreases with decreasing drain current and drain voltage due to the decrease of I_{gsf} and I_{dgr} respectively. Furthermore the parameter D_n decreases with decreasing transistor gate-width. Therefore the corresponding parallel noise contribution to the ENC for peaking times less than 50 ns can be neglected for small transistor gate-widths $\leq 330 \mu m$.

4.5 Input noise optimization

It has been shown [8], that the total noise of the cascode charge preamplifier is by far dominated by the noise generated in the input transistor. We can thus optimize the noise of the whole preamplifier by optimizing the size and the drain current of its input transistor. The ENC of a detector-preamplifier system is given by [1]:

$$ENC^2 = A_n C_{tot}^2 \frac{S_a}{\tau} + A_f C_{tot}^2 S_c$$

Fig. 8. The measured contributions to the gate current at $V_{ds} = 1$ V for transistor A15.330(2).

$$+(D_n + 2qI_{det})S_b\tau \quad (5)$$

The noise integrals S_a , S_b , S_c are calculated for a RC-CR² unipolar shaper. C_{tot} is the sum of detector capacitance, the transistor gate-source and gate-drain capacitance, and the feedback capacitance. The functional dependence of the noise parameters A_n and D_n on the DC parameters of the transistor and the good correspondence between their calculated and measured values for transistors

with 330 μm gate-width, and the good agreement between the normalized DC values of transistors with different gate-widths (Table 1), permit us to extrapolate the noise parameters to smaller gate-widths and different drain currents (by keeping similar drain current densities). For this purpose the parameters A_n and D_n were extracted from the transistor DC measurements at $V_{ds} = 0.5\text{V}$ using the following equations:

$$A_n(I_d) = \frac{4kT \cdot 0.6}{Wg_m(I_d)} \quad (6)$$

$$D_n(I_d) = 2qW \left[|i_{gsf}(I_d)| + |i_{dgr}(I_d)| \right] \quad (7)$$

where W is the gate-width of the transistor. The parameter A_f for $1/f$ noise is independent of the biasing conditions at the investigated drain current densities and drain voltages. Therefore the latter was extrapolated according to:

$$A_f = \frac{a_f}{W} \quad (8)$$

where a_f is the $1/f$ noise parameter normalized to $W = 1\text{ mm}$ obtained from the ENC measurements of transistors with 330 μm gate-width.

The optimization is performed assuming a pixel detector with an area of 125 $\mu\text{m} \times 125\text{ }\mu\text{m}$. The detector and stray capacitance C_{det} are estimated to be 150 fF and the detector dark current is taken to be $I_{det} = 0.3\text{ nA}$ per pixel. Fig. 9 demonstrates the total ENC of the input transistor as a function of its drain current and its gate-width for a peaking time of 20 ns and a drain voltage of 0.5 V. As seen in the figure the noise can be made lower at the expense of power consumption. Since for the pixel detectors the power consumption is of primary concern, the transistor should be biased with a drain current close to 6 μA . (Point A in Fig. 9). For these biasing conditions ($I_d = 6\text{ }\mu\text{A}$, $V_{ds} = 0.5\text{V}$) the noise contributions of each noise source are shown in Fig. 10 as a function of a gate-width. For the

Fig. 9. The calculated ENC of the input transistor as a function of drain bias current and transistor gate-width. ($C_{det} = 150\text{ fF}$, $\tau = 20\text{ ns}$, $V_{ds} = 0.5\text{V}$).

Fig. 10. The contribution of each noise source to the total noise as a function of the transistor gate-width for a constant power dissipation of 3 μW ($I_d = 6\text{ }\mu\text{A}$, $V_{ds} = 0.5\text{ V}$).

total noise we observe a flat minimum of roughly 90 electrons at $W = 25 \mu\text{m}$. The series white noise contribution for a constant drain current increases with increasing gate-width (except for small values of the gate-width $\leq 5 \mu\text{m}$). This is due to the fact that the transconductance is almost independent of the gate-width at constant drain current (see Fig. 2), but the total input capacitance increases due to the increase of gate-source and gate-drain capacitance. We notice also that the white series noise dominates. To minimize its value, the length of the transistor should be as short as possible. However a limit of such an optimization is given by the $1/f$ noise which is inversely proportional to the gate length.

6. CONCLUSION

We have investigated the DC-, AC- and noise parameters of GaAs-based transistors in C-HFET technology. We have measured transistors with two different architectures (wafer "A" and wafer "T"). The wafer "T" has been processed in the standard way described in ref. [2]. Wafer "A" has a new type of buffer between the heterostructure and the substrate. This buffer improves the amplification factor g_m/g_{ds} of the transistors, but does not have any significant influence on the noise parameters.

It is shown that the transistors have excellent amplification behaviour in the low power region. We found that the $1/f$ noise is independent of the drain current and of the drain bias voltage. The white serial noise increases with decreasing drain current density and for transistors with gate-width $W = 330 \mu\text{m}$ it becomes dominant at peaking times smaller than 25 ns and drain current densities i_d less than 1 mA/mm. The parallel white noise is mainly generated by the shot noise of the gate-source forward current I_{gsf} and the shot noise of the drain-gate reverse current I_{dgr} . The data indicate that for this technology the shot noise decreases with decreasing drain current density and drain

voltage due to the lower contributions to the gate leakage current. Its contribution to the total noise at short peaking times can be neglected for the transistor gates considered here ($W \leq 330 \mu\text{m}$).

An extrapolation shows that the total ENC of a C-HFET input transistor with $25 \mu\text{m}$ gate-width and $3 \mu\text{W}$ power dissipation would be about 25 electrons at zero detector capacitance with a slope $\Delta(\text{ENC})/\Delta C_{det}$ around 440 electrons/pF.

ACKNOWLEDGEMENTS

The C-HFET transistors and preamplifiers used in this study were produced by Honeywell Technology Centre, Bloomington, Minnesota, USA. We acknowledge the efforts of Steven Baier at Honeywell. We would like also to thank Bernhard Opitz and Meskida Küsters from the Institut für Halbleitertechnik der RWTH Aachen for their support.

REFERENCES

- [1]. D. DiBitonto et al., "Radiation and Cryogenic Test Results with a Monolithic GaAs Preamplifier in C-HFET Technology", *Nucl. Instr. and Meth. A* 350 (1994) p. 530.
- [2]. Karpinski et al., "Characteristics of GaAs Complementary Heterojunction FETs (C-HFETs) and C-HFET based Amplifiers Exposed To High Energy Neutrons" *RWTH Aachen Report PITHA 94/44, accepted for publication in Nucl. Instr. and Meth. A*.
- [3]. N. Cirillo et al., "Realisation of n-channel and p-channel HIGFETs on a Planar Wafer Surface", *IEEE Electron Device Lett.*, Vol. 6, No. 12, (1985), p. 645.
- [4]. P. Paul Ruden et al., "Quantum-Well p-Channel AlGaAs Heterostructure Insu-

- lated-Gate Field-Effect Transistors" *IEEE Transactions on Electron Devices* 36 (1989).
- [5]. C. Chung et al., "A New and Simple Model for GaAs Heterojunction FET Gate Characteristics", *IEEE Transactions on Electron Devices* 35 (1988), p. 570.
- [6]. T. Cunningham et al., „Noise and current-voltage characterisation of complementary heterojunction field-effect transistor (CHFET) structures below 8 K" SPIE Vol. 1684 Infrared Readout Electronics (1994). p. 84.
- [7]. W. Karpinski et al., "Noise and DC Characteristics of GaAs FET's for their use in Front-End Electronics at Future Colliders" *RWTH Aachen Report PITHA 94/3*.
- [8]. F. Robinson „Noise and fluctuations in electronic devices and circuits", Clarendon Press, Oxford, (1974) p. 143.
- [9]. Ando et al., „DC, small-signal, and noise modelling for two dimensional electron gas field effect transistors based on accurate charge control characteristics" *IEEE Trans. Electr. Dev.* vol. ED-37 p. 67, 1990.