Status Report on CERN's participation in the GPMIMD ESPRIT project

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1. Aim of Report

CERN signed the contract for its participation in the GPMIMD, General Purpose MIMD Machines, ESPRIT P5404 project in July 1991 following approval at the Research Board. The aim of this report is to inform the DRDC of the progress made since this time as well as plans and prospects for the next year.

2. Brief Description of GPMIMD project and CERN's participation

GPMIMD is a three year project funded under the EEC Esprit programme. Esprit is the European Strategic Programme for Research and Development in Information Technology. The aim of the project, which involves European industrial partners (INMOS, Meiko, Parsys, Parsytec and Telmat), is to define and develop commercial products based on a new family of distributed memory MIMD parallel computers, and to mount a range of applications which demonstrate the power of these machines. These computers will be based on Transputers and SPARC microprocessors interconnected by very high performance networks and expandable to large numbers of nodes.

CERN's role in the GPMIMD project is predominantly in the area of hardware and application software for real time parallel computing using INMOS Transputers. We are also studying how to parallelise large HEP FORTRAN programs. The overall project is described in a GPMIMD Technical Annex [1] which describes the contractual commitments between the partners, including CERN and the EEC. This includes Milestones, Deliverables and Dependencies which will be quoted in this report.

All of CERN's tasks are proceeding well. The hardware is in an advanced state of development, the data acquisition software is demonstrable on a network of Transputers, and the SIXTRACK simulation program has been parallelised and the parallel version will be the main production code once the CRAY has departed.

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3. Parallel Processing in High Energy Physics

The computing requirement for next generation high energy physics experiments will increase dramatically (see [2], [3] and [4]) over the next five to ten years. The estimated increase in computing power ranges up to three orders of magnitude, depending on the area of application.

The last decade has seen a migration from high cost mainframes to very cost effective and powerful microprocessor based workstations. The performance of single microprocessors continues to increase, however, the technical limits of their performance appear to be in sight and manufacturers are more and more turning to multi-processor parallel machines to provide very high computing power. Manufacturers who are actively pursuing parallel computing include DEC, IBM, CRAY, Intel, Silicon Graphics, Thinking Machines in the USA and Meiko and Parsytec in Europe. The significance of parallel processing is also recognised in the two recent Rubbia Committee reports on High Performance Computing in Europe ([5] and [6]).

In general, HEP is not seeking to develop its own computing solutions but rather to investigate the potential impact and use of new developments from industry, including parallel processing. We must know how existing applications programs can be ported and how future programs have to be structured in order to exploit parallelism. It is essential to carry out these investigations in order to gain expertise in the two to three years before final decisions have to be taken on the architecture and development of software for new generation experiments.

CERN is already obtaining experience of shared memory MIMD, on the Cray and the IBM 3090, and of loosely coupled distributed memory using clusters of high performance workstations. SIMD architecture has also being investigated.

Parallelism in the form of FORTRAN farming has been shown to be effective on loosely coupled workstations and arrays of microprocessors (see [7] and [8]). A natural evolution from farming requires investigation of the parallelism inherent at all levels in HEP codes. New forms of parallelism in HEP can offer both reduced response times, important for real time and interactive computing, as well as better exploitation of new cost effective parallel computers from industry.

In March 1992, the leaders of ECP and CN Divisions appointed a small steering group to make an initial study of the relevance of parallel computing in HEP. The steering group is finalising its recommendations and plans which include a GPMIMD-2 ESPRIT project based on commercial products which are the result of R&D carried out in GPMIMD. The GPMIMD-2 project will mount a variety of high energy physics applications on a SPARC based GPMIMD multi-processor which will be installed in the computer centre.

4. Transputers

Transputers [9] [10], manufactured by INMOS, are a family of microprocessors which have the following components packaged in a single integrated circuit (see figure 1):

* 16 or 32 bit integer central processing unit, CPU;
* fast on-chip memory/cache, RAM;
* optional processor for floating point arithmetic unit, FPU;
Computational power a factor 10 greater than the T800. The existing C004 crossbar OCR Output which will be used in the GPMIMD project, uses four 100 Mbits/s links and has a bandwidth of 20 Mbits/s per link. The next generation T9000 Transputer, which will be potted in the GPMIMD project, will provide communication support.

- Programmable interface to external memory;
- Communication system comprising 4 bi-directional serial links which can be connected to other Transputers either directly or via crossbar switching components.

![Transputer Block Diagram](image)

In addition there is a small on-chip kernel which organises the different processes being executed on a Transputer, supports extremely fast context switching and provides communication support.

![A Typical Transputer System](image)

Present generation T800 Transputers have a computing power of 0.75 CERN units and communicate at 20 Mbits/s per link. The next generation T9000 Transputer, which will be used in the GPMIMD project, uses four 100 Mbits/s links and has a computational power a factor 10 greater than the T800. The existing C004 crossbar...
Transputers and the CHORUS operating system; OCR Output

2. CERN is developing and testing scalable real time data acquisition systems using
Transputer link extender and a HIPPI interface, source and destination, driven by a
development of a T9000 based VME interface, a long distance optical fibre
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Transputer link extender and a HIPPI interface, source and destination, driven by a
T9000 Transputer;

5. Trends in Real Time Systems

High energy physics experiments have until now based their detector readout systems
on standard buses such as CAMAC and more recently VME and FASTBUS. It has
become apparent that the higher performance systems for future experiments will
require a departure from this way of working towards schemes based on high speed
(Gbits/s) point to point links and switches connecting large numbers of data sources
and sinks (see [16]).

With the ever increasing numbers of information sources in view for next generation
experiments, it has become economically and technically necessary to migrate more
and more of the electronics, including microprocessors, physically onto the detectors.
We are passing from off-detector electronics connected via buses, to an on-detector
approach using large numbers of microprocessors, links and switches, to achieve the
required level of performance through parallelism.

The Transputer concept with its minimal component count and its simple serial links,
which can span sizeable distances, is a natural building block for next generation
systems of the type outlined above. Transputer link technology looks very promising
for high rate data capture especially when combined with optical fibre technology.

Next generation experiments are capable of producing large volumes of data that will
need to be recorded in real time for subsequent analysis. This will almost certainly
require highly parallel data recording systems and the means to process large numbers
of particle interactions. The Transputer style of machine architecture can address this
problem through its high performance distributed input/output system and scalable
processing power.

6. CERN's role in the GPMIMD project

The role of CERN in the project is as follows:

1. CERN is developing input/output interfaces between Transputer based machines,
data acquisition equipment and high speed data recording devices. This includes the
development of a T9000 based VME interface, a long distance optical fibre
Transputer link extender and a HIPPI interface, source and destination, driven by a
T9000 Transputer;

2. CERN is developing and testing scalable real time data acquisition systems using
Transputers and the CHORUS operating system;
3. Off-line applications are also being targeted, we are pursuing methods and tools for parallelising HEP programs.

A grant has been made by ESPRIT to CERN for the hiring of personnel (8 man years) and for purchasing equipment. The total value of this grant is approximately 1.4M SFr. CERN is providing complementary resources of 690k SFr and 15.75 man years, to be spread over the three year duration of the project.

7. Status and Future Plans for Hardware Development

The hardware task in GPMIMD involves development in the three areas of VMEbus, HIPPI and fibre optic links.

Background

**VMEbus.**

The VMEbus is widely used in data acquisition systems at CERN and has extensive industrial support for third party modules. A VME to T9000 interface allows the interconnection of VME crates over cheap, high performance serial links.

In addition, VMEbus offers a gateway to different industry standards such as SCSI, FDDI, Ethernet, IBM channel, Ultratek etc. which can be exploited by the GPMIMD machine.

**HIPPI.**

In order to provide high performance visualisation it has been decided to connect the GPMIMD machine to high performance graphics workstations via the HIPPI standard. HIPPI interfaces may also be used to connect to high performance disk systems.

There is a base of expertise at CERN in the design and exploitation of HIPPI and HIPPI is finding a role in data acquisition systems and for connecting clusters of workstations.

The proposed HIPPI interface uses a single T9000 processor. It will be able to support a peak transfer rate of 160 Mbytes/s and sustain 40 Mbytes/s.

**Fibre-Optic Links.**

The third activity is a study of how to pass the DS links over fibre-optic media. High speed serial link technology is of great interest and importance to CERN for both current and future applications.

The INMOS T9000 DS links are defined in a four wire protocol over copper at 100 Mbaud. Differential drivers in pseudo-ECL can carry such signals up to 30 metres at the design speed but of course using eight conductors per link. For greater distances in noisy environments with minimum material cross section the obvious choice is fibre-optics although the cost per connection will be higher.

The effective throughput of such links depends critically on the error rate since error detection and correction protocols, if required, can introduce large software overheads and may significantly degrade raw link speeds.

The purpose of the R&D carried out is to determine the feasibility of using standard low cost (100 SFr) optical components for such a link. Assuming the results to be
positive then a prototype circuit will be built to demonstrate the viability of a commercial product.

Current Status.

T9-VMEbus Interface.

A block diagram showing the main features of the design is shown in figure 3.

Figure 3 - T9000 to VMEbus Interface Block Diagram

The design of the T9-VMEbus interface is complete. The internal operations have been fully simulated as well as most of the VME data operations. A provisional PCB layout was successfully done at the end of 1992, see figure 4. Some revisions to the layout have been agreed to and the final routing is now underway. It is expected to have a printed circuit for this board in the first half of February 1993.

A software test package has been prepared. It consists of a set of library routines for initialisation, diagnostics and exploitation of the board. On top of this there is a menu package that allows user access to the library primitives. The whole package is written in C and documentation is about 50% complete. There is a C compiler, simulator and Toolset for the T9000 running on a Sun which is being used to check the library routines.

The main use for this interface in the GPMIMD environment is as a gateway to third party VME modules. A demonstration driver for a Radstone SCSI interface has been written using an Exabyte drive as the target device. This has been tested using a T8 based board having similar architecture to the T9-VME interface. It is expected that the port from one to the other will present no problems.
HIPPI

The HIPPI interface is itself in three parts. There is a T9000 packaged on a VME board with a block of high speed memory and a connector to carry address, data and control information to daughter boards. The block diagram is shown in figure 5.

Figure 5 - T9000 to HIPPI Motherboard.

There are two daughter board options; a HIPPI Source and a HIPPI destination. The motherboard may carry one or both these boards.

The HIPPI source board had already been built and tested in a separate project between CERN and an industrial partner, CES Geneva. The design of the destination board is nearly complete and should be frozen by the end of January 1993.
The design of the motherboard is complete and it has been extensively simulated. It will be frozen once the final details of the destination board are known and will be ready to go for PCB layout at the end of February 1993.

The test software platform developed for the VME interface will be modified to support this board.

*Fibre-Optics*

A test bench has been established with a 1Ghz digital scope, a BERT (Bit Error Rate Detector) and programmable pulse generator.

In the first instance it was necessary to measure the error rates attributable to the various components of a fibre link especially since it is proposed to use low cost parts. This work has been completed and a report issued³. Figure 6 shows one of the 'eye diagram' results from the study. A pseudo-random bit pattern similar to link packet structure was transmitted through a fibre-optic link under study. The eye opening defines that period in which a bit value may be unambiguously regenerated. The measured eye opening of over 7 ns confirms the excellent quality of the link.

![OTX output eye, PRS6 pattern, 125MBaud, 1m of 62.5um fiber](image1)

![OTX output eye, PRS6 pattern, 125MBaud, 1m of 62.5um fiber](image2)

Figure 6. - OTX output eye, PRS6 pattern, 125MBaud, 1m of 62.5um fibre

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³ GP-MIMD T9000 Fibre Optic Link Extensions, GP-MIMD Confidential, S. Haas, Div. ECP CERN, Oct. 92
The bit error rate due to the optical components has also been measured using the BERT and an optical attenuator. Measurement of error rates this low has to be done by extrapolation of results from attenuated signals. Without attenuation a link was run over 200 metres for 480 hours with no errors. This only means however that the rate was less than $4.6 \times 10^{-15}$. The results of the attenuation measurements as shown in figure 7 shows that the fibre-optic components may be expected to perform with an error rate of $10^{-20}$.

![BER vs Optical Power](image)

Figure 7. - BER versus Optical Power.

We have carried out a similar study of the components of a differential copper link. This work has been recently completed and the report is being prepared.

The results of the fibre-optic study were very positive and the second stage is now underway. A circuit to encode the DS links to a serial stream fit for fibre transmission and another circuit to receive and decode the serial stream are under development at CERN and at INMOS. These are expected to be operating and under test before the end of May. The layout and the division of responsibilities is shown in figure 8.
The test facilities for this part of the work have been established using INMOS prototype Link Test Chips. We have been able to demonstrate that DS links perform to specification (and above) over a 10 metre copper connection.

**Future activities**

The VME board will soon be ready for the debugging of both hardware and software. This will be quickly followed by the debugging of the HIPPI motherboard, first alone and then with the HIPPI Source board. Towards the end of 1993 it is expected to be able to have finished testing the destination board as well. The work on the links is going well and are expected to yield results on schedule.

8. Status and Future Plans for Scalable Data Acquisition Systems

**Motivation and general approach**

To achieve the required high performance, future generation acquisition, triggering and control systems will need to exploit parallelism in many different ways, for example:

- multiple data streams will need to be acquired in parallel for each event
- multiple distributed recording devices will be operated in parallel
- multiple data processing and monitoring tasks will need to run concurrently
- multiple users will need to simultaneously interact with the system

These needs can be most naturally met using a tightly coupled multi-node computing system which can be easily expanded (scaled) in terms of its computational power, inter-node communication bandwidth and I/O bandwidth to meet the evolving needs of experiment. It is essential that scalability up to hundreds of nodes is supported efficiently.

The design of the T9000 Transputer family allows such systems to be realised and simply implemented. As part of the GP-MIMD project we are developing Transputer based scalable acquisition systems (SDAS). Needs of different experiments can be taken into account by configuring the Transputers and their I/O as appropriate.

Software is the key element in the successful exploitation of parallel systems. We use the CHORUS operating system technology [17], [18] as the basis for our software...
development. CHORUS is a family of operating systems which is centred around a compact real time distributed micro-kernel which in turn provides a minimum set of essential services, such as process management, scheduling and inter-process communications via message passing. CHORUS Systemes are collaborating with CERN on the development of the real-time aspects of their operating system on Transputers in such a way that CERN experience is reflected in improvements to real-time performance and functionality.

Where necessary, full UNIX features can be added on top of the underlying micro-kernel while still conserving the real time distributed computing capabilities.

CHORUS technology is widely used in both Europe and United States. Its customers includes Motorola, Alcatel, Cray, Unisys and ICL. CHORUS runs on a variety of different processors, including Motorola 68K family and 88110, Intel 386 (IPSC/2 and Compaq), SPARC and on the Transputer family. CHORUS supports portability and runs on heterogeneous processor systems.

The combination of CHORUS and Transputer technologies allow nodes in our parallel systems to be configured in three different ways according to their role:

1. for the most performance critical areas of use, for example a well-defined physics trigger using a fixed array of processors, we use only the Transputer's own on-chip kernel;

2. where increased functionality is required, the CHORUS micro-kernel is run, for example to provide dynamic process loading, multi-level scheduling and thread support;

3. full UNIX functionality may be made available on any nodes, for example to access a file system or for network support.

Prototype System using T800 Transputers

Pending the availability of the T9000 Transputer we have developed and tested a prototype system running on an array of twelve (12) T800s, housed in VME and hosted by a SUN workstation, see figure 9. These T800s are running a software emulation of the T9000. The basic design allows a combination of existing T800 Transputers with the new T9000 hardware. The final performance evaluation will be done with the T9000.

The following functionality has been implemented:

- Data is acquired and buffered for each event via two external links;
- Data can be processed in parallel by one or more different trigger algorithms;
- Accepted data can be recorded using SCSI devices, in this case Exabyte drives, in Zebra format on 8mm tapes. These have been used off-line as direct input to PAW;
- VME I/O is supported using a Transputer based VME master/slave board and SCSI devices have been driven in this way;
- User monitoring tasks can request events and call standard histogramming routines (HBOOK). Many such monitoring tasks can run concurrently on different Transputers each building up their own histograms;
- A user can access these histograms from a host workstation running PAW;
- A simple message system and run control have been implemented

Dynamic code loading has been tested
For benchmarking of CHORUS, see Real Time Performance requirements for CHORUS distributed system with increased performance and functionality.

We will introduce, validate and benchmark new releases of the Chorus Operating Full dynamic code loading.

Carry out scalability testing (up to at least 128 nodes);

Add an experiment data base option (calibration and survey);

Add interrupt handling and support for CAMAC and VME;

Add a data replay option;

Provide an improved messaging system (distributed EMU);

Introduce FORTRAN 90 at the user level;

Add support for parallel data recording on multiple drives;

We will continue to develop the scalable data acquisition system in the following ways:

Future Plans

We will introduce, validate and benchmark new releases of the Chorus Operating system with increased performance and functionality.

Figure 9 - SDAS Prototype System

This system was available in September 1992 to take data from the RD5 Honeycomb chambers in a test beam. This constituted a GP-MIMD CERN milestone. The supported event rate had to be around 0.5 kHz, for a maximum event size of 256 bytes. The events are recorded presently on one Exabyte tape in Zebra file exchange format at a maximum rate of 0.48 Mbytes/s. The deadtime per event was 160μs.

Future Plans

We will continue to develop the scalable data acquisition system in the following ways:

Add support for parallel data recording on multiple drives;

Introduce FORTAN 90 at the user level;

Provide an improved messaging system (distributed EMU);

Add a data replay option;

Add interrupt handling and support for CAMAC and VME;

Add an experiment data base option (calibration and survey);

Carry out scalability testing (up to at least 128 nodes);

Full dynamic code loading.

We will introduce, validate and benchmark new releases of the Chorus Operating system with increased performance and functionality.

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4 For benchmarking of CHORUS, see Real Time Performance requirements for CHORUS distributed OS, M.P. Ward et al., Div. ECP CERN, Harmony Confidential Technical Note, Dec. 92
We plan to test the SDAS system with the NIKHEF Honeycomb chambers in the next RD5 test beam in the spring and are studying the possibility of incorporating our system into the CPLEAR experiment to provide enhanced data recording and monitoring during the summer of 1993. This would include running and benchmarking a parallel version of the CPLEAR reconstruction program on line.

The performance of the T9000 and C104 networks for data capture and triggering will be evaluated with a view to apply this style of MIMD parallel systems to next generation experiments.

9. Status and Future Plans for Off-line Applications

The work in this area has consisted of studies to review the different methods or paradigms used in parallel programming [19] followed by their application in two programs, SIXTRACK and the CPLEAR analysis code, which represent the two principal categories of off-line applications at CERN, namely simulation and reconstruction. The work on paradigms and the SIXTRACK application has been completed and work on CPLEAR program began in January 1993.

Paradigms

A programming paradigm is a programming model which abstracts the details of a real world problem into a computer programmable form. This enables a solution to be formalised to run on a computer. A parallel programming paradigm is targeted at parallel computers.

A parallel programming paradigm is implemented in a programming language. This can be a specifically designed language for parallel programming, for example OCCAM, or it can be in the form of extensions to an existing sequential language like FORTRAN or C, for example, Linda, PVM.

Each paradigm will implement a model which allows a class of real world problems to be mapped to parallel programs. One example of this is the message passing model in which data is always local to a process. Data is communicated between processes by explicitly sending messages from one process to another. Another paradigm is to use a global memory model in which all processes simultaneously have access to the same memory.

There has been considerable research into parallel programming paradigms. It is difficult to produce an objective comparison of one paradigm against another. The effectiveness of a particular paradigm is in most cases highly application and architecture dependent.

The suitability of a paradigm to a particular application is dependent on many factors, some of which are:

- the hardware architecture: message passing or shared memory;
- the level of abstraction, i.e. how much the paradigm shields the user from the hardware model and architecture;
- the trade off of programming simplicity versus run time efficiency;
- dataflow versus control flow synchronisation.

Recent findings are detailed in a GPMIMD deliverable report which gives a review of a selection of paradigms in use in the parallel programming world [20].
Global Memory Paradigms

INMOS investigated an approach to programming which involved shared global memory with a view to supporting this in the system software of the GPMIMD machine and in the hardware of future Transputer machines. CERN evaluated this model for use in HEP applications and found it unsuitable on several grounds. Firstly, the model necessitated programming at a low level (being essentially an assembler language for parallel machines). Secondly, it over emphasised an SPMD style of working, whereby every processing node must be loaded with an identical copy of the program and run in a synchronised fashion. Lastly, it was implemented as an extension to the C programming language, and no FORTRAN support was available.

MonaLisa

We have produced the MonaLisa paradigm, which is a high level extension to FORTRAN designed to suit CERN’s needs.

CERN’s experience with fine-grained parallelism is extensive, for example the CRAY vector processing model, however, the results have not been encouraging. On the other hand farming has worked well and has been widely used.

MonaLisa [21] offers a new convenient way to program HEP applications which includes farming as well as other approaches. It was designed to be a coarse grained, data synchronised paradigm offering a high level of abstraction to the programmer. This paradigm is suited to HEP applications because:

1. The high level of abstraction offers a suitable method for a physicist to program his class of applications without having to know details about the underlying hardware architecture or operating system;

2. The data synchronised aspect maps well onto message passing machines of the GPMIMD type.

Off-line Application Parallelisation

SIXTRACK

SIXTRACK is an accelerator simulator program used in the design of the LHC accelerator. It tracks particles of various energies around a model of an accelerator for many turns in order to predict and avoid chaotic behaviour. The number of turns required is at least 10,000, and more accurate results are obtained with larger numbers of turns. SIXTRACK is therefore CPU intensive but there are no input/output bottlenecks. Limits to the accuracy of the results are at present set by the run time available on the CRAY X/MP at CERN. A typically useful run consisting of tracking 10 particles each for 1,000,000 turns requires a real time of just over 2 days on the CRAY. There was a need to examine possibilities for parallelisation in order to reduce the run time of the program.

The resulting parallel version of SIXTRACK ran twice as fast as the CRAY version using 8 IBM RS6000/550 workstations. In addition, the size of the system can be expanded to 64 workstations in a highly scalable fashion giving an extremely cost effective platform for running SIXTRACK.

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5 The use of GPMIMD UBIK for Data -Synchronised Parallelism, A. Schneider and A. King, ECP Division, CERN, GPMIMD Technical Note
This program, consisting of over 13,000 lines of FORTRAN 77 code, was successfully analysed and parallelised on a network of eight IBM RS 6000/550 workstations (see figure 10) under the Parallel Virtual Machine (PVM [22]) message passing system. PVM is a message passing de facto standard which is well suited to running on distributed networks of UNIX workstations, is available freely as public domain software and has been ported to a large number of computers. Versions are being optimised for parallel machines.

A MonaLisa version of SIXTRACK will be ported to the GPMIMD machine during 1993 and the results compared to the PVM implementation.

Figure 10 - Configuration for Running SIXTRACK

SIXTRACK makes extensive use of the CRAY at present and the parallel version of the program running on workstations will be used after the CRAY is phased out of CERN. The workstation parallel implementation runs at very high efficiency (better than 80%), and since each of the 8 workstations is rated at 10 CERN UNITS the complete system offers around twice the computing power of the CRAY for this application. (The CRAY X/MP is rated at 8 CERN UNITS/processor and has 4 processors.)

**CP-LEAR**

The aim of this work is to demonstrate a parallelised version of the CP-LEAR event reconstruction software running on an array of Transputers. The resulting reconstruction code will be able to run on a number of parallel machines. Implementations in MonaLisa and PVM will be compared.

It is a generally accepted strategy in the world of parallel processing that a complete re-write of algorithms is usually necessary to get the best performance. There will be an examination of the existing algorithms, and a re-write of the code to exploit parallelism at the detector level.

A version of the parallelised CP-LEAR reconstruction code will be tested and benchmarked in conjunction with the SDAS system, both running in real time.

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6 Parallelising SIXTRACK under PVM on a Distributed set of Workstations, B. Sarosi, ECP Division, CERN, GPMIMD Technical Note
10. Budget and Resources

A grant has been made by ESPRIT to CERN for the hiring of personnel (8 man years) and for purchasing equipment. The total value of this grant is approximately 1.4M SFr. CERN is providing complementary resources of 690k SFr and 15.75 man years, to be spread over the three year duration of the project.

The total manpower so far expended is approximately 10.5 man-years by CERN and 4.25 man-years from the EEC funding.

Due to the late signature of the original GPMIMD contract, July 1991, significant EEC funded staff were only taken on in 1992. This turned out to be fortunate as the T9000 was delayed, necessitating more effort towards the end of the project. We plan to retain our present level of EEC funded staff until the end of the project. Due to the hiring of young people, EEC funding gives us 10 man-years in total instead of the original 8 man-years foreseen. This does not affect the financial envelope.
11. GP-MIMD Milestones, Deliverables and Dependencies

This section lists the official milestones, deliverables and dependencies as they are set out in the GPMIMD Technical Annex.

**Hardware Deliverables:**
- Q293 Prototype VME interface
- Q493 Prototype HIPPI board
- Q493 Prototype long haul hardware

**Hardware Dependencies:**
- Q193 T9000 Transputer delivery

**Data Acquisition Deliverables**
- Q193 Interim report on data acquisition
- Q493 Demonstration and report on real time applications

**Data Acquisition Dependencies**
- Q192 Interim T800 based platform running CHORUS operating system
- Q293 Interim T9000 platform running CHORUS operating system
- Q393 Fully integrated T9000 machine running CHORUS operating system

**Off-line Application Deliverables**
- Q492 Report on Programming Paradigms
- Q493 Demonstration and final report on parallelisation of HEP application programs
Off-line Application Dependencies
Q192 Interim T800 based platform running CHORUS operating system
Q293 Interim T9000 platform running CHORUS operating system
Q393 Fully integrated T9000 machine running CHORUS operating system

Comment

The time scales quoted above are critically dependent on the supply of T9000 chips. The latest information that we have is that a Beta test version of the processor is functioning and should be available during Q193.

12. Conclusions

The GPMIMD ESPRIT project is dedicated to the commercial development of a General Purpose Multiple Instruction Multiple Data (GPMIMD) machine. All of CERN's major tasks within the project are well advanced. The hardware is in an advanced state of development with real commercial potential, the data acquisition software is demonstrable on a network of Transputers, and a large application has been parallelised and will become the main production version once the CRAY has departed.

CERN has met all of the EEC milestones to date, by providing prototype hardware and associated test software, a scalable data acquisition system with innovative functionality, a detailed study of programming paradigms and an off-line parallelisation of HEP application code.

The deliverables and milestones for 1993 include:

1. the T9000 VME interface, the T9000 HIPPI board and the fibre optic link extender;
2. a demonstration of a T9000 based data acquisition system running in an experiment;
3. the parallelisation of further off-line application programs.

These systems should run on a fully integrated T9000 machine running the CHORUS operating system.

A workplan diagram covering the entire three year period with all principal tasks, milestones and deliverables is provided below.
References


[20] Report on Paradigms D3.1/1 André Schneider, Adrian King, Ian Willers 22/1/92


[22] PVM: A Framework for Parallel Distributed Computing, V.S. Sunderam, Emory University, Atlanta