R&D Proposal

A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics:

DMILL (Durci Mixte sur Isolant Logico-Linéaire)

Spokesman : M.Dentan (Technology)
Co-spokesman : E. Beuvil (Design)

E.Beuvil, P.Borgeaud, M.Dentan, N.Fourches, M.Rouger
CEA-DSM-DAPNIA Saclay, F-91191 Gif-sur-Yvette, France.

J.P.Blanc, M.Bruel, E.Delevoye-Orsier, J.Gautier, J. de Pontcharra, R.Truche
CEA-DTA-LETI, F-38041 Grenoble, France.

E.Dupont-Nivet, O.Flament, J.L.Leray, J.L.Martin, J.Montaron
CEA-Centre d'Etudes de Bruyères le Châtel, F-91680 Bruyères-le-Châtel, France.

G.Borel, J.M.Brice, P.Chatagnon, C.Terrier
Thomson TMS, F-38521 Grenoble, France.

J.J.Aubert, P.Delpierre, M.C.Habrard, R.Potheau
IN2P3-CPPM, F-13288 Marseille, France.

Abstract:

The high radiation level expected in the inner regions of the high luminosity LHC detectors (γ and neutrons) will require radiation hardened electronics. A Consortium between the CEA (Commissariat à l'Energie Atomique), Thomson TMS (Thomson Composants Militaires et Spatiaux) and IN2P3 (National Institute for Nuclear Physics and Particle Physics) has been created to push for the development and the industrialization of a nascent technology which looks particularly adapted to the needs of HEP electronics.

This technology, currently under development at the LETI (CEA), uses a SIMOX substrate with an epitaxial silicon film. It includes CMOS, JFETs and vertical bipolar transistors with a potential multimegarad hardness. The CMOS and bipolar transistors constitute a rad-hard BiCMOS which will be useful to design analog and digital high-speed architectures. JFETs, which have intrinsically high hardness behaviour and low noise performances even at low temperature, will enable very rad-hard, low noise front end electronics to be designed.

Present results, together with the improvements under way, will lead to a mixed analog/digital technology with a high level of radiation hardness (neutron fluence, cumulated gamma dose, immunity to upset).

The aim of this proposal is to describe this technology, and to ask DRDC to be the interface between the high energy physics community and our Consortium in order to allow us to orientate the technology in the best suitable way for LHC rad-hard electronics.
CONTENTS

1. INTRODUCTION
   1.1 Presentation
   1.2 Radiation level at LHC
   1.3 Electronics specifications for LHC

2. NEEDS FOR LHC ELECTRONICS
   2.1 General specifications and devices required
   2.2 Operation at cryogenic temperatures

3. DESCRIPTION OF THE CONSORTIUM
   3.1 Goal of the Consortium
   3.2 Roles of each partner

4. DESCRIPTION OF THE TECHNOLOGY

5. PRESENT STATUS
   5.1 Preliminary results
   5.2 Circuits and prototypes presently under process

6. TIMETABLE

7. REQUEST TO CERN
   7.1 Interface of DRDC between users and the Consortium
       for final orientation of the technology
   7.2 Funding
   7.3 Beam test

8. CONCLUSION

APPENDIX 1. Examples of readout circuits architectures
APPENDIX 2. Designed prototypes circuits currently in process

REFERENCES
1. INTRODUCTION

1.1 Presentation

Three divisions of CEA (DSM-Saclay: Matter Science Directorate; LETI-DTA: Advanced Technology Directorate; and CEA/Centre d'études de Bruyères-le-Châtel), the IN2P3 (National Institute for Nuclear Physics and Particle Physics) represented by CPPM (Particle Physics Center of Marseille) and the firm Thomson TMS, have decided to merge their experiences and competences to develop and industrialize a high level hardness technology needed for the electronics of the future proton-proton colliders. This new radiation hardened analog and digital technology called DMH [1-2] results from a first study started in 1989 by the CEA-DTA-LETI and the CEA/Bruyères-le-Châtel for other needs than those of the high energy physics community.

This proposal describes the work of the Consortium CEA-TMS-CPPM and how this technology could satisfy most of the high energy physics requirements with reasonable prices. Preliminary results and the planning of the different development and industrialization steps are presented in this document.

1.2 Radiation level at LHC

Due to the high luminosity ($L = 10^{34} \text{cm}^{-2}\text{s}^{-1}$) expected for the LHC collider, part of the electronics of the detector will be exposed to high levels of radiation with a low dose rate (1 to 5 Mrad/year and up to $5 \times 10^{13}$ neutron/cm$^2$/year).

The inner region, corresponding to charged particle detection and tracking, is located between 10 cm to 150 cm from the beam. The level of irradiation, obtained by simulation, reach about 5 Mrad/year at 10 cm from the beam and 1 Mrad/year at 100cm. The neutron fluence is approximately constant in this volume and is in the order of $10^{13}$ neutron/cm$^2$ per year.

The energy measurement region from the preshower detector to the electromagnetic and hadronic calorimeters will be irradiated with around 0.1 to 0.01 Mrad/year and a neutron fluence around $10^{13}$ neutron/cm$^2$ per year.

Electronics located behind the hadronic calorimeter, where all neutrons and most of the gammas are absorbed, will not be exposed to significant radiation levels.

1.3 Electronics specifications for LHC

In contrast to the last generation of colliders, the electronics inside the detectors is subject to severe requirements:

- high radiation level hardness ($\gamma$, neutrons, charged particles)
- monolithic integration of both analog and digital functions (simplification of the integration)
- high speed (fast detector's signal and high rate of collision: 66MHz)
- low noise (small detector's signal)
- high integration density (high number of readout channels)
- high reliability

Those new specifications necessitate major research and development of new new rad-hard technologies and new architectures.
2. NEEDS FOR LHC ELECTRONICS

2.1. General specifications and devices required

There are now many well-advanced electronics projects for future LHC detectors. Circuits for these projects have to be functional for 5 to 10 years under the specifications described above. We have looked carefully at some of the electronics R&D proposals for the LHC which, of course, will not be all present in a real future detector, but nevertheless are representative of its needs. Table 1 summarizes some of these projects. Appendix 1 gives more details on their architectures.

<table>
<thead>
<tr>
<th>PROJECT</th>
<th>SPECIFICATIONS</th>
<th>HARDENING</th>
<th>DETAILS</th>
<th>COMPONENTS PROPOSED</th>
</tr>
</thead>
<tbody>
<tr>
<td>SILICON-PRESHOWER</td>
<td>Room temperature</td>
<td>1 Mrad/year</td>
<td>Bias ±3V</td>
<td>CMOS or BiCMOS (analog)</td>
</tr>
<tr>
<td>20 10^6 channels</td>
<td>C_{det} = 6 pF</td>
<td>1 to 5 \times 10^{13} n/cm^2/y</td>
<td>Low noise preamplifier</td>
<td>CMOS or BiCMOS (analog)</td>
</tr>
<tr>
<td></td>
<td>Noise &lt; 1/10 MIP</td>
<td></td>
<td>Pipeline : OTA</td>
<td>CMOS (digital)</td>
</tr>
<tr>
<td></td>
<td>Power ≤ 5 mW/ch</td>
<td></td>
<td>Shift registers</td>
<td>CMOS (digital)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Multiplexer</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interfaces</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADC 1 MHz, 8 bits / 2V</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td>SILICON-STRIP READOUT</td>
<td>Room temperature</td>
<td>1 to 2 Mrad/year</td>
<td>Low noise preamplifier</td>
<td>JFET + CMOS (hardness)</td>
</tr>
<tr>
<td>20 10^6 channels</td>
<td>C_{det} = 10 pF</td>
<td>\times 10^{13} n/cm^2/y</td>
<td>Analog pipeline</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td>Noise &lt; 1/10 MIP</td>
<td></td>
<td>Digital control</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td>Power ≤ 3 mW/ch</td>
<td></td>
<td>(hybridation on detector)</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Charge amplifier</td>
<td>JFET + CMOS (hardness)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Digital functions</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td>SILICON-PIXEL READOUT</td>
<td>Room temperature</td>
<td>1-5 Mrad/y</td>
<td>Amplifier-shaper</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td>5.4 10^8 pixels</td>
<td>C_{det} = 2 fF</td>
<td>\times 10^{13} n/cm^2/y</td>
<td>(hybridation on detector)</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td></td>
<td>Noise &lt; 1/20 MIP</td>
<td></td>
<td>Charge amplifier</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td>Power ≤ 30 µW/pixel</td>
<td></td>
<td>Comparator</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Digital functions</td>
<td>CMOS or BiCMOS</td>
</tr>
<tr>
<td>LIQUID ARGON-CALORIMETER</td>
<td>Liquid Argon: 90°K</td>
<td>&lt;100 Krad/y (barrel)</td>
<td>Amplifier-shaper</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td>=200 000 channels</td>
<td>15 bits dynamic range</td>
<td>&lt;&lt;4 Mrad/y (end cap)</td>
<td>(hybridation on detector)</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td></td>
<td>C_{det} = 400 pF</td>
<td>10^{13} -10^{14} n/cm^2/y</td>
<td>Charge amplifier</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td>LIQUID ARGON-PRESHOWER</td>
<td>Liquid Argon: 90°K</td>
<td>1 Mrad/year</td>
<td>Amplifier-shaper</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td>=300 000 channels</td>
<td>10 bits dynamic range</td>
<td>1 to 5 \times 10^{13} n/cm^2/y</td>
<td>(hybridation on detector)</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td></td>
<td>C_{det} = 30 pF</td>
<td></td>
<td>Charge amplifier</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
<tr>
<td></td>
<td>Power ≤ 15 mW/ch</td>
<td></td>
<td>Comparator</td>
<td>JFET (low noise + hardness at cryogenic temperatures)</td>
</tr>
</tbody>
</table>

Table 1: Summary of the specifications for some of the R&D proposals for LHC.

An analysis of this table shows the advantages of a rad-hard technology including the three following types of devices:

CMOS:

**Analog** CMOS are required to design most of the readout electronics

**Digital** CMOS are required to design the control electronics of these circuits (today, most of the digital electronics is done in standard CMOS; this know-how is used in most of the LHC prototypes).

A rad-hard CMOS with a large breakdown voltage and a linear transfer characteristic Id(Vds) will fulfill these needs.

A 1.2 µm gate should be suitable for high speed applications (66 MHz).
**Bipolars:**

Bipolar transistors would enable various speed and noise requirements to be satisfied, which would be difficult to meet with CMOS technology for high speed circuits (bipolar transistors give better performances than CMOS: larger transconductance $g_m$, larger current drive per unit area, higher speed with lower noise, better linearity,...). Associated with CMOS, they constitute a BiCMOS technology which would permit fast analog as well as digital architectures.

**JFETs:**

The JFETs are low noise devices. They are intrinsically hardened to high ionizing radiation doses and have a stable behaviour under neutrons, even at low temperature. Therefore these devices are very well suited for low noise and high radiation level applications operating at room or at cryogenic temperature (Applications like Liquid Argon Calorimeter and Preshower require electronics operating at 90 K).

A technology including these three families of components with radiation hardening, electrical performances and integration density can thus ensure a large number of possible architectures (design flexibility).

### 2.2 Operation at cryogenic temperatures

Table 2 summarises the expected radiation hardening for the three families of transistors at room temperature and at cryogenic temperatures (77 - 90 K):

- At room temperature, the expected characteristics of the three families of devices are in sufficient conformity with LHC requirements. Each devices is potentially suitable, the interest of each one depends on the type of the circuit to be designed.

- At 90 K, only the JFETs can reach LHC requirements (the bipolar gain decreases very strongly with the temperature and becomes very small at 90 K, and MOS transistors are not hardened to gamma radiations at this range of temperatures [14]). This shows that complementary JFETs are useful in order to design both analog and digital functions operating at cryogenic temperatures.

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>Bipolars</th>
<th>JFETs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Room T°</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(300°K)</td>
<td>10 Mrad</td>
<td>more than 10 Mrad</td>
<td>more than 10 Mrad</td>
</tr>
<tr>
<td></td>
<td>5 $10^{14}$ n/cm$^2$</td>
<td>2-5 $10^{14}$ n/cm$^2$</td>
<td>5 $10^{14}$ n/cm$^2$</td>
</tr>
<tr>
<td><strong>Cryogenic T°</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(77 to 90°K)</td>
<td>around 10-100 Krad</td>
<td>bad gain (β ≤ 10-15)</td>
<td>more than 10 Mrad</td>
</tr>
<tr>
<td></td>
<td>5 $10^{14}$ n/cm$^2$</td>
<td></td>
<td>5.10$^{14}$ n/cm$^2$</td>
</tr>
</tbody>
</table>

Table 2: Expected hardness for the three component families.
3. DESCRIPTION OF THE CONSORTIUM

3.1 Goal of the Consortium

An overview of the industrial technologies currently available in Europe has shown that there are, for the time being, no processes which could completely cope with all the requirements for the LHC electronics we have mentioned previously (analog and digital circuits). Some of these rad-hard technologies are currently under investigation by experimental particle physics groups. These includes the SOS-CMOS technology (Silicon On Saphire) of ABB-HAFO studied by the University of Upsala [4]; the Harris process studied by the Rutherford Appleton Laboratory and the digital rad-hard SOI-CMOS HSOI3HD from TMS studied by CERN [5] (...).

Convinced that DMILL, with the three types of radiation hardened components (CMOS, Bipolars and JFETs), could be a solution for most of the electronics specifications of the new generation of colliders, CEA and Thomson-TMS have decided in september 1991 to create a Consortium for the development and the industrialization of DMILL [1-3]. In january 1992, this Consortium was joined in its efforts by IN2P3.

3.2 Roles of each partner

**Saclay** (CEA) has been involved, for many years, in different particle physics projects (CERN, DESY, FERMILAB, SSC...) and has carried out much of the associated electronics. In relation to the development of DMILL, it is responsible for:

(i) General organisation of the development of DMILL technology for LHC
(ii) Tests of components (static parameters and noise measurements after gamma irradiation, cryogenic tests)
(iii) Designs and tests of some prototype circuits to assess the validity of the technology

**LETI** (CEA) has a large experience in development of rad-hard integrated circuits processes and in their transfer to industry. It is responsible for:

(i) Development of DMILL technology (from R&D to process stabilization)
(ii) Electrical characterizations before irradiation
(iii) Parameters extraction and design rules definition.

**CEA/Bruyères-le-Châtel** has been involved for many years in radiation hardened systems design. It is responsible for:

(i) Expertise of radiation hardening for the development of DMILL technology
(ii) Tests of components (static parameters after X-ray and neutrons irradiations)
(iii) designs and tests of some critical prototype circuits to assess the validity of the technology.

**TMS** (Thomson) has industrialized bulk and SOI radiation-hard technologies such as HSOI3-HD (CMOS) or HF3C (bipolar) and has for many years developed a large experience in the production of rad-hard circuits. It is responsible for:

(i) Industrialization of the DMILL technology
(ii) Qualification of the technology
(iii) Quality and Radiation-Hardening insurance.
IN2P3 (CNRS) is represented by CPPM (Particle Physics Center of Marseille) for the organization of the work for all his laboratories. CPPM is responsible for:

(i) Evaluation of circuits before and after irradiation
(ii) Tests of components (static parameters after neutrons, protons and pions irradiation)
(iii) Layout of circuits elements proposed by IN2P3.

4. DESCRIPTION OF THE TECHNOLOGY

DMILL technology uses an SOI substrate made with the SIMOX process (Silicon IMplanted with OXYgen), which is one of the most reliable SOI processes (high material quality). During the first part of R&D, devices are designed with a mesa structure. In order to simplify the process, we plan to use if successful a planar structure plus an insulating trench (to separate each device) which are presently under study. The SOI substrate, together with the mesa structure or the planar structure plus insulating trench, gives a complete dielectric isolation between transistors and thus avoids latch-up effects (which can appear in standard bulk technologies if a high ionizing particle goes through a complementary MOS cell). It also avoids Single Event Effects (SEE) which can produce parasitic signals in standard technologies if a large quantity of carriers are collected in the sensitive region of the device, by "funnelling" along the trajectory of a high ionizing particle.

A thin epitaxial layer is grown on this substrate in order to obtain a 1.2 μm thickness silicon film on the SiO2 buried layer. This thickness is necessary to realize Bipolars and JFETs transistors.

A buried doped layer is obtained by ionic implantation in the top SiO2 film under every device. This buried doped layer acts as a collector for the bipolars and as a buried gate for the JFETs. For the MOS, it constitutes a shield which screens positive charges induced by gamma irradiation in the buried oxide layer and then prevents the creation of any parasitic back-side MOS. It also provides a body contact with very low resistivity which avoids the kink effect in NMOS and therefore allows a linear behaviour \( I_d(V_{ds}) \) for both NMOS and PMOS. The elimination of this kink effect is a condition for obtaining the large linear transfer characteristic needed for analog devices.

During the development phase, the DMILL technology includes the NMOS, PMOS, NJFET, PJFET, NPN and PNP transistors. The aimed characteristics for those devices are:

CMOS:
- 1.2 μm gate length (high frequency operation)
- 230 Å gate thickness (to reach the LHC radiation-hard requirements)
- Hardened lateral oxide (to avoid lateral parasitic MOS)
- No kink effect, no latch-up, no SEE.

Bipolars:
- Vertical structure which allows a thin base to be build, which is necessary to obtain a fast electrical response and a good neutron hardening.

JFETs:
- 1.2 μm gate length
- Closed shape structure (devices without channel edges) to avoid leakage current after very high radiation doses.

Figure 1 shows a schematic cross-section of the three types of devices of DMILL technology.
The R&D of the process is made by LETI on the same up-to-date equipment as that used by Thomson-TMS for production. This is very important to simplify the transfer of the technology to Thomson-TMS for the industrial phase.

With the same aim of simplifying industrial transfer, it might be advisable to remove some of the devices. A first trial of reduction to four transistors (NMOS, PMOS, NPN and PJFET) is at the present time being carried out. The final set of devices will be chosen, after discussion with the users (CERN and related laboratories needing rad-hard technology) in order to fulfill most of the LHC rad-hard electronics.

Figure 1. Schematic cross section of the devices developed in DMILL technology
5. PRESENT STATUS

In 1989, CEA Bruyères-le-Chatel with CEA-DTA-LETI started the R&D of an analog/digital radiation hardened technology with the aim of including the 3 main families of components (complementary MOS, JFETs and Bipolar transistors).

A first batch, including only PJFETs, has been processed and successfully tested up to 30 Mrad (integrated dose) and $10^{14}$ neutron/cm$^2$.

Subsequent batches (1990-91) were processed, including 6 components: NMOS and PMOS, NJFET and PJFET, and non-optimized bipolars NPN and PNP transistors stemming from JFET structure. They have already produced promising results.

Batches with 6 components and batches with only 4 components (NMOS, PMOS, PJFET and Bipolar NPN), including test devices and test circuits, are currently in process. They are expected in June and July 92.

5.1 Preliminary results

Tests performed on devices from 1989-1991 batches have given the first following results:

CMOS:
- Neutron irradiation: as expected, they have a small sensitivity to neutrons: after $10^{15}$ n.cm$^{-2}$ their threshold voltage shift is about 100 mV and their transconductance remains very stable.

- Gamma irradiation: Figure 2a and 2b show the measured threshold voltage shift ($\Delta V_t$) versus gamma irradiation for 300 Å gate thickness in various bias conditions (continuous lines). It also shows the results extrapolated for 230 Å gate thickness (dotted lines).

NMOS are less sensitive to ionizing radiation than PMOS (for PMOS the interface and volume oxide charge effects are cumulated, producing a large $V_t$ shift; for NMOS these effects have opposite signs, producing lower $V_t$ shift). The voltage shift depends also on the gate bias during irradiation [14].

For the most sensitive device (PMOS), the worst case we have measured is the logic mode ON (-5V maintained on the gate during irradiation); it gives a $V_t$ shift of about 740 mV after 10 Mrad for 300 Å gate thickness. A more realistic “analog” bias condition (saturation mode with $V_{gs}$ = -2V), for the same gate thickness, gives a $V_t$ shift of about 330 mV.

For the NMOS, the worst case is +5V maintained on the gate during irradiation; it gives a $V_t$ shift of about 380 mV after 10 Mrad for 300 Å gate thickness. The "analog" bias gives a $V_t$ shift of about 190 mV.

In order to reduce this $V_t$ shift, subsequent batches will be realized with 230 Å gate thickness (see dotted lines in figures 2a and 2b). With such a gate thickness, the calculated $V_t$ shift after 10 Mrad would be about 440 mV for the PMOS worst case and about 190 mV for the “analog” case. It would be about 220 mV for the NMOS worst case and about 110 mV for the “analog” case.

The cumulated dose expected at LHC is high, but the average dose rate will be very low, that would allow annealing. First measurements on NMOS with "analog" bias during irradiation show a typical $V_t$ shift recovery greater than 100 mV (room temperature, no bias during annealing).
Periodic annealings are performed. The possibility of using MOS devices at cryogenic temperature under high ionizing dose except if significant recovery after about 10 to 100 Krad (230 Å gate oxide). Therefore, we do not expect any accumulation of positive charges in the gate oxide producing a dramatic $V_t$ shift without any irradiation are bad. Experimental results [14] show that ionizing radiation will induce a very large threshold voltage shift with various bias conditions, 0-10 Mrad.

**Figure 2a:** NMOS Threshold voltage shift with various bias conditions, 0-10 Mrad

- **P1**: $V_{gs} = -2V$ and $V_{ds} = 4V$ (saturation mode)
- **P2**: $V_{gs} = 5V$ and $V_{ds} = 0V$ (switch mode ON)

**Figure 2b:** PMOS Threshold voltage shift with various bias conditions, 0-10 Mrad

- **P1**: $V_{gs} = -2V$ and $V_{ds} = -4V$ (saturation mode)
- **P2**: $V_{gs} = -5V$ and $V_{ds} = 0V$ (switch mode ON)

Cryogenic tests: at 77 °K, the performance of the CMOS devices remains very good. But the prospects for the use of CMOS at liquid nitrogen or liquid argon temperature under ionizing irradiation are bad. Experimental results [14] show that ionizing radiation will induce a very large accumulation of positive charges in the gate oxide, producing a dramatic $V_t$ shift without any significant recovery after about 10 to 100 Krad (230 Å gate oxide). Therefore, we do not expect any possibility of using MOS devices at cryogenic temperature under high ionizing dose (except if periodic annealings are performed).
**JFETs:**

*Gamma irradiation:* as expected, JFETs have a very small ionizing radiation sensitivity (It does not use gate oxide). Measurements after 10 Mrads on PJFETs show a negligible pinch-off voltage shift, a drain-source leakage current in the OFF mode less than 50 pA (W/L = 48/2) and a drop of transconductance less than 10% (Id = 100 μA).

*Neutron irradiation:* JFETs have also a stable behaviour under neutron irradiations: after $2 \times 10^{14}$ n.cm$^{-2}$, measurements on PJFETs show a pinch-off voltage shift less than 100 mV (figure 3).

*Cryogenic tests:* Figure 4.a and 4.b show the drain current versus gate voltage and the transconductance versus drain current characteristics, at room and cryogenic temperatures, for a PJFET. One can see that the main effect of the temperature decrease is a shift of the drain current characteristic near low gate voltage. In other words, the pinch-off voltage $V_p$ decreases and the drain source saturation current decreases when the temperature decreases. These shifts can be corrected using a high initial $V_p$ value. Conversely, the transconductance for a given drain current remains stable even if the temperature decreases to cryogenic values. Therefore, one can expect an adaptation of JFETs for cryogenic temperature. JFETs should be gamma rad-hard even at cryogenic temperatures. Their behaviour under neutron irradiation at low temperatures should be assessed but prospects are good.
Noise measurement: PJFETs have a low $1/f^n$ noise ($0.5 < n < 1.5$) and will exhibit a corner frequency of several KHz to several 10 KHz, depending on the batch. By way of comparison with MOSFET components ($n = 1$), the one hertz noise factor is extrapolated from a $1/f$ slope. Before irradiation, a typical value is 2 to 4 $\mu$V/Hz. It increases with ionizing irradiation but remains below 10$\mu$V/Hz. Thermal noise seems to be in good accord with theoretical values (about 2 to 4 nV/Hz, see Figure 5).

Figure 4b: Transconductance versus drain current at room and cryogenic temperature (W/L=48/2)

Figure 5: Noise characteristic (by reference to the input) of a PJFET (W/L = 48/2)
Bipolars:
Bipolar transistors from these batches have non-optimized structures stemming from JFETs structures. Nevertheless, non optimized NPN transistors show a gain $\beta$ close to 90 ($I_c = 1$ mA) before irradiation. The gain decrease is about 32% after $10^{14}$ n.cm$^{-2}$ (Figure 6).

![Figure 6: Bipolar behaviour under neutron irradiation (non-optimized structure)](image)

Cryogenic tests: At low temperature (77 or 90 K) carriers are "frozen" in the emitter. It produces a strong reduction of their injection in the base. Therefore the gain $\beta$ becomes very small, which presents an impediment for cryogenic operations.

5.2 Circuits and prototypes presently under process

In addition to the circuits implanted by CEA/Bruyères-le-Châtel, Saclay has designed some functional blocks and prototype circuits specially dedicated to high energy applications. The chips will be received from the LETI in mid 92 and will be tested on an automatic test bench (gain, linearity, noise,...)

These chips contain discrete devices and various types of charge and current amplifiers, track-and-hold stages, shift registers (see Appendix 2). CEA/Bruyères-le-Châtel has designed operational amplifiers, digital functions, ring oscillators, a 16 bits microprocessor containing 11000 transistors, etc.

Simulation of DMILL components does not require special models. As regards modelling, this thin silicon film technology is comparable to a bulk technology. Experimentations show that usual CMOS (level 3), Bipolar and JFET SPICE models seem to be suitable. Careful SPICE parameters extraction (static and dynamic) is under way and precise sets of parameters will be extracted from subsequent batches which will be slightly modified before the stabilization stage.

Future designs will include more complex analog and digital circuits with CMOS, Bipolars and JFETs. Functional blocs will be implemented to test DMILL with existing architectures already designed in standard technologies (RD2, RD3, RD19, RD20...).
6. TIMETABLE

Table 3 gives the timetable for the development and industrialization of DMILL.

<table>
<thead>
<tr>
<th>ACTIVITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHASE 1: Evaluation: (6 components) basic components choice</td>
</tr>
<tr>
<td>PHASE 2: (3+2 lots) Process qualification: Circuits hardening evaluation (various tox= 30 nm and 23 nm) SPICE parameters extraction comparison with other techn.</td>
</tr>
<tr>
<td>PHASE 3: (8 lots) End of stabilisation Industrial transfer Design rules for other institutes</td>
</tr>
<tr>
<td>PHASE 4: Transfer (end) + qualification</td>
</tr>
<tr>
<td>PHASE 5: First industrial production</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PHASE 1:</td>
<td>Evaluation of the high energy physics specifications</td>
<td>component choice</td>
<td>first design rules</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHASE 2:</td>
<td>Component and circuits assessment</td>
<td>comparison with other technologies</td>
<td>design of specific functional blocks for LHC applications</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHASE 3:</td>
<td>Qualification and assembly of DMILL</td>
<td>final modifications (two metal layers)</td>
<td>final design rules and SPICE parameters open to external institutes</td>
<td>design of specific circuits for LHC proposals (RD2, RD3 and RD19)</td>
<td>first yield evaluation</td>
<td>beginning of stabilisation</td>
</tr>
<tr>
<td>PHASE 4:</td>
<td>End of stabilisation, beginning of industrial transfer</td>
<td>circuit yield evaluation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHASE 5:</td>
<td>End of industrial transfer, industrial qualification.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PHASE 6:</td>
<td>End of industrial qualification, first industrial production</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3: Timetable for the development and industrialization of DMILL
An important milestone of this project is the comparison of DMILL with other technologies currently under evaluation by different groups [4,5]. The evaluation is forecast to take place at the end of 1992 and at that time final decisions to pursue development and industrialization will be taken.

At the end of phase 3 (mid 93: process qualification and stabilisation), design rules and SPICE parameters (compatible with standards SPICE models) will be made available for other research institutes. Specific public domain simulator as SPICEPAC, specially suited for circuit simulation under integrated dose irradiation and circuit improvement, could be given to research institutes. Layout files should be GDS2 compatible files. A MPC (Multi-Project Chip) dedicated to high energy physics customers will be organized.

7. REQUEST TO CERN

7.1. Interface of DRDC between users and the Consortium for final orientation of the technology

During its development phase, DMILL technology includes six devices: NMOS, PMOS, NJFET, PJFET, NPN and PNP transistors.

In order to simplify the industrial production, it might be advisable to remove some of these components. A first trial of reduction to four devices (NMOS, PMOS, PJFET and NPN) is at the present time being carried out.

The purpose of DMILL is to provide an answer to most of the various LHC rad-hard electronics. The final set of devices must take into account as best as possible the different needs expressed by rad-hard microelectronics users.

With this aim, we are asking DRDC to be the interface between rad-hard microelectronics LHC users and our Consortium in order to allow the consortium to orientate the industrialization of the technology in the right direction. Advices on likely numbers and most likely circuits would also be welcome. Of course, this kind of information would be of general character and would not be specially reserved for our consortium.

7.2. Funding

As this project, if it continues on after the milestone of the end of 1992, will enter into an industrial phase after which its technology will be in free competition with other technologies, the Consortium does not intend to ask for external funding. However, if CERN is interested in joining the R&D phase, the Consortium is open to any suggestion.

7.3. Beam test

Most of the high radiation dose tests have been done either with gamma or with low energy neutrons (few MeV). Those measurements do not take into account the effect of the nuclear fragment from nucleus broken by high energy particles (pions, kaons, protons, neutrons). In particular, the total cross section pion-proton has a peak at 300 MeV, which is a value close to the most probable energy for charged particle in the LHC experiments. The interaction length in silicon is 45 cm, which means that in a detector of 0.3 mm thick, about one particle per thousand will produce an inelastic scattering with a silicon nucleus. An elastic scattering will produce a defect in the cristal (atom displacement) whereas an inelastic scattering will not only create such a defect but also leave the nucleus in an excited state and often eject one proton, one neutron or even an alpha particle. These recoil particles can produce more atom displacement and heavy ionisation (SEE, SEU or latch-up effects).
At the LHC, at 10 cm from the beam, the number of expected charged particles is about $1.2 \times 10^{15}$ p/cm² (30 Mrad) in 5 years. An ideal test beam would be made of pions or protons ranging from 200 MeV to 1.5 GeV with an intensity of $10^9$ p/cm² per second (15 days for 30 Mrad). If such an intensity is possible only in a target area with an energy of several hundred GeV, irradiation at this energy would give results which probably are not easy to extrapolate to low energy elastic scattering but which would be relevant for inelastic collisions where the cross section grows smoothly from one GeV and stays almost flat after a few tens of GeV.

In order to be able to do these tests, we are asking authorization to put samples of 0.3 mm thick of silicon in a beam which can give about $10^9$ p/cm² per second of pions or protons with an energy between 200 MeV and 1.5 GeV for two periods of 15 days.

8. **CONCLUSION**

The mixed analog-digital rad-hard technology DMILL includes the three families of transistors: MOS, JFET and bipolar. Its purpose is to provide an answer to most of the various LHC rad-hard electronics.

First batches have already produced promising results.

The timetable for the development of DMILL is in tune with that of LHC and will allow the production of circuits in 1996.
APPENDIX 1: examples of readout circuits architectures

A.1.1 Silicon Preshower [9-10]

General specifications:

- Irradiation level: 1 Mrad/year (SiO₂) and 1-5.10¹³ neutron/cm²/year
- Number of channels: 20 10⁶ (64 channels / chip)
- Detector capacitance: 6 pF
- Shaping time: ≤ 15 ns
- ENC at the input: < 2000 e⁻ rms
- Power consumption: ≤ 5 mW / channel

Figure A.1.11 shows the basic principle of the analog pipeline memory which allows writings and readings to be carried out simultaneously in different storage capacitors. Writing and reading pointers are generated by the writing and reading shift registers. During writing and reading sequences, the storage capacitor is connected to the amplifier as in a charge amplifier, integrating the amplified and filtered signal coming out of the preamplifier.

Figure A.1.1: Preamplifier followed by the analog pipeline SITP

SITP has already been designed and tested successfully by CERN in a standard CMOS 1.5μm technology. This kind of architecture necessarily requires an analog CMOS, which has also to realize digital functions with 66 MHz clock period (shift registers, multiplexer...). The noise and speed specifications imposed on the front-end amplifier are difficult to reach with CMOS devices; it has been shown that a bipolar transistor, with good performances (ft > few GHz, β around 100), represent the best transistor choice for low-noise, fast pulse processing [11]. Moreover, a BiCMOS technology allows the design of fast architectures (BiCMOS preamplifiers, buffers, ECL gates...) with maximum flexibility for the designer.
A.1.2 Silicon Strip Detector Readout [12]

General specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irradiation level</td>
<td>1-2 Mrad/year and $10^{13}$ n/cm$^2$/year (10 cm from the beampipe)</td>
</tr>
<tr>
<td>Number of channels</td>
<td>3 to 5 millions (128 channels/chip)</td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>10 pF</td>
</tr>
<tr>
<td>Shaping time</td>
<td>$\approx$ 45 ns</td>
</tr>
<tr>
<td>ENC at the input</td>
<td>$700 \text{ e'}_{\text{rms}}$</td>
</tr>
<tr>
<td>Power consumption</td>
<td>$\leq 3 \text{ mW/channel}$</td>
</tr>
</tbody>
</table>

The architecture of the readout electronics is based on the same principle as that of the preshower. But here the electronics will be placed closer to the beampipe and will be exposed to a higher dose of radiation. Until now, only the JFET component is known to be sufficiently rad-hard to ensure functionality up to 20 Mrad (10 years operation).

A.1.3 Pixel Detector Readout [8]

General specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irradiation level</td>
<td>1-5 Mrad/year and $10^{13}$ n/cm$^2$/year</td>
</tr>
<tr>
<td>Number of channels</td>
<td>5.4 $10^8$ pixels (16384 to 32768 pixels/chip)</td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>2 fF</td>
</tr>
<tr>
<td>Shaping time</td>
<td>5 to 10 ns</td>
</tr>
<tr>
<td>ENC at the input</td>
<td>$&lt; 500 \text{ e'}_{\text{rms}}$</td>
</tr>
<tr>
<td>Power consumption</td>
<td>$\leq 30 \mu W$/pixel</td>
</tr>
</tbody>
</table>

Two projects are under study, one is a digital pixel detector readout where only the bit of the hit pixel is read out (figure A.1.2). The other one is an analog pixel detector readout where the signal of the deposited energy is amplified. Digital circuits are known to be much more insensitive to radiation damage than analogs [6], but the rad-hard CMOS or BiCMOS may not be sufficient for those kind of applications where the level of radiation is very high. Here again, JFET would allow improved rad-hard architectures.

![Digital pixel readout diagram](image)

Figure A.1.2: Digital pixel readout.
A.1.4 Liquid Argon Calorimeter

General specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Liquid Argon Calorimeter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irradiation level</td>
<td>&lt; 100 Krad/year and $10^{13}$ neutron/cm²/year (Barrel)</td>
</tr>
<tr>
<td></td>
<td>&lt; 4 Mrad/year and $10^{14}$ neutron/cm²/year (End Cap)</td>
</tr>
<tr>
<td>Number of channels</td>
<td>200,000 channels</td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>400 pF</td>
</tr>
<tr>
<td>Shaping time</td>
<td>45 ns</td>
</tr>
<tr>
<td>Cryogenic T°</td>
<td>90°K (Liquid Argon)</td>
</tr>
</tbody>
</table>

Radiation specifications are much less severe but circuits have to drive large detector capacitances with a large dynamic range at cryogenic temperatures. Preamplifiers with adapted shaping will be put in the liquid argon and cables will drive the signal outside the calorimeter. Bipolar transistors do not work at cryogenic temperatures. CMOS transistors are no longer rad-hard (fixed positive charges in the gate oxide) [14].

First prototypes of preamplifiers and shapers have been realized for the liquid Argon calorimeter (RD3) with low noise discrete and monolithic JFET devices [13] and also with III-V components (AsGa).

A.1.5 Liquid Argon Preshower

General specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Liquid Argon Preshower</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irradiation level</td>
<td>1 Mrad/year and $1-5.10^{13}$ neutron/cm²/year</td>
</tr>
<tr>
<td>Number of channels</td>
<td>300,000 channels</td>
</tr>
<tr>
<td>Detector capacitance</td>
<td>30 pF</td>
</tr>
<tr>
<td>Shaping time</td>
<td>45 ns</td>
</tr>
<tr>
<td>Power</td>
<td>&lt; 15 mW/channel</td>
</tr>
<tr>
<td>Cryogenic T°</td>
<td>90°K (Liquid Argon)</td>
</tr>
</tbody>
</table>

After preamplification and fast shaping, the signal should be memorized to await the level one trigger and to be readout (extracting 300,000 signals through cables appears to be barely possible). Feasibility studies of analog pipeline or equivalent architectures with JFETs are under way.
APPENDIX 2. Designed prototypes circuits currently in process

CHIP 1: Charge amplifiers
(folded cascode configuration with input n channel).

CHIP 2: Charge amplifiers (folded cascode)
with CMOS, JFET and Bipolar NPN.

CHIP 3: Track-and-hold stage and bipolar
current amplifiers

CHIP 4: Shift registers (2 phase D Flip/flop)
REFERENCES


[9] Preshower SiTP collaboration RD2, Design proposal for the 64 channel readout chip of the Silicon Tracker PRESHOWER SiTP detector, CERN Note ECP 3/91.


[12] P.Weilhammer et al., Development of high resolution Silicon strip detectors for experiments at high luminosity at the LHC, CERN/DRDC/RD20.


[14] T.P Ma and P.V. Dressendorfer, Ionizing radiation effects in MOS devices and circuits p. 172 Wiley Interscience (1989) and references herein
