KEK Preprint 95-144
TMU-9552
November 1995
H

A Prototype Data Acquisition System for the BELLE Vertex Detector

T. NOBORI, T. UCHIDA, C. FUKUNAGA,
M. TANAKA and H. IKEDA

SCAN-9603148

CERN LIBRARIES, GENEVA

SC9612

*Submitted to IEEE Transaction on Nucl. Sci., IEEE Nuclear Science Symposium,
San Francisco, U.S.A., October 21 - 28, 1995.*

National Laboratory for High Energy Physics, 1995

KEK Reports are available from:

Technical Information & Library
National Laboratory for High Energy Physics
1-1 Oho, Tsukuba-shi
Ibaraki-ken, 305
JAPAN

Phone: 0298-64-5136
Telex: 3652-534 (Domestic)
(0)3652-534 (International)
Fax: 0298-64-4604
Cable: KEK OHO
E-mail: Library@kekvox.kek.jp (Internet Address)

A Prototype Data Acquisition System for the BELLE Vertex Detector

T.Nobori, T.Uchida and C.Fukunaga

Tokyo Metropolitan University

1-1 Minami-Osawa, Hachioji, Tokyo, 192-03, Japan

and

M.Tanaka and H.Ikeda

National Laboratory for High Energy Physics (KEK)

1-1 Oho, Tsukuba, Ibaraki, 305 Japan

Abstract

A prototype data acquisition(DAQ) system for the BELLE silicon vertex detector has been constructed. We measured its performance using a test board for a front-end readout system emulation. While signals were generated in a test module, the process sequence of interrupt, data transfer and digitization were set up as a design which we will adopt in the final production. In this report we discuss the details of the DAQ system and its data processing capability. We then conclude that the prototype system satisfies the requirement initially given regarding the system construction.

I. INTRODUCTION

We are constructing a silicon vertex detector(SVD) for the BELLE experiment at KEK, the major purpose of which is to exploit the CP-violation expected to occur in B meson decays from $\Upsilon(4S)$ s produced by e^+e^- collisions. The data taking of the BELLE detector is planned to be start at the beginning of 1998. Detailed discussions of the detector design, experimental motivation as well as the planned schedule will be found in [1], where further references are also cited.

The silicon vertex detector comprises 32 detector modules with a double-sided readout scheme. This detector component is installed in the very vicinity of the e^+e^- interaction point in the BELLE detector. For the SVD structure we adopt two concentric super layers with an octagonal configuration around the beam pipe. The radii of the inner and outer layers are 27 mm and 48 mm. One super layer has two sub-layers and one sub-layer has one detector module. In the present detector design we have about 100000 readout channels.

In order to perform data processing of such a number of readout channels within at most 200 μ sec to keep the live time greater than 90% with a 500 Hz trigger rate, we have designed an SVD Data acquisition(DAQ) system incorporating some novel features. These are, for example: the application of a distributed parallel mechanism of the

data accumulation for each detector unit of the SVD and the introduction of a CPU chip in the very front-end system for buffer managing.

In the present report we discuss the system performance of the minimal unit of the data acquisition system and its access to the VME bus. The minimal unit consists of a data scanner and slave memory modules, the functionalities of which are discussed in the following section. We use a total of 48 of minimal units in the SVD total DAQ system. These units are processed concurrently according to the distributed parallel nature. Acquaintances from the measurement and evaluation of the system performance of the minimal unit is very substantial for predicting the total SVD DAQ system performance. Although each component of the minimal unit is still in a prototype stage, we constructed the system based on a final electronics design with final device components. Therefore, the numbers cited in this report will be equivalent to those which will be found in the real DAQ system.

II. THE PROTOTYPE DATA ACQUISITION SYSTEM

In this section the components used in the prototype system are overviewed. The actual design of the SVD DAQ system contains a readout LSI board and a so called DMA master module besides the data scanner and slave memory module. In the current prototype test, instead of using the readout system on the LSI board, which comprises a preamplifier and its control circuit, we use a simple circuit for emulating signals (analog and digital) which come from the detector readout system.

The DMA master module is a VME module which is used to merge the addresses of data which are fragmented over several slave memory modules, and to collect and build one contiguous event data via a local address bus and the VMEbus. We have already designed the system. Since its functionality will be best displayed when more than a few minimal units take part in the data taking, we will not hurry in its construction.

A. Data Scanner board

We use a total of 48 data scanner(DS) boards in the actual SVD DAQ system. While two DS boards will manage signals from a detector unit in the outer layer, one DS will do so for a detector in the inner layer. The main tasks of this DS stage are:

1. to do Analog-to-Digital(AD) conversion of the received signals from an LSI board,
2. to perform formatting of the digitized signals with their channels as a hit basis and
3. to store them in an intermediate buffer in order to release inhibit of the preamplifier circuit as soon as possible.

For these operations in the DS board, since processing in each DS board can be made independently of the other boards, we adopt a parallel distributed method for the overall data acquisition system of the SVD.

For the buffer managing business, we introduce a CPU, Transputer T805 of SGS Thomson. Transputer has four embedded serial interfaces(links) to communicate to other Transputers in a system. The transfer rate of the link is about 1.8 MBytes/sec. A user can use this link with a plug-in-cable and can make transactions of any protocols over the link if the user specifies the protocols in the control software. A Transputer is therefore suitable as a basic element of our parallel distributed system. In Figure 1 we show the conceptual structure of a DS board.

Fig. 1 Block diagram of the data scanner system

The analog and digital mixed data are sent from a custom chip called control-C on a readout LSI board, and then are received by a receiver chip on the DS board. The analog data are AD converted and put in the FIFO memory together with the channel number. This data formatting is done by a sequencer of a so called control-A chip. The Transputer initiates the sequencer. When the data formatting is finished in the sequencer, the control-A interrupts the Transputer and the data stored in the FIFO are moved

to an event buffer of the SRAM under the Transputer control. The formatted event data are eventually output serially through a link to the next stage. The total sequence in the DS is driven by a 16 MHz clock.

B. Slave Memory Module

While the DS boards are located in the vicinity of the detector, we have to bring the event data to the VME buffer where the BELLE central DAQ system can access. Then, as the next stage of the data processing, we introduce a slave memory module(SMM) board. This board receives the data from a DS board, which are sent through the links, and puts them into a dual port RAM(DPM) from the Transputer side. The another port of the DPM faces to the VME data bus. Figure 2 shows a block diagram of the slave memory module. In the present system the SMM operation is based on 33 MHz clock.

Fig. 2 Block diagram of the slave memory module(SMM) system

III. SETUP OF THE PROTOTYPE SYSTEM

The prototype DAQ system, which we constructed, consists of one set of the minimal system(DS and SMM boards) and one VME master system which we use a board of SGS Thomson(INMOS) product called B016[3] for the current setup. The emulation of the detector signal is made by a circuit which generates analog hit signals and their channel numbers (digital signals). We call this circuit board a readout emulation board. The height of the analog signals and the channel numbers are adjustable by the Transputer although all of the channels have the same analog signal and the number of the hit channels is always fixed as 28. This number is determined as the average number of hits for a minimal unit, or equivalently for a detector unit in the inner super layer. The number of channels processed is smaller than the total number of channels connected to one minimal unit, which is about 2000. This is due to application of the sparsified data scan technique installed in the readout system. B016 is a VME module

and contains the Transputer T801 and the 4 Mbytes memory which is not a DPM, but we can access from both the Transputer side and the VME bus side. We can use this as a VME master or slave by changing the internal configuration accessible from the Transputer side.

Fig. 3 Setup diagram of the prototype DAQ system with emphasis on the Transputer network

The data taking sequence is as follows: a forced Trigger is generated by the Transputer on the DS according to a Poisson distribution with a mean frequency; an interrupt occurs for this Trigger to allow the Transputer to move data from the FIFO to its event buffer and reset the readout emulation board so that it can accept the next Trigger; the data stored in the event buffer is sent to the SMM via the INMOS link; all of these three processes are run parallel and independently; the DPM buffer on the SMM is managed by two Transputers in which the input side is controlled by one on the SMM while the output side is done by one on B016; actually, the data sequence is terminated when the SMM is acknowledged to the data strobe of B016.

IV. RESULTS

The buffer managing system in the DS Transputer makes it possible for the system reset just after event information is stored in the event buffer. The system can be ready for the next Trigger before the data are sent and stored in the VME buffer. Thus, the capability of the front end system is determined simply by measuring the live time fraction of the DS system, which has been already published in [4], but with old control software. Our definition of the live time fraction (ϵ) is $\epsilon = \frac{1}{1+f\tau}$, where f is the trigger rate and τ the time needed to process one trigger. We have measured τ and calculated the live time according to the equation. The most up-to-date version of a plot for the live time versus the Trigger frequency is shown in Figure 4. We made the measurement with a fixed data length based on the fixed number of hits given by the emulator

board.

Fig. 4 Live time fraction versus the Trigger Rate for fixed event size (28 hits))

For the present situation we can not vary the event length in the measurement due to the hardware constraint. In order to extend this measurement for the general consequence of system performance, we performed a Verilog system simulation for the current prototype system. After we found good agreement of the data shown in Figure 4 with the simulation, we studied the live time fraction in terms of the event size for various Trigger rates. In Figure 5 we show a plot of this relation. The abscissa indicates in bytes the event size. We designed the event format to have a unit of eight bytes for one hit. A detailed discussion of the simulation for the SVD DAQ system can be found in [2].

Fig. 5 Verilog Simulation: Live time fraction versus Event size for various Trigger rates

The next measurement concerns the output capability of the minimal system to the VMEbus. We measured the transfer rate in the VMEbus from the DPM of the SMM to the current master system of B016. In this measurement we varied the minimum data size with 20, 200 and 800 bytes for one event transfer. We stored some artificial data with various lengths in the DPM of the SMM and moved them to B016 buffer. We then measured the data transfer duration in terms of the total buffer length to be transferred for these three transfer units. Figure 6 shows the results. All three curves are well fitted with a simple linear form. The fitting results are also shown in the

figure. The offset of a fitting line means the time needed for initialization of the data transfer. The offsets of the lines are scattered in $60 \mu\text{sec} \pm 30 \mu\text{sec}$. An inverse of the linear coefficient is the transfer rate. For a transfer unit of 200 bytes, a transfer rate of 4.8 Mbytes/sec is observed from its slope. If a total of 1000 hits is generated in all of the detector units of the SVD under a 500 Hz trigger rate, a band width of at least 4 Mbytes/sec is required because of 8 Kbytes/2 msec. The present measurement of 4.8 Mbytes/sec passes this criterion.

Fig. 6 Data transfer time from the DPM of the SMM to B016 versus data size. Transfers are performed in 20, 200 and 800 bytes unit

In this prototype setup, we used B016 as the VME master. If we use another VMEbus master module which accesses the VMEbus faster than the B016 module, we can achieve a higher rate of the event transfer without any modification of the minimal system. We checked this possibility. For a four bytes transfer of the SMM, it firstly asserts AS* (address strobe), which is indicated in the second wave in the logic analyzer chart shown in Figure 7.

Fig. 7 Timing chart of VMEbus read Process for the VMEbus master B016

After three clocks, it sets DTACK* (Data Acknowledge) and waits. At three clocks later than the negation of DS0* or DS1* by the master module B016, the SMM negates

the DTACK*. Then, the sequence terminates. The SMM needed inherently three clocks for its reaction time. The time duration between the DTACK* asserted by the SMM and the negation of the DS0* or DS1* is due to the response time needed for the master module. In the present case, B016 takes about seven clocks, as one can count from Figure 7. If we use a master module of the most ideal one, which takes only one clock for this time duration, the four byte transfer takes only seven clocks (3+3+1). The SMM is driven with a 33 MHz clock. We will be able to achieve 15 MByte/sec data transfer. It is, thus, the VMEbus master, not the SMM module, which binds the data transfer rate from the SMM to the master module.

V. SUMMARY

In the present study, we made a prototype system of the SVD DAQ. Actually, the system was a minimal part, which consisted of one DS and SMM. The detector signals emulated in the readout emulator board were successfully processed through the DS, SMM and eventually stored in a VME memory buffer.

Although the hardware system was still prototype, we confirmed that all of the intended operations of the hardware and software worked according to our expectations. The DS live time fraction was more than 94% with a Trigger rate of 1 KHz when the number of hits was about 30. The data of the live time fraction versus the trigger frequency agreed well with the verilog system simulation so that we could predict this relation with other event sizes.

We measured the VMEbus event transfer rate from the SMM to the master system B016, which we used temporarily in this setup. The rate was found to be 5 Mbytes/sec. This value just satisfied our requirement of the data transfer, which is to transfer 10 KBytes within 2 msec. However, after an inspection of the timing chart of the VMEbus transfer, we found that the transfer rate was bounded by the access speed of the master module. If we can use another master module or construct a dedicated one, we can achieve transfer rate of up to 15 Mbytes/sec.

REFERENCES

- [1] M.T.Cheng et al., the BELLE Collaboration, "Technical Design Report", KEK Preprint 95-02, 1995.
- [2] M.Tanaka et. al., "Data Scanner and Event Builder for the SMVD of the KEK B-factory", IEEE Trans. on Nuclear Science, 41, 252, 1994.
- [3] INMOS limited., IMS B016 VMEbus master card, Nov., 1991.
- [4] C.Fukunaga et al., "Data Scanner System of the Belle Silicon Vertex Detector", proceedings of RT95 conf., Michigan State Univ., MI, USA, May 1995.