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Preliminary test results from a single-sided two-dimensional detector using pMOS pixels *

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Abstract

As a part of the R&D for the BELLE experiment at the KEK-B-factory a strip-like two-dimensional readout single-sided detector using pMOS pixels has been developed and tested. It may be used in upgrades of the vertex detector. A double drain pMOS transistor, implanted in the $100 \times 100 \mu\text{m}^2$ n-well collecting electrode, amplifies the signal, while the low detector capacitance lowers the noise. A high signal-to-noise ratio is expected. Ganging the pixels at the drain nodes in a strip-like configuration provides a two-dimensional readout. The superior characteristics of the proposed device are attractive for charged particle detection as well as X and γ -rays.

We present here results from electrical and IR light tests of prototypes of the pMOS pixel.

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1 Introduction

1.1 A pMOS pixel

To overcome the limitations of the double-sided silicon strip detector to be used in the first stage of the BELLE-SVD [1], we propose a pMOS pixel detector for possible upgrades. A theoretical study has been previously published [2]. Figure 1 shows a schematic view of the proposed single-sided, two-dimensional readout device. In a $300\mu\text{m}$ thick substrate a p^+ area is implanted on the back side, and n^+ areas are implanted on the top, forming a pin diode. The n^+ area is composed of a $200\mu\text{m}$ pitch array of n^+ wells. Each n-well is separated from adjacent ones with LOCOS¹. A pMOS transistor is implanted in each n-well, providing amplification of the signal. The drains of this double drain pMOS transistor are ganged together with metal strips in X and Y direction, providing a two-dimensional strip-like readout on a single-sided device. With a built-in amplification and a pixel configuration a high signal-to-noise ratio is expected for this pMOS pixel detector. The design parameters for the pMOS pixel are listed in Table 1.

1.2 Operation principle

The operation principle of the pMOS pixel is described in the bottom part of Figure 1. The detector bias voltage is applied to the back side p^+ implantation while the n-well is grounded through the bias resistor (R_B). As in strip detectors, charged particles are detected in the depleted junction. The signal charge (Q_0) deposited in the substrate is accumulated on the n-well, and decays through the bias resistor. The accumulated charge provides a voltage shift in the n-well (V_{sub}), which modulates the drain current (I_d) of the pMOS transistor operating in the saturation region. The drain current is then differentiated through the R_0C_0 network before being fed into the preamplifier.

The properties of the pMOS pixel during signal processing, such as amplification and noise performance, have been presented in [2]. In order to extract a signal from the charge accumulation in the n-well, the time constant of the differentiation network ($t_0 = R_0C_0$) is chosen to be much shorter than the decay time in the n-well. The charge amplification gain (A), is given for each pixel by

$$A = \frac{g_{sub}t_0}{C_B}, \quad (1)$$

where C_B is the n-well-to-back capacitance and $g_{sub} = dI_d/dV_{sub}$ the transistor's back-transconductance which represents the drain current sensitivity for an input signal on the n-well node. Assuming a RC-CR type shaping amplifier which shaping time (τ_s) equals the differentiation time, the electronic noise charge per pixel(enc) is calculated as

$$enc^2 = \frac{e^4}{128} \frac{s_n^2 C_B^2}{\tau_s} + \frac{3e^4 p_n^2 \tau_s}{128}, \quad (2)$$

where

$$s_n^2 = \left\{ \frac{8kT}{3} (g_m + g_{sub}) + (2qI_d + \frac{4kT}{R_0}) \right\} \frac{1}{g_{sub}^2}, \quad (3)$$

and

$$p_n^2 = 2qI_L + \frac{4kT}{R_B}. \quad (4)$$

I_L is the leakage current per pixel. Parameters for the proposed signal processing are listed in Table 1.

¹LOCOS stands for LOCal Oxidation of Silicon

2 Prototypes fabrication

To verify the pMOS pixel feasibility and measure its performances, we designed and fabricated pMOS pixels prototypes. At the present stage, the prototypes include single pixel and 3×3 pixels test structures.

2.1 Design

The different test structures are designed in independent samples. Each sample consists of a 7×7 n-wells array. The test structure is located in the middle of this array and the outer n-wells are connected together forming the well-ring. The p^+ back side implantation is located in the middle of the sample, surrounded by a p^+ ring and drawn $500\mu\text{m}$ wider than the n-well array, so that the electric field underneath it, is vertically oriented.

The pin diode is surrounded on both side by n^+ guard-ring which isolate the sensitive area in the middle of the sample. The well-ring and guard-ring on the top side are grounded while the back side guard-ring is kept floating.

The n-wells are isolated between each other when the pin diode is fully depleted. As they are implanted in a n-type substrate, electrons may accumulate underneath the LOCOS and short all the detecting elements together. To prevent this, we add a floating p^+ stopper ring around each n-well.

2.2 Process

The prototypes were processed in a $1.2\mu\text{m}$ CMOS technology at Seiko Instruments Incorporation. 4 inch diameter and $300\mu\text{m}$ thick wafers are used. The substrate is a high resistivity n-type ($4\text{k}\Omega\text{cm}\sim 6\text{k}\Omega\text{cm}$) silicon, and (100)-oriented. The pMOS pixel requires a gate oxide of at least 300nm thick. To obtain such a thickness, the oxide is grown with typical $1\mu\text{m}$ thick LOCOS. A few prototypes include a bias resistor processed in high resistive polysilicon.

2.3 Samples

Single pixel test structures

Different types of test structures are designed. A single n-well is for measurements of the pin diode leakage current and the detector capacitance. A single n-well containing a single drain pMOS transistor will be used to check the transistor operation and properties (PIXEL02). With a double drain pMOS transistor implanted in a single n-well the two-dimensional readout possibility will be checked. A single n-well containing a single drain pMOS transistor and a polysilicon bias resistor in between n-well contact and source is designed (PIXEL03). This basic structure of the pMOS pixel will be used to check the detection of particle by the pMOS pixel. The possibility of integrating the bias resistor on the device itself during the fabrication is verified, too.

3×3 pixels test structures

Two 3×3 pixels test structures are designed to test the pMOS pixel behavior in an array. PIXEL08 is a 3×3 n-wells test structure to be used to check the charge sharing of the n-wells array. PIXEL11 is a 3×3 pixels with double drain pMOS transistor in the n-wells, and with the drains X and Y ganged in column and row respectively. It will be used to check the feasibility of the strip-like idea.

3 Electrical properties

In the first step we measured electrical parameters of the pMOS transistor and pin diode. The measured parameters are summarized in Table 3.

3.1 pMOS transistor characterization

We measured the pMOS transistor DC characteristics and determined its operation point on the $I_d V_G$ characteristic. We chose the gate voltage which provides 200nA drain current. The operation point is visualized with the "marker" on Figure 2(a). This figure is the typical $I_d V_D$ characteristic of a pMOS transistor, it has been measured on the pMOS transistor implanted in the n-well. The good nature of the IV curve is observed. The transconductance $g_m = dI_d/dV_G$ is calculated on the $I_d V_G$ characteristic. The pMOS transistor back sensitivity can be simply checked by applying a potential on the n-well node which simulates the potential shift. On the $I_d V_{well}$ characteristic shown in Figure 2(b), the back-transconductance $g_{sub} = dI_d/dV_{well}$ is calculated. During this measurement, the transistor was kept at its operation point determined previously, such that the "turn-on" due to the back-gate can be visualized.

3.2 pin diode parameters

The leakage current per pixel is measured under such condition that -50V bias voltage is applied on the back-side while n-well, well-ring and guard-ring are grounded. The average leakage current over the different samples is 300pA.

The resistance of the polysilicon bias resistor located in between the source and the n-well contact is measured on PIXEL03. The average bias resistance is $1G\Omega$. These results yield to a voltage shift in the n-well of 300mV, which consequences will be discussed in section 4.2.

3.3 Pixel capacitance

To measure the total detector capacitance per pixel (C_P), we use the model proposed by S.Kavadias [3], where $C_P = C_B + 4C_i + 4C_j$ with C_i and C_j are the inter pixel capacitances between adjacent neighboring pixels on the same row and column, and between diagonal pixels, respectively.

4 Test with IR light

In a second step the prototypes are tested with a 1071nm-wave-length infra-red light.

4.1 Output signal from the drain

The target for evaluation was PIXEL03. The output signal at the drain node is measured in the differentiation readout configuration described in section 1. The measured pulse height (Signal), the signal-to-noise ratio ($S/N = \text{Signal}/\text{NoiseRMS}$) and the deduced charge amplification gain ($A = \text{Signal}/\text{Reference}$) and electronic noise charge ($enc = Q_0 N/S$) are listed in Table 3.

Using the DC parameters measured in section 3, the expected values of the charge amplification gain and electronic noise charge are calculated using Eqs (1) and (2). The electronic noise charge is as expected between 500 to 600electrons. Even though a charge amplification gain of about 8 is calculated at this operation point, it is measured to be of only about 1.2, which is related with the discussion in section 4.2. The details are described below.

4.2 Operation with a high bias resistor

In order to understand the low charge amplification, the pMOS pixel operation is checked with PIXEL02, which is biased with an external resistor R_B . The measurements described below are performed with different resistor values; 2 of them are summarized in Table 2.

For a large bias resistor, the current flowing in the source is larger than the drain current. A certain amount of current is flowing into the n-well (I_{well}), in the source-to-well diode and/or in the bias resistor, leading to a polarization of the n-well (V_{well}). The current flowing in the bias resistor is calculated as

$$I_R = \frac{V_{well}}{R_B}. \quad (5)$$

If the source-to-well is forward-biased, the current flows as controlled by the IV characteristic given by

$$I_D = I_s(e^{\frac{qV_{well}}{nkT}} - 1) \quad (6)$$

where $I_s = 67pA$ and $n=1.03$ are the diode parameters measured on the IV characteristic. Considering that the current flows in the source-to-well diode, the n-well potential is calculated to be negative, the diode is forward biased. Its dynamic resistance R_D is calculated as

$$R_D = \frac{\delta V_{well}}{\delta I_D} = \frac{nkT/q}{I_D}. \quad (7)$$

The dynamic resistance is found to be much smaller than the bias resistor, which explains the fact that the leakage current flows into the source-to-well diode instead of flowing into the bias resistor.

In terms of signal processing for the pMOS pixel, this means that the charge decay, in the n-well, through the dynamic resistance of the source-to-well diode. The decay time is therefore quite fast ($\tau = R_D C_P \approx 1.3\mu s$) compared with the differentiation time ($t_0 = 1\mu s$). The fast decay does not provide a voltage shift in the n-well long enough to be differentiated and transferred to the preamplifier.

It is not a good solution to use smaller R_B than R_D to have the leakage current flowing into the bias resistor and thus keep the source-to-well diode reverse biased. The pMOS transistor operation is correct, but since the dynamic resistance of the not-strongly-reverse-biased source-to-well diode is rather low ($200M\Omega$), the decay in the n-well is too fast for the differentiation network being able to process any signal. In such a case the signal can be seen in a direct readout configuration as explained in next section.

4.3 Pixel array

We understand by charge sharing how the charge deposited are collected by only one n-well, depending on the photon beam impact. To verify it, we shine the IR light on a 3×3 n-wells array. The charge sharing can simply be visualized with a 3-dimensional representation of the pulse height measured on the n-well array. Figure 3 shows the pulse height measured on the n-well nodes of PIXEL08. The hit on a n-well delivers 13500electrons, without sharing with the neighbor. The n-well isolation is perfectly operating.

Eventually the possibility of a strip-like readout configuration is checked by shining the IR light on PIXEL11. This sample consists of a n-well array with double drain pMOS transistor implanted in them. Drains X_i and Y_j are ganged for strip-like readout. No polysilicon bias resistor are included in this sample. The output signal is extracted from the drain node in a

direct readout configuration mode. $t_0 = 1ms$ is chosen to be much larger than the decay time in the n-well, therefore the accumulated charge is directly transferred to the preamplifier. But such a simple method is very slow and can not be use in real detector application.

A preliminary measurement of the position resolution obtained is given Figure 4 where Y_{ac} is the analog calculated position and y the true photon beam impact location. The position resolution is calculated to be of $41.2 \mu m$.

5 Summary

To summarize we list designed and measured parameters, expected and measured performances of the pMOS pixel, Table 3.

- The pMOS transistor implanted in a n-well showed good operation.
- The feasibility of a pMOS pixel for charged particle detection was checked.
- By ganging the pixels in pixel-line a two-dimensional strip-like readout detector can be designed.

The measured large leakage current and pixel capacitance are the reasons for the lower gain and larger electronic noise charge than expected. Further studies are on going to explain it, and to propose another pMOS pixel biasing configuration. We are now preparing the design of improved new prototypes.

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Detector thickness,	d	$300\mu m$
Pixel area,	A_d	$200\mu m$ by $200\mu m$
N-well area,	W_{well}	$100\mu m$ by $100\mu m$
Gate size,	W/L	$4\mu m/4\mu m$
Gate oxide thickness,	t_{ox}	330nm 540nm(typ) 1100nm
Drain current,	$I_{d(DC)}$	200nA
Transconductance,	g_m	$0.56\mu S$
Back-transconductance,	g_{sub}	$3.03\mu S$
Capacitance of differentiation network,	C_0	$1pF$
Resistance of differentiation network,	R_0	$1M\Omega$
Differentiation time constant,	$t_0 = R_0 C_0$	$1\mu s$
Shaping time,	τ_s	$1\mu s$

Table 1: Parameters for the pMOS pixel.

Bias resistor,	R_B	$820k\Omega$	$820M\Omega$
Drain current,	I_d	-275 nA	-4.45 μA
Well current,	I_{well}	0	$\approx 20nA$
Current in R_B ,	I_R	$I_L=300pA$	180pA
N-well potential,	V_{well}		
	calculated	-0.246mV	-147mV
	measured	-0.240mV	-258mV
Source-to-N-well diode		Reverse	Forward
Dynamic resistance,	R_D	$\approx 200M\Omega$	$1.3M\Omega$
Decay in the n-well,	in	$(R_B//R_D) \approx R_B$	$(R_B//R_D) \approx R_D$
	$\tau = RC_P$	820ns	$1.3\mu s$

Table 2: Behavior of the pMOS pixel biased with different R_B .

Process parameters		
Gate oxide thickness	t_{ox}	1136nm
Deep n-well concentration	N_D-	$1e16at/cm^3$
N-well channel concentration	N_D+	$3.9e17at/cm^3$
Electrical parameters		
at $V_g=-52V$		
Drain current	I_d	1700nA
Transconductance	g_m	$0.37\mu S$
Back-transconductance	g_{sub}	$8.3\mu S$
Leakage current at $V_{bias} = -50V$	I_L	300pA
Polysilicon resistor	R_B	$1.4G\Omega$
Bulk capacitance,	C_B	0.025pF
Inter-pixel capacitance,	C_i	0.058pF
	C_j	0.04pF
Total pixel capacitance,	C_P	0.42pF
Performances	calculated	measured
Charge Gain, $A = g_{sub}R_0C_0/C_B$	A=8.3	Signal= -176mV 1.1
Electronic Noise Charge	enc=406electrons	S/N=30 625electrons
Position resolution	σ_y	$41.2\mu m$

Table 3: Measured parameters and performances of the pMOS pixel

Figure captions

Figure 1 The upper part is a schematic view of the pMOS pixel detector with strip-like two-dimensional readout. And a schematic description of the pMOS pixel operation principle appears in the bottom part.

Figure 2 (a), $I_d V_D$ and (b), $I_d V_{well}$ characteristics of the pMOS transistor implanted in the n-well.

Figure 3 Charge collection over the n-well array.

Figure 4 Variation of the analog calculated position Y_{ac} with the true photon beam position.

pMOS pixel: Double DRAIN pMOS Transistor in the N-well

Figure 1:

Variable1:
 VD -Ch1
 Linear sweep
 Start .0000V
 Stop -5.0000V
 Step -.0800V

Variable2:
 VG -Ch4
 Start -40.200V
 Stop -41.800V
 Step -.4000V

Constants:
 VW -Ch2 .0000V
 VS -Ch3 .0000V

Variable1:
 VWELL -Ch4
 Linear sweep
 Start .2000V
 Stop -.2000V
 Step -.0100V

Constants:
 VS -Ch1 .0000V
 VD -Ch2 -1.0000V
 VG -Ch3 -42.000V
 WR -Vs1 .0000V
 GR -Vs2 .0000V

GSUB (A/) = $\Delta I_D / \Delta V_{WELL}$

Figure 2:

Figure 3:

Figure 4: