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**A self adjustment technique minimizing channel to
channel variations in VLSI readout chips ***

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Abstract: Modern VLSI readout chips for strip and pixel detectors contain many electronic channels which all should behave exactly alike in order to give the optimal performance. However, good matching is often very difficult to achieve due to many design constraints. In this paper, a simple concept for automatic adjustment of important VLSI circuit properties simultaneously in all readout channels is presented. The tuning is performed by applying a test injection pulse and, if necessary, a reference signal to all cells simultaneously. A simple circuit in each channel adjusts the control voltage on a storage capacitor until matching is optimal. An application of this concept in a self adjusting delay circuit is presented and other possible applications are discussed.

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Abstract

Modern VLSI readout chips for strip and pixel detectors contain many electronic channels which all should behave exactly alike in order to give the optimal performance. However, good matching is often very difficult to achieve due to many design constraints. In this paper, a simple concept for automatic adjustment of important VLSI circuit properties simultaneously in all readout channels is presented. The tuning is performed by applying a test injection pulse and, if necessary, a reference signal to all cells simultaneously. A simple circuit in each channel adjusts the control voltage on a storage capacitor until matching is optimal. An application of this concept in a self adjusting delay circuit is presented and other possible applications are discussed.

1 Introduction

Semiconductor detectors with VLSI readout electronics are widely used in particle physics [1] and gain increasing importance in biomedical and other applications. While early readout chips for strip detectors contained only charge sensitive preamplifiers and fairly simple readout schemes [2], modern chips for special applications often include additional circuitry like comparators for hit detection or sparse readout capabilities [3]. This requires very compact designs, especially for pixel readout chips [4][5], where preamplifier, discriminator and sparse readout logic must fit onto a circuit area of only $\approx 0.02 \text{ mm}^2$. Each

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pixel circuit may only dissipate very little power (a maximum power dissipation of $\approx 60\mu W$ per Pixel is allowed in the ATLAS experiment) in order to keep the self heating of the chips at a reasonable level.

While an *offline* correction of pedestals or gain values for every individual channel is possible for the 'simple' readout concepts, this is no longer true for more complex readout schemes and applications with more than 10^6 channels. Channel to channel variations in gain, dc-offset or comparator threshold result in a loss of data or excessive noise hit rates, which has to be avoided. Therefore it is necessary in these systems to achieve a very good uniformity of several circuit properties among different channels and, even more importantly, among different readout chips. The requirements of small circuit area, high speed, low power consumption and good channel to channel matching often cannot be fulfilled simultaneously. Furthermore, chip to chip component mismatch, temperature effects, ageing and the deterioration of transistor properties after radiation damage have to be considered.

In this paper, we propose to simplify the chip designs and to improve circuit performance by dropping the requirement of matching circuit properties. Instead, matching performance is achieved by providing the possibility for *adjusting important circuit properties* individually in each channel. With the proposed simple concept, it is possible to perform these adjustments simultaneously in all channels with no need for external action on each cell (as it would be the case if, for example, DACs or analog storage cells were programmed externally for each cell). Even the several thousand cells of a pixel chip can thus be tuned very easily. Due to a slow drift of the parameters with time, the adjustment has to be regularly refreshed. This should be possible even in accelerator experiments and is straightforward e.g. in biomedical applications. A major advantage of this concept is the complete independence of channel parameters from component matching, temperature, ageing and radiation induced damage.

After a general description of the concept, we describe a self adjusting timer circuit suitable for pixel readout applications as an example and then discuss briefly other possible applications.

Fig. 1. General concept of a self adjusting circuit

2 General Concept of Self Adjusting Circuits

In order to adjust circuit properties individually in each cell of a multi-channel circuit, a corresponding control value has to be stored in each cell. The simplest way is to use a voltage stored on a capacitor, as indicated in fig. 1 (other solutions are possible). This voltage controls the property which is to be adjusted like the threshold of a discriminator, the gain of an amplifier or internal delays. It can be increased and decreased in very small steps by a simple charge redistribution circuit. The decision whether to increase or decrease the control value is taken by an evaluation section in each cell which analyses the output of the circuit. This section may compare the output signal with an external reference signal which is distributed to all cells. The adjustment procedure is very simple: the evaluation circuits in all cells are enabled by a global signal, and input pulses as well as a possible reference signal are distributed to all cells. After each test injection, the control voltage in each cell automatically increases or decreases in small steps until the desired output behaviour is reached. It is evident that care must be taken to reduce all possible leakage currents which may slowly discharge the storage capacitor and therefore produce a slow drift of the control voltage. Regular 'refresh' tuning cycles will therefore be needed in this analog concept which can be easily accepted as long as the rate is reasonably low. A digital storage of the control value is also possible, but such solutions require much more chip area.

3 A Self Adjusting Monostable Circuit

As an example, a self adjusting monostable circuit has been designed, build and tested. The circuit can be used in pixel readout chips like the LHC1 chip, which is presently being developed at CERN, based on the OMEGA design [5]. After a short description of the LHC1 chip, the self adjusting monostable circuit is described, measured results are presented and possible improvements are discussed.

Fig. 2. Simplified pixel cell of the LHC1 chip

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- (i) A *ramp generation circuit* which consists of switch $S1$, current sources I_{coarse} and I_{fine} and capacitor C_{ramp} . The input signal IN opens $S1$ which starts a linearly decreasing ramp at C_{ramp} . Current source I_{coarse} provides the major part of the current needed to discharge C_{ramp} in the desired delay time T_{del} , while current source I_{fine} is controlled by the voltage V_{fine} and supplies a small correction current. V_{fine} can be different in each channel and is adjusted by the feedback loop. Increasing V_{fine} results in a higher current I_{fine} which discharges C_{ramp} faster and produces a shorter T_{del} . (The extra current source I_{coarse} is used to keep the current through I_{fine} as small as possible in order to obtain a small $\partial T_{del}/\partial V_{fine}$.)
- (ii) A *comparator* with threshold close to GND which simply consists of four cascaded inverters to provide a fast output signal. C_{ramp} is, in fact, the parasitic input capacitance of the comparator.
- (iii) A simple *logic* (consisting of 2 three-input gates). It compares the external reference signal REF with the output of the comparator OUT and generates a *faster* or *slower* signal depending on whether the delay time T_{del} is too long or too short, respectively. The $ENABLE$ -signal is used to switch off the regulation.
- (iv) A very simple *charge redistribution circuit* consisting of four transistor switches $S2 - S5$, the (parasitic) capacitors C_{hi} and C_{lo} and the storage capacitor C_{fine} (which is implemented as the gate capacitance of the I_{fine} current source transistor) is used to increase or decrease the control voltage V_{fine} in small steps.
- (v) The *pass transistor* $S6$ which isolates the storage capacitor from the charge redistribution circuit in order to reduce the drift of the control voltage to a minimum.

Before an input signal is applied, the capacitors C_{hi} and C_{lo} are charged to voltages V_{hi} and V_{lo} , respectively, by closing switches $S2$ and $S5$ with the $PRECHARGE$ signal. An input signal is then applied ($S1$ is opened). The voltage at C_{ramp} decreases linearly and when the threshold of the comparator is reached after the time T_{del} , the OUT -signal becomes active. If the OUT -signal is faster than the reference signal REF , the logic generates a *slower* signal which closes switch $S4$. This decreases V_{fine} by a small amount (which depends on the difference between V_{fine} and V_{lo} , on the ratio between C_{lo} and C_{fine} , the resistance of the switches and the time mismatch) resulting in a longer T_{del} in the next cycle. Correspondingly, V_{fine} is increased if T_{del} is too long. After many cycles, the output signal and the reference signal coincide. Further regulation is disabled with the $ENABLE$ signal. This signal also controls the pass transistor $S6$ in order to reduce leakage currents which might discharge C_{fine} .

It is obvious that the regulation steps using the simple charge redistribution circuit a priori do not depend on the time difference between the output and reference signal. A slightly more complicated circuit using switched current

sources (as used for instance in [7]) can have regulation steps which are proportional to the time mismatch. Such a circuit would therefore converge faster to the correct delay time. In practice, a fast regulation of large differences between *OUT* and *REF* is not needed (assuming that this is done only once), and therefore the simpler circuit, which also has less charge injection problems, is used. For very small time differences between *OUT* and *REF* (some ns), the regulation steps become in fact smaller in this circuit because the charge redistribution is not complete. This leads to a very smooth regulation and a low time jitter when the regulation is operating.

In a realistic application, the test signal should be injected at the input of the preamplifier so that delay time variations in other parts of the circuit are included in the calibration as well.

Finally, it should be noted that due to the automatic adjustment, component matching is uncritical in the whole circuit. The precise value of the threshold of the comparator, for instance, is of no importance.

3.3 Circuit Performance

The circuit which was described in the previous section has been implemented using the MIETEC $2.4\ \mu\text{m}$ technology. 28 FETs are used to implement the ramp generation (3), the discriminator (8), the logic (12), the charge redistribution section(4) and the pass transistor (1). The circuit is operated with a supply voltage of 5 V, voltages $V_{lo} = 0\text{ V}$, $V_{hi} = 2\text{ V}$ and a current $I_{coarse} = 120\text{ nA}$ which supplies 80% of the current needed to discharge $C_{ramp} = 90\text{ fF}$ within the desired delay time $T_{del} = 2\ \mu\text{s}$. This choice of I_{coarse} leads to a range of possible delay times from $300\text{ ns} \cdots 2.4\ \mu\text{s}$. The rms time jitter of the *OUT*-signal without regulation is below 1 ns and increases to about 1.5 ns when the regulation is active. The regulation time steps are $\approx 20\text{ ns}$ (depending on V_{hi} and V_{lo}) for large time differences between *OUT* and *REF*, and they get smaller for smaller time differences as explained above. For example, an initial time mismatch between *REF* and *OUT* of 200 ns is readjusted after ≈ 10 cycles.

When the regulation is switched off, the delay time slowly drifts to lower values with a rate of below 1 ns per second at room temperature. The drift increases strongly with increasing chip temperature or with light exposure due to increased leakage of the reverse-biased drain-well-diode of pass transistor *S6*.

As these measurements show, this circuit is suitable for an application in an ATLAS pixel readout chip. Its time jitter is small (1 ns) compared to the 25 ns bunch crossing intervall and its time drift being less than 10^{-9} , the

refresh cycles can have an extremely moderate rate of below 5 Hz .

Fig. 4. Improved self adjusting delay circuit

3.4 Possible Circuit Improvements

Following the general idea of the prototype circuit, several improvements are possible:

- The well of the pass transistor can be connected to a voltage which always equals V_{fine} (supplied by a simple unity gain buffer) so that leakage to the well is suppressed even more.
- The logic gates can be incorporated in the charge redistribution circuit which reduces the number of transistors.
- Finally, a process with smaller transistor dimensions will automatically improve on the drift due to a favorable scaling of the ratio between gate capacitance and drain leakage current.

Figure 4 shows an improved analog circuit using only 19 transistors which is presently under test.

It should also be possible to use analog EEPROMS [8] to permanently store V_{fine} so that tuning has to be performed only once.

The digital storage of control values eliminates the drift problem, but the circuit gets more complicated and requires much more chip area. In multichannel systems, however, parts of the feedback circuit, like the Evaluation Section,

are needed only once. The tuning is then performed sequentially by connecting individual cells to a common Evaluation Circuit.

4 Examples for Other Applications

Some other examples for the application of self adjustment are given.

The most interesting case probably is the **correction of threshold variations of discriminators** where the requirements of good threshold uniformity, low power consumption and fast response time are hard to fulfill simultaneously. The adjustment of thresholds does not need an external reference signal: all channels are pulsed with the desired threshold charge through on-chip pulsing capacitors (or via the detector backplane, if possible). If the discriminator fires upon an injection, its threshold is increased. The threshold is decreased if the discriminator does not fire. After many cycles, all discriminator thresholds correspond exactly to the injected charge. It should be noted that this procedure automatically corrects for gain variations in the preamplifier. This method requires good matching of the on-chip charge injection capacitors which is usually the case for devices with the same geometry [9].

Another example is the **automatic masking of noisy channels**. The procedure here is even simpler. After resetting mask flipflops in all channels, the chip is operated normally without any input signals applied. If a discriminator fires, it automatically sets the mask bit of its cell and disables further unwanted signals. This method does not require a shift register or similar circuitry to access the individual mask flipflops.

A **compensation of detector leakage currents** can be performed with adjustable current sources. In a standard charge amplifier configuration with resistive feedback the compensation current can be adjusted until the dc output level of the preamplifier is in the active range.

The **adjustment of the charge gain** (in an analog readout scheme) is more complicated, because an analog comparator is needed. If such a discriminator is already present in the cell, a two step procedure could be used: First, the comparator is adjusted to a given threshold *voltage* which is supplied externally. Second, the gain of the preamplifier is adjusted as described in the first section with a fixed input charge.

5 Summary

The concept of self-adjusting circuits for VLSI readout chips has been presented. By including a simple regulation circuit in each channel, the adjustment of various circuit properties can be performed without external action on every individual cell by applying test pulses and, if needed, reference signals to all cells simultaneously. The adjustment is then automatically performed independently in each cell.

In order to apply this concept, the chip must contain a precise pulsing possibility for all channels and the chip should be capable of processing a large number of simultaneous signals. If this is not possible, the adjustment has to be performed in smaller groups of channels.

Due to slow drifts in the adjustment values, short 'refresh' cycles have to be repeated regularly. As the deviations from the desired value are very small, only few iterations are needed to reestablish matching. In most applications, the refresh cycles can be performed during already existing dead times so that no additional data loss is introduced. The reduction of the drift and hence of refresh cycles is the most challenging part of the design. The influence of radiation damage and ionizing particles traversing the readout chip have to be studied.

The benefits of self-adjusted circuits are excellent channel to channel matching independent of device properties, ageing or radiation damage, and superior circuit performance due to fewer constraints on the circuit design.

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