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An area efficient 128 channel counter chip^{*}

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Abstract: A shift register of N bit length can be configured (for most N) with a single exclusive-OR gate to generate periodically $2^N - 1$ different states. As each state is directly related to the number of clock pulses received, such a circuit can be used as a counter. The sequential readout of the bit pattern requires nearly no additional logic and many 'shift counters' can easily be daisy chained during readout in a multichannel system. A very regular and compact layout is possible due to the simple structure. The maximum clocking frequency of the circuit is high (above 50 MHz in a 2.4 μm process) and independent of the length. A 128 channel scaler chip has been designed and tested to be used in the Bonn Compton Polarimeter for a fast measurement of beam profiles with silicon strip detectors. Other possible applications of this concept are specialized readout chips for microstrip and pixel detectors.

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An area efficient 128 channel counter chip[★]

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Abstract

A shift register of N bit length can be configured (for most N) with a single exclusive-OR gate to generate periodically $2^N - 1$ different states. As each state is directly related to the number of clock pulses received, such a circuit can be used as a counter. The sequential readout of the bit pattern requires nearly no additional logic and many 'shift counters' can easily be daisy chained during readout in a multichannel system. A very regular and compact layout is possible due to the simple structure. The maximum clocking frequency of the circuit is high (above 50 MHz in a $2.4\text{ }\mu\text{m}$ process) and independent of the length. A 128 channel scaler chip has been designed and tested to be used in the Bonn Compton Polarimeter for a fast measurement of beam profiles with silicon strip detectors. Other possible applications of this concept are specialized readout chips for microstrip and pixel detectors.

1 Introduction

In some applications of VLSI readout chips, e.g. X-ray detection with silicon strip or pixel detectors, digital signals must be counted simultaneously in many channels. This is usually done using standard synchronous or asynchronous binary counters. In order to read out the contents of these counters, a bus system is needed or the counter status is transferred to additional shift registers (one for each counter) which are then read sequentially. Both solutions require additional chip area and circuitry.

In most applications, however, there is no need to generate a counting code of a particular type, like binary or Gray code. In fact, any state machine which

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steps through its possible bit combinations in an unambiguous way can be used as a counter. The simplest way to implement an N bit state machine with a maximum number of states is probably a linear feedback shift register (LFSR) which consists of an N bit shift register and an exclusive OR (or exclusive NOR) gate with two inputs, which feeds back the output and an intermediate tap to the input of the shift register (fig. 1). For most N , it is possible to find a tap T so that the period of the sequence is $2^N - 1$ [1]. This is nearly the same length as for a binary counter with 2^N states.

Fig. 1. Simple linear feedback shift register.

The obvious advantage of such a circuit is its simplicity. It allows a very regular and compact layout and can reach very high counting speeds due to the short logic delay in the feedback path. Furthermore, the complexity of such a 'shift counter' does NOT increase with increasing length N . For the sequential readout of the bit pattern almost no additional logic is needed. Moreover, many counters can be daisy chained very easily in a multichannel system.

A minor disadvantage is the randomness of the generated bit pattern (in fact, this kind of circuit is usually used to generate pseudo random bit sequences) which has to be decoded offline in order to reconstruct the number of counting pulses. For moderate lengths N the decoding can be easily done with the help of a lookup table. For large N , where simple lookup tables are no longer feasible, more involved reconstruction algorithms must be used. It has been pointed out in [2] that it can be advantageous to use taps which generate slightly shorter sequences, but which can be decoded more easily. Another advantage of such near maximal sequences is the fact that configurations which require only one tap (i.e. an exclusive OR gate with only two inputs) exist for all lengths N while maximal length sequences require more than one tap for some N (e.g. all multiples of 8). A list of taps for maximal length sequences up to $N = 100$ can be found in [3], taps for near maximal sequences up to $N = 64$ are given in [2].

A 128 channel scaler chip has been designed and processed using this concept. It will be used in conjunction with a separate preamplifier chip [4] for the fast readout of a silicon strip detector to determine the beam profile in the Compton Polarimeter which is under construction for the measurement of the beam polarisation of the Bonn 3 GeV electron stretcher ring ELSA[5].

2 The 128 Channel Scaler Chip

2.1 Principle of Operation

Fig. 2. Schematic circuit diagram of the multichannel counter with sequential readout and programmable OR-logic.

Fig. 2 shows a schematic circuit diagram of the scaler chip. Each of the 128 channels consists of a 15 bit shift counter (right part) and a simple logic to generate the OR of a programmable subset of the 128 inputs (left part). In each shift counter, the exclusive OR of the last flipflop and the tap at bit 14 is fed back to the input via a multiplexer. With the switch in the lower position, the shift counter is set to the 'counting' mode where clock pulses from the inputs increment the counters ($EnClk = 1$, $ExtClk = 0$). When the switch is set to the upper position, all shiftregisters are connected in series. By clocking all flipflops simultaneously with the *ExtClk* signal, the contents of all counters appears serially at the output *SerOut*. Individual clocking, which would completely corrupt the information in the counters, is disabled during this 'readout' phase by setting *EnClk* to 0. External clock pulses which appear during readout are therefore lost.

An additional OR-logic is included on the chip for debugging, monitoring and triggering purposes. It consists of a static latch and an AND gate with open drain output in each channel as shown in fig. 2. An input signal can pull the *OR*-signal low if the corresponding channel is enabled by setting the latch. The latches are programmed very easily with the help of the shift register which is

loaded serially with the appropriate bit pattern (via the input *SerIn*, clocked by *ExtClk* in 'readout' mode). A *Load* signal then transfers the pattern into the latches.

Fig. 3. Inverting dynamic one phase flipflop requiring only one clock polarity used in the prototype circuit.

2.2 Circuit Implementation and Performance

A minimal chip area was the main goal for the implementation of this circuit in order to allow the inclusion of such counters in other VLSI readout chips. As the flipflops are the main component of the circuit, several different circuit concepts and layout topologies were studied. Finally, a dynamic one phase flipflop [6] was chosen because of its simplicity, speed and robustness (fig. 3). As this flipflop has an inverted data output and an odd number of flipflops is used, an inverter is added to each channel in order to simplify the decoding and clearing (fig. 2) .

The use of a dynamic flipflop significantly reduces the chip area. However, if no clocks appear for a long time, the counters lose their information. Therefore, additional 'refresh' clocks are injected periodically during the 'counting' phase via the *ExtClk* input simultaneously to all counters. As long as their number is known, they can be subtracted in the decoding procedure (even if these clocks overflow the counters). This simple approach introduces a pileup problem: signals which occur during the refresh clock are lost. However, the pileup probability is very small due to the short width of the refresh pulses (10 ns), and known, so that offline corrections are possible. If needed, the pileup can be completely avoided by using a slightly more complex exclusive OR gate to add the *ExtClk* signals.

The floorplan of the chip very closely follows the simple topology of the circuit. All flipflops are arranged in a horizontal row with the supply, clock, feedback and tap signals running on top (a two metal layer process was used). A logic block which generates the exclusive OR and the multiplexer functions (with

a two gate delay) is placed at the right end of the row. The OR-circuit, clock selection and buffering are located at the left side. The 128 counters are stacked vertically with the control signals like *ExtClk* running vertically. Using a single poly, double metal process with $2.4\ \mu\text{m}$ design rules, each counter has an effective height of $40\ \mu\text{m}$ and a length of $250\ \mu\text{m} + N \times 51\ \mu\text{m}$, where $N = 15$ is the number of bits. The 128 input pads are arranged in two staggered rows with a pitch of $44.5\ \mu\text{m}$ to match the output pitch of the preamplifier / comparator chip [4] which will be used to read out the silicon strip detector. The preamplifier chip has current outputs, so that current inputs (optionally voltage inputs) are used in the scaler chip. The total chip size is $6.2 \times 4\ \text{mm}^2$. Fig. 4 shows a photograph of the chip.

Fig. 4. Photograph of the 128 channel scaler chip.

The chip performs as expected in all functions. Operated at a supply voltage of $3.5\ \text{V}$, the clocking and readout frequency (via *ExtClk*) exceeds $50\ \text{MHz}$ which corresponds to a minimum width of the refresh pulses of $10\ \text{ns}$. External clock signals also must have a width of at least $10\ \text{ns}$. The minimum refresh rate is $\approx 1\ \text{kHz}$.

3 Other Possible Applications of Shift Counters

There are more applications in which shift counters can be used to improve or simplify a circuit design.

- In a logic sequencer, for instance, there is no need to count in binary code. The simplicity and speed of a shift counter could be worth some address decoding when loading the sequencer. (However, the dynamic power consumption of a shift counter is higher than e.g. for a Gray counter, as there are more bit flips per clock.)
- An up/down counter can be implemented fairly easily by constructing a shift register which can shift in both directions (left/right). This requires an additional multiplexer per flipflop. A second exclusive OR gate is used to supply the input signal for the second shift direction.
- It is fairly simple to build a comparator which tests whether two shift counter values differ by one: an identity comparator is connected with one bit misalignment and the extra bit is generated with an additional exclusive OR gate. Such a comparison can be useful e.g. in FIFO control blocks or in a neighbour logic included on chips for the readout of silicon strip detectors.

4 Summary

A 128 channel scaler chip which uses linear feedback shift registers as the counting elements has been successfully built and tested. Advantages of this concept over standard solutions are simplicity, compactness, speed, and the built-in readout capability, which makes it a very interesting candidate for counters in VLSI chips for pixel or strip readout applications. Scaling down the present design from the $2.4\mu\text{m}$ process used to a modern $0.8\mu\text{m}$ technology will decrease the area needed to implement a 15 bit shift counter to $\approx 50 \times 90\mu\text{m}^2$.

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