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KEK Preprint 95-164
November 1995
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October 25, 1995

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Abstract

A pMOS pixel to be used in a striplike two-dimensional readout single-sided detector has been developed and tested. It is originally proposed for upgrades of the vertex detector of the BELLE experiment at the KEK B-factory in order to overcome low signal-to-noise ratio of the double-sided silicon strip detector to be used presently. This device gathers the pMOS transistor amplification with the typical silicon pin diode used in particle detection. In a $100 \times 100 \mu m^2$ n-type collecting electrode, a double drain pMOS transistor is implanted, providing (1) a two-dimensional readout and (2) direct signal amplification. With the subdivision in pixels, which lowers the detector capacitance, a high signal-to-noise ratio is expected. The two-dimensional readout and the low noise advantages of this structure can be used for detection of any electro-magnetic radiation as well as high energy charged particles. Nuclear physics, space and astrophysics instrumentation are also potential field of application for the pMOS pixel. We briefly review here the principle of the structure and described the test of the prototypes in details.

*To be presented at IEEE 1995, Nuclear Science Symposium and Medical Imaging Conference, October 21-28, 1995, held in San-Francisco.
Will be published in the IEEE Transactions on Nuclear Science.

National Laboratory for High Energy Physics, 1995

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Abstract

A pMOS pixel to be used in a striplike two-dimensional readout single-sided detector has been developed and tested. It is originally proposed for upgrades of the vertex detector of the BELLE experiment at the KEK B-factory in order to overcome low signal-to-noise ratio of the double-sided silicon strip detector to be used presently. This device gathers the pMOS transistor amplification with the typical silicon pin diode used in particle detection. In a $100 \times 100 \mu\text{m}^2$ n-type collecting electrode, a double drain pMOS transistor is implanted, providing (1) a two-dimensional readout and (2) direct signal amplification. With the subdivision in pixels, which lowers the detector capacitance, a high signal-to-noise ratio is expected. The two-dimensional readout and the low noise advantages of this structure can be used for detection of any electromagnetic radiation as well as high energy charged particles. Nuclear physics, space and astrophysics instrumentation are also potential field of application for the pMOS pixel. We briefly review here the principle of the structure and described the test of the prototypes in details.

I. INTRODUCTION

A. *The pMOS pixel detector*

In order to overcome the limitations of the double-sided silicon strip detector to be used in the first stage of the BELLE-SVD [1], we propose a pMOS pixel detector for possible upgrades. A theoretical study has been previously published [2]. Figure 1 shows a schematic view of the proposed single-sided, two-dimensional readout device. In a $300 \mu\text{m}$ thick substrate a p^+ area is implanted on the back side, and n^+ areas are implanted on the top, forming a pin diode. The n^+ area is composed of a $200 \mu\text{m}$ pitch array of n^+ wells. Each n-well is separated from ad-

jacent ones with LOCOS¹. A pMOS transistor is implanted in each n-well, providing amplification of the signal. The drains of this double drain pMOS transistor are ganged together with metal strips in X and Y direction, providing a two-dimensional striplike readout on a single-sided device. With a built-in amplification and a pixel configuration a high signal-to-noise ratio is expected for this pMOS pixel detector. The design parameters for the pMOS pixel are listed in Table 1.

B. *The Operation principle*

The operation principle of the pMOS pixel is described in the bottom part of Figure 1. The detector bias voltage is applied to the back side p^+ implantation while the n-well is grounded through the bias resistor (R_B). As in strip detectors, charged particles are detected in the depleted junction. The signal charge (Q_0) deposited in the substrate is accumulated on the n-well, and decays through the bias resistor. The accumulated charge provides a voltage shift in the n-well (V_{sub}), which modulates the drain current (I_d) of the pMOS transistor operating in the saturation region. The drain current is then differentiated by the R_0C_0 network before being fed into the preamplifier.

In similarity with the typical transistor transconductance, we define the pMOS pixel back-transconductance ($g_{sub} = dI_d/dV_{sub}$) which represents the drain current sensitivity for an input on the n-well node. Providing that the time constant of the differentiation network ($t_0 = R_0C_0$) is chosen to be much shorter than the decay time in the n-well, the output signal charges are collected by the preamplifier. A RC-CR type shaping amplifier which shaping time (τ_s) equals the differentiation time is used to read out the signal from the drain node. Parameters for the proposed signal processing are listed in Table 1.

¹LOCOS stands for LOCal Oxidation of Silicon

II. PROTOTYPES

A. Fabrication

We designed prototypes of the pMOS pixel. They were processed by Seiko Instr.Inc. in a $1.2\ \mu\text{m}$ CMOS technology on 4 inch diameter and $300\ \mu\text{m}$ thick wafers. The substrate is a high resistivity n-type ($4\ \text{k}\Omega\text{cm} \sim 6\ \text{k}\Omega\text{cm}$) silicon, and (100)-oriented. The $1\ \mu\text{m}$ thick gate oxide of the pMOS pixel is obtained by growing the gate oxide during the LOCOS fabrication. The bias resistor processed in high resistive polysilicon is included on the prototypes.

Different test structures are designed on independent samples. Each sample consists of a 7×7 n-wells array. The test structure is located in the middle of this array and the outer n-wells are connected together forming the well-ring. The p^+ back side implantation is located in the middle of the sample, surrounded by a p^+ ring and drawn $500\ \mu\text{m}$ wider than the n-well array, so that the electric field underneath it, is vertically oriented.

The pin diode is surrounded on both side by n^+ guard-rings which isolate the sensitive area in the middle of the sample, preventing from shorting the pin diode by the die cut. The well-ring and guard-ring on the top side are grounded while the back side guard-ring is kept floating.

The n-wells are isolated between each other when the pin diode is fully depleted. As they are implanted in a n-type substrate, electrons may accumulate underneath the LOCOS and short all the detecting elements together. To prevent this, we add a floating p^+ stopper ring around each n-well.

For the tests, these $4 \times 4\ \text{mm}^2$ devices are wire-bounded into a package. The samples comprise two types of test structures: single pixel and 3×3 pixels.

B. Samples

Single pixel type prototypes are composed of a single n-well containing a single drain pMOS transistor and a polysilicon bias resistor in between n-well contact and source. This basic structure is used to check the pMOS transistor operation, the electrical properties, the basic operation of the pMOS pixel, as well as the signal amplification and noise performance.

3×3 pixels test structures are designed to test the pMOS pixel behavior in an array, and determine its position resolution. Composed of 3×3 pixels with double drain pMOS transistor in the n-wells, and with the drains X and Y ganged in column and row respectively, this prototype is used to check the feasibility of the striplike idea.

Electrical characteristics of the pMOS pixel have been studied and presented previously [3]. The measured electrical properties such as pin diode leakage current (I_L),

pMOS pixel: Double DRAIN pMOS Transistor in the N-well

Figure 1: The upper part is a schematic view of the pMOS pixel detector with striplike two-dimensional readout. A schematic description of the pMOS pixel operation principle appears in the bottom part.

Detector thickness, d	$300\ \mu\text{m}$
Pixel area, A_d	$(200\ \mu\text{m})^2$
N-well area, W_{well}	$(100\ \mu\text{m})^2$
Gate size, W/L	$4\ \mu\text{m} / 4\ \mu\text{m}$
Gate oxide thickness, t_{ox}	$1100\ \text{nm}$
Drain current, $I_{d(DC)}$	$200\ \text{nA}$
Transconductance, g_m	$0.56\ \mu\text{S}$
Back-transconductance, g_{mb}	$3.03\ \mu\text{S}$
Capacitance of diff. network, C_0	$1\ \text{pF}$
Resistance of diff. network, R_0	$1\ \text{M}\Omega$
Diff. time constant, $t_0 = R_0 C_0$	$1\ \mu\text{s}$
Shaping time, τ_s	$1\ \mu\text{s}$

Table 1: Parameters for the pMOS pixel. (Diff. stands for Differentiation.)

bias resistance, total capacitance per pixel (C_P), transconductance and back-transconductance are listed in Table 2.

III. RESULTS FROM TESTS

A. Test with IR light

1) Single pixel:

The feasibility of using a pMOS pixel as a tracking detector is checked with the single pixel test structure. The pMOS transistor amplifies a signal input on the back gate, i.e. a charge accumulation due to ionization by crossing particles. The signal generated in the p-i-n illuminated by a 1071nm-wave-length infra-red light is detected on the n-well node.

The basic performances of the pMOS pixel such as amplification and noise are measured. The output signal at the drain node is measured in the differentiation readout configuration described in section I.. The measured pulse height (Signal), the signal-to-noise ratio ($S/N = \text{Signal}/\text{NoiseRMS}$) and the deduced charge amplification gain ($A = \text{Signal}/\text{Reference}$) and electronic noise charge ($\text{enc} = Q_0 N/S$) are listed in Table 2.

The expected values of the parameters appearing in this table were calculated using the electrical properties measured previously [3]. The electronic noise charge is as expected between 500 to 600 electrons. Even though a charge amplification gain of about 8 is calculated at this operation point, it is measured to be of only about 1.2. This point has been discussed previously [3].

2) 3×3 pixels:

Eventually the possibility of a striplike readout configuration is checked by shining the IR light on the 3×3 pixels prototype. This sample consists of a n-well array with double drain pMOS transistor implanted in them. Drains X_i and Y_j are ganged for strip-like readout. No polysilicon bias resistor are included in this sample. The output signal is extracted from the drain node in a direct readout configuration mode. $t_0 = 1$ ms is chosen to be much larger than the decay time in the n-well, therefore the accumulated charge is directly transferred to the preamplifier. But such a simple method is very slow and can not be use in real detector application.

Figure 2 shows the distribution of pulse height measured on the Y_i strip-like read-out line, when shining the IR light along the X_2 line. The pulse height drops correspond to the readout aluminum lines on the prototype, where the IR light is stopped. The pulse height is measured with a digital oscilloscope with a precision of ± 0.04 mV. A preliminary measurement of the position resolution obtained is given Figure 3. Y_{ac} is the analog calculated position given by

Figure 2: Pulse height distribution measured on Y_j read-out line when IR is shining along X_2 line. The pulse height drops correspond to the position of the readout aluminum lines.

$$Y_{ac} = \frac{\sum_{i=1}^3 y_j P_{Y_j}}{\sum_{j=1}^3 P_{Y_j}} \quad (1)$$

where y_j is the read-out line coordinate and P_{Y_j} the pulse height measured on this line. y is the true photon beam impact location. The position resolution is calculated to be of $43.8 \mu\text{m} \pm 0.98 \mu\text{m}$, which is better than the digital position resolution given by $200/\sqrt{12}$. But, as seen on Figure 3 the response is more or less digitized due to the wide-pitch cell configuration with a p^+ stopper separation scheme.

Figure 3: Variation of the analog calculated position Y_{ac} with the true photon beam position.

Process parameters	
Gate oxide thickness, t_{ox}	1136 nm
Deep n-well concentration, N_D^-	$1 \times 10^{16} \text{ at/cm}^3$
N-well channel concentration, N_D^+	$3.9 \times 10^{17} \text{ at/cm}^3$
Electrical parameters	
at $V_g = -52 \text{ V}$:	
Drain current, I_d	1700 nA
Transconductance, g_m	$0.37 \mu S$
Back-transconductance, g_{sub}	$8.3 \mu S$
Leakage current at $V_{bias} = -50 \text{ V}$, I_L	300 pA
Polysilicon resistor, R_B	$1.4 \text{ G}\Omega$
Total pixel capacitance, C_P	1 pF
Performances	
calculated	measured
Signal	-176 mV
Charge Gain, $A = g_{sub} R_0 C_0 / C_B = 8.3$	1.1 S/N=30
Electronic Noise Charge, enc=406electrons	625electrons
Position resolution, σ_y	$43.8 \mu m$
Energy resolution,	6.6 keV

Table 2: Measured parameters and performances of the pMOS pixel

B. Test with radioactive source

The single pixel type prototype is irradiated with a ^{133}Ba source which emission energy is 81 keV. The detected spectrum is shown in Figure 4. From this preliminary measurement, the energy resolution of the pMOS pixel is calculated to be of $6.6 \text{ keV} \pm 0.4 \text{ keV}$.

IV. SUMMARY

In order to summarize we list designed and measured parameters, expected and measured performances of the pMOS pixel, Table 2.

- The feasibility of a pMOS pixel for charged particle detection was checked.
- By ganging the pixels in pixel-line a two-dimensional strip-like readout detector can be designed.
- The possibility to use the pMOS pixel for radiation measurement was verified.

Further tests with radioactive sources and particle beam are on going. We are now preparing the design of improved new prototypes.

Figure 4: Spectrum detected with a single pixel prototype.

ACKNOWLEDGMENTS

We would like to acknowledge the encouragement of the directors H. Sugawara, Y. Kimura, S. Iwata, F. Takasaki, M. Kobayashi and K. Nakai. The present work is based on the BELLE-SVD group: Y. Higashi, M. Ikeda, H. Ozaki, M. Tanaka, T. Tsuboyama, S. Okuno, S. Mori, K. Yusa, S. Tsuchiya, J. Haba, H. Hanai, D. Tatsumi, K. Adachi, T. Kawasaki, Y. Nagashima, C. Fukunaga, T. Matsushita, H. Miyata, and K. Miyano. The following people at Seiko Instruments Inc. are assisting the prototype fabrication: H. Takeuchi, M. Mandai, S. Miyahara, and K. Kamiya.

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