EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

su 8616

CERN LIBRARIES, GENEVA

CERN-ECP-96-004

CERN-ECP/96-04
09 February 1996**HIGH RATE LARGE DYNAMIC RANGE ANALOG CIRCUITRY AND DIGITIZERS
FOR FAST CALORIMETRY**

B.Hallgren, F.Bal, G.Barr, P.Buchholz (1), F. Formenti, W.Funk, Yu.Kozhevnikov (2),
A.Lacourt, G.Laverrière, M.Martini, A.Papi (3), P.Ponting, M.Sozzi, O.Vossnack, H.Wahl.

CERN, CH-1211 Genève 23, SWITZERLAND

(1) Institut für Physics, Universität Mainz, D-55099 MAINZ GERMANY

(2) Joint Institut for Nuclear Research Dubna, 10100 MOSCOW RUSSIA

(3) Dipartimento di Fisica, Univ.degli Studi di Perugia, IT-06100 PERUGIA ITALY

Abstract

This paper describes the issues encountered in the design of a large dynamic range digitizer for calorimetry. A gain switching technology developed for the liquid krypton calorimeter of the NA48 CP-violation experiment at CERN is described in detail. 14 bit dynamic range and better than 300 ps time resolution were achieved in beam tests with an 8 channel prototype. A mixed analog/digital ASIC has been developed. A 13'500 channel system is being produced which will be put into operation in 1996.

*Presented at the 1995 NUCLEAR SCIENCE SYMPOSIUM
SAN FRANCISCO, USA 21-28 October 1995
Submitted to IEEE Trans on Nuclear Science August 1996*

High Rate Large Dynamic Range Analog Circuitry and Digitizers for Fast Calorimetry

B.Hallgren, F.Bal, G.D.Barr, P.Buchholz¹, F.Formenti, W.Funk, Yu.Kozhevnikov²,
A.Lacourt, G.Laverrière, M.Martini, A.Papi³, P.Ponting, M.Sozzi, O.Vossnack, H.Wahl

CERN, CH-1211 Genève 23, Switzerland

Abstract

This paper describes the issues encountered in the design of a large dynamic range digitizer for calorimetry. A gain switching technology developed for the liquid krypton calorimeter of the NA48 CP-violation experiment at CERN is described in detail. 14 bit dynamic range and better than 300 ps time resolution were achieved in beam tests with an 8 channel prototype. A mixed analog/digital ASIC has been developed. A 13'500 channel system is being produced which will be put into operation in 1996.

I. DETECTOR REQUIREMENTS

A homogeneous liquid krypton (LKr) ionization chamber has been chosen by the NA48 collaboration [1] for its electromagnetic calorimeter to combine good energy, position and time resolution with precise charge calibration and long term stability. A tower structure geometry with 2x2 cm² cells permits low capacitance detector channels, allowing fast ionization charge readout and guarantees good time resolution with high rate capabilities. The energy deposited by a particle is essentially contained in a shower box consisting of 11x11 cells centred on the one containing the maximum energy. The initial current is derived from the charge measured by a preamplifier mounted directly in the detector and operated at cryogenic temperatures. The integration time constant chosen for the charge preamplifier is 150 ns. The signal from the preamplifier is transmitted to a combined receiver and differential line driver mounted outside the calorimeter close to the signal feedthroughs. The receiver amplifies the preamplifier signal and performs a pole-zero cancellation. The signal after pole-zero cancellation has a risetime of about 20 ns and falltime of 2.7 µs. The maximum signal level, 50 GeV corresponds to ±1 V into 100Ω at the digitizer electronics input. The required signal to noise ratio is 15000 to 1. The energy resolution actually achieved is given by the following formula:

$$\frac{\sigma(E)}{E} (\%) = \sqrt{\frac{3.3^2}{E} + 0.4^2} \quad (1)$$

¹Institute für Physik, Universität Mainz, D-55099 MAINZ, Germany

²Joint Institut for Nuclear Research Dubna, 10100 MOSCOW, Russia

³Dipartimento di Fisica, Univ. degli Studi di Perugia, IT-06100 Perugia, Italy

II. DIGITIZER ELECTRONICS

It is not possible to fully exploit the characteristics of liquid sampling calorimeters with conventional charge integrating digitizers due to their long conversion and readout times.

Recently, a number of developments have been undertaken within the framework of the research and development effort for experiments proposed for the LHC collider at CERN. All systems aim at a dynamic range in excess of 14 bits with an overall accuracy of better than 0.5%. This can be achieved in practice when the required square-root or logarithmic response of the ADC is approximated by means of a piecewise linear conversion. By making the frequency of the sampling clock sufficiently high, several samples on the baseline and the signal pulse are available. Digital filtering can then be used to extract both amplitude and time information. An efficient data reduction is possible with a long pipeline memory allowing for the arrival time of the first or second level trigger signal before data read-out.

The basic building blocks of these systems are:

- An analog shaper with a filter to maximize the signal to noise ratio and limit the frequency bandwidth of the signal while optimizing the time resolution;
- A fast sampling ADC (flash or multiplexed successive approximation);
- A pipeline storage placed either in front of the ADC (switched capacitor array) or on the digital output (memory).
- Digital filtering to optimise the pulse height resolution.

A. Analog Memory Based on Switched Capacitors

Systems with switched capacitor pipelines are under development [2], [3]. 13 bits of dynamic range and a timing resolution less than 100 ps has been achieved [2] with a 40 MHz clock. Dynamic range extension can be realized [3] by driving two rows of cells with 1x and 16x amplifiers hence approximating a logarithmic response with two linear segments. The ADC at the output of the capacitor array has 12 or 14 bits at lower speed. A limiting factor for this technique is the maximum capacitor matching possible in an integrated circuit which is better than ±0.1% or <0.03% RMS. The cell to cell dispersions must be minimized to achieve the required accuracy. The length of an analog pipeline is more limited than a digital pipeline.

B. Analog Compressor - RD16 FERMI

Presently the accuracy for fast ADCs is limited to 10 bits as a result of the prohibitive cost and power budget of 12 bit fast sampling clock ADCs (≥ 40 MHz). Hence it is necessary to partition the response into four or more linear pieces rather than two. For such systems a dynamic compressor must be placed in between the channel input and the ADC. In the CERN DRDC RD16/FERMI [4] approach, the calorimeter signal is amplified by a ladder of four differential amplifiers, each of which reaches saturation as the amplitude of the signal grows. This technique is similar to the ones used in logarithmic amplifiers for radar applications. It has a precision of about $\pm 5\%$ before calibration. Each channel therefore contains an individual look-up table in static RAM to linearize and scale the data.

C. QIE - Charge Integrator and Decoder

A circuit intended for the readout of photomultiplier tubes for the KTEV experiment at Fermilab has recently been developed [5]. By combining charge integration in ten gain ranges with a 8 bit FADC a large dynamic range of 17 bit has been achieved. Charge loss due to slightly different parasitic capacitances on each gain range is the main problem encountered.

D. Gain Switching Amplifier - NA48 KRYPTON

A novel compression technique has been designed for the readout of the LKr calorimeter of the NA48 experiment by this group. A block diagram of the gain switching circuit employed is shown in Fig. 1. The signal is received by a fast differential

Fig. 1 Block diagram showing gain switching principle

line receiver and split into two parts. One fraction of this fast signal (risetime = 20 ns, FWHM = 30 ns) goes to three discriminators. The amplitude of the signal is used to select which gain value has to be applied to the shaped pulse, which is delayed with respect to the fast input by the shaper propagation delay. The selected gain is maintained for a

constant, programmable number of clock periods before it reverts to a higher gain. This means that a detector signal is measured with samples having the same calibration constant both in amplitude and in time delay. Passive attenuation before the amplification and independent of the gain selection is a key element and makes it possible to achieve the required time resolution. The switching level is programmable by three threshold values (Thres1, Thres2, Thres3). As seen in Fig.1, the other part of the fast signal enters a Bessel filter. The output signal of the filter is shaped into a quasi-gaussian pulse with a risetime of 50 ns and FWHM=90 ns. The signal is delayed by 80 ns to allow time for the logic decision and for the settling time of the gain switching amplifier.

The gain factors and the number of ranges were chosen taking into account the requirement that the minimum ADC resolution must not impair the performance of the detector by more than 10% when combined quadratically. The commercially available 10 bit ADC used by NA48 has an effective resolution of 8.8 bits. The ratio of the resolution of

Fig. 2 The ratio of the effective ADC resolution versus the scaled detector resolution for the four gain ranges.

the ADC and the detector versus the energy is shown in Fig.2. The detector resolution was scaled such that a 10% contribution to the noise from the ADC would give a ratio of 1. Four relative gain factors of 1, 2.87, 6.95 and 17.16 give satisfactory performance. Fig.3 shows these four linear ranges.

Fig. 3 The piecewise linear gain ranges used in the KRYPTON ASIC.

Fig. 4 Discrete component prototype.

The output signal of the Bessel filter is applied to a passive attenuator with four outputs, with the following attenuation factors 1.0, 0.347, 0.142, 0.0596. The four gain values are controlled solely by the ratio of resistors. In an integrated circuit, the precision can be better than 0.5% and the stability with temperature and time is excellent. The bandwidth of the passive attenuator can be made large. The delay spread of the four equal gain x16 amplifiers is small because four identical amplifiers are used. The 4 to 1 multiplexer at the output of the circuit is controlled by two control bits which are encoded from the output state of the discriminators. The gain change is synchronous with the ADC sampling. In this way the switching transient of the multiplexer occurs between successive ADC samples with ~20 ns settling time before another sample is taken. The gain switching will then not effect the measurement.

A serial interface bus is used for DC level control using DACs and also for the control functions of the gain switching. The gain can be forced to any of the four values in order to calibrate the circuit. Other test functions are also implemented.

III. FIRST PROTOTYPE

Extensive tests of the concept of fast gain switching were performed using standard components under realistic conditions in an 8 channel prototype module. The main characteristics of this design are shown in Fig.4. The detector signal is received in a differential line receiver in a standard instrumentation amplifier circuit. A 4-pole Bessel filter is made with two operational wideband amplifiers. Here, the gain switching is performed by two cascaded switched amplifiers. There is an output amplifier to drive a 40 MHz 10 bits ADC. The digital part of circuit consists of ECL logic: three comparators which are biased at threshold voltages, which correspond to 3%, 18% and 40% of full scale. Each of these comparators constitutes a retriggerable monostable together with a clocked second comparator. The gain bits are stored together with the ADC data in a memory.

In 1993 and 1994 this circuit was tested [6] as part of the complete readout chain with a prototype LKr calorimeter.

The results fulfilled the energy resolution and the noise requirements of the experiment. A typical waveform is shown in Fig.5. The timing resolution achieved was 220 ps at the maximum energy of 100 GeV and 275 ps at an energy of 15 GeV.

95/C9/12 17.09

Fig. 5 Digitized pulse from beam test. The upper plot shows the gain bits, the middle plot shows the ADC output and the bottom plot shows the reconstructed pulse shape.

IV. KRYPTON ASIC

The 5 W per channel of power consumption of the first prototype was excessive for the mass production of 13,500 channels. The cost per channel of about \$100 was also prohibitive. Therefore, a full custom ASIC had to be designed. Several alternatives were studied. The one which was chosen is implemented in a 1.2 μ m BiCMOS technology, which has very fast NPN transistors. The project was done in collaboration with CISS and AMS of Graz, Austria, who were responsible for the circuit design and layout. It was possible to complete the design in 6 weeks by using standard cells, already

The 9 pole Bessel filter consists of three amplifiers with a

Fig. 9 Top curves show high and low gain bits. Bottom curve analog output from ASIC

gain of 1.3 controlled by on-chip resistors. The filter components are not included in the ASIC, because of the needed 1% absolute tolerance. This also permits more flexibility in the choice of the filter characteristics. An example of the response is given in Fig.10. The delay in the filter is 86 ns and

Fig. 10 Bessel filter transient response. Curve A is input to filter. Curve B is filter output.

the output has a width of 100 ns (FWHM). The filter is designed to give approximately the same performance as a classical CR-2RC filter but with a longer propagation delay.

D. Trigger stage.

The output of the Bessel filter is fed to the gain switching circuit and also to a trigger circuit. Two differential current sources are provided in the ASIC which are used for the summing of 16 channels, (see Fig.11). There is a 6 bit programmable attenuator using FET switches and resistors. It is controlled via the serial interface and can be used to equalize gain variations of +25% between detector channels. The current outputs are summed into 100Ω equivalent resistors.

Fig. 11 Analog differential current outputs (two per ASIC).

V. DISCUSSION

The first prototype of the KRYPTON ASIC was functional except for the digital control of the gain multiplexer. The second ASIC proved to be fully functional and presently 150 pieces have been tested. The total development time was one year.

The gain switching ASIC is used in a 64 channel module (FASTBUS, 3 units wide) together with a 10 bit, 40 MHz ADC (Philips TDA8760). The module also includes digital circular buffers and event memories to allow for deadtime-less operation with 200 μs storage capacity before trigger and readout. A first prototype module was recently tested in a high energy electron beam test and the prototype LKr calorimeter confirming the results previously achieved with the discrete component version. Mass production of 13'500 channels will take place shortly.

VI. REFERENCES

- [1] G.D.Barr et al., "Proposal for a precision measurement of ϵ'/ϵ in CP violating $K^0 \rightarrow 2\pi$ decays", CERN/SPSC/90-22/P253.
- [2] J.A. Parsons et al., "Analog Memory Readout Electronics for the ATLAS LAr Calorimeter", .Proceedings of the First Workshop on Electronics for LHC Experiments", CERN/LHCC/95-56, pp.406 -410, October 1995.
- [3] V.Valencic et al., "A Low-Power Piecewise Linear Analog to Digital Converter for use in Particle Tracking", IEEE Trans. on Nuclear Science, Vol.42, pp.772-775, Aug. 1995.
- [4] A.Dell'Acqua et al, "A Digital Front-end and Readout Microsystem for Calorimetry at LHC The FERMI project", IEEE Trans. on Nuclear Science, Vol 40, pp. 516-531, Aug. 1994.
- [5] R.J. Yarema et al., "A High Speed, Wide Dynamic Range Digitizer Circuit for Photomultiplier Tubes", Fermilab-TM-1895.
- [6] G.D.Barr et al., "Performance of an electromagnetic liquid krypton calorimeter based on a ribbon electrode structure", CERN-PPE 95/64 Apr.1995, to be published in Nuclear Instruments and Methods.