Radiation tolerance for the SMASH-series front-end chips for silicon micro-strip detector

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Letter to the editor

Radiation tolerance for the $SMA^2SH$-series front-end chips for a silicon micro-strip detector*

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ABSTRACT

The radiation tolerance for prototype front-end chips designed for a silicon micro-strip detector was examined with a $^{60}$Co irradiation source to establish an allowable range of the radiation dose. The irradiated front-end chips were $SMA^2SH - 64A$, a 64-channel preamplifier array; $SMA^2SH - 1$, a single-channel preamplifier circuit with a comparator; and Control-C, a digital-control chip for the preamplifiers.

We are developing a silicon micro-vertex detector[1] for the B-factory experiment at KEK. Since the silicon micro-vertex detector is located in the vicinity of a beam pipe, we expect a certain amount of radiation dose, which will come from synchrotron X-rays and spent electrons. An estimate of the radiation dose provides a few tens of krad during the 10-year life of the detector.[2] Further work on a more accurate estimation of the radiation dose is currently underway.

A modern CMOS process, which commonly employs thinner and higher quality gate oxide, can cope with a few hundreds krad as long as digital operation is concerned. As for an analog circuit, a shift of bias voltages and an increase in the $1/f$ noise still have serious impacts on the circuit performance.

Possible radiation-damage modes can be separated into four cases: one is degradation of the transistor, itself, such as the threshold shift, $g_m$ degradation, and increase in the $1/f$ noise; the second is degradation of device isolation, such as the leakage path between the source and the drain terminals and/or underneath a LOCOS oxide; the third is a transient-radiation effect, which is associated with a very high dose rate; the fourth is the so-called single event upset. The third one could be assumed to be irrelevant for our B-factory experiment, since the instantaneous rate of radiation is very small. The last one is also regarded as not being of our concern, because we can issue a system-reset for each event in order to recover from an accidental or temporary failure of the DAQ circuits. Since the second damage mode is still moderate for a few hundreds krad range, the degradation of silicon dioxide is the most crucial issue for the B-factory experiment. A text book by T.P. Ma and P.V. Dresedorfer[3] can be consulted for further details concerning the radiation effect on MOS circuits and transistors.

In order to extract practical parameters for radiation doses up to 200 krad, we studied the degradation of non-radiation-hard CMOS transistors,[4] with which prototype preamplifiers were fabricated. The test transistors fabricated on a SOI wafer[5] showed a smaller sensitivity than those from a bulk CMOS process, which was possibly due to an internal (intrinsic) gettering effect. We speculate that the
SOI wafer has a higher density of gettering centers at the interface between the surface silicon layer and the underneath oxide insulator layer than an oxygen rich CZ wafer, and, hence, provides a higher quality gate oxide.

A primary goal of this work is to set an allowable range of radiation dose for the existing $SMAM^2SH$-series front-end chips in terms of the degradation of the signal-to-noise ratio as well as functional operations. Eventually, in order to keep a sufficient contingency for the allowance on the radiation dose, we are moving to a radiation-hard circuit design with a radiation-hard silicon process.

The test chips were fabricated with a 1.2 μm N-well CMOS with double-poly and double-metal capability from Seiko Instruments. The thickness of the gate oxide typically was 26 nm. The chips were mounted in a ceramic package and wire-bonded with the gold wire. We exposed the packaged chips to γ rays from a $^{60}$Co source in AECL industrial irradiator (Gammacell 220) facility at Tokyo Metropolitan University. The irradiation was performed at room temperature with a dose rate of 610 krad/hour (Si). Since we know from previous experiments (refs 4 and 5) that the 1.2 μm process, which we employed for chip fabrication, is not much influenced by a bias condition, we did not apply any voltage to the chips during irradiation. The differences between the biased and non-biased conditions can be corrected based on a previous experiment, if necessary. After irradiation, it took a few days before the test samples were measured at a test bench of KEK. The test samples were Control-C, which is a digital control chip for the preamplifier chips; $SMAM^2SH-1$, which is a single channel preamplifier chip including a complete chain for the B-factory experiment at KEK; and $SMAM^2SH-64$, which is a 64-channel preamplifier array dedicated for a prototype detector evaluation. Their tolerances for radiation dose are described separately below.

Control-C chip was examined with test vectors in terms of a SCHMOO plot. The SCHMOO plot is a two-dimensional GO/NOGO map over static/dynamic parameters for circuit operations. The variables taken for the SCHMOO plot were the supply voltage (from 4.2 to 5.9 V for each 0.1 V step) and the compare level (from 0.6 to 3.8 V for each 0.2 V step). In order to execute a SCHMOO measurement, we employed an LSI verification system (LV500) from Tektronix. The digital signals fed into the Control-C chip was specified as $V_{IL}=0.5$ V, and $V_{IH}=4.0$ V. The cycle time for the test vectors was 48 ns. For each cycle, output signals were compared with the expected vectors at a timing of 42 ns from the beginning of the cycle. Figure 1 shows SCHMOO plots for a) the pre-irradiation condition and b) after 200 krad irradiation. We found that Control-C chip withstood 200 krad, while the "pass" region moved to the higher supply side by 0.4 V. Control-C chip also has unity gain buffers, which were used to buffer analogs from/to preamplifier chips and the back-end system. Figure 2 shows the DC responses of the unity gain buffer for a) the pre-irradiation condition and b) after 200 krad irradiation. Two samples are indicated in the figure with open circles and plus symbols. The design of the buffer amplifier was based on a two-stage operation amplifier, and revealed to withstand 200 krad. The linearity below 1 V was found to be improved, which came from $V_{TH}$ lowering of the nMOS transistor due to irradiation, while the overall integral non-linearity at the mid-range became degraded.

$SMAM^2SH-1$ was examined in terms of the variation in the threshold level of the built-in comparator. Ref 7 can be consulted for details concerning the circuit configuration. The performance might be affected by the shift of $V_{TH}$ of the pMOS and/or nMOS transistors. Figure 3 shows the threshold of the comparator circuit versus the sensitivity control switches $TH[2:0]$, which runs over 1 to 7. The figure shows the thresholds for a) positive and b) negative charge inputs, separately. We like to adjust the threshold level to around 4000 electrons. Under the pre-irradiation condition we can achieve the requirement with an intermediate position of $TH[2:0]$ switch, i.e. 3 or 4. For a positive input charge, the comparator once became slightly easy to turn on, and, then, quickly came to show a very high effective threshold, i.e. 10000 electrons, for a radiation dose of 50 krad. For a negative input charge, the comparator gradually became easy to turn on, and eventually, showed a very low effective threshold, i.e. 500 electrons, for a radiation dose of 50 krad.
SMA$^{3}$SH – 64A is a 64-channel preamplifier array, which was designed to be used for evaluating the prototypes of the silicon-micro vertex detectors. In practice, it was used to study the charge-partitioning properties of a wide-pitch ohmic-side readout. SMA$^{3}$SH – 64A was examined in terms of an increase in the electronic noise with a setup where we had examined a common-mode noise property for SMA$^{3}$SH – 64A. Figure 4 shows the electronic noise versus the input capacitances. We found that the noise slope increased in such a way as 0.6 electrons/pF/krad with an initial slope of 20 electrons/pF, while the offset at zero input capacitance increased very slowly from a few hundred electrons to several hundred electrons. There existed two reasons for the increase in the electronic noise. Major reason came from an increase in the $1/f$ noise; we also found that a decrease in the bias current contributed a finite amount of electronic noise due to a reduction of the transconductance of the input FET. The bias current of the preamplifier circuit was adjusted by a resistor of 36 kΩ located off the chip. Since the resistor was connected to a current mirror of a pair of pMOS transistors, an increase in the threshold voltage of the pMOS transistor by an irradiation reduced the bias current. The voltage appearing on the terminals of a 36 kΩ resistor was 2.7 V for a pre-irradiation condition, while it decreased to 1.4 V after irradiation of 200 krad. By replacing the resistor with 18 kΩ, we confirmed that the noise level was improved, as shown in the figure.

In this work we found that the comparator circuit in SMA$^{3}$SH – 1 was the weakest part for the radiation dose, which could be subject to a rework on the circuit design. The increase in noise for SMA$^{3}$SH – 64A was almost proportional to the radiation dose, which could be allowed up to 20 krad to keep a reasonable signal-to-noise ratio, i.e. 1200 electrons for 30 pF of the input capacitance. The digital circuits in Control-C were sufficiently strong to withstand more than 200 krad. We can set an operationally allowable range of radiation dose at 20 krad for an existing circuit design and an employed silicon process of SMA$^{3}$SH series front-end chips. This is very close to the current estimation of the radiation dose for a steady-state operation over the 10-year life for the experiment. In order to cover a certain amount of uncertainty of dose estimation as well as to keep the contingency for an unexpected dose during beam injection and/or beam tuning, we need to improve the radiation hardness by 10 times, i.e. up to 200 krad. In order to improve the radiation hardness without modifying the existing mask design, we are exploring possibilities to employ a RTN (rapid thermally nitrided) procedure for a gate oxide as well as a special SOI wafer, e.g. a poly-silicon interlayered SOI wafer, which helps to improve the quality of the silicon surface, and, hence, the gate oxide. We also try to adopt a thinner field oxide, e.g. 0.5 μm, which was revealed to be effective to increase an immunity for radiation. A migration and tuning of the silicon process including RTN procedure are currently underway.

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2. H. Ozaki et al., private communication, Mar 1996


FIGURE CAPTIONS

1) a) SCHMÖO plot for the pre-irradiation condition
   b) SCHMÖO plot after 200 krad irradiation
   At the points indicated by open circles, the circuit worked properly, while it failed at the points marked by pulses.

2) Response of the unity gain amplifier
   a) for the pre-irradiation condition
   b) after 200 krad irradiation
   $V_{OUT} - V_{IN}$ represents voltage difference between the input and output terminals.

3) Threshold of the comparator versus sensitivity control $TH[2 : 0]$
   a) For a positive-charge input
   b) For a negative-charge input
   The dotted line shows the threshold level for 4000 electrons.

4) Electronic noise versus input capacitance

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Fig. 1 a)
Fig. 3 a)

Fig. 3 b)