CERN-EF-BEAM 76-1
20 February 1976

Submitted to
Nuclear Instruments
and Methods

HARDWARE PROCESSING OF DATA FROM
MULTILAYER IONIZATION DETECTORS

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P00027221

ABSTRACT

A dedicated hardware processor for calculating the mean of a variable proportion of the smallest ionization values from multilayer proportional counters is described. The total readout and execution time is below 3 ms for a set of 128(8 bit) ionization values. Results of a 32 layer test are presented demonstrating the efficiency of this cut-off method applied to an asymmetric distribution of the ionization losses.

1. INTRODUCTION

Identification of secondary particles produced in high-energy interactions becomes increasingly difficult in the momentum range of about 60 GeV/c and above. The currently used multicell threshold Cerenkov counters tend to be excessively long and mechanically very complex. As an alternative, charged particle identification by measurements of ionization in the region of the relativistic rise is being developed for experiments using either an ordinary [1,2] or a rapid cycling [3] bubble chamber as a vertex detector.

Due to the broad asymmetric distribution of the ionization losses in a single detector the identification of high-energy particles can be achieved only by sampling the ionization in many identical detector layers and when multilayer gas proportional counters are used as a detector, the individual pulse heights corresponding to the ionization deposited within each layer are digitised and processed by a computer. The simplest but very efficient method of data reduction consists of calculating the mean of 40 to 50% of the lowest values from all layers. As a typical example, let us take 128 (6 cm thick) proportional counter layers of the proposed External Particle Identifier (EPI) from Ref. [1,2]. The single layer ionization distribution width is about 55% (FWHM). The "mean of 40% smallest values" method attains a final resolution of about $\pm 3\%$ and the distribution is very close to Gaussian. Such a device is able to distinguish pions and kaons up to 70 GeV/c, with an overall length of the detector of only about 8 m.

During the setting-up and testing period of this External Particle Identifier behind the Big European Bubble Chamber (BEBC) some fast, and computer-independent, method of performance checking and calibration was considered highly desirable. This paper describes a dedicated hardware data processor which has been developed for that purpose at CERN. It is capable of calculating the mean of a variable proportion of the smallest values out of as many as 128 integer 8 bit binary values in a few milliseconds, including the read-in of the data.

2. SPECIFICATIONS

In order to fit into the extensive program of the EPI development the Ionization Data Processor (IDP) should have the following features:

- a) Internal structure compatible with the shift register read-out organisation of the EPI;
- b) Fast (up to 5MHz) shift clock for 128 layer tests;
- c) Slow (max. 0.5 MHz) shift clock for a single-module 32 cell test, interfacing directly to C-MOS circuits;
- d) Selection of a variable proportion of smallest values for the calculation of the mean;
- e) Possibility to reject multiple particle traversals on the basis of too high ionization, e.g. $\geq 25\%$ overflows;
- f) Possibility to reject particles not fully traversing all layers by discriminating against zeroes and noise (variable threshold up to 9);
- g) Printing of the result in a BCD integer format together with data, time and an external monitor value;
- h) Possibility to print all individual values as they are being shifted from the detector read-out for checking.

For use in connection with a system of 64 parallel ADC's with fast pulse train outputs [2] a set of 64 10 MHz binary 8 bit scalers with shift register read-out was incorporated. This system needs another 64 x 8 bit 5MHz shift sequence to be generated in addition to the two routines indicated above.

3. REALIZATION

A hardware system which will fulfill our list of specifications may be realized using wired equivalents of some well-known software methods.

One method would be the "table look up" routine, the block diagram of which is shown in Fig. 1. The individual values are stored in 128 (8 bit) shift registers which are incorporated into the electronics of the detectors. The first value from register 0 is shifted into a parallel output buffer shift register in the processor and compared with the contents of an 8 bit scaler, starting from zero. Data stored in the shift register chain are recirculated i.e. the content of cell 0 is reinserted into cell 127 and so on. The next value is shifted out and the procedure is repeated until zero is found. If there was no zero in all 128 values, the scaler is incremented by 1 and the whole procedure is repeated. When, finally, the smallest value is found it is converted into a corresponding number of pulses which is divided by n ($n = 51$ in case of 40% of 128) and the result accumulated in another scaler. Assuming, as a worst case, that all values are at maximum and using a 5MHz clock we will need $(8 \times 0.2 \mu\text{s shift}) \times (128 \text{ values}) \times 256 \doteq 52.5 \text{ ms}$ for search and an additional $(255 \times 0.2 \mu\text{s} \times 51) \doteq 2.6 \text{ ms}$ for serialization and summing-up. This is clearly not fast enough.

Another possible method is similar to the sorting of an array. The block diagram of Fig. 2 shows again the shift register chain connected as a recirculating loop. The first value is shifted into a shift register A and strobed into a buffer register B. The next value is then shifted into A and compared with B. If the new value is smaller, the contents of B is replaced by A. If $A > B$, another value is shifted into A and this procedure is repeated until the smallest value is found and stored in B and so on. Assuming now, as an extreme case, that the data are arranged just in the opposite order to that required and should therefore be completely rearranged, we will need $(8 \times 0.2 \mu\text{s shift}) \times (128 \text{ values}) \doteq 205 \mu\text{s}$ to find the smallest value and $(8 \times 0.2 \mu\text{s}) \times [127 + 26 + \dots + (127 - 50)] = 1.6 \times (127 + 77) \times 50/2 \doteq 8.2 \text{ ms}$ to find the remaining 50 values. Adding the serialization and summing-up time the total execution time will be about 10 ms but, obviously, under very pessimistic starting conditions. This seems to be acceptable.

Unfortunately, both described methods require long repetitive shifting of data which increases the probability of errors.

A third method (the most suitable for our application) avoids this inconvenience and is also much faster. It was, therefore, chosen as a basis of the processor. The principle of operation is shown in Fig. 3. The values from the shift register chain are shifted consecutively into a buffer shift register. Each value acts as an address to a 256 x 8 bit static Random Access Memory (RAM). The addressed location's content is loaded into a binary Memory Content Scaler (MCS) which is incremented by 1 and the result is immediately written back into the same memory location. This procedure is repeated until all values are stored. After just one scan through, the data are already arranged in the memory in ascending order. Repetitive occurrence of a given particular value represents no problem which is not the case for the other two described methods.

This method of processing enables simple and efficient checking of data. When the contents of the location (255) reaches 8, 16 or 32 for 32, 64 or 128 layers respectively a REJECT signal is produced for $\geq 25\%$ overflows. In a similar way the events containing at least one zero or value of up to 9 may be rejected. Both reject conditions may be switched off if undesired.

Further processing of the data from the RAM is easy. The memory contents is scanned by advancing the Memory Address Scaler (MAS) from zero to 255. When a memory location not containing zero ($ZMC \neq 0$) is detected the address advance is stopped and the corresponding address is strobed into a serializing scaler which is then run down to zero. The number of clock pulses necessary for the run-down represents the particular value converted into a pulse train. When this step is finished (EOS is given) the MCS is decremented by 1 and when zero is reached the MAS is advanced to the next "valid" location. Thus, for the first scan of 128 values we will need $(0.2 \mu s \times 128) \pm 26 \mu s$ plus about 50 μs for switching, loading and incrementing of the MCS and for writing into the memory. The second search for valid memory locations will take in the worst case $(0.2 \mu s \times 256) + 100 \pm 150 \mu s$.

The serialization of the 51 smallest values could be completed, as already mentioned, in about 2.6 ms. One complete memory cycle of 51 μ s will be needed prior to, or after, the event processing to clear the memory by writing zeroes into all locations. So the total execution time will be, in the worst case, slightly less than 3 ms. By using the Address Advance pulse train directly for serialization, the necessary time taken for finding the first value can be eliminated.

The principle of the serialization procedure is shown in Fig. 4. The pulse train corresponding to the processed value comes into a divide-by-n scaler where n can be selected between 1 and 99. When the preselected n is reached this scaler is reset to zero and a 10 bit BCD RESULT scaler is incremented by 1 etc. The serialization routine is interrupted when the required number of steps (equal to n) was counted in another divide-by-n scaler. Then, the End of Cycle (EOC) pulse is generated and the result is displayed and printed out.

Fig. 5 shows in detail the complete flow chart of the data processing.

The output format of the results printed by a HP 5050 printer is shown for several events in Fig. 6. Each "good" event contains, in 18 columns, the day, month, hour and minute from a clock incorporated in the processor, followed by a 3 digit monitor value and the result. Extensive use has been made of the character suppression facility of the HP 5050 printer for creating blank separating columns and for preventing printout of insignificant zeroes. Both the date and time are suppressed from the print-out of rejected events.

Printing of one line takes about 70 ms (controlled from the processor) so that about 73 ms are needed for one 128 values event.

When CHECK INPUT DATA mode is selected, each processed value is converted from binary to BCD and printed together with an automatically generated channel number at a rate of about 15 lines per second as shown

in an example of a "good" event in Fig. 7. Both date and time columns are left blank. When 32, 64 or 128 values are processed as selected, the scanning, serializing and summing-up starts as for RUN. After the printing of the result line one blank space line is provided to improve the optical separation of consecutive events.

Fig. 8. shows an example of an event rejected on the basis of $\geq 25\%$ overflows. This condition has been reached by finding the 8th value of 255 in channel 22. This is a typical example of a double particle traversal.

Fig. 9. is an example of an event in which at least 6 simultaneous particles were crossing the detector at rather large angle. This event was rejected on the basis of the first zero detected, in channel 7.

The total execution and printing time for CHECK INPUT DATA is about 8.6 s for 128 layers printed using the fast shift. In the case of a 0.5 MHz shift and for 32 layers, this time is about 2.3 s.

4. CONSTRUCTION

The processor was built in a 5 unit high 19 inch crate containing the necessary power supplies (5V/20A for the logic circuits and an additional small power supply of 12V for the printer interface circuits). All TTL components are mounted on 5 (182.9 mm wide) boards. Another 4 cards contain the 64 fast scalers and readout circuits. The integrated circuits were fitted into sockets and the connections were made by mini wire-wrapping. Fig. 10. shows the front panel of the instrument. Thumb wheel switches are provided for: selecting the desired percentage value of n , introducing the monitor value and preselecting the date and time. The internal clock is updated to the preselected values by pressing a SET CLOCK button. There is no display of the clock, but the decimal point after the last digit of the 3 decade LED RESULT indication flashes once per second. The manual START button initiates one complete cycle. The

manual RESET provides a general clear signal and interrupts any running routine in a particular cycle. READY indication shows that the processor may accept another event. A set of switches allows the selection of either RUN or CHECK INPUT DATA mode of operation, choice of fast or slow shift sequence and for enabling the REJECT $\geq$ 25% OVERFLOWS and/or REJECT up to ... (1 to 9 as preselected). The number of processed layers is chosen by another switch. Miniature, 50 Ω coaxial cable terminated inputs to accept (64) 10 MHz pulse trains from ADC's are provided. A test pulse entry is connected to all 64 scaler inputs. When high it inhibits counting via the individual inputs. The TRIGGER input to start the processing sequence may be inhibited by an external veto. The trigger input is also disabled while the BUSY flip flop is set. After the printing of the result an END pulse is available. SERIAL INPUT is a data entry to the main buffer shift register. The outputs from scalers 0 and 32 can be connected to the SERIAL INPUT. An input to channel 63 makes the recirculation of data possible. The RESULT is available in form of a pulse train. SHIFT OUTPUT distributes the necessary shift sequence towards the external readout circuits. Connectors for interfacing to the HP 5050 printer are located on the back panel. The automatic - after the event - reset for the 64 scalers can be switched off. This is very convenient in testing and commissioning of the device.

5. RESULT OF A 32 LAYER TEST

One layer from an EPI module was used in a cosmic ray test of the processor. As shown in Fig. 11, two double layer modules were mounted together vertically between aluminium plates in order to prevent excessive bulging of the 25 μ external Mylar foils. Scintillation counters above and below the frame provided the trigger when cosmic ray particles passed through the 32 proportional counters of 6 x 6 cm² section each. The triggering scintillators of dimensions 4 x 60 cm² were 2.6 m apart. Such a telescope has an angular acceptance of $\pm 13^\circ$. 10 cm of lead absorber were inserted between the lower scintillator and the module frame to

filter out the soft C.R. component. No veto was provided against showers generated in the 12 cm thick glass frames and in the concrete floor and roof above the experiment.

Argon with 5% Methane at atmospheric pressure was used as a gas filling.

The electronic circuits mounted directly on the detector contained amplifier, pulse forming, sample and hold, 8 bit ADC and shift register buffer for each cell. A coincidence signal from the telescope triggered the analogue to digital conversion of the 32 ionization pulse heights. Data from the ADC scalers were strobed into the shift register readout and a start signal was sent to the processor to start the procedure as described. After printout the END pulse was used for clearing the readout electronics for the next event. The BUSY signal inhibited the coincidence trigger to prevent superposition of consecutive events arriving close in time. The triggering rate was about 1 event per minute. About 48% of the events were rejected, mostly due to "zeroes".

Fig. 12. shows, at the top, the distribution of ionization losses in a single 6 cm thick cell. No corrections were applied for differences in the path length for inclined particles. The temperature and atmospheric pressure drifts over the full week of running were not corrected for. The momentum spectrum of C.R. particles is also contained in the distribution. The plot is a result of summing data from all 32 cells from a sample of "good" events. Individual cells were equalised only roughly to about $\pm 15\%$. The overflow peak contains about 5% of the distribution, which has about 65% FWHM.

The bottom part of Fig. 12. shows the distribution of the mean of 40% of the smallest values as produced by the processor with all REJECTS applied. Altogether, 3784 events are plotted. The distribution has about 38% FWHM. Note that the integral of this distribution was chosen to be the same as for the single layer distribution plotted, using identical scale.

The predicted value from [1,2] is about 55% FWHM, for a 6 cm single layer, assuming perpendicular incidence of detected (monoenergetic) relativistic particles. The resulting distribution for 32 layers should have about 13% FWHM for identical response of all layers. In our conditions, we would expect about 20% FWHM. The discrepancy could be easily explained by heavy contamination of our event sample by "partial" multiple hits which are responsible for broadening of the distribution on the high ionization values side. From the position of the peak in the distribution of the mean of 40% of smallest values taken from the 3458 rejected events, it is clear that there is also some contamination affecting the lower ionization values side. This effect is caused by multiple hit events where the particles tend to escape sideways near the detector edges.

6. CONCLUSIONS

The described processor facilitates fast computer-independent testing of data from multilayer ionization detectors. In the case of application to the EPI there will be at least 5 seconds interval between successive events so printout will be no problem.

Accumulation of data and immediate display of histograms is possible using any PHA in a multiscaler mode.

The described device could have been realized using a dedicated microprocessor but such a solution is likely to be more expensive (at present) and not very practical for the programming effort required for a single instrument. Some hardware will none-the-less be necessary, to cope with the fast shifting of data from the external readout system. The rather complex interfacing would lead to problems in our case.

The application of the hardware processor to multilayer detectors is not limited to the field of the ionization measurement only. It would in principle be used also in connection with transition radiation detectors [4].

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FIGURE CAPTIONS

- Fig. 1 Table search method of arranging the data.
- Fig. 2 Array sorting hardware equivalent.
- Fig. 3 Local RAM application for a single scan array sorting.
- Fig. 4 Serialization and summing-up routine.
- Fig. 5 Flow chart of the operation of the processor.
- Fig. 6 Printout example of RUN mode.
- Fig. 7 Example of an event in CHECK INPUT DATA mode.
- Fig. 8 Example of an event rejected due to $\geq 25\%$ overflows.
- Fig. 9 Example of an event rejected due to zeroes.
- Fig. 10 Front panel of the processor.
- Fig. 11 Layout of the cosmic ray 32 layer test.
- Fig. 12 Mean of 40% smallest values of 32 layers and single layer
distributions from C.R. test.

Fig.1.

Fig.2.

Fig.3.

Fig.4.

Fig.5.

DAY MONTH HOUR MIN. MONITOR RESULT

```

2610 1715 139 63
    0 139*000
    0 139*184
    0 139*073
2610 1713 139 83
2610 1713 139 75
2610 1712 139 85
2610 1710 139 73
2610 1710 139 64
2610 1709 139 68
2610 1709 139 58
    0 139*072
    0 139*241
2610 1706 139 93
2610 1705 139 66
    0 139*051
2610 1704 139 70
2610 1704 139 91
  
```

← all zeroes

← "bad" events

← multiple hit

↑ sense of printing

R U N

Reject 0 - 9

Reject $\geq 25\%$ OVERFLOWS

Fig. 6

CHANNEL No.

0	3	116
0	2	75
0	1	100
0	0	82
2310	1655	139 76
0	31	127
0	30	110
0	29	132
0	28	134
0	27	87
0	26	165
0	25	93
0	24	92
0	23	106
0	22	138
0	21	67
0	20	124
0	19	122
0	18	217
0	17	82
0	16	94
0	15	116
0	14	78
0	13	110
0	12	207
0	11	88
0	10	71
0	9	255
0	8	255
0	7	125
0	6	67
0	5	89
0	4	70
0	3	76
0	2	73
0	1	52
0	0	102
2310	1654	139 84
0	31	78
0	30	72
0	29	50
0	28	92
0	27	99
0	26	217
0	25	109

C H E C K I N P U T D A T A

1 event (32 channels)

Mean of 13 smallest values: 76.3077

↑
sense of printing
↑↑

Fig. 7

Fig. 8

Fig. 9

Fig. 10.

Fig.11.

Fig.12.