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**DESIGN OF A SECOND-ORDER CMOS SIGMA-DELTA A/D
CONVERTER WITH A 150 MHz CLOCK RATE**

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ABSTRACT

A continuous time filter current switching sigma-delta converter operating at a frequency of 150 MHz has been developed in 2 μ m CMOS technology. The design of the main components of the converter is described including a very high speed comparator, an integrator and a one-bit D/A converter. Measurements show a 10-bit dynamic range with a 9-bit resolution at an oversampling rate of 128.

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1. INTRODUCTION

Very high speed A/D converters with a large dynamic range are needed in instruments for particle physics detectors. A typical signal of a calorimeter has a rise time of a few nanoseconds and a fall time of around 2 μ s. This signal is amplified and filtered to produce a semi-gaussian pulse with ~ 100 ns width suitable for being digitized by a flash A/D converter. As was recently discussed [1] the same function could be implemented with a high speed sigma-delta converter replacing analog filters with digital ones. The potential for high speed operation in CMOS technology has been demonstrated with clock speeds up to 50 MHz [2, 3].

This paper describes the design of the critical components needed to realize a 150 MHz VLSI-compatible CMOS sigma-delta modulator. First a comparator with very fast performance including comparison time and delay is described. The operation of a transconductance amplifier has been extended into gigahertz frequencies so that high-frequency continuous time filters and integrators might be built. A fast 1-bit D/A converter is also shown. These components have been put together in a test chip as a 150 MHz second-order sigma-delta converter configuration utilizing a 2 μ m CMOS process.

2. COMPARATOR

The comparator consists of an input amplifier, a regenerative amplifier made of a cross-coupled latch, an RS flip-flop and an enable latch (fig. 1).

In order to achieve < 10 mV comparison sensitivity the input differential transconductance amplifier has a total gain of ~ 4.6 mA/V. The input differential pair is made of four cross-connected large transistors (MND1 and MND2) in order to minimize the static offset voltage and sensitivity to substrate induced noise. The width of MND1 and MND2 is 325 μ m. Each transistor has 0.5 mA bias current. The bias current generator consists of four current sources. The output stage is a current mirror with a gain of 1.4 driving the regenerative amplifier. Simulations show that the -3 dB bandwidth is ~ 220 MHz. This is sufficient to make the recovery time of the comparator < 2 ns from a full negative voltage to a 5 mV positive input voltage.

There is one single phase clock used throughout the circuit suitably inverted and delayed for the different stages. The regenerative stage is reset when the clock is high and amplifying when the clock is low.

A simple analysis shows that the speed of the regenerative stage is proportional to capacitance on the nodes 4 and 5 of fig. 1, while inversely proportional to the transconductance of cross-coupled transistors. Therefore, the doughnut layout style [4] which minimizes capacitance has been chosen everywhere speed is important. The design of this stage was simplified to the choice of the relative number of transistors of identical

size to use in parallel. The time response t (in ns) of the regenerative amplifier for differential input current ΔI (in μA) is, according to simulations

$$t = 1/\tau \ln (1170/\Delta I) + 0.5 , \quad (1)$$

where $\tau = 3.8 \text{ ns}^{-1}$. As an example, the circuit requires 1.5 ns to resolve a 5 mV input to the differential pair. If the current difference ΔI is too small the circuit will enter into a metastable state. The voltages on nodes 4 and 5 are then equal to $\sim 2.5 \text{ V}$. The set and reset transistors of the RS flip-flop are dimensioned such that this flip-flop does not change.

The state of the RS flip-flop is transferred to the enable latch on the positive edge of the clock. This flip-flop is made of enabling gates and large set and reset transistors. These work in push-pull fashion to speed up the changing of state of the flip-flop and make the rise and fall times more symmetrical. It should be noted that timing jitter in the output transition times will directly degrade the resolution of the converter.

3. TRANSCONDUCTANCE AMPLIFIER

The transconductance amplifier is based on the circuit described in ref. [5]. The high-frequency response has been augmented by the neutralization of the gate drain capacitance [6] as shown in fig. 2. The effect of which is to make the high-frequency response of the integrator more than 1 GHz (fig. 3). The layout is straightforward as shown in ref. [6]. An improved common-mode regulator amplifier is also needed because the comparator is not sensitive to the common mode signals.

4. D/A CONVERTER AND BIAS CURRENT SOURCES

A complementary current switch together with respectively a NMOS and a PMOS regulated current source (80 μA) is used as a single-bit D/A converter (fig. 4). Neutralization is also used in this stage to minimize parasitic switching transients.

The bias circuitry is distributed as currents in order to reject substrate voltage fluctuations. The total power consumption is $< 50 \text{ mW}$ at 150 MHz.

5. SIMULATIONS

The design of a second-order sigma–delta converter was made with help of a custom high-level discrete time simulator. The block diagram of fig. 5 shows the components with values as simulated. The effect of the delay and time amplitude

dependence of the comparator was modelled as shown in eq. (1). Also table look-up methods were used to model the non-linearity of the transconductance amplifier.

6. EXPERIMENTAL RESULTS

Figure 6 shows the layout of the test circuit which has been integrated using a 2 μm CMOS technology. The size of the modulator is $930 \times 1040 \mu\text{m}^2$. The performance of the converter has been measured using a 150 MHz oscillator and signal generator with sinewave output with a frequency of 146 kHz. The output bit stream was analyzed using a 32 K fast Fourier program. An example is shown in fig. 7 where also the result from a simulation is plotted. As seen, the agreement of the theoretical and the experimental performance is excellent for high frequencies. It should be noted that simulations show that by lowering the value of transconductance of g_{m2} (fig. 5) by a factor 2 the peak in the quantization noise will be moved to a higher frequency and a better performance could be expected. The difference in the noise floor at lower frequencies is believed to be due to packaging, the measurement set-up and also substrate coupling. Figure 8 shows the signal-to-noise plus distortion (SNDR) as a function of input voltage. A 60 dB dynamic range with 9-bit resolution has been measured.

7. SUMMARY

This paper describes the design of a new continuous time current switching second-order sigma–delta data converter in 2 μm CMOS process and shows the operation of the circuit at a clock frequency of 150 MHz.

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Fig. 1 The schematic of the fast comparator

Fig. 2 Schematic diagram showing the principle of the transconductance amplifier used for the integrators

Fig. 3 Phase shift (top) and frequency response of the integrator (from simulations)

Fig. 4 The D/A-converter schematic

Fig. 5

The block diagram of the sigma-delta converter. $R1 = R2 = 100\text{k}\Omega$, $C1 = C2 = 7.5\text{pF}$, $gm1 = gm2 = 1.2\text{ mA/V}$ and $g1 = g2 = 0.16\text{ mA/V}$

Fig. 6 Plot of the layout of the sigma-delta converter

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Fig. 7 Measurement (top) and simulation 32k FFT spectrum showing the performance of the 150 MHz sigma-delta converter

Fig. 8 Measured signal to noise and distortion ratio versus input signal level