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A self adjusting delay circuit for pixel readout chips

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Abstract

A simple concept for automatic adjustment of important VLSI-circuit properties was proposed in [1]. As an application, a self adjusting monoflop is reviewed, and detailed measurements are discussed regarding a possible implementation in the LHC 1 readout chip for the ATLAS-experiment [2].

1 Introduction

Semiconductor pixel detectors gain importance not only in particle physics but also in medical and biological applications. Due to the system requirements and modern submicron technologies the readout chips are getting more complex. Besides the preamplifier and comparator additional digital and analog components are implemented for example for trigger generation or data sparsification. Pixel detectors for the ATLAS-detector at the LHC collider at CERN contain more than 10^8 channels. In order to obtain an optimal performance the whole system has to be very uniform, e.g. all channels should behave exactly alike. In these complex cells however good matching is very difficult to achieve due to many design constraints, for example a limitation in power consumption and space.

In [1] a method to overcome these matching problems is presented. The important circuit properties are set by control values in each pixel cell individually. This control value is adjusted automatically by applying an external calibration pulse, so that a complete independence from component mismatch is achieved. In this paper we shortly review the general concept and discuss as an example a self adjusting monoflop. Emphasis is put on the detailed measurements and the possible implementation in the LHC 1 [3] chip for the ATLAS-experiment. The possibility to use self adjusting circuits without introducing additional deadtime is investigated.

2 General Concept

The concept of the self adjustment circuit is shown in figure 1. The circuit block which performs the desired feature (for example a monoflop or a comparator) has a control input. The control value is stored here on a capacitor and is automatically adjusted in order to obtain system uniformity. A simple logic unit analyses the output signal and compares this signal with an external reference signal if necessary. If the output signal differs from the intended value the control value is decreased or increased respectively until the output signal matches.

Fig. 1. General concept of a self adjusting circuit

The adjustment procedure in a complex chip is very simple. One pixel cell is chosen, the adjust circuit is enabled, and a calibration signal is applied. The control value is thus regulated automatically. After a few cycles the circuit property is adjusted and the next cell is chosen until the whole system is tuned.

Due to the analog storage of the control value, leakage currents cause a slow drift. This limits the storage time before new adjustment cycles have to be executed. The rate of these 'refresh cycles' has to be reasonably low. In order to avoid this drift, analog EEPROMs or a digital storage could be used but with an increase of circuit area and complexity.

3 A self adjusting delay

The idea of automatic adjustment was implemented in a monostable circuit which produces a delay of a predefined time. This circuit can be used for example in the LHC 1 chip which was developed by the RD19 [3] group at CERN for the ATLAS-experiment. Due to the bunch structure of the LHC p-p-collider collisions occur every 25 ns. Interesting events are selected by a Level-1 trigger signal which is available exactly ($2\mu\text{s}$) after the interaction. The pixel data has to be stored in each pixel cell until this trigger signal occurs. The LHC 1 chip uses monoflop with $\approx 2\mu\text{s}$ pulse width to perform this function.

The comparator starts a delay chain with an overall delay (preamplifier, comparator and delay chain) of $2\mu\text{s}$. If the trailing edge of the signal after the delay chain coincides with the level 1 trigger, the pixel cell will be read out. In order to get a correct association between the event and the trigger signal, the delay has to be precise to 25 ns. Three trimming bits are used to adjust the delay in the current design. Recent measurements show [4] channel to channel mismatch due to large process parameter variations. Two approaches are proposed to overcome this problem. Detailed process characterizations and simulations are performed by [5] to optimize the delay chain. Another possibility is the principle of the self adjustment.

Figure 2 shows the self adjusting monoflop circuit [1]. The output signal of the comparator opens switch $T1$ so that the input node of the comparator is discharged with the currents I_{coarse} and I_{fine} . The voltage V_{ramp} reaches the threshold of the comparator after approximately $2\mu s$, and an output signal is produced. The delay time is determined by the value of C_{ramp} , the threshold of the comparator V_{thr} , and the currents I_{coarse} , and I_{fine} . I_{coarse} provides approximately 80% of the current, the rest is provided by I_{fine} , which is used as an adjustable current source. The current, which can be sunk by this source, is set by the control value V_{fine} stored on C_{fine} .

Fig. 2. Self adjusting monostable circuit

the transistors $T2$ and $T3$ of the charge redistribution circuit conduct, and $C_{correction}$ is charged to V_{high} . Then the enable signal opens the pass-transistor ($T5$) and the charges of C_{fine} and $C_{correction}$ redistribute. If $V_{correction}$ is higher than V_{fine} , V_{fine} and also the current I_{fine} are increased. The delay time is decreased. The size of these regulation steps is basically determined by the ratio of $\frac{Q_{correction}}{Q_{fine}}$ and the transconductance of the transistor T_{fine} .

3.2 Circuit Performance

The performance of this circuit is characterized by the following measurements which were obtained with a prototype of the self adjusting delay in the $2.4\ \mu\text{m}$ technology from MIETEC.

– Jitter

The delay time of one single channel shows variations if measured several times. This jitter is caused by the noise on the falling edge of the mono-flop and by the size of the regulation steps. For a large difference between the output signal and the reference signal the regulation steps are approximately 10 ns, but they are decreasing if the difference is getting smaller. For a delay time of $2\ \mu\text{s}$ the jitter of the system after the regulation is dominated by the noise. The jitter at room temperature is $\sigma = 1.0\ \text{ns}$.

– Drift

As mentioned earlier, the time stability of the analog storage is limited by leakage currents which change V_{fine} . The drift without regulation is shown in figure 3. For room temperature a value of approximately 10 ns drift for a duration of 100 s without regulation is achieved. The value of the leakage current depends on the temperature, on the radiation damage and on the technology size. For lower temperatures and smaller technology sizes as planned in the ATLAS-experiment the drift is reduced. In order to minimize the leakage current the well of the pass-transistor $T6$ has a separate bias connection.

– Spread

The self adjusting systems do not suffer from parameter variations. The effects which can cause some channel to channel or chip to chip variations are different noise or leakage current values. Therefore the jitter and the drift show variations. Five chips were tested, the jitter was in the range of $0.8\ \text{ns} \leq \sigma \leq 1.6\ \text{ns}$ and a drift $5\ \text{ns} \leq t_{\text{drift}} \leq 20\ \text{ns}$ in 100 s without regulation was observed.

– Refresh-rate

Refresh cycles are required to avoid drift of the control value. The refresh rate is determined by the leakage currents and the size of the regulation steps. For the worst drift in the given setup a refresh frequency of $\approx 5\ \text{Hz}$ is necessary to obtain a constant delay time. These refresh cycles introduce

Fig. 3. The drift of the delay time without refresh cycles

additional deadtime, because the monoflop is not sensitive for hits during the regulation cycles.

– **Size and complexity of the circuit**

The circuit should be as 'simple' as possible. The new design in a modern $1.0\ \mu\text{m}$ -technologie (FASELEC CMOS) contains 23 transistors and the used area of $40\ \mu\text{m} \times 50\ \mu\text{m}$ is dominated by the for the moment conservative size of the current source transistor T_{fine} . The layout is adapted to the LHC 1 front end design, e.g. it could be implemented in the design without any further modifications.

Possible problems of this circuit are based on the analog storage of the control value. Due to radiation damage the leakage currents and the drift get worse, the refresh rate could be too high in this case. Another problem is the single event upset in the pass transistor. If a particle crosses the p-n-diode of the pass transistor, an additional charge is deposited on the storage capacitor.

4 The ATLAS bunch structure

The LHC bunch structure is shown in figure 4. It can be seen that there is a gap of $3.17\ \mu\text{s}$ every $89\ \mu\text{s}$. This gap could be used to inject the calibration pulses used for the self adjustment of the delay. According to the drift measurements only 1 pixel per chip¹ has to be refreshed per gap. It is possible to refresh several pixel per column simultaneously.

¹ The current LHC 1 chip contains 16 columns with 127 sensitive rows.

Fig. 4. The LHC bunch structure

In addition to this the 11 gaps of 950ns could be used for example for threshold tuning.

5 Possible improvements

- Instead of the analog storage a digital storage could be implemented. The drift would be avoided and refresh cycles with a very low rate to update the digital value would be sufficient. The digital value has to be adjusted from time to time to scope with ageing or temperature effects.
- The size of the circuit is dominated by the transistor T_{fine} . This transistor has to be very long to minimize the g_m , and to obtain therefore small regulation steps. Another possibility is to use a short transistor as current source and use the Early-effect to adjust its current. The drain voltage of this transistor is set by a cascode transistor. Besides the size reduction, the voltage range of the control value is increased. A prototype based on this principle has recently been submitted.

6 Summary

A self adjusting technique for VLSI readout chips was reviewed and a delay circuit was described in detail. This concept is completely independent from component mismatch caused by process parameter variations, temperature effects or ageing.

The measured performance of the delay was presented and it was shown, that this circuit fullfills the requirements for the ATLAS-experiment. The needed refresh pulses can be adapted to the LHC bunch structure without introducing any additional deadtime.

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