UNIVERSITÄT BONN

Physikalisches Institut

SCAN-9711032

CERN LIBRARIES, GENEVA

First results from ATLAS pixel detectors *

Sw 9746

P. Fischer

Physikalisches Institut der Universität Bonn

Abstract: The ATLAS experiment at LHC will use several layers of silicon pixel detectors as the innermost elements of the semiconductor tracker. The barrel layers in the central region and the disks in the forward regions will be assembled from detector modules with active areas of $\approx 10 \text{ cm}^2$ each. Every module will contain a silicon sensor with pixels of $50 \times 300 \mu\text{m}^2$ size and 16 (10) VLSI frontend chips which are connected to the sensor using a flip chip technology. Each of the overall $> 10^8$ pixel elements is connected to a low power, high speed charge sensitive preamplifier, a fast discriminator, and a readout system which operates at the 40 MHz rate of LHC.

The pixel system is presented with an emphasis on the readout electronics. The requirements for ATLAS are discussed and compared to the measured performance of the front end electronics.

* Work supported by the German Ministerium für Bildung, Wissenschaft, Forschung und Technologie (BMBF) under contracts no. 05 7BN 18P 4 and 05 6BN 10I and by the Ministerium für Wissenschaft und Forschung des Landes Nordrhein-Westfalen under contracts no. IV A5 – 106 001 94 and IV A5 – 9036.0.

Post address:
Nussallee 12
D-53115 Bonn
Germany

BONN-HE-97-03
Bonn University
July 1997
ISSN-0172 8733

First results from ATLAS pixel detectors[★]

P. Fischer

Physikalisches Institut der Universität Bonn, Germany

for the ATLAS Pixel Collaboration [1]

Abstract

The ATLAS experiment at LHC will use several layers of silicon pixel detectors as the innermost elements of the semiconductor tracker. The barrel layers in the central region and the disks in the forward regions will be assembled from detector modules with active areas of $\approx 10\text{ cm}^2$ each. Every module will contain a silicon sensor with pixels of $50 \times 300\text{ }\mu\text{m}^2$ size and 16 (10) VLSI frontend chips which are connected to the sensor using a flip chip technology. Each of the overall $> 10^8$ pixel elements is connected to a low power, high speed charge sensitive preamplifier, a fast discriminator, and a readout system which operates at the 40 MHz rate of LHC.

The pixel system is presented with an emphasis on the readout electronics. The requirements for ATLAS are discussed and compared to the measured performance of the front end electronics.

1 Introduction

The ATLAS [2] experiment at the future LHC collider will contain several layers of tracking devices as the innermost detection elements [3]. They are arranged as cylindrical 'barrels' in the central region and as 'disks' in the forward and backward regions. While the barrel layers of the outermost transition radiation detector and the intermediate silicon strip detector provide one dimensional hit information in crossed layers, the innermost layers will consist of silicon pixel detectors which provide the true two dimensional information needed in the very high multiplicity environment of LHC. At the design beam luminosity of $10^{34}\text{ cm}^{-2}\text{ s}^{-1}$, the maximum track density at the

[★] Work supported by the German Ministerium für Bildung, Wissenschaft, Forschung und Technologie (BMBF) under contracts no. 05 7BN 18P 4 and 05 6BN 10I and by the Ministerium für Wissenschaft und Forschung des Landes Nordrhein-Westfalen under contracts no. IV A5 – 106 001 94 and IV A5 – 9036.0.

innermost pixel layer is expected to be ≈ 3 tracks per bunchcrossing per cm^2 . This would produce by far too many ambiguous hit positions in crossed strip layers.

The ATLAS pixel detector will provide one space point per layer with a resolution of $\sigma_z = 60 \mu m$ in the beam direction and $\sigma_{r\phi} = 12 \mu m$ in the other direction. The interaction rate at LHC is 40 MHz so that the electronics must be able to identify a particle impact within a 25 ns time window. The hits must be stored temporarily on the readout chips until a trigger signal, which has a latency of 80 – 100 bunch crossings, selects events for readout through a serial data link. The pixel system has to withstand a high radiation dose during the anticipated 10 years of operation of ATLAS. The expected integral dose for the innermost pixel layer is 200kGy or $5 \times 10^{14} n cm^{-2}$. This requires the use of radiation hard technologies for the electronic chips and an appropriate design of the silicon sensor.

Fig. 1. Simplified schematic layout of one of the staves which form the barrel pixel layers. Several modules consisting of the silicon sensor and a support structure are mounted on a thin cooling tube. The modules are tilted so that a perfect overlap is guaranteed for tracks with $p_T > 0.5$ GeV. The electronic readout chips are mounted upside down on the detector substrate using a flip chip technology.

2 Geometrical layout of the pixel detector

The pixel detector system will consist of 3 barrel layers at $r = 4.7, 10.5$ and 13.7 cm with a length of 77 cm each and 2×4 disks in the forward and backwards regions at $z = 49, 61, 76$ and 104 cm with inner radius $r_i = 11$ (15) cm and outer radius $r_o = 20$ cm. This adds up to a total active pixel area of $2.3 m^2$. The barrel consists of several 'staves' running in the z (beam)-direction which are mounted on a support structure at the ends. Fig. 1 shows a simplified schematic view of a section of a stave. 13 modules are mounted on the support tube which is also used to carry the coolant needed to remove the heat generated in the module electronics and the sensor (in order to reduce the effects of irradiation on the sensors, they are cooled to below $-6^\circ C$). The modules are mounted with some overlap in the z direction (and the individual staves have some overlap within the barrel). This hermetic coverage in every layer for tracks with $p_T > 0.5$ GeV guarantees three pixel space points for $|\eta| < 2.5$ for

collision positions up to $2\sigma_{beam}$ (11 cm) from the nominal collision point. Due to an aggressive use of low-Z materials (graphite, carbon fiber, carbon-carbon composites), the radiation length will be between 1.1 and 1.6% X_0 per barrel layer, depending on the detailed implementation.

Every barrel module has an active area of $16.4 \times 60.4 \text{ mm}^2$ and consists of a support structure, the silicon sensor and 2×8 front end (FE) readout chips which are mounted upside down directly on the sensor substrate using a flip chip technology. The interconnection between the chips can be provided directly on the detector substrate and with thin capton cables mounted on top of the chips. An additional module control chip (MCC) controls the FE chips and transfers the hit data serially off the module. Wedge shaped modules with 12 FE chips are used in a similar way for the disks.

3 The silicon sensor

The silicon sensor is made of $< 250 \mu\text{m}$ thick (the minimal possible thickness will be used to reduce the radiation length) n -type silicon which will convert to p -type like material after irradiation. On the active area of $16.4 \times 60.4 \text{ mm}^2$, more than 60000 pixels with a size of $50 \times 300 \mu\text{m}^2$ will be implemented. The pixels in the edge regions are slightly bigger so that no active area is lost. No bias structures have to be implemented as the pixels are dc-coupled to the preamplifier inputs. Several designs are being investigated for the pixel structure including p -stop designs and p -spray solutions (see ref. [4] in these proceedings). Some important aspects of the sensor design are:

- *The radiation hardness:* The irradiation of the sensor has two major consequences:
 1. Fixed charges are introduced at the $\text{Si} - \text{SiO}_2$ interface. This can lead to very high local fields and subsequent breakdown which has to be avoided by appropriate design. According to simulations, the maximal fields at the surface decrease with the build-up of the oxide charge layer in p -spray designs [4]. Initially good p -spray devices should not degrade after irradiation.
 2. As the resistivity of the bulk material decreases after type inversion, the voltage needed to fully deplete the sensor must be increased. This requires in particular a careful design of the guard structures [6] where the full voltage drop occurs. A high collecting field is also needed to reduce the effects of trapping in damaged sensors. Recent results (ref. [5] in these proceedings) show, that the collected signal charge after full irradiation is still acceptable, if the detector is operated at high bias voltages.
- *Capacitances:* The noise and speed of the preamplifiers at a given power budget depend strongly on the total capacitance of the pixel diode which should therefore be minimized. Another aspect is crosstalk between adja-

cent pixels. Due to the limited dynamic input impedance of the preamplifiers, a signal charge causes a small voltage swing at the input. This signal can capacitively couple into the neighbour pixel through the inter-pixel capacitance. Decreasing the inter-pixel capacitance and increasing the other contributions decreases crosstalk through the detector. Several structures with different capacitance ratios are presently being studied.

- *Testability:* Due to the large number of pixels on one sensor, the characterization of standard pixel detectors prior to mounting is very difficult. In particular, the leakage current cannot be measured easily as there is no common bias line in the dc coupled designs. Some of the sensors which are presently produced therefore include the possibility to bias the pixels for testing with a punch-through mechanism. This should also provides an operational safety if individual pixel diodes are left unconnected during the flip-chip assembly.

4 System readout architecture

The front end chips (FE) which are flip-chip mounted directly onto the sensor substrate have a size of $11 \times 7.4 \text{ mm}^2$. The layout of the electronic circuitry has a one to one correspondance to the detector geometry so that elements of $50 \times 300 \mu\text{m}^2$ size will be arranged in 24 columns of 160 pixels each. Every pixel contains a preamplifier, a discriminators (two in a dual discriminator scheme) and logic to transfer the hit data as fast as possible towards the chip periphery (this zero supression at this level is needed to reduce the data rate by a factor 10^4). Two architectures are presently being pursued, one using a synchronous shift register to clock out the addresses of hit pixels, one using a time-stamping mechanism and a fast asynchronous scan for hit pixels. At the periphery of the chip, the hit address and a crude analog pulseheight information (the width of discriminator output signal in units of the crossing clock) is stored in a pool of buffers until the trigger signal accepts or discards the hit. Accepted hits are serialized and transferred on a single low voltage differential line pair with 40Mbps to the module control chip (MCC). The MCC collects the data from all 16 (10 for the disks) FE chips, bundles them according to the trigger number and sends a compressed event to the end of the stave / disk where a ladder controler chip LCC performs the same operation on a stave / disk level. The data is then sent to readout buffers in the counting room for storage. Trigger and event number in every data block guarantee the consistency of the event.

5 Requirements for frontend chips and measured performance

Several partially conflicting requirements, some of which are valid in general for a pixel system, some of which are particular to the high rate, high irradiation environment of LHC have to be met by the FE readout chips. These requirements mainly concern the pixel part which consists of a low noise charge sensitive preamplifier, a discriminator with adjustable threshold (two discriminators in a dual discriminator scheme), charge injection and masking possibilities and a digital readout logic which transfers the hit information to the chip periphery. A maximum power consumption of $40\,\mu\text{W}$ per pixel cell is allowed in order to limit the cooling effort which is required to keep the sensor at a temperature below -6°C . (An increase in cooling power would add unacceptable radiation length to the module.)

As many chips are mounted on one module, they must be carefully tested on a probe station before assembly in order to select known good dies. The injection of an analog charge signal is therefore possible in every pixel. The design of the chips should be as tolerant as possible with respect to single point failures. In particular, single bad pixels, which could fire all the time, may not flush the data acquisition. Every pixel can therefore be masked by disabling the hit signal.

In the following sections, we discuss some other important requirements and compare them with measured results obtained with two different FE prototype chips which have also been bumped to detectors and studied in a test beam.

5.1 Pixel size / spatial resolution

The pixel cells should be as small as possible in order to achieve the best possible spatial resolution. For a purely binary readout (e.g. no amplitude information available) with pixels of $50\,\mu\text{m}$ width, the expected resolution is $50/\sqrt{12} = 15\,\mu\text{m}$. With a small fraction of double hits, the $\sigma_{r\phi} = 12\,\mu\text{m}$ - requirement of ATLAS will be easily met. For a satisfactory z -resolution, pixels of $300\,\mu\text{m}$ length or slightly longer pixels in a 'bricked' geometry (every second row shifted by half a pixel length) are needed. The presently existing FE chips have active pixel lengths of $536\,\mu\text{m}$ resp. $336\,\mu\text{m}$ and the next generation will use $400\,\mu\text{m}$ for more design freedom in the prototyping phase. Beam measurements with pixels of $50 \times 536\,\mu\text{m}$ size using only binary information (analog information is available but has not been used yet) showed resolutions of $15 - 12\,\mu\text{m}$ in the short direction, depending on the amount of charge sharing due to inclined tracks. In the long direction, resolutions up to $\sigma_z = 82\,\mu\text{m}$ could be observed for optimal charge sharing with bricked pixels.

5.2 Noise

The signal charge which is collected at the preamplifier input (depending on the detector thickness, charge sharing, the depletion depth and on trapping) is not precisely known for highly irradiated detectors, but recent measurements indicate, that charges above $6 ke^-$ can still be expected after 10 years of operation [5]. The threshold must be set as low as possible in order to achieve a high detection efficiency. The r.m.s. noise should therefore be in the order of $200 e^-$ so that the noise hit rate at a threshold of $2000 e^-$ is below 10^{-6} hits/pixel/crossing. Due to the low input capacitance of < 300 fF, this goal is relatively easy to achieve. Measurements have shown typical r.m.s. noise values of $60 e^-$ without and $130 e^-$ with bonded pixel diodes of $436 \mu m$ length.

Fig. 2. Threshold distribution of a pixel readout chip with threshold tuning in every pixel. Without adjustment, the dispersion is $90 e^-$, after adjustment in every pixel, it is negligible.

5.3 Threshold variations

The thresholds in the pixel elements on one chip have a spread σ_{Thr} . Pixels with particularly low thresholds are susceptible to noise hits, while pixels with high thresholds are less efficient. σ_{Thr} should therefore be in the order of the noise, e.g. $\sigma_{Thr} < 200 e^-$. Fig. 2 shows the distribution of pixel thresholds across a chip which uses a bipolar discriminator for good matching (upper curve). Random fluctuations and systematic variations (partially due to a mirrored geometry of the pixel cells) can be clearly seen. In the unirradiated

ted chip, $\sigma_{Thr} = 90 e^-$ is measured. The chip offers the possibility to adjust the threshold individually in every pixel. In the lower curve, the thresholds are shown after adjustment. The dispersion is now negligible. If the initial threshold spread increases after irradiation, the adjustment can be used to reestablish excellent uniformity.

5.4 Response time

In order to associate the hit signal from the discriminator to the correct beam interaction, the response time must be below 25 ns. Every discriminator needs more time to respond for signals just above the threshold. We require a signal to be 'in-time' for charges which are at least $1000 e^-$ above the threshold. Measurements at the nominal power dissipation show that a charge of only $200 e^-$ above a threshold of $2000 e^-$ is needed for full in-time efficiency if no detector is bonded. This value increases to $1000 e^-$ with $436 \mu\text{m}$ long pixel diodes connected to the input. With smaller pixels, the required overdrive will be at an acceptable level. If the amplitude of the signal is measured, it can be used to correct for the time walk. A two discriminator concept, where one discriminator with a low threshold performs the timing, the second with a higher threshold performs the amplitude discrimination, could avoid the time walk problem. It is presently being implemented in a FE chip.

Fig. 3. Averaged output signal of a charge sensitive pixel preamplifier with dc feedback for an input charge of $\approx 20 ke$ measured with a buffer with a gain of ≈ 0.4 . The different curves correspond to increasing feedback currents. The shaping loss is small and the stability even for short shaping is very good.

5.5 *Leakage current tolerance*

As the pixels are dc coupled, all detector leakage current flows into the preamplifier input, which must therefore be able to source currents of up to ≈ 100 nA for particularly bad pixels. Such a high current produces large dc shifts in the output voltage if traditional resistive feedback configurations are used. A constant current dc feedback scheme with high leakage current tolerance and high stability has therefore been developed. Fig 3 shows a buffered output signal where the very good stability and the small shaping loss for short shaping times is visible. The leakage current tolerance could be measured up to 30 nA using an indirect method and a chip with dedicated test structures is presently being studied.

5.6 *Analog possibility*

For monitoring purposes and in order to improve the spatial resolution, a low precision readout of the signal charge is desirable. The present implementations both use a time-over-threshold scheme where the width of the discriminator output (which is a function of the signal amplitude) is measured in units of the crossing clock. This is achieved by sending hit information for both, the leading and trailing edge of the hit signal to the chip periphery where the data is sorted and stored in temporary buffers. This introduces very little extra circuitry in the space-constraint pixel cell. The quality of the analog information depends on the uniformity of the preamplifier/discriminator chains and on the maximum length allowed for the hit signal (long signals introduce deadtime). A resolution of ≈ 4 bits can be achieved easily.

5.7 *Radiation hardness*

The chips must survive very high irradiation doses and therefore have to be implemented in 'radiation hard' processes offered by different chip vendors. Several test structures have been designed in such technologies. As an example, a DMILL preamplifier shows a small ($\approx 10\%$) increase in signal amplitude after an initial irradiation of 5 kGy. The gain then remains constant up to the maximal measured dose of 150 kGy. A DMILL discriminator shows an initial threshold shift of 500 e⁻ and remains then within 200 e⁻ up to the maximal measured dose of 15 kGy.

6 Summary

The latest generation of ATLAS pixel frontend chips meets most of the demanding specifications of the experiment like power consumption, noise, threshold variations, speed and testability. The next generation will implement a fully ATLAS compatible readout architecture and will have pixel sizes of $50 \times 400 \mu\text{m}^2$ (close to the ATLAS goal of $50 \times 300 \mu\text{m}^2$) so that a further improvement in performance (lower input capacitance) is expected. A demonstrator module consisting of these chips bonded to optimized pixel sensors will be assembled at the end of 1997.

References

- [1] Member institutes of the ATLAS pixel collaboration:
State University of New York, Albany, USA; LBNL and University of California, Berkeley, USA; Physikalisches Institut Universität Bonn, Germany; Experimentelle Physik IV, Universität Dortmund, Germany; University of California, Irvine, USA; Dipartimento di Fisica e INFN Genova, Italy; Centre de Physique des Particules de Marseille, France; Dipartimento di Fisica e INFN Milano, Italy; NIKHEF, Amsterdam, Holland; New Mexico Center for Particle Physics, University of New Mexico, Albuquerque, USA; Department of Physics and Astronomy, University of Oklahoma, Norman, USA; Academy of Sciences of the Czech Republic, Institute of Physics, Prague, Czech Republic; Charles University, Faculty of Mathematics and Physics, Prague, Czech Republic; Czech Technical University, Faculty of Mechanical Engineering, Prague, Czech Republic; University of California, Santa Cruz, USA; Fachbereich Physik, University of Siegen, Germany; Dipartimento di Fisica e INFN Udine, Italy; Department of Physics, University of Wisconsin, Madison, USA; Fachbereich Physik, Bergische Universität, Wuppertal, Germany.
- [2] Letter of Intent of ATLAS, CERN/LHCC/92-4 LHCC/I2 (1992); ATLAS Technical Proposal, CERN/LHCC/94-43, LHCC/P2 (1994).
- [3] Technical Design Report of the ATLAS Inner Detector, CERN/LHCC 97-16 (1997).
- [4] Design of the Sensor for the ATLAS Pixel Detector, G. Lutz, R. H. Richter, T. Rohe, these proceedings.
- [5] Recent Results of R&D for the CMS Pixel Detector, W. Bertl, K. Gabathuler, R. Horisberger, B. Henrich, M. Lechner, these proceedings.
- [6] A. Bischoff et al., Breakdown protection structures for silicon strip detectors, Nucl. Inst. Meth. **A236** (1993) 27-37