A Large Dynamic Front End Integrated Circuit for Avalanche Photo Diodes

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Abstract

Results on a large dynamic front end integrated circuit for readout of Avalanche Photo Diode with an associated low consumption non linear compressor scheme are presented.

I. INTRODUCTION

The challenging experimental conditions, under which the LHC detectors will have to run, have triggered a series of R&D activities in many fields, particularly in photodetectors and their associated electronics. We present a front-end electronic designed to be a trade-off between wide band low noise and low power consumption. The huge dynamic range of the detector is compressed to fit within a

fast (40 MHz) 12 bits digitization. This electronic consists of a large dynamic, low-gain preamplifier, coupled to a shaping-amplifier set and an analog compressor [1]. The synoptic diagram is shown on Fig. 1. An ASIC has been designed in the framework of Cadence software with Spice+ of AWB and Spectre of Artist respectively for the simulation and the layout. The technology used is the 1.2 μm BiCMOS of A.M.S.*. This design should be easy to move to radiation-hard technology such as DMILL. An ASIC realization has been done in DIL-8 pin package for the preamplifier and in a JLCC 28 pin package for the compressor shaping amplifier part. All amplifier elements of the chain are similar and cascaded to the next one through a 50-ohm load, the output of each stage can be extracted to operating test purposes.

Fig. 1. General scheme of the very-front-end electronics.

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II. THE PREAMPLIFIER

The structure of the preamplifier is shown in Fig. 2a. The circuit accepts positive and negative input pulses and has a 50-ohm output driver, able to drive signal from 1.2 V to -2 V with a linearity better than 1%. The set-up is designed to be used for a direct or an ac coupling to the Avalanche Photo Diode [APD]. Most of the result presented here has been obtained with a 100 pF capacitance detector, but the circuit has been designed to accept detector capacities up to 800 pF. The power consumption is 46 mW with the foreseen +5 V and -5 V power supplies. With $R_i = 1.6 \text{ kohm}$ and $C_i = 15 \text{ pF}$ (Fig. 2a), a maximum ac input current of 4.8 mA is obtained, that corresponds to a maximum charge of 72 pC and a minimum of 103 nA corresponding to 1.5 fC. The sensibility to supply drifts has been tested in the $\pm 100 \text{ mV}$ range around the nominal supply voltage and exhibits a maximum output variation of $2.5 \mu\text{V/mV}$.

Fig. 2a. Functional scheme of the preamplifier.

The realized preamplifier has been tested with input square pulses of 15 ns duration generated by a Hewlett-Packard 8082A and a Phillips PM 5786 generator fed through a 10-kohm or a 1-kohm in series respectively for the low and the high dynamic tests. The injected charge at the input is $\sim 100 \text{ e/nA}$. The output waveform has been measured with a 500 MHz TDS 640A Tektronix oscilloscope. For the noise evaluation an amplifier with a gain of 100 has been put in series with the oscilloscope. Fig. 2b shows typical output waveforms on 50 ohm load. The measured noise with the full bandwidth found to be $66 \mu\text{V}$ R.M.S. is displayed in Fig. 2c. The slope is $623 \mu\text{V}/\mu\text{A}$ in these conditions.

The reduction of the bandwidth decreases the R.M.S. noise as expected. A value of 4100 e has been measured for a 100 MHz bandwidth which is often used for comparison in other work [2] and a value less than 3000 e for a reduced bandwidth down to 20 MHz.

At the full bandwidth a peaking time of 15 ns is measured with a 1 ns drift for the negative output. For a bandwidth reduction down to 20 MHz the peaking time = 30 ns, the slope = $0.454 \text{ mV}/\mu\text{A}$, the fall time = 180 ns and the input noise < 3000 e (2500 e is the lowest limit for the LHC physic and corresponds to 25 MeV). For positive signal input a little increase of the peaking time drift is observed up to 2 ns. At the same time the saturation current of the pulse occurs at -3 mA instead of 4.8 mA for the positive input.

In Fig. 3 the variation of the waveform for the input capacity ranging from 100 to 800 pF is shown.

For all the range of variation the overall R.M.S. noise varies only by a factor 3 as the result of a compensation effect with the bandwidth reduction, due to the input capacity increase on the $\sim 50\text{-ohm}$ -equivalent impedance of the input. The bandwidth reduction even for 800 pF is acceptable and gives the following parameter values: peaking time $_{\text{max}} = 25 \text{ ns}$, fall time $_{\text{max}} = 250 \text{ ns}$, slope = $0.400 \text{ mV}/\mu\text{A}$. The parameters of the preamplifier are summarized in Table 1.

Fig. 2b. Output pulses of the preamplifier driver.

Fig. 2c. Noise for different bandwidth conditions.

Fig. 3. Output pulse shapes for different detector capacities.

Fig. 4b. Compression function: output voltage versus input current for one stage compressor (measured) and four stage compressor (simulated).

For the measuring conditions of Fig. 4a, decompression has been made with measured Look-Up Tables (LUT) establishing the correspondence between the compressed amplitude and the not compressed ones, versus time. Taking into account the time drift mentioned above as displayed on Fig. 5, the decompression has been made with a 40 MHz clock through 5 LUT used for the waveform reconstruction and 1 LUT for the amplitude correction. Fig. 6a shows the reconstructed signal, measured after compression in the conditions of Fig. 4a (one compression stage) and the amplitude error caused by the peaking time drift is shown in Fig. 6b. This last correction measured by the calibration is included in the LUT used for the pulse reconstruction.

V. CONCLUSIONS

A complete front end chain has been designed, including a preamplifier shaper-driver associated with one or four shaping-amplifier-compressor-drivers. The compression setup does not increase the consumption nor the noise of the system. In the present design, for a full bandwidth, an equivalent input noise of 2300 e has been reached with a peaking time of 35 ns stable within 6 ns in the full dynamic range greater than 17 bits. The compression/decompression scheme, with the measured LUT implemented on a PC, is able to reconstruct the current input within some 10^{-3} and for a 12 bits the error of the measurement at peak after decompression in a LUT is dominated by the digitization.

Fig. 5. The full dynamic range peaking time drift for the single compression stage.

Fig. 6. a) Decompressed pulse: an example. b) Amplitude correction due to the drift in time versus the current at the preamplifier input.

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Table 1
The measured parameters of the preamplifier module unit.

Bandwidth	Cin = 100 pF			Cin = 800 pF
	Full	100 MHz	20 MHz	100 MHz
Peaking Time	15 ns	17 ns	30 ns	25 ns
Fall Time	160 ns	~160 ns	180 ns	250 ns
Slope ($\mu\text{V}/\mu\text{A}$)	623	590	454	400
Output RMS noise	66 μV	25 μV	< 18 μV	~ 55 μV
Equiv. input noise	10300 e (103 nA)	4100 e (41 nA)	< 3000 e	~ 13000 e
A.C input current	+ 4.8 mA	+ 4.8 mA	+ 4.8 mA	
" " "	- 3 mA	- 3 mA	- 3 mA	
Dynamic	+ 47 000 (16 bits)	+ 117000 (17 bits)		
"	- 29 000 (15 bits)	- 73 000 (17 bits)		
Dissipated power	46 mW			

III. THE SHAPING-AMPLIFIER CHAIN

As shown on Fig. 1, the preamplifier has been associated with four amplifiers of similar structure linked by simple integrating RC filters. Each amplifier is designed to drive a 50-ohm load and can be used individually in the test circuit. These RC filters adjust the peaking time at the required value (40 ns for the LHC-CMS experiment) and decrease the noise for each stage; the equivalent noise measured at the first stage amplifier with 35 ns of peaking time is 2300 e. The maximum gain expected for the complete chain is of about 40 for the smallest detectable input signals which are small as 20 nA. Nevertheless the measurement presented below on the compressor function has been done with only one stage due to improper polarization of some of them caused by technology parameter variations, which present to use of the full chain.

IV. THE COMPRESSOR

A compression function has been designed through the four stages shaping-amplifier chain with the use of MOS transistors in derivation on the feedback resistor of each stage. The distributed compression function on the four amplifier stages has been chosen to cover 300 μA input current (~300 GeV) into a 11 bit range and the overall dynamic needed to fit the full range of amplitude into the limited 12 bit adc range presently available on the market. The compression is obtained by the progressive conduction of the MOS transistors controlled by the amplitude of the output signal according to the polarization threshold of the transistors. The total gain of the shaping-amplifying chain is decreased from its maximum value (40) to ~1. For a square test pulse similar in charge and current to the expected APD signal like in CMS detector [3], Fig. 4a displays the non-compressed negative signal and the compressed output signal measured with one compression stage only, followed by a RC filter slowing down the output signal to a peaking time of 40 ns. The peaking time drift stays within the 6 ns width in the full amplitude range to be compared to the 4 ns obtained by the simulation in the same conditions. Fig. 4b shows the measured compression function for one stage and

the simulated one for the four compression stages of Fig. 1. The right scale of Fig. 4b refers to the slope of the system. With Fig. 1 configuration, a sufficient gain would be obtained for the small signals as well as a sufficient compression function for the full dynamic range foreseen, with a minimum peaking time shift.

The present compressor scheme does not increase power consumption in its steady state and does not add extra noise.

Fig. 4a. Square input test pulse; output pulse shape, compressor "off" and output pulse shape, compressor "on".