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READ OUT ELECTRONIC DEVELOPMENT

FOR MICROSTRIP DETECTORS

Université Louis Pasteur

IN2P3

23 rue du Laess, BP 20
67037 STRASBOURG-Cedex 02
FRANCE
Téléphone : (33) 0-388 777 555
Télécopie : (33) 0-388 283 485
<http://www-lepsi.in2p3.fr/>

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A 128 CHANNELS VLSI MIXED FRONT-END READ OUT ELECTRONIC DEVELOPMENT FOR MICROSTRIP DETECTORS

F. ANSTOTZ¹, Y. HU, J. MICHEL, J.L. SOHLER, D. LACHARTRE*

LEPSI² IN2P3/CNRS, Université Louis Pasteur Strasbourg

* CEA, DSM/DAPNIA/SEI CE-Saclay F-91191 Gif-sur-Yvette cedex

ABSTRACT

We present a VLSI digital-analog readout electronic chain for silicon microstrip detectors. The characteristics of this circuit have been optimized for the high resolution tracker of the CERN CMS experiment. This chip consists in 128 channels at 50 μm pitch. Each channel is composed by a charge amplifier, a CR-RC shaper, an analog memory, an analog processor, an output FIFO read out serially by a multiplexer. This chip has been processed in the radiation hard technology DMILL.

This paper describes the architecture of the circuit and presents test results of the 128 channel full chain chip.

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¹ Corresponding author - email : anstotz@lepsi.in2p3.fr - Phone : 33 388 777 551 - Fax : 33 388 283 485
² 23 rue du Loess BP 20 F-67037 STRASBOURG Cedex [http ://www-lepsi.in2p3.fr/](http://www-lepsi.in2p3.fr/)

1. INTRODUCTION

FILTRES (First Level TRacking Electronic System) follows closely the structure proposed by the RD20 collaboration [1][2][3][4]. This chip allows to read out 50 μ m pitch silicon strip detectors. Each microstrip is read out by a preamplifier-shaper and the output signal is sampled and stored in an analog pipeline. Only those events tagged by the Level 1 Trigger (TLv1) are deconvoluted by an analog signal processor and read out serially.

An output analog buffer (FIFO) placed between the processor and the multiplexer allows five different operating modes of this chip. The motivation for the FIFO is efficiency and enhanced analog testability.

Different elements of this chip were developed at LEPSI in the AMS technology [5] and then translated into the Radiation hard technology DMILL.[6]

DMILL is a 0.8 μ m technology with CMOS, P-JFET and NPN transistors and two families of resistors and capacitors. This technology provides an excellent radiation hardness[7].

The architecture of the first 128 channels prototype and the different building blocks are described in section 2. Section 3 reports on test results and features of FILTRES128.

2. ARCHITECTURE

A schematic overview of the 128 channels FILTRES is presented in Fig. 1. It consists of a low noise charge preamplifier followed by a CR-RC shaper with 75ns peaking time. The shaper output is sampled and stored in an Analogue Delay Buffer (ADB) at the Beam Crossing Over (BCO) frequency (40MHz). After the fixed trigger latency of 3.2 μ s (eg. 128 BCO of 25ns) events tagged by the TLv1 signal are transferred to the Analog Processor (AP) at a rate of 1MHz. The output of the Analog Processor is written into the FIFO at a frequency of 1MHz and read out serially by a multiplexer (MUX) with a frequency of 40MHz.

All digital inputs and outputs are in the differential ECL level standard.

The circuit FILTRES can work in five different operating modes (fig.2), to be selected by a logical word of 3 bits.

- Mode 1 : Deconvolution

In this mode three samples of the pulse are transferred to the Analog Processor and only the weighted sum is read out by the FIFO-MUX.

- Mode 2 : Peak

The peak value of the pulse shape is transferred to the FIFO and read out.

- Mode 3 : Deconvolution + Peak

Both, the result of the deconvolution and the peak value are transferred to the FIFO at an interval of 1 μ s.

- Mode 4 : Test of deconvolution

In this mode the 3 samples used in the deconvolution, the deconvolution and peak value are transferred to the FIFO at an interval of 1 μ s. This mode is devoted to test the deconvolution algorithm.

- Mode 5 : Samples

20 consecutive samples of the pulse shape are read out. This mode can be used to test and tune the peaking time and the gain of the preamplifier.

The modes 3, 4 and 5 are only possible due to the presence of the output FIFO. In fact the serial read out time needed with a multiplexer frequency of 40MHz is $3.2\mu\text{s}$ (128 channels), but the data output rate of the processor is $1\mu\text{s}$ (same as the transfer rate between ADB and AP), so we need an intermediate memory.

In the working modes 1 to 4 we store 5 samples per event, thus we have a dead time after trigger (TLv1) of 5 BCO. This dead time may be easily reduced in further versions of this chip to 3 BCO in deconvolution mode and 1 BCO in peak mode.

2.1. Preamplifier - Shaper (PR-SH)

The preamplifier topology is a single-ended folded cascode [8] to give high gain, broad bandwidth and good noise performance. The shaper is based on a CR-RC active band pass filter. Its function is to limit the bandwidth of the preamplifier and to increase the signal to noise ratio of the system.

This block is designed for a noise performance of $\text{ENC} = 410e^- + 35e^-/\text{pF}$, for a peaking time of 75ns, a gain of 75mV/MIP (Minimum Ionizing Particle of charge equivalent of 22000e⁻) and a power consumption of 1.2 mW for an preamplifier bias current of 250 μA .

2.2. Analog Delay Buffer (ADB)

The analog pipeline is the central part of the chip. It allows temporary storage of the analog signal needed by the TLv1 signal latency. The pipeline has a depth of 145 analog cells which allows a TLv1 latency of 125x25ns and the storage of 4 events with 5 samples per event. The storage cell was designed to minimize its size (50 μm x 30 μm). Each storage cell contains one write and read switch and a storage capacitor of 234fF (without reset switch). The layout of this analog storage cell has been optimized to limitate charge injection from the logic control signals.

The read and write command signals to the analog storage cells are generated by a ring counter with a skip logic.

2.3. Analog Processor (AP)

The analog processor has two internal operating modes : AP_readout and AP_processing.

First, in the AP_readout mode, the triggered ADB cells are read out by a charge sensitive amplifier (main bloc of the Analog Processor). Their data, depending on the chip working mode, are stored in the weighted capacitors of the analog processor and-or stored in the FIFO.

In the second mode (AP_processing), three weighted data are processed [9]. This mode follows the first one in the deconvolution mode.

To summarize, in the chip working mode 2 and 5 the AP operates in the AP_readout mode only, while in chip working mode 1, 3 and 4 the circuit first operates in AP_readout mode and then in AP_processing mode.

The processor architecture is based on a switched capacitors circuit. Its operating frequency is 1 MHz in order to minimize the power dissipation. A digital state machine controls the switch sequence in the different operating modes.

2.4. Output FIFO

This FIFO is based on a switched-current mode memory. The memory cells use the well-known basic current copier with performance enhanced by suppression of the static current source and

addition of other elements [10]. The FIFO is readout serially by the multiplexer controlled by an independent asynchronous clock signal.

The output FIFO is absolutely needed by the implementation of the modes 3, 4 and 5, in order to increase the testability of the chip.

In the chip working modes 1 and 2, the advantage of the FIFO is to keep the efficiency constant when the multiplexer frequency decreases. A simulation of FILTRES for a realistic sequence of TLv1 (fig 3a) gives the maximum number of FIFO cells occupied simultaneously as a function of the multiplexer frequency (fig 3b) in order to preserve full efficiency of the front end chip. Figure 6c shows the efficiency of a FILTRES chip without the FIFO as a function of multiplexer frequency. This simulation was carried out for the case of an asynchronous read out system, a mean TLv1 frequency of 100KHz, 5 samples per event and a maximum of 4 events accepted in the ADB.

This chain can be optimized easily in terms of efficiency and number of FIFO cells in the main working modes (peak and deconvolution).

2.5. Calibration-Test

In this circuit we have included internal injection capacitors (100fF) at the input of the PR_SH. This test structure allows us to inject test pulses in 32 channels selected by a multiplexer.

S3	S2	S1	S0	Channels
0	0	0	1	0,4,8,12,.....,124
0	0	1	0	1,5,9,13,... ...,125
0	1	0	0	2,6,10,14,.....,126
1	0	0	0	3,7,11,15,.....,127

For test reasons and for building blocks characterization, we have also added test pads at the output of the PR_SH and of the AP in channel 0.

3. MEASUREMENTS

3.1. Testing setup

The FILTRES128 chips are bonded on a dedicated hybrid which can be connected on a 'mother board'. This 'mother board' includes all independent power supplies (-2V and +2V for chips on hybrids, +/- 5V for external buffer CLC114 and digital ECL to CMOS translator).

The 'mother board' receives the voltage and current bias from a HP VXI bias card and the logical control signals generated by a sequencer (SEQSI VME card) or from a HP82000 digital tester for fast digital functionality test of the FILTRES chips (33 chips tested).

The analog signal is sampled by a Flash ADC (SIROCCO) and the data are transferred to the host computer. All these cards are installed together in a VXI rack driven by a HP workstation through the HPVEE software.

A design fault in the logical part of the ADB, now understood, limits the BCO frequency at about 15MHz. All measurements described here have been carried out with a BCO frequency of 12.5MHz.

The measurements presented in this paper are all from the same chip (FILTRES_Tr14_Ch31) processed in the DMILL run GLUON. This chip presents typical characteristics in terms of gain, uniformity and dynamic range.

3.2. Measurements of the building Blocks

The broken channel 0, with a test pad at the output of both the shaper and the analog processor, allows a characterization of the different building blocks of the full chain.

The pulse measured at the output of the preamplifier-shaper from -4 to +4 MIP (fig. 4) show a peaking time of 70 ns. For positive pulses, we observe a shift of the peaking time of 1ns per MIP which is due to the nonlinear feedback resistor of the preamplifier.

In a new design of this preamplifier-shaper, the shift is corrected by using a resistor serially with a tuning transistor to minimize the non-linearity of the transistor.

Figure 5 shows a good linearity of this preamplifier-shaper over a range of 8 MIP and a gain of 87mV/MIP for the nominal bias. Both the gain and the peaking time can be adjusted by tuning the bias of the PR_SH.

The gain and the dynamic range of the analog processor are measured at the analog processor output pad in channel 0 as function of the DC level at the output of the preamplifier.

The gain in readout mode (peak mode) and in deconvolution mode are respectively:

$$G_{AP_readout} = 1.8$$

$$G_{dec} = -4.0$$

A dynamic range of 1.4V at the output of the AP is obtained corresponding to a dynamic range of 8.6 MIP in peak mode and 4 MIP in deconvolution mode.

The high gain in the deconvolution mode needs different DC level for the analog processor in order to cover a dynamic range of 0 to +4 MIP for positive pulses and of -4 to 0 MIP for negative pulses with a good linearity.

The gain of the FIFO/MUX (G_{FIFO}) is measured at the output buffer of the chip loaded by a 1kOhm resistor :

$$G_{FIFO} = 0.11 \text{ (110}\mu\text{A/V in 1kOhm) for an output dynamic range of 600}\mu\text{A}$$

These measurements allow us a characterization of each building block in channel 0. From these results we can deduce the gain of the whole chain in both peak and deconvolution modes, namely.

$$G_{peak} = 87 * 1.8 * 0.11 = 17.2 \text{ mV/MIP and}$$

$$G_{dec} = 87 * -4 * 0.11 = - 38.3 \text{ mV/MIP}$$

3.3. Measurements of the 128 channel whole chain

For the test of the whole chain, all measurements were done in mode 4 (Test). This mode allows us to measure the characteristics of this chip in both peak and deconvolution modes. The 3 first samples, used in the deconvolution, have been used to verify the deconvolution algorithm implanted in this chip over all 128 channels.

All the following measurements have been performed by loading a charge signal in the analog channel using the internal injection capacitors.

The multiplexer operates at a frequency of 20 MHz and the analog data come out in consecutive channel numbered from 0 to 127.

Figure 6 shows the output streams of the analog signal from 128 channels after digitization. We need 5 consecutive streams of 128 analog data in order to read out the data from one event in the operating mode 4. Figure 6a shows the output stream without any input signal (1 ADC unit=320 μ V). It corresponds to the channel pedestal. The channel to channel spread shows a dispersion of 5mV(rms) in peak mode and 11mV(rms) in deconvolution mode. Figures 6b and 6c show the response of the chip for an input signal of 1MIP in channel 0,4,8 ... ($S_3S_2S_1S_0=0001$) respectively in peak and in deconvolution mode after channel pedestal subtraction.

The pulse shape and the deconvolution shape were measured at the output of the whole analog chain for all 128 channels. For a given input pulse we measured the sampled output value of the pulse in both deconvolution and peak mode. The same input pulse is then delayed by a time step of 5ns and another sample is measured. The whole pulse shape is reconstructed by 300 such measurements. In this test setup, only one ADB cell is used, to avoid the non-uniformity effects of the pipeline. Figure 7 shows the results of this measurements in both peak and deconvolution modes after pedestal subtraction for a 1 MIP input signal.

From these measurements we can extract the channel gain distribution in peak mode (figure 8) and in deconvolution mode (figure 9), namely:

$$G_{\text{peak}} = 18,6 \text{ mV/MIP} \quad \pm 3\% \text{ and}$$

$$G_{\text{dec-12.5MHz}} = 63.6 \text{ mV/MIP} \quad \pm 5.8\%$$

The high gain in the deconvolution mode is due to the slow working frequency (12.5 MHz). In fact the 3rd sample used in the deconvolution is a factor 1.54 higher than at 40 MHz (figure 10). The gain at 40 MHz can be estimated as :

$$G_{\text{dec-40MHz}} = 63.6 / 1.54 = 41.3 \text{ mV/MIP}$$

Figure 11 shows the linearity in the needed dynamic range of ± 3 MIP for a typical channel (channel 9) in both modes. The non-linearity in the deconvolution mode is an effect of the high gain at this working frequency.

Apart the pedestal an other source of non-uniformity of the pipeline (ADB) is the spread of the storage capacitors in the ADB. This non-uniformity can not be corrected in the FILTRES chip because the addresses of the cells triggered by the level one trigger (TLv1) are unknown. For this reason it is very important to measure the cell-to-cell variation. The measurements of the pipeline uniformity (over all the 128 x 145 cells) show an equivalent input noise of 567 e⁻ (1.5 ADC units) in peak mode (Figure 12) and 807e⁻ (4.7 ADC units) in deconvolution mode (Figure 13). This non-uniformity has to be considered as an equivalent input noise added in quadrature to the noise contribution of the analog chain with the input detector capacitance. Figure 14 gives the noise measurement of one analog channel versus the input capacitance in peak mode. This curve shows an equivalent noise charge of 805 + 66/pF e⁻. This high value of noise is mainly due to bad noise filtering efficiency of the CR-RC at this low working frequency (12.5MHz instead 40MHz) and of an excess noise added by the analog processor.

In terms of yield, 30 over 33 chip work correctly for the digital part. For the analog part 22 over 30 chips have acceptable features in terms of gain, dynamic range and pipeline uniformity.

4. CONCLUSIONS

A fully functional front end chip for the CMS tracker has been designed, manufactured and tested. The results presented here are in good agreement with the technical requirements for the CMS silicon tracker apart from the frequency limitation which is by now understood.

This 128 channel chip was implemented in the radiation hard technology DMILL with a die size of $12500 \times 6500 \mu\text{m}^2$.

Two chips have been bonded together with a 64 strip silicon detector and tested in a particle beam at CERN.

Two other chips have been tested under irradiation up to 10 Mrad and the first results are promising.

A new version of this chip has been designed including an internal bias generator and some corrections in the logical part.

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FIGURES

- Fig. 1 FILTERS Block diagram for 128 channels
- Fig. 2 Operating modes of FILTERS128
- Fig. 3 Simulation of the FIFO depth for different readout multiplexer frequencies.
- Fig. 4 Preamplifier-Shaper output.
- Fig. 5 Preamplifier-Shaper linearity
- Fig. 6 Channel pedestal (6a) - Response for 1MIP in peak mode(6b) and in deconvolution mode (6c)
- Fig. 7 Pulse and deconvolution function for the 128 channels in the whole chain.
- Fig. 8 Channel to channel gain distribution in peak mode
- Fig. 9 Channel to channel gain distribution in deconvolution mode
- Fig. 10 Pulse sampling at 12.5 MHz
- Fig. 11 Linearity and dynamic range for channel 9
- Fig. 12 Cell to cell variation in Peak mode
- Fig. 13 Pipeline uniformity in deconvolution mode
- Fig. 14 Noise performance versus input capacitance

Figure 1 : FILTRES Block diagram for 128 channels

Figure 2 : Operating modes of FILTRES128

Figure 3 : Simulation of the FIFO depth for different readout multiplexer frequencies.

Figure 4 : Preamplifier-Shaper output.

Figure 5 : Preamplifier-Shaper linearity

Figure 6 : Channel pedestal (6a) - Response for 1MIP in peak mode(6b) and in deconvolution mode (6c)

Figure 7 : Pulse and deconvolution function for the 128 channels in the whole chain.

Figure 8 : Channel to channel gain distribution in peak mode

Figure 9 : Channel to channel gain distribution in deconvolution mode

Figure 10 : Pulse sampling at 12.5 MHz

Figure 11 : Linearity and dynamic range for channel 9

Figure 12 : Cell to cell variation in Peak mode

Figure 13 : Pipeline uniformity in deconvolution mode

Figure 14 : Noise performance versus input capacitance