Fourth Workshop on Electronics for LHC Experiments

INFN - Section of Rome
University of Rome «La Sapienza»

Rome, September 21-25, 1998

Organized by INFN - Section of Rome and the University of Rome «La Sapienza» on behalf of the CERN LHCC Electronics Board
Proceedings of the

Fourth Workshop on

Electronics for LHC Experiments

Rome, September 21-25, 1998

Organised by INFN, Section of Rome and the University of Rome "La Sapienza" on behalf of the CERN LHCC Electronics Board
DISCLAIMER

In order to publish with minimum delay, the information contained in these proceedings did not undergo a peer review by the Program Committee of the Fourth workshop on Electronics for LHC Experiments. As a result, Authors of each contribution are deemed to be fully responsible for their claims and the content of their papers. Publication by the organisers of the Workshop does not imply any judgement whatsoever on the quality of the work or the actual use in experiments to take place at the Large Hadron Collider at CERN.

ADDITIONAL COPIES

Requests for additional copies should be addressed to:

Catherine Decosse, CERN, 1211 Geneva 23, Switzerland

Email: cdecosse@mail.cern.ch

COPYRIGHT

Literary and scientific copyrights reserved in all countries of the world. This report or any part of it may not be reprinted or translated without written permission of the copyright holder, the Director-General of CERN. However, permission will be freely granted for appropriate non-commercial use.
# TABLE OF CONTENTS

## ORGANISATION

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

## OVERVIEW

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
</tr>
</tbody>
</table>

## PLENARY SESSION

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
</tr>
</tbody>
</table>

- P. JARRON (CERN, Geneva, Switzerland)
  Radiation Tolerant Electronics for the LHC Experiments

- V. RADEKA (Brookhaven National Laboratory, Upton, USA)
  Shielding and Grounding in Large Detectors

- H.J. BURCKHART (CERN, Geneva, Switzerland)
  Detector Control System

- A. OAKLEY (Integrated Measurements Systems, Bracknell, UK)
  Advanced Testing Techniques for ASICs and MCMs

- P. SHARP (Rutherford Appleton Laboratory, Didcot, UK)
  The Management of the Electronics for LHC Experiments

- A. MARCI-IIORO (CERN, Geneva, Switzerland)
  Deep Submicron Technologies for HEP

- E. EISENHANDLER (Physics Department, Queen Mary and Westfield College, University of London, UK)
  Hardware Triggers at the LHC

- G. HALL (Blackett Laboratory, Imperial College, London, UK)
  CMS and ATLAS Tracker Readout Systems

- H.F. HOFFMANN (CERN, Geneva, Switzerland)
  Electronics in the ATLAS Environment

- J. HUMPHRIES (Honeywell Control Systems Ltd., Aldermaston, Berkshire, UK)
  VCSEL Components for Data Communication Links

- C. WILLMOTT (CIEMAT, Madrid, Spain)
  Electronics for Muon Detectors

## RADIATION TOLERANT ELECTRONICS

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>77</td>
</tr>
</tbody>
</table>

- M. DENTAN (CEA-DSM-DAPNIA Saclay, Gif-sur-Yvette, France)
  Final Acceptance of the DMILL Technology Stabilized at TEMIC/MHS

- W. KARPINSKI (I. Physikalisches Institut RWTH, Aachen, Germany)
  Pixel Readout Electronics in Honeywell SOI CMOS

- M. RAYMOND (Blackett Laboratory, Imperial College, London, UK)
  Radiation Tolerance Studies of Harris Test Structures

- K. GILL (CERN, Geneva, Switzerland)
  Comparative Study of Radiation Hardness of Optoelectronic Components for the CMS Tracker Optical Links

- J. SWAIN (Physics Department, Northeastern University, Boston, USA)
  Radiation Hardness of Avalanche Photodiodes Using Californium-252

- F. FACCIO (CERN, Geneva, Switzerland)
  Total Dose and Single Event Effects (SEE) in a 0.25 μm CMOS Technology

- W. SNOEYS (CERN, Geneva, Switzerland)
  Radiation Tolerance Beyond 10 Mrad for a Pixel Readout Chip in Standard Submicron CMOS

- F. FACCIO (CERN, Geneva, Switzerland)
  Estimate of the Single Event Upset (SEU) Rate in CMS

- S. WATTS (Brunel University, Uxbridge, UK)
  Status of the RD48/ROSE Collaboration
ELECTRONICS FOR TRACKERS

A. Joshi (Lawrence Berkeley National Laboratory, Berkeley, USA)
Dead-time Free Pixel Readout Architecture for ATLAS Front-End IC

L. Blanquart (IN2P3 / CPPM, Marseille, France)
MAREBO, a Full Radhard Pixel Detector Prototype for ATLAS

R. Baur (Paul-Scherrer-Institute, Villigen, Switzerland)
Front-End Electronics for the CMS Pixel Detector

D. De Venuto (Department of Material Science, Faculty of Engineering, University of Lecce, and INFN, Lecce, Italy)
Testing the Analogue Front-End of a Pixel Detector for Radiation Damages

G. Mazzia (INFN, Torino, Italy)
The Silicon Drift Detector Readout Scheme for the Inner Tracking System of the ALICE Experiment

D. Lo Presti (INFN, Catania, Italy)
Switched Capacitor Arrays Analog Memories for Sparse Data Sampling

J.-R. Lutz (Institut de Recherches Subatomiques IReS - IN2P3/CNRS - ULP, Strasbourg, France)
Electrical Characterization of ALICE128C: A Low-Power CMOS ASIC for the Readout of Silicon Strip Detectors

L. Musa (CERN, Geneva, Switzerland)
Front-End Electronics for the ALICE TPC Detector

J.-R. Lutz (Institut de Recherches Subatomiques IReS - IN2P3/CNRS - ULP, Strasbourg, France)
Detector and Front End Electronics for ALICE and STAR Silicon Strip Layers

W. Dabrowski (Faculty of Physics and Nuclear Techniques, UMM, Cracow, Poland)
The ABCD Binary Readout Chip for Silicon Strip Detectors in the ATLAS Silicon Tracker

P. Schmitt (IReS, Strasbourg, France)
Performance of a CMOS Mixed Analogue-Digital Circuit (APVD) for the Silicon Tracker in CMS

J.-P. Walder (Institut de Physique Nucléaire de Lyon, Villeurbanne, France)
Analog Signal Processing for the CMS Electromagnetic Calorimeter

P. Denes (Physics Department, Princeton University, Princeton, USA)
Digitization and Data Transmission for the CMS Electromagnetic Calorimeter

J.-P. Mendiburu (LAPP, Annecy-le-Vieux, France)
An Electronic Calibration for the Electromagnetic Calorimeter of CMS

H. Brettel (Max-Planck-Institut for Physics, Munich, Germany)
Front-End System for the ATLAS Hadronic End-Cap Calorimeter

F. Tang (Enrico Fermi Institute, University of Chicago, Chicago, USA)
Front-end Electronics for the ATLAS Tile Calorimeter

C. Bohm (University of Stockholm, Sweden)
The ATLAS Tile Calorimeter Digitizer

ELECTRONICS FOR CALORIMETERS
ELECTRONICS FOR MUON DETECTORS

M. PEGORARO (INFN, Padova, Italy)
A Prototype Frontend ASIC for the Readout of the Drift Tubes of CMS Barrel Muon Chambers

T. Y. LING (Ohio State University, Columbus, USA)
Front-End Electronics of the CMS Endcap Muon System

TRIGGER ELECTRONICS

E. PETROLO (INFN and University of Rome "La Sapienza", Rome, Italy)
Hardware Implementation of ATLAS Level-1 Muon Trigger in the Barrel Region

C. SCHWICK (CERN, Geneva, Switzerland)
The ATLAS Muon Trigger Interface (MUCTPI)

H. SAKAMOTO (Department of Physics, Kyoto University, Kyoto, Japan)
A Star Switch Readout Architecture for ATLAS Muon TGC

P. ZOTTO (INFN, Padova, Italy)
Local Track Reconstruction for the First Level Trigger in the CMS Muon Barrel Chambers

F. ODORICI (INFN, Bologna, Italy)
Pattern Unit for High Throughput Device Testing

A. MONTANARI (INFN, Bologna, Italy)
Track Segment Sorting in the Trigger Server of a Barrel Muon Station in CMS

G. WROCHNA (CERN, Geneva, Switzerland)
Synchronization of the CMS Muon Detector

T. TOIFL (CERN, Geneva, Switzerland)
A Radiation-Hard 80 MHz Clock and Data Recovery Circuit for LHC

R. VARI (INFN, Roma, Italy)
A 4-Channels Rad-Hard Delay Generator ASIC with 1 ns Minimum Time Step for LHC Experiments

U. PFEIFFER (Institut für Hochenergiephysik, Universität Heidelberg, Germany)
ATLAS Level-1 Calorimeter Trigger System Architecture

V.J. PERERA (Rutherford Appleton Laboratory, Didcot, UK)
The e/y and τ/hadron Processor System for the ATLAS First-Level Trigger

W.H. SMITH (Physics Department, University of Wisconsin, Madison, USA)
CMS Calorimeter Trigger Receiver System

A. MASS (H.H. Wills Physics Laboratory, Bristol University, Bristol, UK)
The Global Calorimeter Trigger for CMS

V. LENTI (Physics Department, University of Bari and INFN, Bari, Italy)
The NA57 Trigger Processor

OPTOELECTRONICS AND DATA TRANSFER SYSTEMS

M.G. BISOGNI (University of Pisa and INFN, Pisa, Italy)
Optically Activated GaAs Devices for MSGC Cathode Strip High-Voltage Control in the CMS Tracker

F. VASEY (CERN, Geneva, Switzerland)
A 4-Channel Parallel Analogue Optical Link for the CMS Tracker

A.R. WEIDBERG (Oxford University, UK)
Development of Radiation-hard VCSEL/PIN-diode Optical Links for the ATLAS SCT

A. RUDGE (CERN, Geneva, Switzerland)
Tests of Prototype ATLAS SCT Data Links

J.A. WILSON (University of Birmingham, Birmingham, UK)
Radiation Tests of Optical Link Components for the ATLAS SCT
M. Pearce (Royal Institute of Technology (KTH), Physics Department Frescati, Stockholm, Sweden)
Development of Radiation Tolerant Gb/s Optical Links for the Front-end Readout of the ATLAS Liquid Argon Calorimeter .................................................. 364
G. Rubin (CERN, Geneva, Switzerland)
The ALICE Detector Data Link Project .................................................. 369
E. van der Bij (CERN, Geneva, Switzerland)
S-LINK: a Prototype of the ATLAS Read-out Link .......................... 375

DAQ .............................................................................................................. 381

A.J. Lanford (Department of Physics and Astronomy, University of California, Irvine, USA)
Architecture of the BABAR Electronics System .................................. 383
M. Niculescu (CERN, Geneva, Switzerland)
The COTS Approach to the Read-Out Crate in ATLAS DAQ Prototype -1 ................................................................. 387
P. Lichard (CERN, Geneva, Switzerland)
Backend VME Module for ATLAS TRT Read-Out System .................... 393
R. Cranfield (University College, London, UK)
Prototyping Hardware for the ATLAS Readout Buffers ........................ 397
A. Kugel (University of Mannheim, Mannheim, Germany)
MicroEnable A Reconfigurable FPGA Coprocessor .................................. 402
M. Dell’Orso (Physics Department, Pisa, Italy)
A Real-Time Tracker for Hadronic Collider Experiments........................... 407

Detector Control Systems ........................................................................... 413

P. Farthouat (CERN, Geneva, Switzerland)
Timing Set-Up Strategy for the ATLAS Experiment ............................... 415
R. Fantechi (INFN, Pisa, Italy)
The Slow Control System for the NA48 Experiment ................................ 419
B. Hallgren (CERN, Geneva, Switzerland)
Frontend I/O via CANbus of the ATLAS Detector Control System ............. 423

Power Supplies .......................................................................................... 429

S. Leonardi (ST-Microelectronics, Catania, Italy)
RHBip1 Technology Evaluation to Total Dose, Low Dose Rate and Neutrons, for LHC Experiments and Space Applications .......................................................... 431
M. Mélotte (Société de Microélectronique, Charleroi, Belgium)
A Rad Hard PWM Integrated Circuit for Power Supplies Control ............... 435
G.M. Grieco (CAEN SpA, Viareggio, Italy)
CAEN SY1527: a New LHC Dedicated HV Power Supply System .............. 439
M.C. Spitalieri (Laboratori Nazionali di Frascati dell’INFN, Frascati, Italy)
ATLAS MDT High Voltage Generation and Distribution ............................. 440

Posters ........................................................................................................... 445

V. Popov (Institute for Theoretical and Experimental Physics, Moscow, Russia)
Readout and Pretrigger Logic of the HERA-B High-pT Pretrigger .................. 447
Y. Hu (LEPSI - IN2P3/ULP, Strasbourg, France)
Design of a High Performance, Low Noise Charge Preamplifier with DC Coupling to Particle Silicon Detectors in CMOS Technology .......................................................... 452
J.-F. Genat (LPNHE, Universités Paris VI et VII, Palaiseau, France)
A 16-channel Digital TDC Chip with Internal Buffering and Selective Readout .......................................................... 456
V.V. Sushkov (University of California, Riverside, USA)
Differential Non-Linearity Compensation in ADC of Binary Weighted Capacitances Array Type .................................. 463
D. DE PEDIS (INFN, Rome, Italy)
TASS, An Interactive Graphical Tool for DAQ and Trigger Design ........................................... 468

B. DINKESPILER (CPPM, Marseille, France)
A Multichannel Gb/s Bit Error Rate Tester for the Evaluation of Front End Optical Read-out Link Solutions of the ATLAS Liquid Argon Calorimeter .................................................................................. 470

A.S. ARTAMONOV (Specialized Electronic Systems, Moscow, Russia)
Laser Technique of Single Event Latchup Threshold Estimation .................................................... 471

A.I. CHUMAKOV (Specialized Electronic Systems, Moscow, Russia)
Correlation of Ion- and Proton-Induced Single Event Upsets .......................................................... 476

A.Y. NIKIFOROV (Specialized Electronic Systems, Moscow, Russia)
Radiation Response of Hall Sensor Based on SOI Double Gate Field Effect Resistor ....................... 480

O.A. KALASHNIKOV (Specialized Electronic Systems, Moscow, Russia)
CMOS Integrated Circuits Total Dose Functional Upset Sensitivity to Operation Mode .................. 484

P.K. SKOROBOGATOV (Specialized Electronic Systems, Moscow, Russia)
A Way to Improve the Efficiency of Laser Simulation Tests Adopted to SOI/SOS Devices .................. 486

Z. MEGGYESI (CERN, Geneva, Switzerland)
Developing a Gigabit S-LINK Card .................................................................................................. 489

C. POSCH (CERN, Geneva, Switzerland)
A Mixed Signal Data Receiver/Clock Synchronizer ASIC for Analog Front End Chips in LHC Experiments 494

A. RIVETTI (Politecnico and INFN, Torino, Italy)
Two 2-Stage Transimpedance Amplifiers for Silicon Drift Detectors Readout .................................. 499

T. KISS (Technical University BME MHT, Budapest, Hungary)
Development of Media Interfaces for Gbit/s fibre-optic Links .......................................................... 503

E. DÉNES (KFKI Research Institut for Particle Physics, Budapest, Hungary)
Test of ALICE DLL: Test Setups and Test of ALICE DLL Integration to Alice TPC Test System ............ 508

S. BOUVIER (Laboratoire de Physique Subatomique et des Technologies Associées, Nantes, France)
TAB: A Packaging Technology Used for Silicon Strip Detector to Front End Electronics Interconnection 511

G. MAGAZZU (INFN, Pisa, Italy)
A Standard Cell Based Content-Addressable Memory System for Pattern Recognition .................. 514

D. CROSETTO (3D-Computing Inc., DeSoto, USA)
Fast Particles Identification in Programmable Form at Level-0 Trigger by Means of the 3D-Flow System 517

J. SWAIN (Department of Physics, Northeastern University, Boston, USA)
Novel Electronic Sensors at CMS ...................................................................................................... 523

H. ZIMMERMANN (Fermi National Accelerator Laboratory, Batavia, USA)
High Readout Speed Pixel Chip Development at Fermilab ............................................................... 528

R. SHARMAN (UTMC Microelectronic Systems, Colorado Springs, USA)
Semi-Custom Gate Arrays and Standard Product Suitable for Use in Radiation Environments up to 10Mrad(Si) 533

U. TRUNK (Max-Planck-Institut für Kernphysik, Heidelberg, Germany)
The Helix128 Readout Chip Family for Silicon Microstrip Detectors and Microstrip Gaseous Chambers 538

G. BOUCHARLAT (Thomson-CSF Semiconducteurs Spécifiques, St-Egrève, France)
High Performance Image Sensors ....................................................................................................... 543

A.I. GOLDSHER (State Scientific Research Institute "Pulsar", Moscow, Russia)
Components of Fast Analog Integrated Micocircuits for Front-End Electronic Systems .................. 545

E. ATKIN (Department of Electronics, Moscow Engineering Physics Institute, Moscow, Russia)
Discriminator ICs for Tracking and Time-Of-Flight Detectors ......................................................... 550

Yu. VOLKOV (Department of Electronics, Moscow Engineering Physics Institute, Moscow, Russia)
16 Channel Printed Circuit Units for Processing Signals of Multiwire Chambers. A Functionally Oriented Semicustom Array .............................................................................................................. 555

H. GEMMEKE (Forschungszentrum Karlsruhe, Karlsruhe, Germany)
A Fast and Simple Trigger for High Energy Cosmics ....................................................................... 560
H. FISCHER (Universität Freiburg, Fakultät für Physik, Freiburg, Germany)
TDC Chip and Readout Driver Developments for COMPASS and LHC-Experiments 564

J. KAPLON (CERN, Geneva, Switzerland)
DMILL Implementation of the Analogue Readout Architecture for Position Sensitive Detectors at LHC Experiments 569

K. KLOUKINAS (CERN, Geneva, Switzerland)
Development of a Radiation Tolerant 2.0 V Standard Cell Library Using a Commercial Deep Submicron CMOS Technology for the LHC Experiments 574

M. SAMPIETRO (Politecnico, Dipartimento di Elettronica, Milano, Italy)
Low Power BiCMOS Charge Amplifier with Current Conveyor Feedbacks 581

R. MARIANI (CAEN Microelettronica, Viareggio, Italy)
MCM Production: Testing and Related Aspects 584

B. EGED (Technical University BME MHT, Budapest, Hungary)
Signal-Integrity Measurements on VME320 Backplane 589

P. NUGENT (ITALTEL SpA, Castelletto di Settimo Milanese, Italy)
Four Channel Fibre Optic Transmitter and Receiver Modules for CMS Detector Tracker Readout Links 594

A. MEKKAOUI (Fermi National Accelerator Laboratory, Batavia, USA)
Results from an FPIX0 Chip Bump-Bonded to an ATLAS Pixel Detector 599

E. DURIEZ (Dassault Electronique, Saint-Cloud, France)
Key Industrial Technologies for ALICE TPC Detectors and other Detector Applications 602

B. WIKSTROM (Xicon AB, Malmö, Sweden)
Production Technologies for High Performance Electronics 604

B. JUNNO (EtchTech Sweden AB, Malmö, Sweden)
Field Activated Anisotropic Wet Chemical Etching and its Applications 604

N. RANDAZZO (Department of Physics, University & INFN, Catania, Italy)
CMOS and BiCMOS Transimpedance Preamplifiers for Silicon Drift Detectors Read-Out 606

C. PETTA (Department of Physics, University & INFN, Catania, Italy)
Simulation and Characterization of the Front-End of SDD in ALICE ITS 610

F. GIANNINI (Department of Electronic Engineering, University of Rome "Tor Vergata", Rome, Italy)
Front-end Electronics for Particle Detection and Data Communication 615

LIST OF PARTICIPANTS 621

INDEX 629
ORGANISATION

The fourth in this series of workshops on Electronics for LHC Experiments, was organised for the CERN LHCC Electronics Board by INFN section of Rome.

The Workshop was held on September 21-25, 1998 in the Physics Department "G. Marconi" of the University of Rome "La Sapienza".

Local Organisation Committee
Bruno Borgia University of Rome
Speranza Falciano INFN Rome
Lamberto Luminari INFN Rome
Franco Meddi University of Rome
Emilio Petrolo INFN Rome
Riccardo Vari INFN Rome
Stefano Veneziano INFN Rome
Lucia Zanello University of Rome

Workshop Secretariat
Veronica Buccheri INFN Rome
Anna De Grossi University of Rome
Catherine Decosse CERN
Gigliola Gori INFN Rome
Anne Johnson Rutherford Appleton Laboratory
Bruno Pellizzoni INFN Rome

Proceedings Organizer
Catherine Decosse CERN

The Program Review Committee was comprised of the members of the LEB, namely:

Pierre Borgeaud Saclay
Francesco Corsi Politecnico di Bari
Hans Dijkstra CERN
Philippe Farthouat CERN
Fabio Formenti CERN
Geoff Hall Imperial College
Michael Letheren CERN
Emilio Petrolo INFN Rome
Steve Quinton Rutherford Appleton Laboratory
Veljko Radeka Brookhaven
Peter Sharp Rutherford Appleton Laboratory
Wesley Smith University of Wisconsin
Giorgio Stefanini CERN
Ulrich Straumann Heidelberg
Michal Turala CERN
OVERVIEW

The theme of the workshop was to identify areas and encourage common efforts for development of electronics within and between the different LHC experiments, and to promote cross-fertilisation in the engineering and physics communities involved in the LHC activities, with particular emphasis to the system design issues.

The programme consisted of both plenary talks and parallel working groups.

The welcome address was given by Peter Sharp, Chairman of the CERN LHCC Electronics Board, and by Francesco Guerra, Director of the Department of Physics of Rome University, Maurizio Lusignoli, Director of INFN Section of Rome, and Emilio Petrolo, chief of the Local Organisation.

PLENARY SESSION
Chairman: P. Sharp

Invited speakers:
P. Jarron, CERN Radiation tolerant electronics for the LHC experiments
V. Radeka, BNL Shielding and grounding in large detectors
H. Burckhart, CERN Detector control system
A. Oakley, IMS Advanced testing techniques for ASICs and MCMs
P. Sharp, RAL Managing large LHC projects

RADIATION TOLERANT ELECTRONICS & TRIGGER ELECTRONICS
Chairman: S. Quinton

Invited Speakers:
A. Marchioro, CERN Deep submicron technologies for HEP
E. Eisenhandler, QMW London Hardware Triggers at the LHC

ELECTRONICS FOR TRACKERS & ELECTRONICS FOR CALORIMETERS
Chairman: M. Turala

Invited Speakers:
P. Denes, Princeton Calorimeters readout at the LHC
G. Hall, Imperial College CMS and ATLAS tracker readout systems

ELECTRONICS FOR MUON DETECTORS & OPTOELECTRONICS AND DATA TRANSFER SYSTEMS Chairman: P. Farthouat

Invited Speakers:
H. Hoffmann, CERN Electronics in the ATLAS environment
J. Humphries, Honeywell VCSEL components for data communication links
C. Willmott, CIEMAT Electronics for muon detectors
The two parallel working groups focused on the system design issues involved in the electronics for:

**WORKING GROUP A:**

RADIATION TOLERANT ELECTRONICS, Chairmen: V. Radeka & G. Hall  
ELECTRONICS FOR TRACKERS, Chairmen: F. Corsi & P. Borgeaud  
ELECTRONICS FOR CALORIMETERS & MUON DETECTOR, Chairman: F. Formenti

PANEL DISCUSSION chaired by P.F. Manfredi

**WORKING GROUP B:**

TRIGGER ELECTRONICS, Chairmen: W. Smith & E. Petrolo  
OPTOELECTRONICS AND DATA TRANSFER SYSTEMS, Chairman: M. Letheren  
DAQ, Chairman: L. Mapelli  
DETECTOR CONTROL SYSTEMS AND POWER SUPPLIES, Chairman: A.J. Lankford

PANEL DISCUSSION chaired by P. Sphicas

**POSTERS**

The poster session was chaired by Steve Quinton.

**INDUSTRIAL EXHIBITION**

Companies attending were:

- CAEN SpA  
- Dassault Electronique

**NEXT WORKSHOP**

The Fifth Workshop on Electronics for LHC experiments is expected to take place in the United States, in September 1999.

Further information will be made available in due course on the World Wide Web.
PLENARY SESSION
Radiation tolerant electronics for the LHC experiments
P. Jarron
CERN 1211 Geneva 23 Switzerland

ABSTRACT
The harsh radiation environment at the LHC poses formidable challenges to the design, fabrication and test procedures that must be applied in the development of ASICs embedded in the detectors. The use of Commercial-Off-The-Shelf (COTS) components in the LHC environment also requires a careful evaluation of the impact of radiation-induced effects on their performance and reliability. This review paper discusses the issues of Total Dose effects (TID), displacement damage and Single Event Effects (SEE) expected in the LHC environment, and discusses the relevance for LHC experiments of the experience gained by the Space community in this field.

1 INTRODUCTION
For several years, HEP community has studied and selected radiation hard technologies suitable for the development of mixed signal ASICs for the readout electronics of LHC experiments [1,2,3]. In the meantime, vendors of radiation hardened technologies have faced a considerable shrinkage of the Defence market, and the Space community has focused its interest more on the use of Commercial-Off-The-Shelf (COTS) components rather than in highly expensive and less advanced Hi-Rel electronics components traditionally used in the past.

The consequence of this situation is that several semiconductor companies have abandoned the radiation hard electronics market, and presently only very few companies in the world propose radiation hard technology suitable for LHC front end electronics ASICs.

It has also been realised that the design and qualification of radiation hard mixed-signal ASICs for the LHC readout electronics systems poses formidable technical challenges. Traditionally, radiation hard electronics chips in CMOS technologies have been mostly developed for digital circuits applications, and consequently almost no existing experience concerning mixed signal ASICs was available for the HEP community. However, thanks to considerable R&D efforts carried through the HEP community, complex and sophisticated radiation hard mixed signal ASICs for LHC experiments have now reached a sufficient stage of maturity to be ready soon for volume production [4, 5, 6, 7, 8].

However, several factors such as the uncertainty about the long term survival of radiation hard technologies, the need for low-power high-speed digital circuits (e.g. gigabit link) and extremely dense ASICs (e.g. pixel readout chip), have spurred the development of an alternative approach based on radiation tolerant design techniques in deep sub micron CMOS technology [9].

The rapid and continuing scaling of microelectronics technology has an impact on the radiation-induced effects. As feature size and voltage levels decrease some radiation effects are considerably reduced (total dose effects), whereas Single Event Effects (SEE) becomes more a problem. Papers presented in LEB conference last year [10] and in this conference [11,12,13,14] confirm the tremendous potential of this approach, and propose design solutions in deep sub micron technology for minimising the risk of Single Event Upset (SEU) [11].

Radiation tolerant and radiation hard custom ASICs are not the only components to be used in LHC experiments. Large volumes of COTS components like power devices, SRAM memories, microprocessors, FPGA’s, will be placed in the LHC radiation environment. It is beyond available resources to make a custom radiation tolerant redesign of all the COTS components envisaged for the use in the LHC experiments. However, there are few exceptions such as the development of a radiation tolerant voltage regulator presented in this conference [16]. In this case, there is no available COTS components with sufficient neutron and total dose hardness, and such a component has a potential commercial viability in the market because of its wide application range.

In most cases, selection and qualification of COTS components will remain for LHC teams the only approach for standard electronics of detectors, control and power systems. In addition to total dose effects and single event upset, the risk associated with Single Event Latch-up (SEL) has to be seriously considered and assessed for the LHC environment. SEL affects potentially all COTS components fabricated in CMOS processes, and its effects could threaten the overall system reliability. SEL also raises safety issues in the case where electronic boards are not properly monitored and
protected against the large supply currents that can be induced by latch-up.
The Space community has intensively studied the SEE issue on COTS for more than 2 decades, and the LHC community should profit from this experience and use available space radiation data.

2 LHC-SPACE RADIATION ENVIRONMENT
Space radiation data on electronic components is available through several channels, such as databases from Space and Defence agencies, and companies. However, before applying Space radiation data for LHC purposes, it is necessary to assess the equivalence between the Space and LHC radiation environments. There are similarities and differences between these 2 environments. Protons and charged particles trapped in the Earth’s radiation belts constitute a radiation environment quite similar to that expected at the LHC, whereas the presence of heavy ions and the absence of neutrons in space are the main differences with the LHC.

Trapped protons with energies above 50 MeV have similar TID and single event effects as those caused by high energy particles encountered in LHC detectors. Peak proton fluence levels observed in radiation belts at an altitude of 2500 km is about $5.10^9$ proton/cm$^2$ daily[17], which is in the range of a few $10^{12}$ proton/cm$^2$ for 10 years LHC operation (operation time=510’s).

Therefore, all SEE radiation data collected on COTS [17,18] in this Space region, where radiation effects of high-energy protons dominate, are applicable to LHC experiments. However, one should note that the pion interaction cross section with silicon is higher than for high energy protons, in particular around the 250 MeV delta resonance[19]. Therefore, existing space radiation data on COTS taken with protons should be re-normalised in the case of pions.

Neutrons are predominant in the LHC calorimeter regions [20], muon detectors and caverns, whereas the neutrons fluence is almost inexistent in radiation belts and in cosmic rays. Atmospheric neutrons observed at an altitude of 15 km have peak fluence less than 1 neutron/cm$^2$/s, and have been recognised as a potential source of SEU for avionics [21]. This level is 6 orders of magnitude smaller than the LHC cavern levels, and no systematic study of displacement and single event effects induced by neutrons on COTS is available. Therefore, the LHC community has unfortunately no neutron database on COTS components at its disposal from the Space community, and should therefore perform COTS qualification with neutrons in most cases.

3. RADIATION EFFECTS
Radiation impacts integrated circuits in two different ways:

- Aging effects, which create a drift of the electrical characteristic of devices, which results in gradual degradation of the electrical characteristics of an integrated circuit in proportion to the total dose or fluence.
- Single Event Effects (SEE), which can upset logical states (SEU) or abruptly degrade ICs such as Single Event Latch-up (SEL). SEE effects are random with a rate of occurrence depending on the vulnerability and the number of electronics components in the full system under radiation.

The risks associated with SEE are considered by the Space community to be severe and the most difficult to assess. SEE risk will be an issue from the very beginning of the LHC operation. This is not the case for total dose effects and displacement damage risks, which depend on the total elapsed operation time, and will only affect components at a later stage.

3.1 Total dose effects
TID effects have been studied since a long time, and considerable experience is now available. The 2 main TID effects which directly affect the reliability of CMOS integrated circuits placed in a radiation environment are the threshold voltage shift of the NMOS and PMOS transistors, and the leakage current of NMOS transistors. Carrier mobility, noise and weak inversion slope of PMOS and NMOS transistors are also degraded, leading to a loss of performance of analog circuits.

It should be noted that the magnitude of all total dose effects is strongly dependent on the technology considered. In general, old CMOS and power technologies with thick gate oxide are extremely vulnerable and exhibit large threshold voltage shifts.

Total dose effects also affect bipolar technology. A parasitic base leakage current occurs after irradiation due to the increase of surface recombination in the base-emitter depletion region, leading to a decrease of the transistor’s bipolar gain Hfe. A low dose-rate enhancement effect has also been observed [22] which affects especially COTS integrated in bipolar technologies containing circuits operating at low bias current or employing lateral pnp devices.

3.2 Displacement damage
Displacement damage is caused by interactions of neutrons, protons and pions with silicon.
Displacement damage affects electronics components based on bipolar technology by decreasing minority carrier lifetime of the base region consequently decreasing the current gain $\alpha_{fe}$. For this reason, CMOS integrated circuits are not vulnerable to displacement damage, since the MOS transistor operation is based on the charge transport of majority carriers.

3.2.1 neutrons
Displacement damage can be described in terms of Non Ionising Energy Loss (NIEL) [23], as is done to quantify radiation damage to silicon detectors. The displacement damage due to low energy neutrons is difficult to estimate because its cross-section in silicon drops considerably below 1 MeV, and usually neutrons with energies below 100 KeV are not accounted in the displacement damage calculation. For electronics, a standard hardness test procedure has already established since 10 years by the Defence community [24]. These qualification protocols include:

1. Determination of the neutron energy spectrum in the environment where it is placed electronics.
2. Calculation of the 1 MeV equivalent fluence using Kerma factors. The displacement Kerma factor is a response function of the energy deposition which normalises at 1 MeV equivalent the displacement damage caused by the entire neutron energy spectrum of the environment.

So far, the LHC community has not studied the effect of thermal neutrons on electronics. Damage effects on bipolar transistors have been reported [25], and explained by the reaction with boron, $^7$Li ($n$, $a$) $^4$Li. $^10$B is a contaminant of the natural boron dopant in silicon chips. Thermal neutrons have also been recently considered as a cause of SEU for SRAM [26], provoked by the same reaction. Further study should be done to confirm these risks of bulk damage and SEU in LHC electronics.

3.2.2 protons
From the point of view of device operation, the nature of the displacement damage produced by neutrons and high energy protons is essentially the same, except that total dose effects should be taken into account. However, it should be noted that low energy protons (5 MeV) cause 8.5 times more damage to bipolar devices than do neutrons, whereas high energy protons of 60 MeV are only about 1.8 times more damaging[27].

3.2.3 pions
No existing experimental data concerning the pion displacement damage factor for bipolar technology is available. However, the NIEL factor of pions obtained for silicon detectors should be a good reference for a preliminary estimate [24].

3.3 Single Event Effects
There are 2 important types of SEE which are matter of concern in the LHC environment. One type causes an error by upsetting a logical state in memories and digital circuits, it is SEU. The other type provokes a permanent hardware failure, such as Single Event Latch-up (SEL), Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB).

SEE are provoked by a single particle strike in silicon. There are two sources of SEE which are of important concern for IC performance. The first one, which is not relevant in LHC experiments, is due to direct ionisation by heavy ions striking silicon. The second one is due to the nuclear inelastic interaction of a neutron, proton or pion with a silicon nucleus of electronics chips, and this will be the main source of SEE at LHC [15].

At high energy, above about 50 MeV, neutron-nucleus reactions and proton-nucleus reactions are very similar [19]. The ionising secondary fragments produced by nuclear spallation provoke a SEE when the total energy they deposit in a sensitive node of a circuit is above a certain critical threshold. Several secondary fragments are produced: neutrons, protons, alpha particle and recoil nucleus. Usually, the charge should be deposited in the sensitive volume of 1 or 2 $\mu$m cubic in the order to trigger a SEE [15]. For such a short distance, the charge contribution of heavy ionising recoils is predominant.

For latch-up (SEL), layout and design rules play a major role in hardening ASICs. The application of radiation tolerant layout practices [11] considerably minimises the risk of latching up the parasitic p-n-p-n.

4. IMPACT OF TECHNOLOGY SCALING
Over the last two decades, a tremendous device scaling has been applied to commercial CMOS processes, and today technology is commercially available with a feature size of 0.25 $\mu$m. It is possible to identify areas relating to scaling that are expected to have the largest influence on the radiation tolerance of highly scaled technology. These are discussed in the following subsections.

4.1 Gate voltage threshold shift
For technologies above ~ 1 $\mu$m, the threshold shift which results from hole trapping in MOS gate oxides decreases as the square of the oxide thickness [28]. The 1970's CMOS technology exhibited more than -1 Volt of shift after 10 krad, whereas 0.5$\mu$m technology exhibits a shift of less than -150 mV after 300 krad. Figure 1 shows experimental radiation test results obtained by
RD49 [10] for 6 different processes ranging from feature size of 0.5μm to 0.25 μm.

Threshold voltage shift scales faster than the square of the oxide thickness in submicron processes, as has previously been shown on thin MOS oxide [29]. Figure 2 shows the calculated annealing effect induced by electron tunnelling for 3 different gate oxide, 12nm, 9nm and 6nm used in the 0.5, 0.35 and 0.25 μm CMOS processes tested.

For oxide thicknesses in the range of the tunnelling wavelength, electrons tunnelling from gate electrode and silicon to gate quickly neutralise trapped holes. In addition, trapped holes in gate oxide can also tunnel out of the thin oxide.

For 6nm gate oxide or thinner the annealing mechanism becomes sufficiently fast to be effective and to totally neutralise trapped holes.

It turns out that this tunnelling mechanism starts to be fully effective for the quarter micron technology generation. Two quarter micron technologies have been tested to total dose, and results show the same gate oxide hardness [10, 11].

4.2 Subthreshold characteristic
The increase of the slope of the subthreshold characteristic of the MOS transistor after radiation is due to the increase of interface states density Dit. N. Saks has shown [30] that radiation-induced Dit in thin oxide (tox<12 nm) is much smaller than would be predicted based on results from thick oxides. Measurement of subthreshold characteristic of 0.25 μm NMOS and PMOS transistors irradiated up to 10 Mrad [10] confirms this prediction. An increase of a few mV/dec of the subthreshold slope after 30 Mrad has been observed [11].

Since interface state density determines electrical surface properties, the stability of the subthreshold characteristic is a strong indication that carrier mobility and noise of 0.25 μm MOS devices are not significantly affected by radiation. Results presented in this conference [11, 14] fully confirm this expectation. The 1/f noise and white noise measurements of 0.25μm PMOS and NMOS devices do not change significantly to doses of 30 Mrad, and mobility decrease is less than 5%.

4.3 NMOS parasitic leakage current
Compact device isolation between transistors in 0.25μm technology and below is achieved by Shallow Trench Isolation STI [12].

Threshold voltage shift scales faster than the square of the oxide thickness in submicron processes, as has previously been shown on thin MOS oxide [29]. Figure 2 shows the calculated annealing effect induced by electron tunnelling for 3 different gate oxide, 12nm, 9nm and 6nm used in the 0.5, 0.35 and 0.25 μm CMOS processes tested.

For oxide thicknesses in the range of the tunnelling wavelength, electrons tunnelling from gate electrode and silicon to gate quickly neutralise trapped holes. In addition, trapped holes in gate oxide can also tunnel out of the thin oxide.

For 6nm gate oxide or thinner the annealing mechanism becomes sufficiently fast to be effective and to totally neutralise trapped holes.

It turns out that this tunnelling mechanism starts to be fully effective for the quarter micron technology generation. Two quarter micron technologies have been tested to total dose, and results show the same gate oxide hardness [10, 11].

4.2 Subthreshold characteristic
The increase of the slope of the subthreshold characteristic of the MOS transistor after radiation is due to the increase of interface states density Dit. N. Saks has shown [30] that radiation-induced Dit in thin oxide (tox<12 nm) is much smaller than would be predicted based on results from thick oxides. Measurement of subthreshold characteristic of 0.25 μm NMOS and PMOS transistors irradiated up to 10 Mrad [10] confirms this prediction. An increase of a few mV/dec of the subthreshold slope after 30 Mrad has been observed [11].

Since interface state density determines electrical surface properties, the stability of the subthreshold characteristic is a strong indication that carrier mobility and noise of 0.25 μm MOS devices are not significantly affected by radiation. Results presented in this conference [11, 14] fully confirm this expectation. The 1/f noise and white noise measurements of 0.25μm PMOS and NMOS devices do not change significantly to doses of 30 Mrad, and mobility decrease is less than 5%.

4.3 NMOS parasitic leakage current
Compact device isolation between transistors in 0.25μm technology and below is achieved by Shallow Trench Isolation STI [12].
Soft thick field oxides, which are not employed in commercial-grade technology, are still an issue because of charge trapping. Measurement of the parasitic leakage current after radiation is shown in figure 3 for 6 different submicron technologies [10].

NMOS transistors from two quarter micron technologies show different behaviour. A more recent measurement on technology B [11] indicates a much better hardness of the field oxide.

The use of radiation tolerant design practices for ASIC design with enclosed NMOS geometry prevents post radiation parasitic leakage independently of technology changes and technology vendors. The development of a radiation tolerant standard cell library in quarter micron technology [13] is presented in this conference, and shows that the device density obtained is compatible with the requirements of ASICs for LHC experiments.

4.4 SEU vulnerability

It is believed that device scaling increases the SEE vulnerability. This idea is based on the assumption that node capacitance of integrated circuits decreases accordingly to scaling, and thus the critical charge. However, factors related to circuit design techniques can considerably influence SEU vulnerability. As an example, a comparison based on the threshold LET for several commercial microprocessors [31] suggests that there is little difference between a 1986 Z-80 (3um process) and a 1997 Pentium (0.35um process). Both microprocessors have a threshold LET in the range of 1 to 3 MeV cm²/mg.

For ASICs, special techniques for the design of digital circuit circumvent radiation-induced SEU. Recently, results obtained with SEU hardened circuits in quarter micron technology, are very promising [15].

4.5 SEL vulnerability

Layout and design rules play a major role in the latch-up vulnerability of ICs. For ASICs, the application of radiation tolerant layout practices[15] considerably minimises the risk of latch-up at a negligible level. For COTS components, results from the Space community show huge variations of latch-up vulnerability. Device scaling has generally a positive impact on the latch-up hardness of devices. Shallow Trench Isolation used in the 0.25um technology generation improves isolation between devices, and minimises the effect of the lateral parasitic p-n-p-n structure. Advanced CMOS technologies use a shallow epitaxial low resistivity substrate [32]. However, a counter example is provided by the K5 AMD processor [33] that exhibits an extremely small threshold LET of 0.4 MeV cm²/mg. This case shows that though scaling trends are favourable, a careful latch-up assessment of COTS is mandatory, and a blind use of non-qualified COTS is too risky.

4.6 SEGR vulnerability

Among all COTS components vulnerable to gate rupture, DRAM and FPGA are those with the highest susceptibility [34]. FPGA will be a COTS component widely used at LHC and its vulnerability to SEGR remains a potential issue [35].

For ASICs fabricated in 0.25um technology, recent results show that it is difficult to establish definite trends of the SEGR issue with device scaling. However, the risk of gate rupture in advanced technologies seems to be less important than previously expected [36].

5.COTS SELECTION AND QUALIFICATION

Electronics of LHC experiments will use a considerable volume of COTS components, and therefore selection and qualification of their radiation hardness is an issue. With the limited resources and development time available within the LHC community, the most effective approach to COTS would be standardisation among all experiments. Unfortunately, this is not easy because the LHC community has not the experience and the organisational structure of the Space community.

The evaluation of the radiation tolerance of electronics can be done at different levels, technology, component and system level. Several LHC teams have already started radiation tests at these 3 different levels. In the following subsections we discuss these different approaches for assessing COTS components for LHC.

5.1 Technology testing.

Whenever a COTS component for a given function is not available, the development of a custom component is one possible solution. The technology is tested to radiation at elementary device level, and based on the knowledge gained, a custom component is designed and fabricated using radiation tolerant practices. This approach is very effective in term of radiation assurance, but necessarily limited to few key electronic components because of the resources needed.

5.2 COTS selection using databases

COTS components can be selected from existing radiation databases. It is usually the first step in selecting devices for Space systems, and this approach is applicable to LHC as well. This is the best cost-effective solution, but one must be aware of pitfalls and limitations. Several radiation databases contain obsolete information, e.g.
components are not available any more, or dates of the radiation test are older than 2 or 3 years making the data irrelevant for the currently available version of the components. Radiation test can be also incomplete, this is especially the case for most linear bipolar components which were not tested at low dose rate. Usually, the main problem encountered by users is the absence of available radiation data for the most recent COTS components, which are usually those most sought after because they are the most advanced.

A fundamental limitation of the radiation databases for LHC users is the lack of neutron radiation data, which are generally kept partly confidential by Defence Agencies, and are usually missing in Space database.

5.3. COTS testing
Radiation testing is very often the only possible solution for most of the recent COTS components, and for the qualification of COTS with uncertain radiation data. After the qualification, COTS for Space applications are usually procured in a single buy of the tested batches in order to guarantee radiation assurance. The LHC community has not yet clarified its COTS purchasing procedure.

5.4 System level testing
Radiation testing of electronic systems would be seen to be by far the more attractive approach for LHC users. In one single test, a full electronic system such as a power supply, a CAN Bus, a VME module can be tested. Unfortunately, this approach is risky because of the lack of traceability of COTS components inside the system.

The traceability is an issue at two levels. First, manufacturers of electronic equipment do not care about the origin of components. Very large variations of radiation hardness have been observed by the Space community [37] for a given COTS components provided in different batches of at the same semiconductor foundry. Large differences are also observed for the same component produced in different semiconductor foundries, Second, in order to be sure of a latch-up free system one usually must test individual components with open packages. There is still the possibility to test the full electronic system with a proton beam, but when SEE problems are encountered, the analysis and understanding of the failure mode is difficult. Therefore, this approach is valid for electronic systems for which a certain level of risk is tolerable. This can be envisaged for LHC electronic systems that are accessible for maintenance, and for which the failure modes caused by radiation effects are well-predicted, and can be circumvented or mitigated by techniques at the system level.

6. SUMMARY
The radiation environment of Space and LHC experiments have similar aspects. This enable the LHC community to exploit existing know-how and radiation data accumulated by the Space community since many years. However, neutron-induced radiation effects are an issue at LHC, and little radiation data are available on COTS.

Emerging new technology, such as the quarter micron CMOS technology, offers a new opportunity for the design of radiation tolerant ASICs. Recent results of demonstrator circuits based on the use of radiation tolerant practices have demonstrated that this approach is very promising and should have a large impact for electronics of LHC experiments.

REFERENCES

[8] L. Blanquart, Marebo, a full radhard pixel detector prototype for ATLAS. In this proceedings.
[11] F. Faccio et al., Total dose and SEU measurements of test structures in a deep submicron technology. In this proceedings

[12] A. Marchioro. Deep submicron technology for HEP: Heaven or Hell? In this proceedings


[14] W. Snoeys et al., Radiation tolerance beyond 10 Mrad demonstrated on a pixel readout chip in standard submicron CMOS.


[16] S. Leonardi et al., RHBip1 technology evaluation to total dose, low dose rate and neutrons, for a voltage regulator application to LHC experiments. In this proceedings


[20] ATLAS and CMS technical proposals


SHIELDING AND GROUNDING IN LARGE DETECTORS*

Veljko Radeka
Brookhaven National Laboratory, Upton, NY 11973-5000 (radeka@bnl.gov)

Abstract

Shielding effectiveness as a function of shield thickness and conductivity vs the type and frequency of the interference field is described. Noise induced in transmission lines by ground loop driven currents in the shield is evaluated and the importance of low shield resistance is emphasized. Some measures for prevention of ground loops and isolation of detector-readout systems are discussed.

1. INTRODUCTION

Prevention of electromagnetic interference (EMI), or "noise pickup", is an important design aspect in large detectors in accelerator environments. It is of particular concern in detector subsystems where signals have a large dynamic range or where high accuracy position interpolation is performed. Calorimeters are very sensitive to coherent noise induced in groups of readout channels where energy sums are formed, covering a large dynamic range. There are several potential noise sources and means of transmission:

1) Noise from digital circuits generated locally on a single front end read-out board on the detector;
2) electromagnetic radiation in the space around the detector generated by other detector subsystems, power supplies, silicon-controlled rectifiers, machinery, etc.;
3) noise induced by penetrations into the detector enclosure (e.g., cryostat) and the front end readout electronics located on the detector;
4) currents coming through ground loops, of which the detector enclosure and the front end electronics are a part, caused by any apparatus and machinery outside the detector.

Problem 1) of internally generated noise is being addressed by a careful layout and filtering on the board(s), shielding of preamplifiers, and by minimizing digital operations on the board.

The effects of externally generated noise in the form of EM radiation are best reduced by a well designed Faraday shield ("cage"). The effects of noise currents flowing through the shields, due to ground loops, are also reduced by the Faraday cage.

Ideally, ground loops should be avoided entirely. In practice, preventing formation of ground loops means to increase a ground loop impedance over most of the frequency range as much as possible.

*This work is supported by the U.S. Department of Energy: Contract No. DE-AC02-98CH10886.
2. SHIELDING EFFECTiveness AGAINST EM RADIATION

2.1 Thick Shields (t $\geq$ $\delta$)

Shielding properties of enclosures are analyzed in detail in Ref. 1. Only some main points are emphasized here. A hermetic detector or an electronics enclosure of highly conductive material, such as copper or aluminum, provides very high attenuation against external EM fields in the frequency range from a few kHz up to very high frequencies. The shielding effect is obtained by reflection and absorption of the EM wave. Attenuation by reflection of an external plane EM wave at normal incidence to the shield, with wave impedance $Z_w$ is:

$$A_r = 20 \log \frac{|Z_w|}{4|Z_s|} \ [\text{dB}]$$  \(1\)

where $Z_s$ is characteristic impedance of the shield material,

$$|Z_s| = (\omega \mu / \sigma)^{1/2} = 3.7 \times 10^{-7} f^{1/4} \ [\Omega]$$  \(2\)

(for copper)

where $\omega = 2\pi f$ is the frequency, $\mu$ is the permeability, and $\sigma$ is the conductivity of the shielding material. $Z_s$ can be expressed in terms of the skin depth $\delta = 2/ (\omega \mu \sigma)^{1/2}$ as,

$$|Z_s| = \frac{\sqrt{2}}{\delta \sigma}.$$  \(3\)

$1/\delta \sigma$ is simply dc sheet resistivity per square of the shield layer, one skin depth thick. Characteristic impedance of the shield is very low, $Z_s = 1 m\Omega$ at 10 MHz; $0.1 m\Omega$ at 100 kHz.

The wave impedance $Z_w$ (the ratio of the electric field and the magnetic field) depends on the nature of the source (electric or magnetic antenna) and the distance from the source. In the far field, i.e., distance greater than $\lambda / 2\pi$, it approaches the impedance of the free space (and air), $377 \Omega$. At $f = 10$ MHz, $\lambda = 30$ m, so that for frequencies less than 10 MHz, most detectors will be in near field conditions. For an "electric antenna" (high voltage and low current), the wave impedance varies as $1/r$, and for a "magnetic antenna" (high current and low voltage), it varies as $r$ in the near field $r < \lambda / 2\pi$. Taking the above values for $Z_s$ and for $Z_w = 377 \Omega$, the shielding effectiveness in the far field, due to reflection, is:

$$A_r = 9.4 \times 10^4 = 99.5 \ [\text{dB}] \ A_r = 9.4 \times 10^5 = 119.4 \ [\text{dB}]$$

At lower frequencies ($\lambda > 10 \Omega$), the attenuation reduces to zero $\Omega$ at the wave guide cutoff frequency, $\lambda / 2L = 1$. The attenuation can be increased if the openings form a wave guide of some length (e.g., a honeycomb structure).

At lower frequencies ($1 \text{kHz}$–$1 \text{MHz}$), it is possible to achieve very high shielding attenuation. At high frequencies ($> 10 \text{MHz}$) shielding effectiveness will be aperture-limited. The importance of electrical continuity of any shield cannot be overemphasized. This is also important for ground loop-driven currents (section 3).

A copper shield 0.5 mm thick provides a far field attenuation at 100 kHz of about 21 $\text{dB}$ by absorption, and nearly 120 $\text{dB}$ by reflection. In this case, absorption becomes dominant only above ~5 MHz. The reflection attenuation increases with the angle of incidence.

2.2 Very Thin Shields (t $<$ $\delta$)

For very thin shields, multiple reflections of the magnetic field component within the shield reduce shielding effectiveness. Total attenuation, including multiple reflections, is then given by[1],

$$A = 20 \log \frac{|Z_w|}{4|Z_s|} + 20 \log (2 \sin \frac{t}{\delta})$$  \(5\)

For very thin shields $\sin (t/\delta) = t/\delta$, and by substituting Eq. (3) for $Z_w$, and $1/\sigma$ for shield dc resistivity per square $\rho_d$,

$$A_r = 20 \log \frac{|Z_w| \sigma}{2\sqrt{2}} = 20 \log \frac{|Z_w|}{2\sqrt{2} \rho_d}.$$  \(6\)

Thus, for very thin shields, attenuation due to reflection is determined simply by the ratio of the wave impedance and the sheet resistivity of the shield. Low mass shields, such as aluminized Mylar windows on gas proportional chambers, can still provide very useful shielding. For example, 1000 $\AA$ (0.1 $\mu$m) of aluminum, which is about 1/800th of the skin depth at 1 MHz, gives $\rho_d = 0.25 \Omega$/square and $A_r = 533 = 55 \text{dB}$.

A closer inspection shows that Eq. (1) for thick shields is approximately valid down to $t/\delta = 0.2$, with an error of 9.6 $\text{dB}$.

2.3 The Role of Apertures (Gaps) in the Shield

Any gaps in the shield interrupt the flow of currents which are essential for field attenuation provided by the shield. Attenuation by an aperture in the shield is given by[2],

$$A_{ap} = 20 \log \frac{\lambda}{2L} \ [\text{dB}]$$  \(7\)

where $\lambda$ is the wavelength and $L$ is the longest dimension of the aperture, regardless of its shape. This indicates significant field penetration, which increases with frequency. For example, for $L = 10 \text{cm}$, at 10 MHz, $A_{ap}$ is barely above 40 $\text{dB}$. The attenuation reduces to zero $\Omega$ at the wave guide cutoff frequency, $\lambda / 2L = 1$. The attenuation can be increased if the openings form a wave guide of some length (e.g., a honeycomb structure).
It is based on the magnetic coupling between the ground loop current and the resistance and impedance. The ratio of the shield resistance to the inductance of the transmission line determines the magnitude of the noise current into the receiver. In many cases the ground loop voltage, $v_{ext}$, between the sending end and the receiving end is generated with a very low impedance. The ratio of the shield resistance to the shield inductance is then a determining parameter for the receiver noise current.

For shielded, balanced transmission lines, noise rejection is improved by the common mode rejection of the receiver (i.e., $cmr/4$). A principal role of double shielding for terminated transmission lines is to reduce further the shield resistance, $r_s$. Figure 3 illustrates a transmission line connection for analog signals with a very high dynamic range ($\sim 5 \times 10^6$), which has been proven in practice. Inductance of the shield can be artificially increased by several turns on a ferrite core. The noise current in Fig. 3 is given for a direct connection in place of $C_{p}$. A capacitance, $C_{p}$ of 100-300 pF reduces further the shield currents at lower frequencies, and prevents unbalancing the transformer due to the stray capacitance, $C_{12}$ at high frequencies. Differential amplifiers are also commonly used instead of transformers, with somewhat lower rejection of the noise and crosstalk.

The transmission line case illustrates the importance of low shield resistance. The same conclusion can be reached, albeit in more complex geometry, for any Faraday cage and, in particular, for any configuration where front end electronics is located in a shielded enclosure attached to the detector. This is the case for almost all subsystems in LHC experiments. Any gaps in the enclosures are particularly important. This is where the well developed technology[2] of rf gaskets may have to be applied. Special attention has to be paid to galvanic compatibility of the metals used, to ensure low contact resistances over the lifetime of the experiment. In particular, contacts with bare aluminum have to be avoided. Aluminum has to be chromate or tin-plated or, if that is not practical, a brush-on coating has to be applied to contact surfaces.

Prevention of noise injection by ground loop currents is usually more difficult than shielding against EM radiation.

### 4. Potential Ground Loops in a Large Detector Subsystem

Large detector subsystems have a large number of connections to the surrounding world for signals, monitoring, cooling, power, etc., that if left to chance, a bewildering network of ground loops will arise. Even in cases where all signal transmission to and from the detector is digital, and via optical links, power and ser-
5. AN OUTLINE OF SOME ISOLATION MEASURES

Figure 5 illustrates some of the practical configurations for communicating signals, power and various sensor lines with the interior of a Faraday cage. The intent of all of them is to divert any ground loop currents into the shield (enclosure). In examples 2 and 3, the impedance of the connecting lines is increased by a balun transformer, or by resistors in each line where the current in the leads is very low.

Figure 6 illustrates floating dc supplies for low voltage (high power) and for high voltage (very low currents).

6. THE QUESTION OF SAFETY GROUND

Prevention of ground loop currents, by increasing the impedance of any loop as much as possible, leads to the following guidelines:

- All detector subsystems will be electrically isolated;
- There will be no connection to ground other than "Safety Network";
- There will be no connection between different detector subsystems.

(These have been adopted as the primary guidelines in the ATLAS Policy on Grounding.)

The goal of the isolation is to prevent numerous possible ground loops (illustrated in Figs. 1 and 4), to allow checking for inadvertent connections to various "grounds" (i.e., objects which appear to be near zero potential, such as the experiment support structure), and to allow for a safety connection to a single point without creating a ground loop.

Figure 7 shows the connection for multiple remotely sensed power supplies. The "common" can only be at the location of front end electronics (to avoid making interdependent feedback loops).

---

Figure 4. Vital lines in the ATLAS Liquid Argon Calorimeter (i.e., potential ground loops).

An objection is sometimes made that a large object, such as a cryostat, has a capacitance of several nanofarads to the support structure and other subsystems. However, at some intermediate frequencies, say 100 kHz, this presents several orders of magnitude higher impedance than the resistance of a direct connection. Noise at frequencies lower than the center frequency of the signal processing chain is important, since it can be induced by various paths of currents through nonhermetic shields, into the wide band stages of front end electronics, such as analog memories and ADCs.

1. Coaxial Cables

- Shield connected to cryostat before penetrating Faraday cage
- Short connection, low inductance
- Performed on standard feedthroughs

2. Power Supplies

- Capacitors with short leads, close to cryostat, low inductance connection
- No net DC Current in Balun to avoid saturating Ferrite (pass power and return). In magnetic field up to ~ 300-400 gauss, use 3D3 type ferrite

3. Probes, HV

- Capacitors with short leads, close to cryostat, low inductance connection
- R > 1 kΩ can be replaced by L > 1 mH when no current flows

---
1. LV Supplies $<50V$

2. HV Supplies $>50V \rightarrow -kV$ Supplies, low current

3. Supplementary safety grounding:
   high impedance at low voltage

Figure 6. An illustration of “floating” low voltage and high voltage power supplies and supplementary safety grounding.

Figure 7. Connection of remote multiple power supplies.

Once the subsystem isolation has been ensured, a well-defined safety ground must be established. To what point?

In the case of the LAr Calorimeter, a dominant consideration is to preserve from EMI the Level 1 trigger signals. This is the only analog transmission of electrical signals from the calorimeter. It will be accomplished by differential transmission, with high common mode rejection (push-pull drivers, shielded twin lead transmission lines, differential receivers). It is reasonable to require that any potential difference between the sending end and the receiving end be minimized over most of the frequency range. At high frequencies, the current through the shielding braid should be minimized. Thus the safety ground (reference point) should be at the location of Level 1 signal receivers. Each cryostat will have a low resistance connection to that point, as illustrated in Fig. 8 (a part of that connection could be the common braids of Level 1 cables from each crate).

In case of a subsystem where all signal communications (including sensors and controls) are by optical links, and floating power supplies are used, safety ground could be some other point. However, potential differences between adjacent subsystems are minimized when they are connected to the same reference point. If a part of a subsystem could be inadvertently separated during maintenance, and a possible safety question arises, an additional connection could be made to the same reference point, but via a nonlinear network (high impedance for small signals) as in Fig. 6.

**ACKNOWLEDGMENTS**

Discussions on shielding and grounding principles and practice with R. Chase, J. Colas, C. de La Taille, P. Rehak, H. Williams, and B. Yu are gratefully acknowledged.

**REFERENCES**

3. The role of magnetic materials at low frequencies is discussed in Ref.1, p.159.
DETECTOR CONTROL SYSTEM

H.J. Burckhart
CERN, Geneva, Switzerland

Abstract:

The importance of using a powerful Detector Control System (DCS) has much increased with the size and complexity of High Energy Physics detectors. The generation of detectors for the LHC experiments puts further requirements onto DCS due to the inaccessibility of the equipment and the hostile environment concerning radiation and magnetic field. Novel techniques such as fieldbuses for distributed input/output and Programmable Logic Controllers for closed loop control have to be employed. These represent the layer closest to the detector of hierarchically organised multi-layer DCS. After having introduced the general concept of the DCS the paper will concentrate on hardware-related aspects and will stress the desirability of standardisation in the fields mentioned above.

1. MOTIVATION

The necessity of an overall DCS has arisen with the advent of the LEP experiments in the late 1980s. The experiments had become too big and too complex to be controlled manually. The experience gained is an important input to the design of the DCS for the LHC experiments.

Usually one operator supervises the whole experiment, normally a physicist of the collaboration. As he might not be working with the hardware of the detector at all, he might have only little knowledge in this area. But even a hardware expert will know in detail only the part of the detector, which he is involved in. Therefore the usage of DCS must be based on general common sense and must not presume much detailed knowledge. In fact this detailed knowledge about the operation of the different parts of the detector might even get lost over the years of running as experts will leave and new persons will join. However this knowledge can be preserved in procedures defined in DCS.

It is most obvious, that the earlier problems get detected, the lesser the consequences are they have and the easier they can be fixed. Therefore regular checking of the many hundred thousand parameters of a LHC detector is essential. The level of severity of problems together with the appropriate actions to take has to be defined by the experts and the possibility must exist that DCS shuts down automatically (parts of) the detector, i.e. without operator intervention.

The functionality described above was in general implemented in the Slow Controls Systems of the LEP experiments. However the DCS for LHC experiments should include further, more advanced features. Malfunctioning of a subsystem may result in a cascade of error messages and automatic actions. To find the original cause of the problem is sometimes far from trivial and may require the support of an artificial intelligence system. This may also give suggestions and advice to the operator how to react. Such a system may also learn about the normal operational behaviour of the detector and may be in position to give a forecast of the problems, which are about to come up. This may enable the operator to intervene and prevent the fault to develop or this information can be used to carry out preventive maintenance. Such a system may in the end even be able to solve problems autonomously.

2. SCOPE

A homogenous and coherent way of interaction has to be provided with all aspects of the experiment, namely the detector itself, the LHC accelerator, and the infrastructure and services.

2.1 Detector

A LHC detector can be subdivided in a hierarchical way, the highest level consisting of the tracker, the calorimeter, the muon detector, and the trigger and data acquisition (DAQ) system. For DCS a further factorisation into "subdetectors" is appropriate. This is not only influenced by the different technologies used, but also by organisational questions. For example if different groups of institutes build the barrel and the endcap of the electromagnetic calorimeter – even if the same technology is employed – it may be appropriate to define two independent subdetectors concerning DCS. The subdetectors themselves are composed of several levels of subsystems. Two possible examples for the hierarchical organisation of subdetectors are shown in Figure 1. This can be done in many different ways and is completely at the discretion of the groups involved.
DCS should cover all interactions with all subdetectors, ranging from simple operator commands to very involved interactions executed by the subdetector expert. In all cases it has to be verified internally that the interaction requested is safe for the detector. The same procedures may be usable for different detectors and certainly the same type of hardware can be used in many places. This helps in standardisation between the different groups and is economic concerning resources and maintenance.

DAQ also connects to all subdetectors, as DCS does. The borderline between the two systems is naturally defined by the type of data involved. DAQ deals with all the aspects of physics events, like data flow and storage, quality monitoring and such like. These data are organised by event numbers. All other types of data, which are normally organised by a time stamp, are the domain of DCS. Quite intense interaction between the two systems will be needed. This consists of exchange of commands with the replies following and of status information in general. However DCS should operationally be completely independent from the DAQ system, because the latter is normally only running during physics data taking. In contrast DCS has to be operational all the time. In order to avoid negative interference, different communication paths to the detector should be used for both systems wherever possible. The split in two systems does not exclude that tools and services can be used in common. In the case, that the same function is provided by two different implementations, an interface between the two without loss of functionality must be available.

2.2 LHC Accelerator

All interactions with the LHC accelerator should be channelled via DCS. As the detectors are the ultimate sensors for tuning LHC, information needs to be continuously exchanged about the instantaneous luminosity and the backgrounds. In fact all operational parameters of the accelerator, which might have an impact on the operation of the detector or on the subsequent physics analyses have to be available to DCS and must be logged. Also action requests like beam dump or injection inhibit should be transmitted via DCS. Another responsibility of DCS will be to measure integrated radiation doses in the different parts of the detector. As these services are also needed outside the data taking periods, they have to be provided by DCS and not by DAQ.

2.3 Services and Infrastructure

There are various external systems the experiment has to communicate with. Examples for such systems are the cooling, ventilation and cryogenics plants. The state of them and even more importantly, early indications of
problems have to be known. Interaction with the electricity distribution system may also be required. A special case presents the safety system. Information exchange with DCS is needed in both direction, but it should not be possible for DCS to act on the safety system in order not to disturb its operation. However early warnings about safety problems will enable DCS to take corrective actions or to shut down the problematic part of the detector. It is absolutely essential that the global safety status be presented to the operator at all times. DCS should act as user interface to this system.

In summary DCS is the mandatory tool for all actions the operator does and for all status and error reporting. DCS is not responsible for the security of the personal and for the ultimate safety of the equipment. The latter has to be guaranteed by hardwired interlocks and perhaps by local, stand-alone Programmable Logic Controllers (PLC).

3. REQUIREMENTS

In the following only the requirements, which are specific for our environment as compared to industrial controls will be discussed.

It has been shown that the detector is composed of many quasi-independent units. They all go through different phases like R&D, prototyping, pre-series production and tests, mass production, assembly, calibration, installation, and finally operation. Each phase includes controls needs. In fact the functions required increase from one phase to the next. In order to avoid that developments diverge for the different subdetectors, the relevant functions have to be made centrally available in time. In the end one just wants to combine the different control systems into a single one. Once the full detector is integrated one has from time to time operate its different components separately, e.g. for maintenance. Hence DCS needs the capability to work in two ways: in many small partitions and integrated as one overall system.

The existence of external systems, which have their own controls, and the independent DAQ system require, that DCS is open, which means that standard interfaces for communication are defined.

As an experiment is a research facility and is in constant evolution in contrast to a production plant, DCS has to be flexible and allow for frequent changes of the control procedures. These higher level operations must be decoupled from the basic low-level functions, which supervise the safe operation.
A very special requirement on the hardware results from the hostile environment, in which the detector operates. The electronics situated in the experimental cavern has to tolerate radiation and magnetic fields. This implies also, that this part is not accessible during data taking and powerful remote diagnostic tools are required.

4. ARCHITECTURE

DCS will be hierarchically organised in layers as shown in Figure 2.

The top layer consists of operator and server workstations, which are situated in the main control room on the surface and in the accessible electronics rooms under ground. This layer implements the supervisor functions like alarm handling, data and incident logging, operator interface, etc.

In the next layer are the Local Control Stations (LCS). They supervise a subdetector or one of its subsystems in an autonomous way.

The next layer following consists of programmable front-end systems. They are geographically distributed in the cavern over typically 100 meters, according to the needs of the detector. The concept of the fieldbus, which interconnects nodes, is very suited for this purpose. There are different types of nodes. Commercial general-purpose nodes offer e.g. configurable analogue or digital input and output channels. Commercial devices like power supplies, cooling units etc. may comprise a fieldbus interface to a local micro-controller. Individual detector elements like tracking chambers may include in their dedicated front-end electronics a fieldbus node for local monitoring and control. Another possibility to implement robust local supervision is to use a PLC, in which a rather simple program regularly reads the inputs connected and executes the actions defined. This is ideal for closed loop control.

DCS will be organised in such a tree-like structure, which reflects well the organisation of the detector. Depending on the size and complexity of a subdetector or a subsystem one decides onto which controls level to map it. It is important to note that information flow is mainly vertical in the tree.

The boundary between the general DCS and the subdetector equipment is the LCS. It houses both standardised modules like a fieldbus interface and purpose-built connections to the detector. Diagnostic procedures are generally executed in the LCS, but during maintenance periods test equipment can be connected in the cavern.

5. FRONT END SYSTEM

Most of the front-end equipment will be installed in the cavern, giving rise to the following problems:

- Radiation tolerance
- Operation in a magnetic field
- Highly distributed I/O points
- Inaccessible during data taking

The radiation levels vary by many orders of magnitude from up to 100 kGy/year close to the interaction point and in the forward region down to 1 Gy/year in shielded areas. Concerning controls one can distinguish two categories. The Inner Detector radiation hard electronics will be required. This will be part of the read-out electronics and will be designed using special technologies. Outside the calorimeter radiation tolerant electronics will be sufficient. For this electronics, which will be installed at accessible places, one should be able to use standard commercial components of the shelf (COTS). However some special care in the design has to be taken. Only selected components, with samples verified in radiation tests should be taken. The design should aim at higher performances than needed, i.e. using a 16-bit ADC when only 12 bits are needed, in order to allow for degradation due to radiation. For the same reason one should operate the components at lower parameters than specified. During operation one has regularly to check the integrity of memories. And finally one should foresee the possibility to exchange the electronics during the lifetime of the experiment. These preventive measures are still much cheaper than to design everything in a radiation hard technology.

The magnetic field in the cavern will vary in direction and magnitude from place to place and will reach values of a few hundred Gauss. Therefore electronic components like coils, chokes, transformers, and some types of DC/DC converters can not be used. Also power supplies may be sensitive to magnetic field. Therefore one should foresee to feed the electric power via cables.

The I/O points will be distributed over the whole volume of the detector. Cable length of some ten meters will suffice to connect sensors to I/O concentrator of typically some hundred channels. All this electronics is accessible only during periods without beam in the LHC accelerator.

The solutions to all these requirements are fieldbuses and PLCs.

5.1 Fieldbus

A fieldbus is a simple cable bus, connecting "intelligent" nodes by using a well-defined protocol. The nodes usually contain a microprocessor. They can execute simple tasks like data conversion and reduction, error detection, etc. A big variety of fieldbuses is in use in industry. It ranges from simple cables reading out sensors up to the complexity of Local Area Networks. These fieldbuses are well supported by industry both in hardware (chip sets, ready made general-purpose nodes, measurement instruments) and in software (drivers, etc.).
diagnostic and supervisor software). The fieldbuses differ in their technical characteristics like bandwidth, network topology, length, determinism, robustness, error handling, openness, redundancy, etc. An investigation in this field has been performed [1] and 3 fieldbuses are recommended for usage at CERN: CAN, Worldfip and Profibus. They cover all areas of applications needed.

5.2 PLC

PLCs also cover a wide performance range. It starts from small controllers for closed loops with a few parameters and goes up to complex I/O systems of hundreds of channels. They usually have a simple program structure, i.e. one big loop, which gets executed in regular intervals, and the may have interrupt capabilities. As there is no operating system and no multi-tasking involved, they are very robust and are deterministic. However their possibilities and their flexibility is limited. They usually have a dedicated programming environment. Connection is provided via LAN and/or via a fieldbus. They are usually proprietary systems.

5.3 Applications

Both fieldbus nodes and PLCs are very suited for distributed I/O concentrators. They can perform simple data processing and reduction. Also local, low-level control tasks are well within their capabilities. As powerful remote diagnostic tools exist, access is normally not required.

The usage of a fieldbus also helps standardisation. The definition of the electrical characteristics and of software protocols allows different types of nodes to reside on the same bus.

6. PRACTICAL WORK

A joint controls project (JCOP) [2] between the 4 LHC experiments and the CERN IT/CO group has been started. The aim is to use as much components as possible in common for the DCS of the 4 experiments. This should use the resources available in the most effective way, not only in the implementation phase, but also during exploitation. The system should be based on commercial products wherever possible. Dedicated interfacing to the individual DAQ systems, which will be different in the 4 experiments, will be needed. The interfacing to the external services will have to be done only once.

After the collection of the requirements, the high level architecture is being defined. In parallel a technology survey [3] has been carried out in order to investigate commercial control systems. An evaluation of the most promising supervisor systems has started. It will be carried out in 2 phases, first in the laboratory with devices supported by the product, and then in a subdetector project using also specific front-end electronics. Controls aspects of complete subsystems and devices like high voltage supplies, gas systems, and electronics crates and racks are also being studied.

Concerning hardware detailed work with the fieldbus CAN [4] and the software protocol CANopen has been carried out. A general-purpose analogue input device has been built and the performance and the radiation tolerance have been measured [5].

7. CONCLUSIONS

The LHC experiments will need a powerful control system. The tree-like organisation of the detector requires DCS to be structured in layers. For the lowest layer, which connects to the detector, fieldbuses and PLCs are very well suited. Emphasis should be put on the usage of commercial components, both hardware and software. This will help standardisation not only between the different subdetectors of one experiment, but also between the 4 LHC experiments and maybe the LHC accelerator.

8. REFERENCES

[5] B.Hallgren and H.J.Burckhart, “Front-end I/O via CANbus of the ATLAS Detector Control System”, these proceedings
Advanced Testing Techniques for
ASICs and MCMs
Alan Oakley
Integrated Measurement Systems
Bracknell, UK
e-mail: alano@cadence.com

Abstract:
This paper sets out to discuss some of the following subjects associated with testing
today's Mixed Signal, Multi Chip Module and Sub Micron ASICs. Testing during
product development phases of engineering test and production test along with the
economics of test, specifically the criteria needed when considering purchasing a specific
type of tester and what tests are performed on the device under test. There will also be a
description of the utilities available for device debug and an analysis of the testing
challenges, specific tools and methodologies to provide solutions for the devices
discussed in this paper.

Introduction.
Test has always been considered to be an unnecessary overhead during the product
development phase, as a designer would argue that simulators provide sufficient fault
coverage to test the most complex of device. This is not necessarily true when viewed
from the test engineer’s perspective as he would have converted “perfect” simulation files
into his tester format only to find that due to a process fault the device does not work. It is
here that the detective work starts. His first samples will either be on a wafer,
necessitating the use of a wafer prober, or in packaged form, probably assembled from
visually good die. The type of tools he will need to use may be a Photo Emission
Microscope to look for hot spots, an Electron Beam system (Ebeam) to analyze node
voltages and a Focused Ion Beam system (FIB) to repair broken tracks or lay down new
metal. Once all the problems are resolved in this product development phase, then the
device is released for production, but again only after many different process runs at the
extremities of the “recipe” and after exhaustive hot and cold testing and possibly “burn
in” where the device is subjected to varying periods of extremities of hot (>150°C) and
cold (<-55°C)

Economics of Test.
When considering the Economics of test some of the following factors come into play,
such as tester type, tests to perform, and tester utilization. When deciding which tester to
use it is always important to consider whether it is actually worthwhile buying a tester. It
could possibly be better to subcontract test to a test house or a wafer fabrication suppliers
test facility if only a few designs are done each year. Assuming it is worth buying your
own tester, does its price fit your budget ?, is it easy to use ?, will you get a return on
your investment ?, will you have to run it 24 hours a day?, does it need expensive
services such as air conditioning or refrigeration units to run? or can you program it offline?, thus enabling many engineers to prepare test plans without actually using the tester. If the tester is a different type to other Automatic Test Equipment (ATE) then it is worth considering the ease of software program transfer from Tester A to Tester B, and whether a complete set of fixtures are required, or just a compatible mother board which accepts interchangeable device interface boards from either tester.

**How Much Test?**

There has all ways been a concern as to what tests should be performed and how much fault coverage they can achieve. Traditionally Functional tests have found most faults as they check the device as it would work in its typical operation. As devices and systems have become more complex then the need for Scan and Built in Self Test (BIST) methods are needed, however the disadvantage to this is that they consume extra silicon area, which designers are not too willing to give up. Extra silicon area means a higher chip cost, however this is still worthwhile as savings in field returns are almost eliminated if faults are found before customer shipment. Iddq is a more recent technique to find faults where the device is tested with a special set of vectors which are used to put it into a quiescent state and then monitor the supply current. A faulty gate oxide short is normally found using this technique. A monitor is required as it not only has to sink high chip currents when the device is operating normally, but also has to measure femto-amps when in a quiescent mode. Not one of these four techniques is better than the others as these methods complement each other to come closer to achieve that elusive 100% coverage.

**Types of Test Equipment.**

There are five types of test equipment which may be used:

- **System Test** will test parts in the working environment they are destined for by using a dummy package with flying leads to the Device under Test (DUT). The extra leads could cause timing delays and it would be difficult to automate the test process with a handler.

- **Rack & Stack** would utilise GPIB or VXI instrumentation with a fixed configuration controlled by a host computer for test. Although this would provide a better solution for test no automation would be possible.

- **Engineering Testers** are small floorstanding testers, which have many versatile test sources, allowing simple reconfiguration. They have low running costs and are capable of automation of tests.

- **Production Testers** are much larger than an engineering tester and require more elaborate services. Although they cost more, they have more resources per pin with good automation.

- **Home Brew Testers** are designed in house, normally costing the same as an engineering tester, but at the cost of development time and could have support issues if their designers change jobs.
Typical Tests Performed

The following tests are normally performed to completely check device performance.

**Continuity Tests** check that the device is in contact with the tester by checking the presence of an protection diode; they are particularly useful when wafer probing

**Functional Tests/Scan Tests** are normally performed at a Low and High Vcc Level

Power Consumption is measured when the device is either in a Static, Dynamic or Quiescent state

**DC Parametric Tests** check for Input and Output pin Leakage. Gross Pin Leakage Output Level. They require the use of a Parametric Measurement Unit (PMU) which is capable of either forcing voltage and measuring current (or vice versa) on the pin under test.

**AC Parametric Tests** check for Setup / Hold Timing on input pins and Propagation Delay on output pins.

Tools for Automatic Test

**Pattern Conversion** will allow conversion from a simulator output file (for example verilog, vcd format) to create a tester ready setup and pattern file.

**Graphical User Interfaces** make the tester easy to use through a series of windows that instantaneously show and allow modification of the test settings.

**Graphical Programming** makes test flow programming an easy task, with the use of icons (similar to subroutines) and wiring (program flow). This is a much easier than programming in more traditional languages such as "C", Pascal, Basic or Fortran.

![Graphical Programming Software](image)

*Figure 1 - Example of Graphical Programming Software*

**Macros** allow test setups to be stored within the tester, thus eliminating unnecessary communications between a host computer and the ATE.
**Test Sequencers** give a graphical representation of the tests performed with the measured results, Pass/Fail and Failure Bin information.

<table>
<thead>
<tr>
<th>Step</th>
<th>Step Title</th>
<th>P/F</th>
<th>O</th>
<th>Mode</th>
<th>Action/Taken</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Continuity</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Loose Functional</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Tight Functional</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Voh-Vol</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Iih-Iil</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>Vdd</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>SHMOO</td>
<td>Vdd vs Fmax</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>VIDEO</td>
<td>Signal Integrity</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>Full Pattern</td>
<td>Vector Burst</td>
<td>PASS</td>
<td>Normal</td>
<td>Continue</td>
<td></td>
</tr>
<tr>
<td>Func250</td>
<td>350MHz</td>
<td>PASS</td>
<td>Normal</td>
<td>Pass 300MHz</td>
<td></td>
</tr>
<tr>
<td>Func300</td>
<td>300MHz</td>
<td>PASS</td>
<td>Normal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Func250</td>
<td>250MHz</td>
<td>-</td>
<td>Normal</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2 - Example of Test Sequencer**

**Shmoo Plots** are versatile flexible plotting utilities that show how a device reacts to different values of test parameters in 2-D plot. They may display different failure modes, first fail vectors and may be run in batch modes with the results sent to file.

**Figure 3 - Example of a Shmoo Plot**
**Off-line Programming** not only provides an easy test program generation tool, but will also check for tester resource compatibility.

**Conversion to Other ATE** tools help when transferring test setups and patterns to other ATE.

**Virtual Test** gives the test engineer the ability to simulate the test environment with the DUT before it is even fabricated, which in turn reduces the test development time.

**MCM Testing**

Although an MCM provides a neat compact package with more functionality than a semiconductor device due to the ability to mix different technologies, large chips or just to incorporate components that would be restrictive to include on a chip, it is a complex device to manufacture and test. The important ingredients are fairly good die (FGD) to be put down on a known good substrate (KGS) which effectively creates a small equivalent printed circuit board (PCB). The key to testing is to use PCB test techniques such as Structural, Functional and Final test., however due to the value of components being used in the assembly process it is normally cost effective to rework faulty parts. The manufacturing process may be summarized in the following diagram (figure 4)

![Figure 4 - Summary of the MCM Manufacturing Process](image)

It is important that devices with Scan and BIST are used in an MCM, although this may not be possible, and special software is needed to compensate for the lack of testable devices.

The test generation process requires Netlist and Boundary Scan Data Library (BSDL) information which have to be analyzed to prepare a set of Serial Vectors (SVF) for test and a test analysis report (to give an indication of how much fault coverage). Once the MCM has been tested the test failures have to be analyzed with Boundary Scan Map information to create a Fault Dictionary of where the failures are physically located on
the MCM, thus allowing repairs. This process is summarized in Figure 5. The important test tool needed is the ability to analyze long lengths of Scan Data by segmenting it into Frames and Clusters, thus making it easier to check the response from a known stimulus. The benefits from this technique are that the data is viewed logically, the errors are isolated and are interpreted much faster.

![Diagram of MCM test process]

**Figure 5 - Summary of the Fault Isolation Process in MCM Test**

Some of the typical failures are due to wrong and/or missing die, die internal failures, die input/output failure, interconnect opens or shorted and die interactions. The testing methodologies may be summarized by the following descriptors: Interfaces (to other MCMs), Ingredients (of the MCM) Interactions and Interconnects (between die/components).

**Sub Micron Testing**

Sub Micron designs pose a different set of test problems due to the high speeds and lower supply voltages. As the device geometries are much smaller than older devices the gate delays and interconnect delays are becoming the same. Synthesis tools are needed in the design phase and similar tools are needed for test. The two main test techniques used are:

**Flexible Clocking** - High Internal Clock speeds are achieved using a Phase Locked Loop (PLL) circuit and in order to analyze speed failures this PLL needs to be bypassed and the input clock has to have the special feature to provide up to 8 clocks per data cycle (with the added ability to provide odd or fractional clocks per data cycle). This clock should
also be capable of changing the delay and widths of this clock even down to a composite sub-cycle.

Sub-cycle change on-the-fly
Delay, Width, Period

400 MHz Maximum
Clock rate

Clock and Data Cycles
Independent

6 Clock Cycles

8:1 clock:bus
Maximum

2 Data Cycles

50 ps resolution

Figure 6: Flexible Clock Characteristics

**Cycle Stretch and Cycle Shrink** - As there are now critical paths inside the device as gate and interconnect delays are the same there is a need to change the timing on a per cycle basis. This is achieved by being able to either stretch or shrink other pin timings on a per vector basis with the use of different timings or timesets. This provides useful timing information for the test engineer to create a timing fault dictionary to analyze failure mechanisms.

Figure 7: Cycle Shrink Example
**Tools** - An important tool that is used is a Time Navigator which automates the manual process of creating timesets and timing search algorithms such as domino and ripple effects. Domino effects change the timing on successive cycles which causes the timing to be sped up (or slowed down) from a starting vector. Ripple effects also changes the timing on successive cycles but only changes cycle timing on one vector at a time.

Ripple

---

Domino

---

Figure 8: Ripple & Domino Effects

**Mixed Signal Testing**

As semiconductor processes have become much easier to control, so it has been much easier to include analogue circuitry into the digital domain. The mixture of these two separate worlds has lead to a variety of mixed mode solutions in the fields of Multimedia, Datacommunications, Medical, and Telecommunications. When taking a typical Multimedia device such as a RAMDAC, there are many tests needed to check out its functionality for both Audio and Video Performance (see Figure 9)

![Schematic of a RAMDAC Device](image)

Figure 9 - Schematic of a RAMDAC Device
**Typical Video Tests** would be Glitch Energy, Gain Offset, DAC to DAC Matching, White and Blank Levels, Integral Non Linearity (INL), Differential Non Linearity (DNL), Least Significant Bit (LSB) Size, Rise, Fall and Settling Times.


**Test Requirements**

Not only can test can be split into Analog and Digital, but also into Stimulus and Response. To cover all these possibilities the following tester features are required.

**Analog Testing**

The stimulus resources could consist of an Arbitrary Waveform Generator (AWG) and Reference Voltages for extreme DC voltages that could not be provided by the ATE. The response resources could consist of a Digitizer or Digital Storage Oscilloscope (DSO), Network Analyzer and a Spectrum Analyzer. These type of instruments would either be available as a GPIB or VXI instrumentation depending on the performance required.

**Digital Testing**

The digital resources needed would consist of a high speed clock with the ability to provide up to 8 clocks per data cycle and be capable of speeds in excess of 200 MHz. The data stimulus and response section should also be capable of performing at speeds up to 200 MHz.

**Conclusions**

Although design tools have advanced considerably over the years there is still a need for test to investigate all the fabrication defects created in the manufacturing stage of the production cycle, whether it be at naked die level or at packaged part. In order to survive in the competitive world of ATE, Tester Manufacturers have to work closely with Semiconductor Manufacturers to develop solutions for tomorrow’s integrated circuits. Finally although test is sometimes the forgotten process in the manufacturing cycle when budgets are reviewed, there is still an important need for it as the consequence would be the need for expensive field repair or replacement.
The Management of the Electronics for LHC Experiments

Peter Sharp
CLRC - RAL

• Introduction
• Some of the problems
• Some of the Solutions
• Summary
The Management of the Electronics for LHC Experiments

- The objectives of the LHCC Electronics Board (LEB) are:
  - To identify effective solutions for electronics systems
  - To identify common solutions where possible
  - To avoid unnecessary duplication
  - To identify common problems - show stoppers
    - Radiation tolerant electronics in the cavern
  - To identify the engineering problems at this scale
  - To encourage best practice - Test, Reliability, Maintenance, Engineering, etc. - Identify Risk

---

The Facts:

- Large number of highly motivated Physicists & Engineers
- Large number of funding agents
- Very large engineering problem
- Many rapidly developing technologies
- Very tight constraints on money
- Tight constraints on time
The Management of the Electronics for LHC Experiments

The Problem:

- To develop methods of Control which do not constrain Creativity
  - Finance
  - Technical Solutions
  - System Design
  - Reliability and Maintenance
  - Engineering Quality

The Solution:

- Increase Control without reducing Creativity - How??
  - Have a single funding source       Impractical
  - Move everybody to CERN             Impractical
  - Impose technical solutions         Impractical
- How do we harness all of the creativity in the community ??
  - Technical
  - Management
The Management of the Electronics for LHC Experiments

• The Solution:
  • We must make full use of the resources in the member states
  • Research Community - Students - Future of Particle Physics
  • Industry - Partnerships with Universities
  • National Laboratories - Partnerships - Universities & Industry
  • Public Understanding - Science, Engineering, Technology
  • Invest in the Future

---

The Management of the Electronics for LHC Experiments

• We need a framework, a management system that allows everybody to make the maximum contribution without spending a large fraction of their time in the air, travelling
• We need a distributed system that maximises the creativity, adds control, and maximises the work done in the member states.
• How ??
The Management of the Electronics for LHC Experiments

- We need a framework that promotes creativity but provides Control - Quality Management
- Quality management - all things to all men
- What is Quality Management? -
  - Framework to define Responsibility
  - Framework to define Project Specifications
  - Framework to ensure Communication
  - Framework to minimise Risk

The Management of the Electronics for LHC Experiments

- Clear definition of Responsibility
- Everyone can work independently - greater productivity
  - Minimise number of meetings
  - Define issues where communication is essential
  - Add project management tools and an EDM system
- Clear definition of Specification and Review process
- External experts to review progress & design
  - Maximise creativity
- Minimise Risk
The Management of the Electronics for LHC Experiments

- What progress??
  - We have made considerable progress - some way to go
  - Review process is used - external experts really work
  - Not all projects fully use the system
  - EDM systems exist but could be used more
  - Combine project management tools with EDM
  - More strategic management of whole project -
    - Minimise Costs and Risks

---

The Review process must be accepted by Collaborations

- Define and distribute responsibilities
- 'Not invented here' still exists
- Common Solutions - reduced cost now and in future
- Make maximum use of Industry - Make - Test - Maintain
- Consider 'future proofing' - upgrade paths etc.
The Management of the Electronics for LHC Experiments

- Quality management helps add control with creativity
- Quality management provides a framework for:

Continuous Improvement

Summary

- Many TDRs have been approved
- The Solutions are the responsibility of the Collaborations
- Together we manage these projects to maximise creativity and make the best use of our resources
- Together we must minimise the risk
- We can do this if we use intelligent management
Deep Submicron Technologies for HEP

A. Marchioro
CERN – Geneva, Switzerland (Alessandro.Marchioro@cern.ch)

ABSTRACT
This review paper discusses the applicability of advanced deep submicron technologies in the High Energy Physics environment. Most of the read-out electronics required for the generation of experiments scheduled for the future LHC accelerator has to be implemented as custom or semi-custom ASICs; the choice of an appropriate technology for the design of these components has wide ranging technical and economical consequences. In addition to requiring the integration of millions of channels at low cost and extremely low power, experiments demand the availability of components with an unprecedented level of radiation hardness - even when considering the technologies developed for space and military applications - and reliability.

A state-of-the-art deep submicron (< 0.35 μm) technologies can offer several technical and economic benefits. Such advantages come from the high volume, high yield, low cost per wafer fab-lines in which these technologies are produced, combined with the higher density, intrinsic radiation tolerance and low power inherent in deep-submicron CMOS. Nevertheless a number of difficult obstacles still face designers who are trying to find an optimal solution for LHC components.

1 INTRODUCTION
Few fields of technology are changing as rapidly as solid-state circuits. Computer components, their interconnections, consumer and telecommunication electronics are all gaining performance – or decreasing their price/performance ratio – at an exponential rate, thanks to a “continuous revolution” in the field of microelectronics. LHC is coming at a time when Moore’s law is still widely believed to be valid. The semiconductor industry has achieved a 25-30% per year cost reduction per function over the past three decades. While this offers enormous advantages to the quick engineer, it also requires management to understand how to take advantage of this revolution with a minimum of risk.

On the other hand, advanced technologies are today used in industries which are organized in a way vastly different than the HEP community, with typically tens if not hundreds of designers assigned to every aspect of a project and with a hierarchical organization in order to manage teams of many creative individuals.

Time-to-market is the factor driving most industrial projects. Very large investments in technology and design have to be amortized quickly, and new capital has to be raised to invest in the next – more complex and demanding – technology. In some markets products succeed or fail commercially due to just a tiny time difference in their introduction, which can be as short as a few months.

To profit from this Pandora’s box situation, HEP must understand how to handle such technologies and what needs to be put in place to minimize the risk of not being ready for the day the LHC accelerator will be turned on.

2 TECHNOLOGY ASPECTS
The early adoption of a technology inevitably implies that many of the infancy problems of a technology are not yet solved and that a painful learning curve will have to be faced.

The technology generation which some designers are today considering for LHC experiments is basically a digital 0.25 μm CMOS technology. Today a handful of manufacturers have the technical capability of fabricating ASICs based on such a technology, while several more use it to build their 64/256 Mb DRAM and microprocessors; the largest semiconductor manufacturer worldwide has recently announced that all its products starting from 1998 will be produced on 0.25 μm lines or better and describes the basic process in [2].

RD-49 has recently been evaluating two different 0.25 μm CMOS technologies.

<table>
<thead>
<tr>
<th>1997</th>
<th>1999</th>
<th>2001</th>
<th>2003</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. gate L [μm]</td>
<td>250</td>
<td>180</td>
<td>150</td>
</tr>
<tr>
<td>Tw [nm]</td>
<td>5</td>
<td>3-4</td>
<td>3</td>
</tr>
<tr>
<td>VDD [V]</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
</tr>
<tr>
<td>f [GHz]</td>
<td>20</td>
<td>30</td>
<td>35</td>
</tr>
</tbody>
</table>

Table 1 SIA 1997 Forecast for some parameters in VLSI technology (from Ref 3).

Assuming that LHC will start as scheduled in the year 2005, and looking at the forecast issued last year by the Semiconductor Industry Association (SIA) [3], industry at that time should be able to produce ICs with minimum line-width more than a factor of 2.5 - or two generations - denser (see Table 1).
Considering that technologies such as a 0.8 μm CMOS (about 3 generations behind 0.25 μm) are today rapidly becoming obsolete, one could conclude that by the start of LHC even today's jewel will probably be obsolete.

2.1 NEW FEATURES

Deep submicron CMOS introduced several new features in devices; moreover, not all the features listed below are necessarily introduced by all manufacturers:

- Local Oxidation has been replaced by Shallow Trench Isolation (STI), this has changed the profile of devices and potentially their leakage current characteristics. In the measurements performed so far on an STI technology, no degradation has been observed compared to LOCOS, some recent measurements indicate even that devices with non-enclosed structure consistently maintain a leakage current at pre-irradiation levels up to 200 Krad.

- Dual gate implants are now standard, and allows the individual threshold adjustment of N and P devices.

- Thin gate oxides are standard at about 45-60 Å for 0.25 μm technologies and are fundamental to their total dose radiation hardness.

- Shallow Source/Drain and sometimes complex Lightly Doped Drain (LDD) structures are required to minimize short channel effects.

- Silicided Source and Drain are necessary to reduce the series resistance to the metal contact and offer an extra free metal level. The resistance of polysilicon is also often reduced with similar techniques, this step may sometimes be undesired for analog applications, where high resistivity polysilicon or wells might be needed for implementing resistors; and may be optional (masked off) in some processes.

- Lower Supply Voltage has the largest practical impact on designers. VDD of 2.5 V is standard at 0.25 μm gate length and this requires designers to avoid configurations with more than two devices in series. On the other hand, some manufacturers offer options for NMOS devices with a threshold voltage close to 0 V, for application in analog circuits. In addition, as technology is scaling down and the ratio between supply voltage and threshold voltage (Vt) becomes smaller, concern about leakage current for multi-million transistor chips is increasing. Manufacturer are actively looking at processes with two Vt, voltages, low Vt, for high performance but leaky circuits, and high Vt, for low power and slower circuits, or at modulating the Vt through action on the substrate potential [4]. Feasibility studies of large dynamic range analog circuits at the reduced supply voltage are under study and practical solutions are being investigated.

- The number of metal interconnect levels is growing to 5 or more, as commercial microprocessors are definitely limited by the technology’s interconnect capacity and not by the number of transistors. While this development is vital for most commercial circuits, it has a relatively small impact on HEP designs, where mixed signal circuits are more common, except for such density critical applications such as pixel detectors.

- Last but not least, the interconnection to the external world is also changing, as more manufacturers are introducing advanced bonding techniques, using bump-bonding or tape techniques. Wire bonding to 70-80 μm pitch is becoming available and low-cost bump-bonding to 230 μm (area array pitch) is also available.

This change can have a profound impact on HEP ASICs if the new packaging and interconnect techniques are mastered in time. An important fraction of the cost of front-end detectors is contributed by the wire-bonding. A large saving can potentially be achieved by using more automated, and more reliable bonding techniques. The introduction of these bonding technologies nevertheless demands that designers introduce testability features based on scan-path in their circuits.

- Some foundries offer a BiCMOS option, even with exotic SiGe bipolar devices. Such technologies - with bipolar in the range of > 50 GHz - are targeted at very high speed RF and telecom components (see for example [5]).

2.2 RADIATION-HARDNESS: WHAT IS KNOWN

The utilization of enclosed gate MOS devices can be traced back to the early days of commercial field effect devices, when it was immediately recognized that making transistor profiles which would not leak was difficult [6]. The same layout techniques has been used with a commercial technology and has proved to be effective in eliminating radiation induced leakage.

The threshold voltage shift induced by charge trapped in the gate oxide can instead be eliminated by using very thin gate oxides (< 7 nm) which are ‘natural’ in deep submicron technologies [7].

Experimentally we measured threshold voltage shifts of < 5 mV up to 1 Mrad (SiO2) and < 30 mV up to 10 Mrad for both N and P devices in a technology with a 5 nm gate oxide [8]. At the same time, leakage currents are maintained to pre-irradiation levels for all enclosed devices. Finally, a gm degradation of < 7% was measured at 30 Mrad.

Figure 1 shows for example the robust behavior pre-and post irradiation of a ring oscillator implemented with enhanced layout rules.
ized with a process sigma such as to maximize the accuracy in the region $V_{GS} > 1.0\text{V}$ and $V_{DS} = 2.5\text{V}$.

In addition, process spread for analog parameters is still poorly defined and will require the submission of many test wafers to become better known.

The figure below illustrates also that the short channel effects are very important at short channel lengths and that hand calculations based on the simple $I_{DS} \propto (V_{GS} - V_{T})^2$ law can be substantially incorrect.

2.3 DIFFICULTIES AND CHALLENGES

Every new technology brings along a set of new design challenges. In the commercial field the deep-submicron generation has exposed the wiring delay problem to the digital designer and new technologies (for an example of a high performance multi-wire thickness technology see [9]) and tools instructing the synthesis tool to handle wiring delays as a principal constraint are appearing.

2.3.1 MODELING

Enclosed devices require special care in circuit modeling. Enclosed field-effect devices do not exhibit symmetry between source and drain and the modeling of an effective W/L ratio requires special care [10]. In addition, first generation deep-submicron device models are issued by industry mainly for digital application, and the device modeling might be less accurate than needed for an analog circuit. An example of the accuracy that a designer might expect from a BSIM3 model is given in Figure 2.

Published data [11] report a potential large difference (25% to 56% between wafer center and edge) in performance of chips on the same wafer and the exact consequences of this adverse trend for analog design must be understood better.

2.3.2 NOISE

Currently available deep submicron technologies are mainly developed for digital applications. Noise characteristics are modeled with limited accuracy. A preliminary but promising measurement of a noise figure for an NMOS and PMOS devices is shown below.

Figure 2 Comparison of measured and simulated data for a normally drawn 10/0.28 \textmu m NMOS device in linear and saturation region. To cancel out any process dependent effect, the simulated data curve was normal-
2.3.3 SINGLE EVENT UPSET (SEU)

The loss of data bit (configuration, calibration words) in a control circuit might be hard to detect in front-end chips. Scaling of supply voltages and gate capacitance makes deep submicron intrinsically more susceptible to SEU than previous technologies. Solutions to this problem are essentially of three types:

- **Layout level solution**: The capacitance of critical nodes can be increased; this has been done with the enclosed transistor layouts and is partially effective. This technique has an unacceptable high penalty if applied blindly on a standard cell library (high node capacitances give low speed and high power consumption), and one would force the provision of different versions of the same storage cell with different upset strengths.

- **Circuit level solutions**: Redundant storage cells can be designed with a variety of alternatives. This solution is applied also in commercial gate array libraries and can be very effective, provided one can afford the extra area.

- **System level solutions**: Safe circuits can be obtained using normal cells by introducing system level redundancy, such as parity and/or error detection and correction in data paths and state machines controlling the correctness of their states (one-hot etc.). In our opinion this is the best technique because it leaves essentially to the designer the freedom to select his/her optimal point in the redundancy/robustness space.

An LET threshold of 15 MeV cm$^{-2}$/mg has been measured recently on flip-flops implemented on a quarter micron technology with a conventional (non-redundant, static) architecture (Ref. [8]) indicating a good intrinsic robustness. These data have been interpreted taking into account the energy spectrum of the LHC background radiation, before any conclusive result can be drawn. Until now all the modeling and measurement efforts were concentrated on understanding the characteristics of storage cells. It is not excluded that ionizing particles could hit logic cells and/or clock trees at the wrong time and produce unwanted glitches. To the best of our knowledge, no systematic study of such effects in deep submicron has been performed until now.

2.4 *IS YIELD AN ISSUE?*

Industry's standard yield for digital circuits requires today a defect density well below 0.2 defect/cm$^2$. Analog yield can be a strong function of circuit design (if the designer does not take into account process spread appropriately), and its optimization requires an intimate knowledge of the process technology used. This is not easily available outside the foundry. To avoid expensive trimming of pre-packaged parts or low yield, designers will have to include circuitry to self-calibrate their ICs using a suitable external or internal reference.

To perceive the approximate scale of the problem, an 8" wafer can yield more than 500 good chips of ~40 mm$^2$. Such a chip may contain 32 measurement channels and be needed in 2,300,000 channels in a typical medium scale HEP detector. Development effort may run easily to 4-6 man-years.

By using a high volume fab-line, the cost of even a large size HEP ASIC project is therefore clearly dominated by R&D costs. This reality must be understood at the managerial level to avoid unwelcome surprises.

2.5 TECHNOLOGY LIFETIME: WHAT ABOUT 0.18 MICRONS?

Industry is moving towards 0.18 µm CMOS at a very fast pace [12]. This move will be accompanied by another major step, i.e. the introduction of 300 mm wafers. While it is reasonable to assume that the good radiation resistance characteristics will be maintained in this generation, the introduction of the larger wafers will require completely new handling and testing equipment, and this might indeed be late for LHC. In addition, the larger wafer size demands an even larger production volume to become economically attractive to the fabs.

This generation might also see the appearance of new low-K dielectric materials to reduce wiring capacitances; the resistance of such new materials to radiation will have to be studied carefully.

3 KEY CHALLENGES

The key technical and economical challenges associated with the introduction of deep submicron technologies in HEP are briefly discussed below.

3.1 DESIGN REMAPPING

Circuit topologies for analog applications can not always be remapped directly onto new deep submicron technologies. The reduction of $V_{DD}$ with almost constant $V_T$, and the constraint imposed by requiring enclosed NMOS devices may require a total or partial circuit redesign. In addition, the augmented number of available metals can be used for improving density or signal quality.

The W/L parameter in enclosed NMOS devices is no longer free, making some current mirrors painful to implement.

3.2 TOOLS AND DESIGN METHODOLOGY

A typical coupling capacitance of a metal wire in a submicron technology may approach 0.2 fF/µm when adding all parasitics from neighbor wires. This compares with perhaps 15-30 fF of gate input capacitance (these might have been 0.1 fF/µm and ~100 fF respectively in a 0.6 µm technology). Metal interconnections are therefore becoming the dominating delay between logic cells.

Presently available synthesis tools are essentially based on logic optimization, with an option on optimizing for speed or for area. Delays models are associated with gates and these are the principal elements that determine path delays. Deep submicron technologies move the
focus from gates to wires, which unfortunately is a strong function of the number of metals and of the final placement of the ASIC. The recent introduction of copper as interconnection metal for VLSI tends to alleviate this adverse trend moderately.

A much stronger contribution to design optimization needs to be provided by the CAE tools. The simple linear flow from early design synthesis, followed by place and route and capacitance back-annotation becomes complicated by requiring a good back annotation estimation to be known at an early phase of the design. High performance designs will depend heavily on the availability of such tools. Fortunately ASICs for HEP rarely have time critical paths (typical operating speed is < 100 MHz), and synthesis may still proceed along the traditional path.

Tools are also needed for other functions, such as automatic metal filling for planarization purposes. Such tools can be programmed rather easily for digital applications (an application can be seen in [13]), but can be rather difficult for analog designs, because of the extra couplings such floating layers may introduce.

3.2.1 ANALOG MODELS
The accuracy of analog models for deep submicron technologies has been examined in detail in [14] and [15]. In addition to the usual parameters studied in these papers, models for HEP should include the device degradation due to radiation. Fortunately these effects are quite limited in deep submicron, but a detailed study of these effects is still lacking.

3.3 LIBRARIES
For several years the trend in the semiconductor market has clearly been oriented towards a concentration of foundries in large companies, while many design houses are becoming fab-less.

In addition, an increasing number of silicon foundries and their customers are becoming dependent on a few specialized companies providing digital libraries for deep submicron. Today a number of portable libraries are available from several sources, and their cost can be a significant fraction of an HEP ASIC project.

What makes these libraries expensive and difficult to build is not the logic circuit themselves, but the difficulty in providing accurate timing models when long metal interconnects are present.

A special library designed with radiation resistant rules [16] has been developed recently to satisfy the request for total dose tolerance, as well as latchup immunity and single event upset. This library uses very conservative design rules and is therefore far from optimal for a native quarter micron technology; nevertheless it can still be considerably denser (~ 8 times) than in a generic 0.8 micron technology. In addition, the possibility of using more than two metals for signal routing, makes routing channels redundant and another 40% area can probably be gained.

The typical power consumption of a library cell when powered at 2 V is ~0.15 μW/gate*MHz, a reduction of more than one order of magnitude with respect to a 5 V 0.8 μm technology.

3.4 TESTING AND DESIGN VERIFICATION
Testing in deep submicron is in principle no different from testing of previous technologies, apart from potentially having to observe more nodes, given the higher design density offered in new technologies. Nevertheless this aspect of design has been left relatively uncovered until now in our community and will require much more attention in the future.

The testing issue is of paramount importance to guarantee an acceptable level of reliability for modules that can not be accessed — sometimes for many months — such as the front-end cards installed in LHC experiments.

Traditional testing techniques, based on ad-hoc test boards, must be replaced or enhanced by parametric testers, which can exercise a circuit under a whole range of supply, timing and temperature conditions, thus ensuring robustness over a wide range of operating conditions. Self-calibration techniques must also be adopted at the circuit level, to have ASICs adapt themselves to new operating conditions, after — for instance — irradiation induced damage has occurred [17]. Testing can also represent a significant part of the ASIC cost, especially when this aspect is neglected at design time. The operation of a typical integrated circuit tester can cost of the order of several dollars per minute, with an investment ranging in the 5-10,000 USS per channel for a production tester and about one third as much for a design verification tester. In addition, no 'standard' mixed-signal tester exists, and each measurement con-

![Figure 5 Example of NAND2 gate drawn with radiation resistant layout rules. Notice that the two NMOS devices are fully latchup protected in their own well.](image-url)
configuration may require and ad-hoc setup, demanding a large programming effort.

JTAG is a well established standard in the digital test domain, but testing of mixed signal ASICs requires much more designer ingenuity to shorten expensive tester time.

Finally, while digital test vectors translation is painful, but part of many design kits, analog 'test-vectors' are not easily transferable, and each measurement requires a specific configuration. Analog ATPG is not a well defined concept either, making analog testing more expensive than digital testing.

ASICs designed in HEP are largely surpassed by commercial integrated circuits with respect to performance of single channels, but the integration of many analog channels at low power in a single chip is still unique to particle physics data acquisition systems. Pulse electronics and analog memories as used in HEP ASICs are not always susceptible to standard test techniques used, for instance, in commercial RF equipment, such as FFT and spectral analysis. Analog memories would require a per-cell calibration which may need thousand of input pulses to be generated and therefore long testing time might be required.

3.5 ECONOMIC ASPECTS

The global semiconductor market amounts to about 130B$ for 1998 and is growing at about 15% annually. Many fabs worldwide are capable of processing in excess of 10,000 8" wafers per week. Any order coming for LHC electronics can only be of limited interest for such a foundry, especially considering that the investor has to amortize 1-2 B$ to recover the cost of the foundry itself.

Economic factors whose control is totally outside the influence of the HEP community have to be clearly understood through proper cost assessment to minimize the risks and lower the costs. While the investment in microelectronics seems huge from a physicist perspective, our business is next to negligible for any modern high-volume silicon foundry, therefore demanding a much better coordinated approach to the foundry that englobes all collaborating HEP Institutes. The economic trade-offs between a generic high-volume, low cost technology and a special high-quality, expensive one should also be evaluated against the cost of design development.

4 CONCLUSION

Deep submicron technology may allow the construction of ASICs for experiments of the LHC generation with good radiation tolerance and low manufacturing costs. In addition, power consumption reduction of up to an order of magnitude in digital chips can also substantially reduce and simplify the cost of infrastructure equipment on detectors. The total costs of such devices must still be accounted properly by taking into account development and testing costs.

Today's microelectronics industry is chronically much weaker in providing good design tools for leading edge technologies and a large collaborative effort between HEP laboratories is necessary to make this technology generally available, especially for mixed-signal ASICs.

5 ACKNOWLEDGEMENTS

The author is very grateful to all members of the RD49 project who have enthusiastically contributed to the success of the deep-submicron project and to the managers and engineers of the different Companies who have collaborated with us for the design of the demonstrator circuits and have chosen to remain anonymous.

6 REFERENCES.

HARDWARE TRIGGERS AT THE LHC

Eric Eisenhandler
Physics Department, Queen Mary & Westfield College, University of London, London E1 4NS, UK
email: e.eisenhandler@qmw.ac.uk

Abstract

This paper gives an overview of hardware triggers, variously called level-0 and level-1, at the two LHC general-purpose experiments, CMS and ATLAS, and at the two specialized experiments, LHCb and ALICE. The emphasis will be on techniques, technologies and special features chosen to be able to handle the huge numbers of detector channels, unprecedented event rates, and very short bunch-crossing time that characterize experiments at the LHC.

1. INTRODUCTION

Triggering of LHC experiments presents enormous and unprecedented technical challenges. The two general-purpose experiments, CMS and ATLAS, must be capable of running at the LHC’s extremely high design luminosity of $1 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, which produces an inelastic collision rate of $\sim 1 \text{ Ghz}$. The bunch-crossing time of 25 ns is extremely short, requiring that most of the electronics be pipelined, and which implies that on average there are ~20 inelastic collisions per bunch-crossing.

LHCb must confront the long-standing problem of triggering on B-meson production at hadron colliders in the difficult conditions of the LHC, in such a way as to allow it to do high-precision physics. ALICE, on the other hand, does not need a very selective trigger. However, it has to handle a huge volume of data, and also find a way to identify and record events in which its Time Projection Chamber is unusable due to pile-up but useful physics could still be extracted from other parts of the detector.

All four experiments are huge undertakings having enormous numbers of detector channels, both in order to achieve high precision and to cope with the high rates. All use multi-level trigger architectures in order to reduce the raw event and readout-data rates to a level that can be stored and analysed. The first level or two of these trigger systems must work fast enough to rely on general-purpose microprocessors, but instead must consist of custom hardware to carry out specific tasks as quickly as possible. Yet at the same time they must be programmable at the level of thresholds, operating parameters and modes so as to be as versatile as possible. This is necessary in order to be able to adapt to both unexpected operating conditions and to the challenge of new and unpredicted physics that may well turn up. In this brief review the custom ‘hardware’ triggers of all four experiments will be described briefly and, where relevant and interesting, compared.

All of the experiments have higher-level triggers based on software running in processor farms, in order to refine further the event selection and to reduce the rate to a feasible level for permanent storage. Unfortunately, space does not permit discussion of these; nor does it allow any discussion of the physics performance of the hardware triggers described.

2. ATLAS LEVEL-1 TRIGGER

The ATLAS level-1 trigger [1] is based entirely on muon detector and calorimeter information. Two separate trigger systems produce results that are combined for decision-making in a Central Trigger Processor (CTP), as shown in fig. 1.

Fig. 1. Block diagram of the ATLAS level-1 trigger.

The ATLAS level-1 trigger must reduce the rate from the bunch-crossing value of 40 Mhz to 75 kHz (with the possibility of a future upgrade to 100 kHz). The latency allowed between the interaction time and the trigger decision reaching the detector front-ends is 2.5 $\mu$s. For safety about 0.5 $\mu$s is preserved as contingency, and almost half of the remaining 2 $\mu$s is consumed in cables or fibres from and back to the detectors. Since the trigger obviously needs more than 25 ns to do its work, deadtime-free operation demands pipelined operation. The current estimate of level-1 trigger latency is 2.05 $\mu$s.

Other requirements on the level-1 trigger include unique bunch-crossing identification (BCID), which is a particular problem with the calorimeters (see sect. 2.2), and the provision of ‘regions-of-interest’ (ROIs) to the level-2 trigger so that it only has to read in data around all the trigger objects found at level-1.

2.1 Muon trigger

The muon trigger uses dedicated, fast muon detectors in order to achieve the required speed of operation. In the barrel these are resistive-plate chambers (RPC), and in the
endcap thin-gap chambers (TGC). The layout of the three muon ‘stations’ is shown in fig. 2. Each station has a chamber doublet, except for the inner endcap station which has a triplet. The RPCs cover $|\eta| < 1.05$, and since they have no wires are relatively easy to build and can cover large areas inexpensively. The TGCs cover $1.05 < |\eta| < 2.4$, and need finer granularity since the trigger stations are closer together than in the barrel, momenta are higher, and because of higher backgrounds in the forward region, especially in areas outside the toroidal magnetic field. Both types of chambers are fast enough to give unique BCID, and they also provide the second coordinate to ∼5–10 mm precision. There are ∼800k trigger channels to handle.

As illustrated in fig. 2, the inner two muon stations are used in coincidence for the low-$p_T$ trigger, with a $p_T$ threshold range of 6–10 GeV, while all three stations are used in coincidence for the high-$p_T$ trigger, which provides a threshold range of 8–35 GeV.

![Fig. 2. ATLAS muon-trigger detectors.](image)

The two coordinate views and the low-$p_T$ and high-$p_T$ triggers are combined in pad logic boards, which assign candidates to RoIs and resolve overlapping objects.

![Fig. 4. Coincidence-matrix ASIC for barrel muon trigger.](image)

The endcap muon-trigger logic is shown in fig. 5. The low-$p_T$ trigger requires coincidence matrices of 72 × 88 with 3 out of 4 coincidence logic, while the high-$p_T$ trigger needs a 256 × 288 matrix with 2-fold logic. Prototypes have used FPGAs, but ASICs are planned.

![Fig. 5. Endcap muon trigger logic.](image)

Both the barrel and endcap muon triggers send results off-detector optically to sector logic, which examines 64 sectors in the barrel and 72 per endcap and passes the two highest-$p_T$ candidates per sector to the muon-CTP interface. This combines the sector results to produce the total multiplicity passing each of the three low-$p_T$ and the three high-$p_T$ muon thresholds to the CTP. The muon-CTP interface also removes double-counting in muon-chamber overlap regions.
2.2 Calorimeter trigger

The calorimeter trigger uses trigger-tower signals summed on the detector and transmitted in analogue on twisted pairs to the trigger, whose architecture is shown in fig. 6. There are three subsystems: the Preprocessor, the Cluster Processor that finds electron/photon and hadron/tau candidates exceeding any of eight $E_T$ thresholds each, and a Jet/Energy-sum Processor that finds jets and missing-$E_T$ exceeding any of eight thresholds and total scalar $E_T$ exceeding four thresholds. The results are sent to the CTP in the form of multiplicities of each type of trigger object, and as Rols giving the coordinates of each object found to level-2.

The Preprocessor consists of eight crates of 16 preprocessor modules, each module handling 64 trigger towers. In order to achieve this, most of the electronics is on multi-chip modules (MCM), and much is done on an ASIC, as shown in fig. 7. Memories are provided for reading out trigger data to DAQ. Since the calorimeter pulses are several bunch-crossings wide, a crucial issue is bunch-crossing identification, which also requires that an accurate $E_T$ value is extracted. A programmable digital algorithm using a finite-impulse response filter and a peak-finder is implemented on the ASIC, as well as separate logic for BCID on saturated pulses so that they always produce a trigger. A lookup table calibrates $E_T$, subtracts pedestals, and applies a noise threshold. Results are transmitted serially to the cluster processor on HP G-links, and by using the fact that the BCID forbids pulses on two successive bunch-crossings it is possible to transmit four trigger towers per serial link at less than 1 Gbaud. Jet/energy-sum information is pre-summed to $0.2 \times 0.2$ before serial transmission.

<table>
<thead>
<tr>
<th>Trigger type</th>
<th>Granularity Coverage</th>
<th>No. of elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron/photon</td>
<td>$0.1 \times 0.1$ $</td>
<td>&lt; 2.5$</td>
</tr>
<tr>
<td>hadron/tau</td>
<td>$0.2 \times 0.2$ $</td>
<td>&lt; 3.2$</td>
</tr>
<tr>
<td>jet</td>
<td>$0.2 \times 0.2$ $</td>
<td>&lt; 4.9$</td>
</tr>
<tr>
<td>missing-$E_T$</td>
<td>$0.2 \times 0.2$ $</td>
<td>&lt; 4.9$</td>
</tr>
<tr>
<td>sum-$E_T$</td>
<td>$0.2 \times 0.2$ $</td>
<td>&lt; 4.9$</td>
</tr>
</tbody>
</table>

The Preprocessor consists of eight crates of 16 preprocessor modules, each module handling 64 trigger towers. In order to achieve this, most of the electronics is on multi-chip modules (MCM), and much is done on an ASIC, as shown in fig. 7. Memories are provided for reading out trigger data to DAQ. Since the calorimeter pulses are several bunch-crossings wide, a crucial issue is bunch-crossing identification, which also requires that an accurate $E_T$ value is extracted. A programmable digital algorithm using a finite-impulse response filter and a peak-finder is implemented on the ASIC, as well as separate logic for BCID on saturated pulses so that they always produce a trigger. A lookup table calibrates $E_T$, subtracts pedestals, and applies a noise threshold. Results are transmitted serially to the cluster processor on HP G-links, and by using the fact that the BCID forbids pulses on two successive bunch-crossings it is possible to transmit four trigger towers per serial link at less than 1 Gbaud. Jet/energy-sum information is pre-summed to $0.2 \times 0.2$ before serial transmission.

![Fig. 6. Block diagram of the calorimeter trigger.](image)

![Fig. 7. Functional diagram of Preprocessor MCM.](image)

The electron/photon algorithm is illustrated in fig. 8. Two-tower sums are compared to $E_T$ thresholds, and independently-programmable e.m. and hadronic isolation thresholds are available. The overlapping windows slide by 0.1 in both $\eta$ and $\phi$, so a localized shower produces hits in more than one window. The ambiguity is resolved and Rols identified by also demanding that the inner 4 x 4 towers contain a local $E_T$ maximum compared to the eight overlapping neighbours. This algorithm is executed in ASICS, each of which handles eight such windows. The hadron/tau algorithm is very similar, except that the hadron isolation region is the outer 12 cells and the threshold is done on a sum of e.m. and hadronic towers; this is performed in parallel in the same ASICSs.

![Fig. 8. ATLAS electron/photon algorithm.](image)
The CMS level-1 trigger [2-4] has very similar requirements to ATLAS, so much is familiar. However, there are also some interesting differences of approach. Once more, there are separate muon and calorimeter triggers, with a combined requirement of reducing the rate to 75 kHz. The latency permitted is somewhat longer, at 3.2 μs, and the current estimate for the design is 3.0 μs.

One difference of philosophy is that ATLAS compares objects to $E_T$ or $p_T$ thresholds locally and sends hit multiplicities to the CTP, while CMS sorts objects both locally and globally and sends $E_T$ or $p_T$ together with coordinate and quality information to the Global Trigger where thresholds and other requirements are imposed.

3.1 Muon trigger

As in ATLAS there are low-$p_T$ and high-$p_T$ triggers, but in CMS the low-$p_T$ trigger uses dedicated RPCs while the high-$p_T$ trigger uses the main muon detectors — drift tubes (DT) in the barrel and cathode-strip chambers (CSC) in the endcaps, as shown in fig. 11 — to refine the measurement of $p_T$.

3.2 Central Trigger Processor

The CTP receives results from the calorimeter and muon triggers in the form of 3-bit multiplicities above thresholds for electron/photons, hadron/taus, and jets, as well as bits flagging missing-$E_T$ and total-$E_T$ above thresholds. The 128 input bits also allow calibration and test triggers. Combinatorial logic forms up to 96 different types of trigger, permitting combinations such as: at least two jets of $E_T > 50$ GeV AND missing $E_T > 30$ GeV.

Outputs go to the Timing, Trigger and Control system for distribution to detector front-ends, DAQ, etc. as well as telling level-2 what caused the trigger. Other functions of the CTP include deadtime control, prescaling of high-rate triggers, and monitoring of rates and deadtime. The logic is based on FPGAs and CPLDs.

![Fig. 9. ATLAS jet algorithm. The window size is programmable for each choice of threshold.](image)

![Fig. 10. Calorimeter trigger $\phi$-quadrant architecture.](image)

![Fig. 11. Block diagram of the CMS muon trigger.](image)

![Fig. 12. RPC trigger concept.](image)
The RPCs cover $|\eta| < 2.1$, in $\eta-\phi$ strips of $0.1 \times 5/16^\circ$. Hits in the four RPC stations are compared to predefined templates covering different $p_T$ ranges in Pattern Comparator ASICs, as shown in fig. 12. The modularity of the trigger, which can measure $p_T$ up to 50–100 GeV, is 38 rings each divided into 144 $\phi$ segments.

The layout of the DTs and CSCs is shown in fig. 13. Each barrel DT station has one $z$ and two $\phi$ super-layers. Six rings of 0.35 in $\eta$ are each divided into 12 $\phi$ segments. The Bunch and Track Identifier forms $r-\phi$ vectors for each super-layer by solving linear equations for the hits, then the Track Correlator combines the two $\phi$ super-layers to form a vector for each station — see fig. 14 (left). Finally, the Trigger Server sorts these vectors by quality and $p_T$, and outputs the two highest to the Track Finder.

The muon trigger logic has been prototyped using FPGAs, but depending on market developments in FPGAs a number of ASICs might be used; several prototype ASICs either exist or are being designed.

### 3.2 Calorimeter trigger

The overall architecture of the calorimeter trigger is shown in fig. 16. Trigger towers are $0.087 \times 0.087$ in $|\eta| < 2.1$, and in general twice as big in $\eta$ for $2.1 < |\eta| < 2.6$. The total number is $54 \times 72$ towers for each of the e.m. and hadronic calorimeters. Towers are formed on Trigger Primitives Boards, which transmit the tower data to the Calorimeter Regional Trigger on an 8-bit quad-linear scale plus error bits. These links use serial 1.2 Gbaud copper links with Vitesse Gigabit Ethernet chips.

In addition to forming trigger towers, the Primitives Boards also compare pairs of crystal strips with their neighbours to produce very fine-grained isolation bits, as

![Fig. 15. Drift tube and CSC muon-trigger Track Finder.](image)

The Track Finder (fig. 15) combines DT and CSC track segments into full tracks, deals with the DT/CSC overlap region, assigns $p_T$ and quality to each one, and sorts them.

The Global Muon Trigger takes in the four highest-$p_T$ muon candidates from both the RPC Pattern Comparator and the DT/CSC Track Finder, removes ghosts, looks at 'quiet' bits from the hadron calorimeter for isolation, and outputs the four highest muons along with their $p_T$ and location to the Global Trigger.

![Fig. 16. Block diagram of the calorimeter trigger.](image)
shown in fig. 17. The Primitives Boards will do most of their work on an ASIC.

The Calorimeter Regional Trigger carries out the algorithms for electron/photons and jets, and begins global energy sums before passing the information to the calorimeter global trigger.

The electron/photon algorithm is explained in fig. 17. As in ATLAS, pairs of towers are examined. Hadronic veto logic is done separately for the tower behind the peak and for its neighbours. Unlike ATLAS, the e.m. isolation covers corners rather than a full ring in order to minimize the fanout required, but this is compensated by the fine-grained shower-profile cut.

![Fig. 17. CMS electron/photon algorithm.](image)

The jet algorithm uses 4 x 4 non-overlapping windows of 0.35 x 0.35 in \( \eta - \phi \), a size optimized for resolving multi-jet triggers. It is claimed that the non-overlapping windows do not compromise physics performance.

The Calorimeter Regional Trigger uses 19 9U double-depth crates (one is for forward calorimetry needed in energy sums), modularized as two in \( \eta \) and nine in \( \phi \). The crates (see fig. 18) contain eight Receiver Cards which linearize the data to 7-bit precision and do the first stage of jet and energy sums. Eight Electron Isolation Cards carry out the e.m. algorithm using ASICs. Both electron and jet data are sent to a Jet/Summary card, which begins the process of sorting out the best candidates and forms energy sums for the crate, to send on to the Global Calorimeter Trigger. Data transfers within the crate are 160 Mbit/s differential point-to-point; the backplane exists and works.

In order to achieve low latency for this part of the trigger, two ASICs will be used. A GaAs adder ASIC that sums eight 13-bit numbers in 25 ns using a 160 MHz clock has already been produced, and a sort ASIC that will produce the four highest of 32 8-bit input values is being worked on.

![Fig. 18. Calorimeter Regional Trigger crate.](image)

The Global Calorimeter Trigger sorts out the four highest-\( E_T \) isolated and the four highest-\( E_T \) unisolated electron/photons, the four highest jets, and the missing and total \( E_T \) for passing to the global trigger.

### 3.3 Global Trigger

The Global Trigger (see fig. 19) takes in the trigger objects having the highest \( E_T \) or \( p_T \) and quality: four muons, four isolated electron/photons, four unisolated electron/photons, four jets, as well as total-\( E_T \) and missing-\( E_T \). There are 32 inputs, with possible expansion to 40. Combinatorial logic allows up to 128 trigger combinations.

![Fig. 19. Global Trigger.](image)

Unlike the ATLAS CTP, it is here that thresholds are applied. The additional information accompanying each object also allows cuts in quality and in location, e.g. in \( \eta \). It is clear that there is potential for future expansion of capabilities, such as topological triggers — the main limitation is trigger latency.

### 4. LHCb LEVEL-0 AND 1 TRIGGERS

LHCb is a smaller experiment dedicated to b-quark physics [5], and like its antecedents at hadron colliders, triggering is both very difficult and absolutely crucial. As shown in fig. 20, it has a 'level-0' trigger based on calorimetry and muons, and a level-1 trigger on secondary vertices that characterize b-decays, and tracking. As will be seen, the level-1 vertex trigger looks more like a typical level-2 software trigger than others discussed here, but it must be done quickly and is utterly essential to LHCb so it is included for those reasons.
There are several competing options for these triggers. One option, whose principle is illustrated in fig. 21, is 3D-Flow with $3 \times 3$ clustering of calorimeter cells. Programmable processor ASICs running at 80 MHz are arranged in planar layers. To allow 40 MHz pipelined operation, several layers are needed. Cluster logic is done by nearest-neighbour ASICs exchanging data. It is estimated that the electron/photon trigger would need four layers, with ~6000 processors per layer, and that the algorithm would take < 1.5 μs to execute.

Another $3 \times 3$ clustering option is based on what is used in HERA-B, and uses regions-of-interest and a lookup-table technique.

Finally, there is also a proposal to use $2 \times 2$ clustering instead of $3 \times 3$ to simplify the logic and to reduce the necessary connectivity.

### 4.1.2 Muon trigger

Fig. 20. Block diagram of LHCb level-0 and 1 triggers.

The trigger requirements are that level-0 should have a fixed latency of < 3.2 μs and reduce the rate from ~9 MHz (see below) to < 1 MHz. The level-1 trigger has a variable latency of < 256 μs with an average of ~120 μs while reducing the rate to < 40 kHz.

Unlike ATLAS and CMS, LHCb cannot analyse bunch-crossings producing more than one p-p interaction, so its running luminosity will be $\sim 2 \times 10^{32}$ cm$^{-2}$s$^{-1}$, yielding a single-interaction rate of ~9 MHz and a multiple interaction rate of ~3 MHz. A special pile-up veto at level-0 will be used to eliminate multiple interactions.

#### 4.1 Level-0 trigger

This looks for high-$p_T$ electrons, photons, hadrons and muons, although it must be borne in mind that what LHCb regards as 'high-$p_T$' tends to be an order of magnitude lower than ATLAS or CMS.

#### 4.1.1 Calorimeter triggers

Electromagnetic calorimeter information is used to select isolated e.m. showers, with the preshower helping to reject hadrons, and tracker pads in front of the calorimeter used to discriminate between electrons and photons. Hadrons are selected by first examining the hadronic calorimeter, then adding e.m.-calorimeter energy in matching regions.

![Fig. 21. Concept of 3D-Flow processor.](image)

Fig. 21. Concept of 3D-Flow processor.

There are several competing options for these triggers. One option, whose principle is illustrated in fig. 21, is 3D-Flow with $3 \times 3$ clustering of calorimeter cells. Programmable processor ASICs running at 80 MHz are arranged in planar layers. To allow 40 MHz pipelined operation, several layers are needed. Cluster logic is done by nearest-neighbour ASICs exchanging data. It is estimated that the electron/photon trigger would need four layers, with ~6000 processors per layer, and that the algorithm would take < 1.5 μs to execute.

Another $3 \times 3$ clustering option is based on what is used in HERA-B, and uses regions-of-interest and a lookup-table technique.

Finally, there is also a proposal to use $2 \times 2$ clustering instead of $3 \times 3$ to simplify the logic and to reduce the necessary connectivity.

#### 4.1.2 Muon trigger

The muon trigger will use all five muon stations. Two-dimensional pad readout is used to give the necessary trigger speed. Again, there are still options to be decided.
4.2 Level-1 trigger

4.2.1 Vertex trigger

This vital trigger should produce a sufficient rate-reduction on its own. It has been facilitated by a redesign of the silicon-microstrip vertex detector (see fig. 24) to use $r$-$\phi$ geometry, which simplifies the logic greatly. The procedure is first to find two-dimensional $r$-$z$ tracks starting from three consecutive hits in $r$. Then two-track vertices and histograms are used to find $z$ of the primary vertex to $\sim 80$ $\mu$m, and finally $x$ and $y$ of the primary vertex to $\sim 20$ $\mu$m.

Once the primary vertex has been found, the impact parameter of all tracks with respect to the primary vertex can be evaluated, and then the $\phi$ data is used to reconstruct the tracks having large impact parameters fully in three dimensions. A search is then made for two-track secondary vertices.

The implementation will be more like a higher-level software trigger than the others discussed here. Vertex-detector events must be built at $\sim 1$ MHz, and a sustained data throughput of $\sim 2$ Gbyte/s is required. A number of event-building options are being examined, including the use of dual-port RAMs, as shown in fig. 25. Sub-farms of processors, most likely based on PC-like boards, will be used.

4.2.2 Track trigger

A further level-1 trigger, to be staged, uses information from the main LHCb tracking chambers to try to reject false high-$p_T$ level-0 triggers due to decays, secondary interactions, etc. This is based on ideas used in HERA-B. Seeds from the level-0 muon and calorimeter triggers are used to search for tracks (see fig. 26), then a cut is made on the reconstructed $p_T$. The implementation would be based mainly on DSPs, with some custom electronics. Similar logic is being used for a vertex trigger in the H1 upgrade, and LHCb will benefit from this experience.

5. ALICE LEVEL-0 AND 1 TRIGGERS

The heavy-ion experiment ALICE [6, 7, 3] is very different from the other LHC experiments. A selection of relevant parameters is shown in table 2. Some of the most notable ones are the huge charged-particle density, the relatively low trigger selectivity required, and the enormous data volume, due mainly to the large Time Projection Chamber (TPC). In fact, due to the long drift time in this device ALICE also foresees doing physics using other parts of the detector and other triggers — mainly dimuons — while the TPC is unavailable, and this adds to the job of the trigger logic. Note that the discussion here will mainly concern ALICE's lead-lead running.
Table 2. Comparison of ALICE and CMS/ATLAS parameters.

<table>
<thead>
<tr>
<th></th>
<th>Pb-Pb</th>
<th>ALICE</th>
<th>CMS/ATLAS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bunch-crossing period (ns)</td>
<td>125</td>
<td>125</td>
<td>25</td>
</tr>
<tr>
<td>Luminosity (cm⁻² s⁻¹)</td>
<td>10²⁷</td>
<td>3 x 10⁷ (µμ)</td>
<td>10¹⁰</td>
</tr>
<tr>
<td>σ minimum bias (barn)</td>
<td>8</td>
<td>3</td>
<td>0.1</td>
</tr>
<tr>
<td>dN(charged)/dη</td>
<td>8000</td>
<td>1200</td>
<td>8</td>
</tr>
<tr>
<td>Minimum-bias rate (Hz)</td>
<td>8000</td>
<td>3 x 10⁴ (µμ)</td>
<td>10⁵</td>
</tr>
<tr>
<td>Level-1 trigger rejection</td>
<td>10⁻¹</td>
<td></td>
<td>10⁻⁴</td>
</tr>
<tr>
<td>Event storage rate (Hz)</td>
<td>40</td>
<td>150</td>
<td>1000</td>
</tr>
<tr>
<td>Event size (bytes)</td>
<td>33-39 M (µμ)</td>
<td>5-6 M (µμ)</td>
<td>0.5 M</td>
</tr>
<tr>
<td>Data storage rate (bytes/s)</td>
<td>10⁸</td>
<td></td>
<td>10⁸</td>
</tr>
<tr>
<td>Data storage (bytes/year)</td>
<td>10¹⁵</td>
<td></td>
<td>10¹⁵</td>
</tr>
</tbody>
</table>

The hardware triggers are divided into level-0 and level-1. An overall block diagram of ALICE triggering is shown in fig. 27. Level-0 has a relatively short, fixed latency of < 1.2 µs and reduces the rate by about a factor of 10, while level-1 has a latency of < 2.7 µs with a rate reduction of only about a factor of two. The main effect of the two levels of trigger is to select central events.

The reason for this small difference in latencies is that ALICE has some detectors with track-and-hold electronics that need to be strobed very quickly, hence level-0, whose short latency requires the level-0 trigger logic to be in the experimental cavern to minimize cable length. However, the detector used in level-1 is too far downstream to fit inside this latency due to the length of its signal cables, as shown in fig. 28.

Another important ingredient is the ability to associate some of the detector with triggers whose physics analysis does not require the TPC, and logic to select this mode of operation within ±100 µs of any activity in the TPC in order to prevent pile-up. This is called past-future protection.

Many members of the ALICE collaboration also work on NA57, and the trigger for NA57 is being used as a test bed for a number of concepts needed for ALICE.

5.1 Level-0 trigger

5.1.1 Minimum-bias trigger

This aims to select real interactions from backgrounds. It uses the Forward Multiplicity Detector, a device based on microchannel plates. Their signals have a pulse width of ~1 ns and a time resolution of ~50 ps, so timing differences between the forward and backward directions can select vertex z-coordinates and thereby reject beam–gas interactions. The timing logic is based on fast passive summation of pads.

The Forward Multiplicity Detector is also used to trigger on charged-particle multiplicity in specific ranges of rapidity, using the pulse-heights of the signals.
5.1.2 Dimuon trigger

This trigger is used with the TPC, but is also the cornerstone of triggering in events when the TPC is not used. It was originally in level-1, but rearrangement of the cabling now permits it to be in level-0 (see fig. 28).

The dimuon trigger is based on two RPC stations of two planes each, and finds muon tracks using coincidence matrices that will use either FPGAs or ASICs. Simply demanding \( p_T > 1 \) GeV already reduces the rate by a factor of \(-10\).

We have also seen how LHCb is tackling its triggering problems head-on with a secondary-vertex trigger, and also how ALICE plans a variety of triggers and readout options in order to deal its long TPC drift time.

ACKNOWLEDGEMENTS

I would like to acknowledge my friends and colleagues in all four experiments for their help in compiling and correcting this review. Special thanks to Emilio Petrolo (ATLAS), Wesley Smith (CMS), Ueli Straumann (LHCb), and Orlando Villalobos-Baillie (ALICE).

REFERENCES


5.2 Level-1 trigger

The level-1 trigger is now entirely based on the Zero-Degree Calorimeters, a system of small calorimeters in the LHC tunnel at \( \pm 92 \) m. In each arm there is one calorimeter for protons and another for neutrons. Readout uses scintillating fibres and photomultiplier tubes. This trigger helps assure the centrality of events, though it only reduces the rate by a factor of \(-2\).

5.3 Past–future protection

The past–future protection, already mentioned above, is logic that can keep track of all significant interactions, not just triggers, and avoid TPC events over a period of \( \pm 100 \) \( \mu \)s. In \( \text{Pb-\text{Pb}} \) running, it rejects 63% of all potential triggers needing the TPC.

In this dead period, other events that do not need the TPC, such as dimuon triggers, are taken. Thus, there are two types of events recorded, huge events at low rate (with TPC readout), and small events at high rate (without TPC readout). Some parameters of both types of events are shown in table 2.

6. SUMMARY

In this brief overview, we have seen that although the CMS and ATLAS level-1 triggers have the same requirements and thus many similarities in their approach, there are also significant differences in both the choice of algorithms and in the design philosophy of the hardware.
CMS AND ATLAS TRACKER READOUT SYSTEMS

G. Hall
Blackett Laboratory, Imperial College, London SW7 2AZ
g.hall@ic.ac.uk

Abstract

The electronic systems being developed for the CMS and ATLAS trackers are briefly reviewed and the current status and potentially difficult problems discussed.

1. Introduction

In the oral presentation made to the conference, an outline of the systems being developed for the CMS and ATLAS tracking systems was given. These are thoroughly described in some detail in the Technical Design Reports to which the reader is referred for further information [1-3]. It was not thought necessary to repeat those system descriptions. During the conference there were also many talks reporting progress on components of the tracking electronic systems; the reader is invited to consult them for details.

There are some major differences in philosophy between the systems, most evidently that the ATLAS systems are based entirely on binary readout while those of CMS are fully analogue. While the complete polarisation of readout choices initially seems surprising, the decisions have been based on sound logical differences between the tracking systems and the practical difficulties expected to be encountered in constructing them. One example is the fact that in CMS there is a very high solenoidal magnetic field and this brings with it strong Lorentz effects which were a factor in the choice of analogue readout of the microstrips. In the pixel system this feature has been used to advantage by deliberately organising the barrel region of the pixel detector without the usual tilting which would reduce the width of the charge cloud in the azimuthal direction. However, the charge sharing between pixels of the size chosen (~150µm) then allows to improve the position resolution which can be obtained and allow roughly equal point accuracy in each major co-ordinate.

While it is easy to identify differences in the two systems, it is less usual to focus on the similarities. Structurally, both experiments use silicon pixels and microstrips for the inner region and gaseous detectors in the outer layers. However CMS relies on microstrip gas chambers while ATLAS will employ transition radiation straw tubes. They operate at very different gas gains which has driven some of the front end electronic choices. Both experiments require optical links for much of the data transmission. However CMS relies on edge-emitting lasers operating at a wavelength of 1300nm illuminating single mode fibres; ATLAS is investigating VCSELs at 850nm in multi-mode fibres. Both experiments require low cost links for which the packaging is customised for low mass; this is still a topical item for both of them. Both pixel systems plan to make use of the optical links employed in other parts of the tracker. In ATLAS by transferring binary data; in CMS by packing the data and transmitting several bits as one analogue word.

Perhaps the areas where the two experiments have most in common is in identification of similar problems. These become most clear in many of the issues which have been identified as still to be tackled, or pending, and some of them are summarised below.

2. Technologies

Both CMS and ATLAS are prototyping pixel electronics in DMILL and Honeywell SOI processes with a view to selecting one of them for final production. Both experiments report that the radiation hardness requirements of up to about 30Mrad appear to be obtainable. Having succeeded with “proof of principle” prototypes, both experiments plan to move on to larger matrices and control electronics in the coming year. Issues of adequate noise at low power and control of thresholds and cross-talk have been dealt with successfully.

In the outer trackers, i.e. excluding pixels, the technological choices of CMS and ATLAS are rather different. The binary ATLAS system makes use of a bipolar front end, but CMOS is required for the pipeline and logic. Two alternative approaches are being followed for both the Silicon Tracker and the TRT system: a two chip solution with a bipolar chip in MAXIM and a CMOS pipeline and logic chip using Honeywell bulk CMOS, or a single BiCMOS chip in TEMIC DMILL. Bipolar
amplifiers have long been believed to offer best noise for given power compared to available CMOS technologies, but there are overheads from comparators and drivers required in the two chip solution. The BiCMOS solution has the advantage of eliminating a large number of dense bonds which are required for the signal transfer between the comparator and pipeline stages. However, cost is one of the factors which will drive the ATLAS decisions, which are expected next year.

CMS will use modified versions of the same front end APV chip for both silicon and gas microstrips. It is being prototyped in Harris AVLSI-RA bulk CMOS and in the TEMIC DMILL process. The arguments for the CMOS analogue design are based on the desire to construct an analogue readout for robustness and common mode noise immunity and the desire to avoid on-chip thresholds. However, it requires the development of an analogue optical link for data transmission, which is now in an advanced state. The non-technical arguments for the use of CMOS include the desire to ensure the availability of two vendors during the procurement period to minimise both cost and technical risk. However, another risk was the possibility that the chip would become large relative to ATLAS front ends and production yield would therefore be more unfavourable with obvious cost implications. The actual size of 6.4mm x 12mm is not now expected to be excessive.

Despite the advanced stage of prototyping, the impressive results from the deep sub-micron CMOS technologies, which would offer improved noise and power performance, have stimulated interest from CMS in considering this option. Since the radiation tolerance of the process investigated also seems to be excellent, the potential cost savings are difficult to ignore.

The jury is still out on the front end technology decisions to be finally made by the two experiments, and is likely to remain so indefinitely except to those who relish the debating opportunities so offered.

On the data links, the ATLAS TRT has chosen the conservative approach of differential electrical transmission over low mass twisted pairs. This seems most cost effective for the relatively small number of links required. However, for the inner tracker and the pixel detectors, digital optical links were favoured because of the impact on the material budgets. While initially the baseline solution was LED transmitters, the degradation during irradiation appeared to be risky, particularly for the high radiation levels in the pixel volume. Therefore interest has been stimulated in Vertical Cavity Surface Emitting Lasers (VCSELs) which may be an inexpensive alternative once suitable packages have been finalised.

The CMS solution to both data and control and monitoring links has been based on work which was undertaken originally by the RD23 collaboration, which concluded in 1996 with a decision by CMS to utilise 1300nm edge-emitting III-V lasers mounted on silicon carriers. Transmitters, pin diode receivers and fibres and connectors have shown excellent radiation hardness and several prototype links have been operated to demonstrate good characteristics for both analogue and digital data transmission. The remaining issues include the cost and availability of second sources for the packaged transmitters and receivers, since suitable lasers and pin diodes can be obtained from a number of vendors.

3. System summary

ATLAS

Pixel 140M channels
50µm x ~500µm
Binary readout with zero suppression
Radiation hard CMOS
Occupancy < 5 x 10⁻⁴

Inner: Silicon microstrips 6M channels
Binary readout with zero suppression
Bipolar amplifier/discriminator + CMOS pipeline MUX
Digital optical transmission 8k links
VCSEL transmitters
Occupancy <1%

Outer tracker: TRT 420k channels
Dual threshold binary readout with zero suppression
Bipolar amplifier/discriminator + CMOS pipeline/MUX
Digital electrical transmission (LVDS) 27k links
Occupancy 10-40%

CMS

Pixel 40M channels
150µm x 150µm
Analogue readout
Radiation hard CMOS
Occupancy 2-3 x 10⁻⁴

Inner: Silicon microstrips 6M channels
Outer: MSGC 6M channels
Common analogue readout system
CMOS amplifier/pipeline/MUX
Analogue optical data transfer 50k links
No zero suppression on detector
Occupancy <1-2%
4. Some pending items

In private discussions and progress reports the common issues are readily identified:

Radiation hard electronics

There has been constant progress for several years but final solutions are still evolving, mainly for technological reasons; some technical difficulties have been encountered in several prototyping runs. There is still concern about the present and future number of available technologies and their projected cost. Questions of Single Event Effects have not been much investigated yet but they have been on the agenda for some time; progress is now beginning to become apparent.

Hybrids and electrical services

Low mass solutions are under development but not complete. Distributed power and grounds still require demonstration and the location, accessibility and maintenance of supplies is an open question, but where both experiments have chosen the baseline of placing their power supplies remote from the cavern. They are therefore concerned about the cost and cooling of large cables as well as the practical problems of delivering the high currents over long distances with no local voltage regulation. This could have consequences for system noise along with other sources of coherent noise in addition to the front end amplifier, which must dominate for the systems to function well. Measurements are certainly needed.

Power supply reliability is an important issue and would become more so if supplies were relocated to the cavern in the case that radiation tolerant versions became available. Protection circuits to ensure safety of the internal tracker electronics are an issue in either case since access will be limited and response time for problems will be long. The cooling of both racks and cables is a difficult question but which is shared with many other sub-systems.

Data links

Good progress has been made on both optical fibre and electrical links using low mass twisted pairs. Working links exist, and excellent radiation results on components have been obtained. However questions remain on the large scale implementation, since only a few manufacturers have produced packaged transmitters meeting the requirements and low cost is an important target which seems possible but is not yet proven. The congested spaces in the interiors of CMS and ATLAS force the development of low volume interconnections, which is in progress. This is also an issue for other services, especially gas and cooling connections.

System issues

The large scale production and test of components is beginning to occupy more and more of the attention of the system developers and some papers at this conference describe promising progress using customised or commercial test systems. It still has to be agreed whether in-house testing is the right approach for large production volumes or whether this is a task which can be subcontracted to industry; first steps are being taken to identify the possibilities – and costs.

Quality assurance

This is a phrase which is being used more and more frequently. It has still to be identified what it implies at each level of the system, not only the electronics. However maintenance of production standards of front end chips and assembled hybrids is known to be an important issue. What is often neglected is that the module assembly stage, often envisaged to take place in home laboratories, even small drops in module yield could be very expensive since each rejected module would involve the loss of several front end chips, at a cost at least as large as the detector and sometimes much greater. A question also asked more frequently is whether industrial production at module level is a possibility.

Large scale assembly and test

Hybrid and module assembly raise questions not only about quality control at module level but exact criteria and test methods, as well as test time. A more difficult point is the exact methods to be used for testing, since high throughput is essential. However some detectors, like MSGCs, can only be tested at present with the electronics assembled and mounted. Many developers have emphasised the importance of system evaluation, which can take place at several levels. This is known to be important for major issues like overall synchronisation of the sub-detectors with the rest of the experiment, but also for identifying “minor” faults in components which could have much larger implications at the system level, preferably at an early enough point that they can be corrected with sufficiently small cost penalty.

Slow control

The requirements are still being defined. An implied issue of interfaces, protocols, connectors and standards is at an early discussion stage.

Financial issues

The large spending required on many items which are required early in the critical path of detector construction is still a concern. Front end electronics costs are still a major part of the overall detector budget and the components must be delivered on a short timescale to complete construction on time. To manage the income and expenditure profiles will need careful planning to avoid this becoming a major constraint.
5. Summary and conclusions

Many talks at this workshop demonstrate the steady progress which has been made on components and systems. Some of these, such as the results on deep sub-micron CMOS technologies, may hold a key to constructing large systems within the limited budgets and timescales which prevail. However, if so, further developments must be rapid.

There are many issues outstanding but also other positive developments. To name a few, an LHC-like beam now seems to be about to be approved by CERN, although the date is still not finally clear, which will aid in many system tests. There is wider interest in many system issues, especially the organisation and schedules for production and their implications. A better understanding of the procedures for management of large contracts has been achieved in the last year; a radiation hard foundry market survey is under way, which is the first stage of the tendering process, required before contracts are placed. CMS will establish an “Electronic Integration Centre” which will cover areas of common sub-detector interest to be staffed by several full time engineers and it is hoped that this area will, in time, receive as much support as the mechanical integration of the experiment.

Nevertheless, there is a long way to go…

Acknowledgements

I thank many colleagues for valuable discussions, especially P. Farthouat, A. Grillo and G. Stefanini.

References

ELECTRONICS IN THE ATLAS ENVIRONMENT

Hans F. Hoffmann, CERN, Geneva, Switzerland (email: hans.hoffmann@cern.ch)

1. INTRODUCTION

Electronics in the ATLAS environment is subject to a combination of unusual boundary conditions. The most unusual condition comes probably from the distributed, international design and construction teams. Other demanding requirements come from combinations of technical conditions such as number of channels, event rate, event multiplicity, precision, cost, radiation environment, magnetic field environment, accessibility and mean time between failure, transparency to particles in certain cases, low power consumption, safety requirements, cross talk between detectors and others.

Many of these features have been at the basis of years of R&D, also in the context of the LEP activity.

Therefore here some of these points are discussed at the present state of ATLAS, namely having started production of a number of ATLAS hardware items. Electronics for other LHC experiments will not differ too much since there are the same constraints.

2. COLLABORATION ENVIRONMENT

In the ATLAS Memorandum of Understanding the basic structure of ATLAS is described as “bottom up”. Institutes undertake to deliver detector parts, which constitute together the detector according to performance specifications derived from physics goals, interfaces to neighbouring equipment corresponding to the common goals of an operational detector and a common schedule.

Groups of institutes form subsystem and system groups taking responsibility for the construction of detector systems and subsystems. Such groups are supposed to organize the whole construction work for the corresponding system. In terms of execution they follow guidelines from the ATLAS management and report regularly about progress in the ATLAS Executive Committee which is a regular supervisory meeting bringing together all aspects of ATLAS construction.

Such detector parts or systems, regarded as “deliverables”, are described and reviewed in some detail in Technical Design Reports.

All major parts in ATLAS must pass internal reviews before purchasing equipment in industry or constructing equipment in institutes.

The goal of Design Reviews is to evaluate the feasibility and technical validity of the proposed designs for a sub-system or part of it and to assess whether the proposed designs fulfill the ATLAS requirements. Based on the recommendations the design can then be finalised in preparation for the last internal review called the Production Readiness Review (PRR) which precedes purchases or construction in institutes of major detector items. Such reviews address technical and organisational matters.

Before launching the construction of major parts of the systems and engaging major expenditures engineering reviews will be organized to confirm the soundness and completeness of the final design options including all interfaces to neighbouring parts of ATLAS to minimise the risks (cost, function, schedule). Such reviews will be named Production Readiness Reviews (PRR). They are organized by the technical co-ordination and are intended as final cross check before production.

Effectively in the PRR the baseline design of the corresponding components is finally determined.

In the case of electronic parts such reviews are organized by the “Front end electronics co-ordinator” within the ATLAS Technical Co-ordination.

3. ENGINEERING ORGANIZATION

Project organization is an engineering discipline. Normally such an organization starts with a project breakdown structure. This is a description of the parts and items belonging to the project, organized in a hierarchical product- or assembly-breakdown structure, corresponding work-packages describing the tasks to be fulfilled with the items such as design, prototyping, tests, production, installation, systems tests, etc. Such an exercise is often found useful to understand the scope of the project. In the beginning such breakdown structures are limited to rather high levels of breakdown.

Another important ingredient and based on the project breakdown structure are the schedules, the master schedule describing the general features of the project evolution with time and containing “public” milestones, procurement schedules taking all impediments of the formal approval process into account, listing for example at CERN the dates of submission of documents to the Finance Committee, the construction schedule and the test, installation and commissioning schedules. Such schedules also contain milestones for the detailed work organisation.

The next important part of project organization is quality assurance. At each phase of the project the quality of the product has to be assessed. Quality here
means that the product or item is checked to correspond to the requirements in all detail and with all interfaces to surrounding objects taken into account. From this it follows that also the requirements to the corresponding object are noted down in detail and that item per item and corresponding to the phase of the project this correspondence is formally checked. Such formal checks are reviews, internal to the systems or sub-systems, and those organized at the level of the collaboration as described above.

In a formal review the baseline of the project part is normally established, in the ATLAS case this is done in the production readiness review (PRR). To follow up the baseline through the further phases of the project requires configuration management and change control. Configuration management advances all items or products of a system in a coherent way. It can be described as the mechanism which allows everybody in a complex undertaking to work at each moment to the commonly agreed final system or product. A configuration manager watches therefore over all changes to parts of the product. He assures that "engineering change requests" are made and controls the modifications following such changes elsewhere in the project.

Project management as described above is seen to reduce the risks in the execution of a project. The outline above is at the base of ISO 9000 standards.

In a project of the size and complexity of ATLAS it is mandatory to be assisted in project management by a project management software and data base, by an Engineering Data Management System, EDMS. (ref. http://www.cern.ch/ATLAS/TCOORD/TechCoord/organisational/edms/).

The main objects managed by EDMS are items or parts, components and products, bills of material which are made of components and single parts, any type of (technical) documents with files being managed in an electronic vault and projects.

Different relationships are defined between these objects, namely project - item, item -item (as designed, as built,.....) and item – document.

Many other objects are available such as engineering change requests/orders, variants, customer specific, ....

The EDMS at CERN is used by the LHC experiments and the LHC machine project. The system is being introduced, its usefulness is acknowledged and it suffers from lack of manpower to introduce data and to make use of its features. Some of the functionality of the EDMS is still fulfilled by the CERN Drawing Directory, CDD, which allows to get approval of drawings in well determined circles of approvers via their desktops.

Considerable efforts are required to make the system work soon. A project like ATLAS, with a lifetime of about 20 years, needs an organized and reliable storage of all relevant data with easy access over the network via the web from each of the collaborating institutions.

The community working on electronics has not yet really started to make itself familiar with the EDMS and its features. However, there is no doubt that the need of accessible and organized documentation is particularly important in this field. Environmental requirements to electronics: power-heat dissipation and cooling, cable racking accessibilities, transpareny.

4. EXPERIMENTAL AREA

Experiments of the size of ATLAS, comparable to a six story office building, can not be moved into garage positions for undisturbed maintenance. Maintenance periods must therefore be arranged with the accelerator and the other experiments.

Collider experiments are 4-pi detectors reaching down to small angles around the beam pipe. They try to be "hermetic". In turn access to the innermost systems of the experiment are difficult. It is those systems where the density of detection elements and the density of front-end electronics is very high.

Electronics will exist in several locations, in the experimental area itself (UX 15), with constraints of accessibility, radiation and magnetic field, in the side cavern (USA 15) which gives space to 250 racks, in the surface building SDX close to the access pit to USA 15 which will locate up to 3 times 100 racks and finally in the counting room building SCX (Fig. 1, Fig. 2).

The final allocation of the rack space to these different areas is still under discussion.

In ATLAS three types of shutdowns are foreseen, a short access allowing work on equipment surrounding the detector, a medium long access, maybe twice per year, allowing to reach calorimeter electronics and some patch panels of the inner tracker and finally the end-of-the-year shutdown which permits to do repairs on the inner tracker.

As ATLAS does not want to suffer more than 1 or 2 % of missing channels the MTBF and reliability of the equipment must be very high.

As can be seen in Fig. 3 the access conditions are not easy and equipment should not be too heavy.

The area will be connected to electrical power following the example of the LEP experiments. The installation will be designed for high reliability, high availability with adequate re-supply facilities and operational safety. In case of a mains fault that cannot be remedied by a source commutation the CERN diesel generators sets will start automatically and supply a safe network. The network will suffer a cut of 15 seconds.

Uninterrupted power supplies will be based on static systems, rectifier, battery, inverter and static by-pass switch. The use of UPS will be limited to a minimum because of cost.
The area will be equipped with emergency stops which cut all power except particularly protected systems.

The grounding rules for CERN areas are following industrial practice. In case of a fault in an electrical installation, high short circuit currents may follow other paths than the cables and wires foreseen. The currents may follow for example metallic structures, and create dangerous potential differences between parts of stairs, supports, etc. To avoid this, all metallic parts are interconnected and connected to a reference: the earth or the ground.

Since all parts must be interconnected, there can only be one grounding system. At CERN the reference is created at the surface and brought to the underground via multiple copper links. All surface buildings and all underground structures are thus linked to the same surface. The system is designed to have a sufficiently low impedance everywhere.

The grounding and dc-power distribution of ATLAS detector systems are very different.

As is well known from previous experiments, careful attention must be paid to the grounding and power distribution of each of the detector systems if they are to operate successfully at the low signal levels required. While this has been an important issue in previous experiments, it is an especially important issue for ATLAS given the large expense and time required to redo any system, and to the very large power in most systems. Therefore we have outlined the present ATLAS policy on grounding and power distribution in terms of a set of guidelines that have been arrived at via reasonably extensive consultation with each of the subsystems. The intent is that these guidelines must be followed unless specific approval for a deviation is granted.

The primary guidelines are the following:

- All Detector Systems will be electrically isolated
- No connection to ground other than “safety network”
- No electrical connection between different detector systems.
- Low Voltage Power Supplies Floating
  - Power return either fully isolated from Gnd or connected by device which has high impedance for normal operation by low impedance during failure (e.g. saturable inductors or diodes)
- High Voltage Power Supplies Floating
  - HV return likely isolated from detector by resistor
- Data, Clock and Trigger Transmission
  - Optical or Shielded Twisted Pair
- Detector in Faraday Cage
- Monitor and Control Signals
  - Optical, Shielded Twisted Pair, or similar isolation.

More details are given in Ref. (ATLAS Note EB-97-012).

5. RADIATION AND MAGNETIC FIELD

The high design luminosity and the high energy of the LHC beams generate intense secondary radiation in the detector and in the area. To reduce this radiation a complex arrangement of shielding is foreseen around the beam pipe.

As the final design of the shielding is not yet finished the figures of dose rate in Table 1 below are preliminary and indicative.

An additional safety factor of 5 can be introduced to take into account the uncertainty on the electronics behaviour due to low dose rate effects. This additional safety factor should not be taken into account if the irradiation tests follow either the US Military Standard 883D 1019.4 or the ESA Basic Specification 22900 standards.

It is the same kind of environment as that encountered in space applications and it has to be treated very seriously.

The ATLAS detector contains four superconducting magnets, a central solenoid, two end cap toroids and the very large barrel toroid. The solenoid creates a 2 T field along the field axis.

The outer girder and the absorbers of the tile calorimeter form its return yoke. In the volumes of the inner tracker therefore there is the 2 T field which has already important radial components towards the forward parts of the inner tracker.

In the gaps of the tile calorimeter which houses the LAr front end electronics and probably also LAr dc-power supplies there is considerable stray field created by the solenoid return flux. Its indicative values are also given in Table 1.

The magnetic field at the positions of the muon chamber electronics in the barrel toroid varies from several T near the coils to about 1 T in the inner and outer volumes of the Toroid.

The magnetic fields in the innermost big forward wheel of the forward muon detector again varies from several hundred Gauss to more than 1 T close to the coils.

Indicative values are given in Table 1. Equally indicative values are mentioned there for power supplies and other ancillary electronics on the structure surrounding the ATLAS experiment.
A safety factor of 5 has been introduced since this safety factor has been used by the muon instrumentation to evaluate the background rate.

**6. OTHER REQUIREMENTS LIKE TRANSPARENCY TO IONISING PARTICLES, THERMAL NEUTRALITY AND COOLING, SAFETY**

In the inner tracker region the pixel- and SCT-detectors are closely linked to their front end electronics. Low temperature operating conditions and high power dissipation ask for an elaborate cooling system which in the ATLAS case will be based on fluor inert liquids. The very high density of channels, the number of signal and power cables, the expected particle rates and the power required at the front-end of these detectors make the design of a detector, which is transparent to particles, one of the most difficult design challenges of ATLAS.

The masses of the inner tracker elements, their materials and their distributions are described in the Inner Tracker TDR (Ref. CERN/LHCC/97-16, ATLAS TDR 4, 30 April 1997, Vol. 1) and more recently in the Pixel TDR (CERN/LHCC/98-13, ATLAS TDR 11, 31 May 1998), where design requirements and envisaged solutions are given in detail.

As in the inner tracker case also in all other positions of the ATLAS detector there is a general requirement of excellent thermal neutrality.

This requirement means that electrical power dissipated in detector elements must be eliminated to high efficiency by local cooling circuits.

The most important reason for this requirement is that the more than 2 MW of power dissipated in the ATLAS detector cannot be cooled away by any standard ventilation system. The necessary air flow would excite bad vibrations in the all external parts of ATLAS. Further reasons are that proper direct cooling of electronics gives better MTBF and that no local confined spaces are overheated.

Apart from grounding requirements and arrangements already described electronics in ATLAS or similar experiments must fulfill important safety considerations.

The first requirement is in terms of safety for people, namely that all electrical power be enclosed and protected against persons touching it. This must also hold for all cases of possible malfunction. Malfunctioning electronics has been at the origin of several serious fires of experimental equipment. Badly connected low voltage cables can cause local overheating and fire if not properly monitored and designed.

The power available on p-c-boards and breakdown of components can channel sufficient amounts of electrical power on signal cables and cause them to heat up and burn.

In ATLAS cable runs and other flammable parts not protected by inert gases will be protected with sprinklers or a water mist installation to be able to stop any emergence of fire. Any larger fire would seriously endanger the whole ATLAS structure and cannot be tolerated. Electronics for ATLAS will therefore be checked for such fault possibilities and only accepted if a proper fault analysis can be demonstrated.

**7. CONCLUSIONS**

Radiation, magnetic fields, rate, transparency, special grounding, cooling and safety requirements pose an unprecedented combination of partially conflicting requirements on electronics in the ATLAS detector.

The decentralized structure of ATLAS added to the above requirements make a novel engineering organization mandatory to fulfill the requirements and to deliver in time, within specifications and cost for installation and commissioning.
Fig. 1. ATLAS underground caverns
Fig. 2. ATLAS surface buildings
Fig. 3. ATLAS access conditions to the muon detector
VCSEL Components for Data Communication Links

John Humphries
Honeywell Control Systems Ltd.
E-mail: john.humphries@uk.honeywell.com

Introduction

Several technology pieces are required to achieve radiation hard fibre optic links including optoelectronic chips mixed analogue and digital drive and receive integrated circuits and electrical and optical packaging. Honeywell is developing optoelectronics device and link technology for commercial applications, as well as for more rugged environments such as commercial and military avionics and spacecraft. Space applications have the most in common with the fibre optic requirements for the optical readout links in the LHC Project. This paper will discuss the rad hard vertical cavity surface emitting laser (VCSEL) and photodetector technology. It will discuss VCSEL reliability data currently available, its radiation immunity, eye safety issues, as well as environmental and packaging concerns. Finally, cost is a key driver in the LHC Project and the final paragraph is devoted to issues that could impact on cost and delivery.

Honeywell is a multinational organisation with its head office based in Minneapolis in the USA; at that location the technology centre is based and this group were responsible for the development of the implant VCSEL that is currently in production. More recent developments have been the oxide aperture VCSEL that I will talk about later. At Richardson, Texas, commercial VCSEL’s are produced in high volume and the reliability data discussed later is from this location. At Phoenix we have a group also involved in VCSEL packaging for “High Rel” and avionics applications and finally there is a further group in Minneapolis called SSEC that are involved in the development of rad hard ASIC’s and driver IC’s. It is apparent from this brief resume that Honeywell possesses a significant optoelectronics capability that will be of interest to various groups participating in the LHC Project, especially as it progresses towards its production phase.

Product Developments

It will be of interest to consider ongoing developments that are taking place at HTC in Minneapolis such as the oxide aperture laser and this is described in the following paragraphs.

Reliability

This section is an extract from the application notes that are published in the Honeywell Fibre Optic Data Book Catalogue 27 June 1998. This note shows exceptional life times, with virtually no early failures, when failure is defined as a 2dB drop in output power. Burn-in is performed for all VCSEL wafers and is primarily aimed at selecting stable devices for the high-speed data communications market place. This burn-in is not done to weed out early failures (which are very rare) but more for stabilisation of threshold current and slope efficiency. Early in life, proton movement in the VCSEL can cause shifts in threshold current and/or slope efficiency, sometimes resulting in significant output power changes both up or down. A 100 percent production burn-in can reduce that effect to typically less than 1dB change. Without burn-in, changes can be greater than 2dB on individual devices.

Honeywell performs wafer evaluation acceptance burn-in on every wafer used in production. Part of this evaluation process involves both a short-term and a long-term burn-in for a sample of each wafer. The long-term burn-in assures the reliability of the wafer; the short-term burn-in assures that the early life changes in power output is not too great, the 100 percent burn-in done for high speed datacomms. VCSEL’s is adequate to stabilise the power output.
The following table gives predicted reliability for VCSEL’s at 25 degrees C and from the data presented it is apparent that the VCSEL is significantly more reliable than LED’s.

<table>
<thead>
<tr>
<th>Drive Current</th>
<th>Junction Temp</th>
<th>Median Lifetime</th>
<th>MTTF Hours Point est.</th>
<th>MTTF Hours 90% Conf.</th>
<th>FIT Point est.</th>
<th>FIT 90% Conf.</th>
</tr>
</thead>
<tbody>
<tr>
<td>10mA</td>
<td>37°</td>
<td>24,283,929</td>
<td>41,001,822</td>
<td>37,955,301</td>
<td>24</td>
<td>26</td>
</tr>
<tr>
<td>12mA</td>
<td>41°</td>
<td>11,104,809</td>
<td>18,749,743</td>
<td>17,356,598</td>
<td>53</td>
<td>58</td>
</tr>
<tr>
<td>15mA</td>
<td>48°</td>
<td>3,798,041</td>
<td>6,412,743</td>
<td>5,936,263</td>
<td>156</td>
<td>168</td>
</tr>
</tbody>
</table>

Note
1. Junction temperature is based on a reasonably good thermal environment with good airflow around the device.
2. Median Lifetime is based on lognormal statistics.
3. MTTF and FIT calculations based on exponential statistics are included for comparison purposes. MTTF is mean time to failure and FIT is a failure rate unit designating the number of failures per billion device hours.
4. Point estimate MTTF is the number of device hours on operating life test divided by the number of failures. Point estimate FIT is the inverse of the MTTF multiplied by one billion. The figures are based on the meta-analysis.
5. Confidence MTTF and FIT are calculated using chi-square statistics based on the meta-analysis sample size

Reliability Summary

- Latest Reliability Data is from 500 metal TO46 packaged VCSEL devices
- 22 Burn in Groups at 5 temperatures and 5 operating currents
- The study comprised 8 wafers built during a span of more than a year
- 2 million actual burn in device hours logged, additional testing on other VCSEL parts takes the total number of device hours to 3.5 millions of March 1997 (These figures do not include on going production burn in)
- Subsequent testing since March 1997 is continuing and confirms that ongoing device enhancements are further improving the reliability of Honeywell VCSELs

Resistance to high levels of Radiation

FO Links are attractive for harsh environment links

<table>
<thead>
<tr>
<th>Advantages (FO vs coax)</th>
<th>System Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Much higher bandwidth with no RF shielding required (theoretical limit (-10^{17}) bits/second)</td>
<td>Reduced weight, cost, and power (critical issues for aircraft and satellites)</td>
</tr>
<tr>
<td>Immune to EMI/RFI and ground loops, difficult to eavesdrop</td>
<td>Signal integrity and security maintained in noisy environments</td>
</tr>
<tr>
<td>Tolerates wide temperature range, corrosion-resistant, good radiation tolerance</td>
<td>Longer lifetime, more reliable in hot/cold/wet/dirty/rad environments</td>
</tr>
<tr>
<td>No spark or ESD hazard</td>
<td>Safe to use in volatile (explosive) environments</td>
</tr>
</tbody>
</table>
### Typical Requirements for RAD - Hard Links - LHC requirements are challenging but not unique

<table>
<thead>
<tr>
<th>Application</th>
<th>Total Dose (rad)</th>
<th>SEU &amp; Latchup</th>
<th>Dose Rate (rad/sec)</th>
<th>Displacement Damage (equiv n/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orbiting Satellite ¹ (750 - 50,000 Km)</td>
<td>$10^3 - 10^6$</td>
<td>$&lt;10^{10}$ errors/bit/day &gt;90 MeV-cm²/mg</td>
<td>not important</td>
<td>not important</td>
</tr>
<tr>
<td>Strategic Defense ²</td>
<td>classified</td>
<td>classified</td>
<td>classified</td>
<td>classified</td>
</tr>
<tr>
<td>Nuclear Reactor and Storage ³</td>
<td>$10^4 - 10^6$</td>
<td>not important</td>
<td>$10^0 - 10^5$</td>
<td>data not available</td>
</tr>
<tr>
<td>Particle Physics ³</td>
<td>$10^4 - 10^7$</td>
<td>?</td>
<td>$10^1 - 10^2$</td>
<td>$10^{12} - 10^{13}$</td>
</tr>
</tbody>
</table>

### Key issues RAD-Hard Link Development

<table>
<thead>
<tr>
<th>Components</th>
<th>Concerns (vs radiation)</th>
<th>Technologies under Investigation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical Source</td>
<td>Threshold shift, degraded output power &amp; modulation rate</td>
<td>implanted VCSEL, oxide-aperture VCSEL, As, P, and N based</td>
</tr>
<tr>
<td>Optical Detector</td>
<td>degraded sensitivity &amp; speed, bit errors (SEU)</td>
<td>MSM photodetector, PIN photodiode</td>
</tr>
<tr>
<td>Driver &amp; Receiver Electronics</td>
<td>Vt shift, degraded transistor speed, bit errors (SEU)</td>
<td>GaAs CHFET, GaAs MESFET/HEMT, Rad-hard CMOS, Rad-hard bipolar</td>
</tr>
<tr>
<td>Optical Fiber</td>
<td>optical attenuation</td>
<td>silica and plastic fiber, rad-resistant coatings</td>
</tr>
<tr>
<td>Packaging</td>
<td>long-term stability, secondary radiation issues (Au)</td>
<td>connectors, fixturing</td>
</tr>
</tbody>
</table>

### EYE SAFETY

- VCSEL’s without a back monitor Photo diode are class 3 lasers
- Laser radiation is monochrome - it has a single color or wavelength
- A laser beam is directional it is very well collimated and will travel a long distance with very little spread
- A laser beam is coherent all the waves of light energy are in phase with each other
- To use a class 3 laser in the public domain the user/ OEM must employ either:
  - Open fibre control
  - Mechanical interlocks
Environmental Packaging Considerations

Controlled ambient temperature - 25 degrees C
Shock / Vibration ?
Rad-hard
Moisture/Humidity
Package material preferably non-magnetic and Low Mass
Components packages available:
Gold plated Covar TO46 or miniature “Pill Pack” co-axial packages- unsuitable, due to mass at the front end.
Plastic surface mount - Unsuitable at front end due to radiation damage
1X9 pin Gigabit Ethernet plastic transceiver package unsuitable at front end due to radiation.

The only package suitable to date is a ceramic tile with 4 VCSEL / PIN diode channels
Other alternatives - ceramic surface mount

Cost and Supply Considerations

LHC Data link Summary

<table>
<thead>
<tr>
<th></th>
<th>Pixel F-R</th>
<th>Pixel R-F</th>
<th>SCT F-R</th>
<th>SCT R-F</th>
<th>TRT F-R</th>
<th>TRT R-F</th>
<th>LArg F-R</th>
<th>Tiles F-R</th>
<th>Muon F-R</th>
</tr>
</thead>
<tbody>
<tr>
<td>No of Links</td>
<td>4924</td>
<td>2462</td>
<td>8176</td>
<td>4088</td>
<td>27000</td>
<td>27000</td>
<td>1620</td>
<td>256</td>
<td>640</td>
</tr>
<tr>
<td>Length</td>
<td>90m</td>
<td>90m</td>
<td>90m</td>
<td>90m</td>
<td>100m</td>
<td>100m</td>
<td>70m -- 200m</td>
<td>80m</td>
<td>TBD</td>
</tr>
<tr>
<td>Fibre</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>copper</td>
<td>copper</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Reduct</td>
<td>2462</td>
<td>nil</td>
<td>nil</td>
<td>nil</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>nil</td>
<td>nil</td>
</tr>
<tr>
<td>Data Rate</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
<td>40Mb/s</td>
<td>1.28Gb/s</td>
<td>1.28Gb/s</td>
<td>2Gb/s</td>
</tr>
<tr>
<td>Eye Rate</td>
<td>vcsel</td>
<td>vcsel</td>
<td>vcsel</td>
<td>vcsel</td>
<td>n/a</td>
<td>n/a</td>
<td>vcsel</td>
<td>vcsel</td>
<td>vcsel</td>
</tr>
<tr>
<td>Safety</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This is a summary of the LHC data link requirement as defined by Mark Pierce and John Dowell on the www.cern.ch/Atlas/GROUPS/FRONTEND/links

The requirements break down into two groups:

1. Front end (subject to radiation & severe magnetic fields)
   a. Ceramic tile V groove technology either 3 channel or 12 channel or 3/12 channel arrays of hermetic surface mount (ceramic) devices PIN diodes or VCSEL’s

2. Remote end of link, where commercially available product will satisfy the requirement.

Within these two requirements there are two data rates 40Mb/sec and 1.25Gb/sec or 1.065Gb/sec yet to be decided. Finally there are 27,000 copper links (40 Mb/sec.)
A fibre solution in place of the 27,000 copper links could be an elegant alternative if the price is right. The Atlas SCT requirement is in advance of most other applications and this will be a good trial for suggested solutions. With a lot of the lessons being learnt here, a useful objective would be the adoption of this solution if it proves itself in terms of price, functionality and reliability.

It is worth noting that these requirements will be using commercially available fibre optic components / chips. Such standard catalogue parts are always covered by a disclaimer – “the manufacturer reserves the right to make changes in order to improve the design and supply the best products possible” such changes in the “front end process” might affect the radiation immunity of the device. In order to address this issue it is important that selected devices must have a tied listing i.e. no changes can be made to the product or the process without the customers - in this case LHC project – agreement.
ELECTRONICS FOR MUON DETECTORS

C. Willmott, CIEMAT, Madrid, Spain

Abstract
The electronics systems planned for muon detectors of LHC experiments are reviewed, emphasising their special characteristics in view of the challenging operating conditions present at LHC. Different solutions adopted to face common issues are commented.

1. OVERVIEW
The task of muon detectors is to provide:
• Muon identification
• Momentum measurement
• First level trigger
• Bunch crossing identification
At first sight the solutions adopted to fulfil those tasks by the different experimental groups are very different, and somewhat arbitrary. But looking more closely one can find out that this is not the case.

Muon detectors are based in a few chamber technologies: drift tubes, resistive plate chambers and multi-wire chambers (Table 1). The choice between one technology and the other is driven by the physics requirements of each experiment, and the operating conditions like hit rates and background [1-6]. Each detector is optimised to give its best performances in the experimental framework.

Table 1: LHC detector technologies

<table>
<thead>
<tr>
<th></th>
<th>DT</th>
<th>RPC</th>
<th>MWC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALICE</td>
<td>–</td>
<td>RPC</td>
<td>CSC/CPC</td>
</tr>
<tr>
<td>ATLAS</td>
<td>MDT</td>
<td>RPC</td>
<td>TGC, CSC</td>
</tr>
<tr>
<td>CMS</td>
<td>DT</td>
<td>RPC</td>
<td>CSC</td>
</tr>
<tr>
<td>LHCb</td>
<td>–</td>
<td>MRPC</td>
<td>CPC</td>
</tr>
</tbody>
</table>

The operation under LHC condition requires high signal to noise ratio, background rejection, and high speed signal processing. Ionising radiation dose and neutron fluence in the experimental areas impose serious design constraints, not only to front-end electronics but also to equipment place in the cavern outside the detectors.

A large fraction of the electronics is planned to be installed on-chambers, not only to reduce front-end noise pick-up but also to reduce the number of cables and connections coming out of the detectors.

The foreseen operation of LHC for a 10-year period and the difficulty to access to some parts of the on-chamber electronics requires the systems to be design for minimum maintenance and repair.

In the following sections we will examine the different cases, giving a few examples. As we will see, the readout implementation depends on chamber-technology, whilst trigger implementation is more experiment oriented.

2. DRIFT TUBES
This type of chambers is the first choice for precision coordinate measurement in regions where the expected rate is low and with relatively low magnetic fields.

Table 2: LHC drift chamber main characteristics

<table>
<thead>
<tr>
<th></th>
<th>ATLAS</th>
<th>CMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Purpose</td>
<td>p, s, t</td>
<td>p, s, t</td>
</tr>
<tr>
<td>Resolution</td>
<td>80 μm</td>
<td>250/500 μm, 5ns</td>
</tr>
<tr>
<td>Drift velocity</td>
<td>30 μm/ns</td>
<td>57 μm/ns</td>
</tr>
<tr>
<td>Channels</td>
<td>372,000</td>
<td>190,000</td>
</tr>
<tr>
<td>η</td>
<td>0 – 2.7</td>
<td>0 – 1.3</td>
</tr>
<tr>
<td>Hit rates</td>
<td>200 kHz/tube</td>
<td>1-10 kHz/tube</td>
</tr>
<tr>
<td>Occupancy</td>
<td>&lt; 0.3</td>
<td>5x10-3</td>
</tr>
<tr>
<td>Data rate</td>
<td>3.2 Gb/s</td>
<td>TDC</td>
</tr>
<tr>
<td>Trigger</td>
<td>track correlation and sorting</td>
<td></td>
</tr>
</tbody>
</table>

CMS DT trigger is unique, in the sense that makes use of a long drift time detector. It provides track segments with orientation and bunch crossing association using a meantimer technique [7].

In what follows the readout systems for ATLAS and CMS are briefly described.

2.1 Drift tube readout
Fig 1 shows a block diagram of the 8-channel ASD chip been developed for ATLAS MDT. Each channel consists of a differential stage, a tail cancellation with programmable hysteresis, two discriminators, a Wilkinson ADC, output control logic, and an LVDS output driver.

The differential input provides high common mode rejection of noise pick up. The fast switching discriminator has low time walk (<500ps) required for this detector. The ADC codes the charge in the leading edge into a controlled pulse width. This time-coded charge is used off-line as correction for the time slewing and enhances significantly the leading edge spatial resolution. Finally, the output logic selects the information presented to the TDC: leading-trailing edge over low threshold, leading edge plus trailing edge
containing the charge information, and two pulses containing the charge information plus high threshold information.

![MDT ASD block diagram](image)

Figure 1: MDT ASD block diagram

The front-end chip developed for CMS is a 4-channel BICMOS ASIC with a preamplifier stage having a sensitivity of 2mV/μC and a decay constant of 50 ns. It is followed by a discriminator, which includes a latch and hysteresis network to prevent noise retriggering, and an LVDS output driver with programmable width. It also follows by a discriminator, which includes a latch and hysteresis network to prevent noise retriggering, and an LVDS output driver with programmable width. It also includes inputs for test pulses and the possibility of masking any channel.

Both detectors make use of a TDC with very similar characteristics, based on the delay lock loop (DLL) principle. Table 3 summarises MDT TDC requirements.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master gate size</td>
<td>ca. 200 kgates</td>
</tr>
<tr>
<td>Number of channels</td>
<td>24</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Time bin size</td>
<td>0.78 ns</td>
</tr>
<tr>
<td>Time resolution</td>
<td>&lt; 300 ps r.m.s.</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>17 bits</td>
</tr>
<tr>
<td>Min. input pulse width</td>
<td>10 ns</td>
</tr>
<tr>
<td>Min. time between pulses</td>
<td>10 ns</td>
</tr>
<tr>
<td>Maximum input rate</td>
<td>400 kHz</td>
</tr>
<tr>
<td>Maximum trigger rate</td>
<td>200 kHz</td>
</tr>
<tr>
<td>First-level buffer</td>
<td>128 words</td>
</tr>
<tr>
<td>Readout FIFO</td>
<td>32 words</td>
</tr>
<tr>
<td>Trigger FIFO</td>
<td>8 words</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>10 mW per channel</td>
</tr>
<tr>
<td>Signal input</td>
<td>LVDS</td>
</tr>
</tbody>
</table>

Table 3: ATLAS MDT TDC specifications

The TDC prototype used at CMS for evaluation is a highly programmable 32-channel ASIC based on the DLL principle. It has a time bin of 0.78 ns at 40 MHz, with a dynamic range of 21 bits. Each channel consists of two time registers where measurements are stored until they can be written into a common on-chip 256-word deep event buffer. With this mechanism, the two-pulse resolution is 15 ns. A trigger-matching function selects hits related to a given trigger, i.e. hits located within a time window, which is programmable to accommodate the maximum drift time. Overlapping triggers are also supported. As a hit may belong to several closely spaced triggers (it falls inside several trigger windows), a fast and efficient search mechanism, which takes this fact into consideration, has been implemented as two search pointers and two programmable pointer windows. After trigger matching, data are passed to a 32-word deep readout FIFO. In this way one event can be readout while the trigger searching is processing another. The final version being developed for CMS will have serial readout controller by one TDC programmed master.

The role of data collector is played in ATLAS MDT by the NIKHEF MDT Readout Driver (NIMROD), receiving up to 32 front-end links. It also receives and distributes TTC signals, which in CSM is performed by a dedicated control boards (CB) per chamber.

3. RESISTIVE PLATE CHAMBERS

Due to its excellent time resolution, high efficiency, and its low sensitivity to neutrons and photons, this type of chambers is well suited for fast time-space particle tracking, as required for the muon trigger at LHC experiments (Table 4). In addition, they are used in ATLAS for the second-coordinate measurement and, in LHCb, regions where particle fluxes are below 5x10^7 Hz/cm^2, as a general-purpose detector.
Table 4: Resistive plate chambers

<table>
<thead>
<tr>
<th></th>
<th>ALICE</th>
<th>ATLAS</th>
<th>CMS</th>
<th>LHCb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>RPC</td>
<td>RPC</td>
<td>RPC double-gap</td>
<td>MRPC</td>
</tr>
<tr>
<td></td>
<td>streamer</td>
<td>monogap</td>
<td>Z-strips (barrel)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N-strips</td>
<td>R-strips (end-cap)</td>
<td></td>
</tr>
<tr>
<td>Purpose</td>
<td>t</td>
<td>t ((\eta, \phi))</td>
<td>t</td>
<td>p, s, t</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 ns (jitter), 1 cm</td>
<td>3 ns, 1-4 cm</td>
<td>(~30,000)</td>
<td></td>
</tr>
<tr>
<td>Channels</td>
<td>20,000</td>
<td>430,000</td>
<td>160,000</td>
<td>(~30,000)</td>
</tr>
<tr>
<td>(\eta)</td>
<td>0 - 1.05</td>
<td>0 - 2.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Particle rate</td>
<td>10-100 Hz/cm²</td>
<td>1 kHz/cm²</td>
<td>5x10⁻³</td>
<td></td>
</tr>
<tr>
<td>occupancy</td>
<td>2x10⁻³</td>
<td>BCID</td>
<td></td>
<td></td>
</tr>
<tr>
<td>data rate</td>
<td>1.5 Gb/s</td>
<td>BCID</td>
<td>ASD, LVDS, binary</td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>BCID</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trigger</td>
<td>coincidence matrix</td>
<td>coincidence matrix</td>
<td>pattern comparator</td>
<td></td>
</tr>
</tbody>
</table>

These devices can provide resolution in the 1 ns x 1 cm range, the latter depending on the strip width.

As an example of the electronics implementation for this type of chambers a brief summary of CMS RPC detector will be given.

3.1 CMS Resistive Plate Chambers

A general layout of the RPC electronics is shown in Fig. 3. The first element of this chain is a 6-channel front-end chip (FEC) which is been developed for this detector. Each channel, consisting of an amplifier stage, matching the characteristics impedance of a strip, followed by an adjustable threshold circuit, a one-shot giving a controlled dead time, and a differential driver, according to LVDS standard. Common test input pulse and common threshold setting are provided.

Figure 3: CMS RPC electronics general layout.

A front-end board, FEB, contains 24 front-end channels (Fig. 2). It also accommodates 2 synchronisation units, SU, 2 DAC's for threshold setting, and a FEB controller, FEBC.

The SU stores FEC output data if they fall within a pre-defined time window within a bunch crossing period, and synchronises them with a selected bunch crossing period.

Data from FEB is sent to a link board, LB, for zero suppression and transmission via optical link to the trigger crates (TC) located 120 m away, in the counting house. The LB also distributes TTC signals to the FEC's.

Figure 4: CMS RPC Front-end Board.

The main functions of a trigger crate are:
- Elaborate the pattern comparator trigger algorithm, PACT, and produce a list of 4 muon candidates.
- Provide readout of the relevant RPC's.
- Provide control, programming, and calibration functions.
To fulfil these tasks one trigger crate consist of:
- 12 trigger boards, TB.
- 1 sorter board, SB.
- 1 readout board, including FED.
- 1 timing and control board
- 1 crate controller.

The pattern comparison is performed by a fully custom ASIC, PAC, matching actual RPC patterns with a set of predefined programmed patterns. The output is the muon candidate’s momentum code, plus sign and quality bits.
One PAC is connected to one strip in the reference plane and 14, 14, and 18 strips in stations 1, 3, and 4 respectively. The pre-defined patterns have to be chosen from the cone ±5, ±5, ±7, strips in stations 1, 3, and 4. Then a 3/4 algorithm is applied to select a unique candidate.

The function of the sorter board, SB, is to reduce the number of candidates coming out of a trigger crates to 4, having the highest momenta, through 4 layers of sorter chips.

The trigger boards contain:
- Demultiplexing, resynchronisation, and timing/delay circuits.
- PACT segment processor servicing 12 trigger elements.
- The layer of sorter/ghost buster circuits.
- Control and monitoring.

The readout board provides the standard CMS interface (DDU) to the front end driver (FED) the data acquisition module of the CMS DAQ.

4. MULTI-WIRE CHAMBERS

Multi-wire chambers appear to be one of the most versatile devices. Their capabilities range from precision coordinate measurement, high efficiency, fast time response, under very stringent operating condition of high background and high and non-uniform magnetic field.

Table 5 summarises the main characteristics of LHC multi-wire detectors.

As an example of this type of detectors we will present the main characteristics of the ATLAS Thin Gap Chambers.

<table>
<thead>
<tr>
<th>Type</th>
<th>ALICE</th>
<th>ATLAS</th>
<th>ATLAS</th>
<th>CMS</th>
<th>LHCb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Purpose</td>
<td>CSP/CPC</td>
<td>CSC</td>
<td>TGC</td>
<td>CSC</td>
<td>CPC</td>
</tr>
<tr>
<td>Channels</td>
<td>60 μm, 5 mm</td>
<td>67,000</td>
<td>440,000</td>
<td>273,000 strips</td>
<td>75-150 μm, 2-6ns</td>
</tr>
<tr>
<td>η</td>
<td>2 - 2.7</td>
<td>1.05 - 2.4</td>
<td>0.9 - 2.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Particle rate</td>
<td>&lt; 5 kHz/cm²</td>
<td>&lt; 20 kHz/cm²</td>
<td>100 kHz/channel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data rate</td>
<td>5.2 Gb/s</td>
<td>240 Mb/s</td>
<td>150 Mb/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>charge interpolation</td>
<td>coincidence matrix</td>
<td>pattern search</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trigger</td>
<td>-</td>
<td>-</td>
<td>coincidence matrix</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

4.1 Thin Gap Chambers

TGC is a special class of multi-wire chambers in which the anode-to-anode distance is larger than the cathode-to-anode distance.

The font-end is a 4-channel ASD chip with the particular characteristics that this circuit can be used for both, wire and strip signals by setting an appropriate threshold level. The outputs are LVDS standard.

Four ASD chips are mounted in an ASD Board, which also receives the threshold voltage, analog test-pulse, and ±3 V power from the Patch Panel.

The Patch Panel (Fig. 5) receives signals from wire-groups and strip signals from the ASD Boards, performs bunch-crossing identification and treats the physical overlap of TGC by OR’ing the appropriate signals. It also distributes TTC and control signals, as well as DC power to the Slave Boards, and provides interface between the Detector Control System and the trigger electronics. Four Slave Boards are attached to the side of each Patch Panel.

There are four types of Slave Boards: two for triplets and two for doublets. They receive bunch-crossing-id assigned wire and strip signals from the Patch Panel and perform coincidence operations on the input signals to produce low-µt signals (doublet SB) or hits (triplet SB).
Signals from the Slave Boards are sent to the High-p_T Board where high-p_T trigger signals are formed. The High-p_T Boards performs coincidences, in a 256x288 two-fold coincidence matrix, of the input signals and then merges the high-p_T output with the low-p_T signals, giving priority to the high-p_T signals. The coincidence matrix can produce up to 8 track candidates, which are reduced to a maximum of four by the Track Selector, and sent to the Sector Logic in USA15 via optical fiber.

The Sector Logic Board contains a track selector, which selects the two highest-p_T tracks in each sector. The Sector Logic consists of r-θ coincidences matrices, a Track-Preselector, and a Track Selector.

A coincidence matrix element receives δR (Low/High) and δθ (Low/High) information and outputs six levels of p_T; three ranges for each Low- and High-p_T. The Preselector selects the two highest-p_T tracks per pivot TGC and the Selector the two highest-p_T tracks among the inputs. Position information and p_T value are sent to the Muon Central Trigger Processor Interface (MUCTPI).

All chamber hits and intermediate trigger logic results are read out for each trigger. For readout, the Slave Boards are grouped into Local Data Blocks (LDB). Each LDB is comprised of a Star Switch near the detector that routes data from a number of Slave or High-p_T Boards, via an optical link to an intelligent I/O port (Local DAQ Master) in the ROD crate in USA15.

Figure 6: ATLAS TGC Slave Board

5. POWER SUPPLIES

The main issue comes from the stray magnetic field present in the caverns for normal operation of commercial devices. Radiation doses may affect the reliable operation of power supplies and regulators, and calls for a careful design to minimise the risk of undesired over-voltages. Table 6 shows the required LV power for on-chamber electronics for some of the muon detectors.

The solutions adopted to supply and distribute the required power to the on-chamber electronics are as many as the number of detectors.

Table 6: On-chamber power dissipation.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ATLAS MDT</td>
<td>15 kW</td>
</tr>
<tr>
<td>CMS DT</td>
<td>15 kW</td>
</tr>
<tr>
<td>ATLAS RPC</td>
<td>19 kW</td>
</tr>
<tr>
<td>CMS CSC</td>
<td>80 kW</td>
</tr>
<tr>
<td>ATLAS TGC</td>
<td>45 kW</td>
</tr>
</tbody>
</table>

In general LV power supplies will be placed in racks around the detector, either in regions where the magnetic field is sufficiently low for the normal operation of commercial devices, or with the appropriate magnetic shielding (CMS DT and CMS RPC). In the case of CMS CSC the LVPS will be located at 60 m from the detector, on the hall balconies, and will provide a primary ~70 V LV power. Then, Vicor DC-to-DC converters will deliver the required 5 and 3.3 volts, housed in soft iron box mounted on the outer edge of the endcap.

In several cases the on-chamber boards will contain low-drop linear voltage regulators to the working voltages (ATLAS MDT, CMS RPC). Monitoring and ON/OFF switching will be implemented in almost all cases.

For the HV distribution the solutions adopted have similar characteristics. The main frames will be placed in racks (in the cavern or in the control room) and distributed via coaxial cables to the chamber. Monitoring and ON/OFF switching is foreseen.

Acknowledgements

I would like to thank all the people from the different experiments who helped me to find the material to prepare this paper.

REFERENCES

7. M Degiorgi, et al., Local track reconstruction for the First Level Trigger in the CMS Barrel Chambers. This proceedings.
8. F. Gonella, et al., A prototype frontend ASIC for the drift tubes of CMS Barrel Muon Detector. This proceedings.
10. T.Y. Ling, Front-end electronics of the CMS Endcap Muon System. This proceedings.
RADIATION TOLERANT ELECTRONICS
Final Acceptance of the DMILL Technology Stabilized at TEMIC/MHS.


Abstract

DMILL technology integrates mixed analog-digital very rad-hard (>10 Mrad and >10^14 neutron/cm^2) vertical bipolar, 0.8µm CMOS and 1.2 µm PJFET transistors on SOI substrate. In this paper, after recalling the DMILL program goal, we summarize the main milestones from the R&D to the industrial implementation, the main technological choices, and the main results obtained after stabilization of the final process-flow at MHS.

I. Goal of the DMILL program

The goal of the DMILL program is to provide the High Energy Physics (HEP) community, space industry, nuclear industry, and other applications, with an industrial very rad-hard mixed analog-digital microelectronics technology.

II. Main milestones from the R&D to the industry

The DMILL microelectronics technology was developed by the CEA (French Atomic Energy Agency) with the collaboration of IN2P3 (French Nuclear Physics and Particle Physics Institute) between 1990 and 1995 [1-10]. DMILL was presented to the CERN DRDC (Detector R&D Committee, the former LHC Electronics Board) in 1992, and was accepted by this Committee with two requests : 1/ open an access to DMILL for the HEP community as soon as possible, and 2/ transfer DMILL to the industry. Between 1993 and 1996, the CEA processed 7 DMILL « multi-project wafers » (MPW) batches open to all the laboratories participating in the LHC program, so that they could thus start the development of numerous circuits dedicated to ATLAS and CMS. In mid 1995, the DMILL process was stabilized at LETI (the CEA R&D laboratory, in Grenoble, France). In September 1995, the CEA and MHS signed a contract for the industrial transfer and fabrication of DMILL in the 6'' silicon foundry of MHS at Nantes. MHS, which is part of the TEMIC group, was initially held by Lagardère (France) and Daimler-Benz (Germany), and was purchased at the beginning of 1998 in totality by the US semiconductor manufacturer ATMEL. TEMIC/MHS is now the main center of expertise for ATMEL defence and space technologies. In spring 1997, DMILL was stabilized at 95% at the Nantes production plant [11-15] and MHS decided to open this technology to HEP laboratories so that they could continue and complete the development of their circuits before mass production. The last 5% of corrections were made during the period spring 97 - spring 98, leading to the final process-flow.

In spring 1998, MHS processed several batches using the final process-flow. Series of thorough characterizations made in summer 1998 by the CEA and MHS on these batches give fully satisfactory results. The compilation of the extensive measurements made on these batches together with those made on all the previous batches (43 DMILL batches were processed by MHS between spring 96 and summer 98) shows that all the parameters of DMILL technology stabilized at MHS now completely fulfil the specifications based on LHC requirements and previously obtained at LETI. These excellent results enabled the CEA to announce the official final acceptance of the industrial transfer of DMILL to MHS during the LEB 98 Workshop.

III. Recall of the technological choices

DMILL uses an SOI substrate which significantly reduces the sensitivity of the circuits to transient irradiation effects such as parasitic currents or memory cell upsets [17-19] induced by the passage of single ionizing particles.

The DMILL CMOS transistors are separated by a dielectric trench and by the buried oxide; this dielectric
insulation definitively eliminates any possibility of latch-up (triggering of a parasitic thyristor structure constituted by the juxtaposition of two complementary MOS transistors); this phenomenon, initiated in standard technologies by the passage of single ionizing particles, results in circuit malfunctions and, in some cases, in their definitive destruction.

The 0.8-µm CMOS and the vertical bipolar transistor of DMILL provide the advantages of present BiCMOS technologies. The PJFET transistor is used for a number of low-noise or low-temperature applications. The CMOS structure was designed to obtain very high hardness to total ionizing dose (> 10 Mrad) and a low noise level. This type of transistor, which uses majority carriers, is naturally hardened to neutrons. The bipolar transistor uses a vertical structure which provides both high neutron hardness (> 1E14 n/cm2) and high speed operation. Its structure was also carefully optimized to obtain high hardness to ionizing radiation (> 10 Mrad).

The PJFET transistor, which uses majority carriers and whose intrinsic operation does not involve oxides, has low sensitivity to ionizing radiations and to neutrons. Its structure was optimized to obtain an extremely high hardness to these radiation types (>> 10 Mrad and > 1E14 n/cm2).

For analog applications, DMILL integrates two capacitor and two resistor families, both radiation hardened.

DMILL also integrates rad-hard anti-ESD devices, specifically designed for protection of either analog or digital circuits.

The interconnections can be made with two metal layers whose minimum dimensions are those of a 0.6-µm technology, and with a low resistivity polysilicon layer.

The design rules for the components and their interconnections were optimized to obtain a high integration density, which is comparable to that of present 0.8-µm non rad-hard pure-CMOS technologies.

IV. Final acceptance of the industrial transfer

By mid 1997, the industrial transfer was completed and the process-flow was stabilized at 95%. The last corrections made between mid-97 and mid-98 to obtain the final process-flow are:

- Adjustment of the value of the high value resistor « RSRHV »;
- Addition of a new rad-hard high value resistor « Rext » (improved radiation hardness);
- Corrections to the bipolar transistor (improvement of the radiation hardness and of Vearly);
- Elimination of yield problems (which were due to polysilicon residues);
- Improvement of the final DMILL Design Kit.

The final acceptance of the industrial transfer is the last step foreseen in the contract signed by the CEA and MHS in 1995. This final acceptance is based on the results of extensive measurements made of several batches manufactured with the final process-flow, and on all the measurements made of all the previous MHS batches. The criterion used to analyse these results is the technical specification file, based on the complete set of measurements made on DMILL technology stabilized at LETI. The measurements and checking required to decide the final acceptance of the transfer are distributed in the 11 following steps:

1. Statistical Process Control (SPC);
2. Electrical parameters;
3. Radiation hardness;
4. Transistors and OTAs noise (pre-rad and post-rad);
5. Characterization and yield of demonstrator circuit;
6. Characterization of anti-ESD devices;
7. Electromigration tests;
8. Hot carriers ageing tests;
9. Oxide breakdown tests;
10. Approval of the final process-flow;
11. Approval of the final design kit.

In the following, all these measurements or checking steps are briefly described and the main results are summarized:

   SPC enables the verification and control of the critical technological parameters which govern the electrical, noise and radiation hardness characteristics. More than 120 parameters are measured during and after processing for each batch. All the SPC parameters obtained for batches made using the final process-flow are fully within the specifications.

2. Electrical parameters.
   More than 90 electrical parameters are measured on several sites on each wafer, in each batch. All the parameters obtained for batches made using the final process-flow comply with the specifications. Figures 1 and 2 give an illustration of the stability of these parameters for successive batches, after initial adjustments made on the first batches.

![Fig. 1: NMOS Vt(V) versus batch number.](image-url)
LSL and USL are respectively the Lower Specified Limit and the Upper Specified Limit.

3. Radiation hardness.

The most sensitive static parameters of each active and passive device are measured before and after irradiation (10 Mrad, 1E14 n/cm2); values of the most significant of these for several batches are shown in figures 3 to 8 (arbitrary batch numbers are used in the X-axis).

For the bipolar transistor, to ensure that the final gain after 10 Mrad + 1E14 n/cm2 is sufficiently high, the specific minimum gain after 10 Mrad and before neutron irradiation is LSL@10Mrad = 70 (IC = 10 µA). The left side of figure 6 corresponds to non optimized bipolar: the initial post-rad and pre-rad gains were below the specified values, respectively LSL@0rad and LSL@10Mrad. After several experiments, the difference between LETI and MHS equipment responsible for these insufficient gains was ascertained and the subsequent corrections gave the required pre-rad and post-rad gain, as shown in the right side of Fig.6 (final process-flow).

The new high value resistor Rext, which was made available to users in Summer 1998, was also measured before and after 10 Mrad. This resistor has a high radiation hardness: δRext/Rext = +6.5% after 10 Mrad.

It is not possible to describe all the results obtained in radiation hardness tests in this paper. To summarize, here again all the values of the radiation hardness parameters measured on batches made using the final process-flow are within the specification limits.
4-a. Individual transistors noise.
Input noise spectral density is measured before and after irradiation on each type of transistor for various sizes and various biasing conditions [14]. Figures 9 to 16 show the pre-rad and post-rad noise spectral density (nV/Hz) versus Frequency (Hz) measured on the 4 types of DMILL transistors. The dotted lines correspond to the worst cases obtained with the stabilized DMILL-LETI process. The noise spectral density measured on batches made with the stabilized DMILL-MHS process-flow is consistent with that measured on batches issued from the stabilized DMILL-LETI process.

4-b. Operational Transimpedance Amplifiers noise.
ENC is measured on several OTAs designed with various input transistors (NMOS, PMOS, NPN and PJFET). Results obtained for batches from the final DMILL-MHS process-flow are fully consistent with those obtained for DMILL-LETI batches and with individual transistors noise measurements.

5. Characterization and yield of demonstrator circuits.
The goal of this step is to validate the technology by electrical characterization and yield measurement on a
circuit as representative as possible of mixed analog-digital circuits developed for LHC applications. The demonstrator circuit DEMDSM (49,000 transistors, 28 mm²) [14] used for this validation is constructed around a high dynamic range switched capacitor analog memory HPSALM initially developed for ATLAS calorimetry. Some extra-logic has been added to make it self-testable. Table I shows that the main characteristics of this circuit, manufactured using the final DMILL-MHS process-flow, are very similar to those obtained for the reference circuit made in 1995 using the DMILL-LETI stabilized process-flow. The typical yield obtained with this circuit manufactured with the final DMILL-MHS process-flow is about 60%.

<table>
<thead>
<tr>
<th>Technology</th>
<th>DMILL-LETI</th>
<th>DMILL-MHS</th>
<th>DMILL-MHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total dose</td>
<td>0 rad</td>
<td>0 rad</td>
<td>10 Mrad</td>
</tr>
<tr>
<td>Max. Freq.</td>
<td>65 MHz</td>
<td>60 MHz</td>
<td>55 MHz</td>
</tr>
<tr>
<td>Consumption</td>
<td>460 mW</td>
<td>420 mW</td>
<td>310 mW</td>
</tr>
<tr>
<td>Droop rate</td>
<td>20 mV/s</td>
<td>40 mV/s</td>
<td>260 mV/s</td>
</tr>
</tbody>
</table>

Table I.

6. Anti-ESD (ElectroStatic Discharges) devices.
Three families of rad-hard anti-ESD devices are available in DMILL: one for digital input, one for digital output, and one for analog input. Measurements based on the Human Body Model (HBM) show that these devices efficiently protect input or output pads up to 4000V.

7. Electromigration tests.
The goal of these tests is to assess the reliability of metal interconnections stressed by high current density. Their results are in conformity with MHS standards.

8. Hot carriers ageing tests.
The goal of these tests is to measure accelerated ageing of CMOS devices. Their results are in conformity with MHS standards.

9. Oxide breakdown tests.
The goal of these tests is to assess the reliability of CMOS gate oxide under a high electrical field. Their results are in conformity with MHS standards.

10. Approval of the final process-flow.
The DMILL-MHS process-flow is an exact copy of the initial DMILL-LETI process-flow, except for a few adaptations made to take into account certain specific features of the equipment used by MHS. These adaptations were studied by MHS in collaboration with the LETI in order to preserve the structure and properties of all the DMILL components. After an in-depth analysis of the final DMILL-MHS process-flow, the LETI found it to be in conformity with the initial DMILL-LETI process-flow and has approved it.

11. Approval of the final design kit.
A new revision of the DMILL design kit (DDK) was completed by the CEA and MHS in summer 1998. It includes the following improvements:

- $R_{\text{ext}}$: simulation parameters;
- Extraction tools for $R_{\text{ext}}$;
- Simulation parameters of the new NPN;
- Extraction of buried oxide (BOX) capacitances;
- Simulation of parasitic BOX capacitive couplings;
- Guidelines for reducing the effects of these capacitive couplings;
- Device matching parameters.

Table 2 gives an excerpt of the matching parameters which illustrates the very good matching of the new $R_{\text{ext}}$. NPN and CMOS also exhibits good matching parameters. The values of sigma for the CMOS transistors are refered to transistors designed with a gate width $W = 1$ µm and a gate length $L = 1$ µm, and scale as $(WL)^{-1/2}$.

<table>
<thead>
<tr>
<th>Device</th>
<th>Dose</th>
<th>Parameter</th>
<th>unit</th>
<th>sigma</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{ext}}$</td>
<td>0 rad</td>
<td>resistance</td>
<td>%</td>
<td>0.24</td>
</tr>
<tr>
<td>$R_{\text{ext}}$</td>
<td>10 Mrad</td>
<td>resistance</td>
<td>%</td>
<td>0.22</td>
</tr>
<tr>
<td>NPN</td>
<td>0 rad</td>
<td>gain</td>
<td>%</td>
<td>4.0</td>
</tr>
<tr>
<td>NPN</td>
<td>1.2x10</td>
<td>Vbe</td>
<td>mV</td>
<td>0.21</td>
</tr>
<tr>
<td>NMOS</td>
<td>0 rad</td>
<td>$V_t$</td>
<td>mV*µm</td>
<td>14.3</td>
</tr>
<tr>
<td>PMOS</td>
<td>0 rad</td>
<td>$V_t$</td>
<td>mV*µm</td>
<td>23.3</td>
</tr>
</tbody>
</table>

Table 2.

This new DDK is available immediately at MHS and will be available on CD-ROM via IMEC in November.

V. Qualification and Quality Assurance

An initial qualification of DMILL technology was made by MHS in October 1997 [16]. To take into account the corrections made in the process from mid-1997 to mid-1998, an additional qualification was carried out by MHS in June 1998. DMILL is today a fully qualified MHS process.

The quality assurance performed by MHS for DMILL includes three procedures [14]:

1. The standard quality assurance procedures applied to each DMILL batch. These procedures are mainly based on the Statistical Process Control (SPC) tools, on the Process Traceability tools, and on the Control of Process Changes rules. These tools and rules are common to all MHS technologies.
2. The radiation hardness monitoring was specifically studied \[13, 14\] and developed by the CEA for DMILL, and transferred to MHS. This monitoring consists in ionizing radiation and measurements made of test structures up to 10 Mrads using a 10-keV RX ARACOR irradiation machine, and in neutron radiation-hardness tests made on test structures through electrical measurements. These tests made on each batch enable MHS to guarantee that each delivered wafer has a radiation hardness of 10 Mrad and 1E14 n/cm².

3. The noise monitoring was also specifically studied and developed by the CEA for DMILL and transferred to MHS. This monitoring consists in noise spectral measurements made before irradiation and after 10 Mrads on elementary test structures for various sizes and various biasing conditions \[14\]. These measurements made on three batches per year enable MHS to maintain the noise characteristics within the specified limits.

VI. Summary

The DMILL rad-hard mixed analog-digital technology was developed between 1990 and 1995 by CEA with the collaboration of IN2P3, and transferred to TEMIC/MHS from 1996 to mid-1998. After stabilization of the process, series of thorough measurements made by the CEA and MHS show that all the parameters of DMILL stabilized at MHS completely fulfil the specifications. The compilation of these results together with those obtained for all the previous DMILL-MHS batches have enabled the CEA to certify officially the final acceptance of the industrial transfer and stabilization of DMILL at MHS.

DMILL is now a qualified process, manufactured and commercialized by MHS with a quality assurance, including radiation hardness and noise monitoring, which completely fulfils LHC requirements.

Numerous circuit developed since 1993 for the LHC by several laboratories with DMILL-LETI and then DMILL-MHS, give very satisfactory results which demonstrate the good adaptation of this technology to LHC applications \[20-45\]. Various circuits are also under development for the space, nuclear civilian industry, and other applications.

VIII. Acknowledgments

We wish to thank all the laboratories of the HEP community which have contributed to the development of this technology by their circuit developments, by the studies they have made of this technology, and by their very useful technical discussion and suggestions.

We especially wish to thank the CERN for the development of the first DMILL digital library.

We also are very grateful to the following for the valuable assistance they provided in carrying out the DMILL-LETI MPWs in 1996:

- IN2P3-CNRS (France);
- University of Pavia (Italy);
- CERN (Switzerland);
- University of Basel (Switzerland);
- Paul Scherrer Institut - PSI (Switzerland).

IX. References


Pixel Readout Electronics in Honeywell SOI CMOS

W. Karpinski, K. Lübelsmeyer, G. Pierschel
I. Physikalisches Institut RWTH Aachen, 52056 Aachen, Germany

Abstract

Our aim is to design radiation-hard front-end electronics for pixel detectors at the Large Hadron Collider. The anticipated high radiation and collision rate environment at LHC places demanding requirements on the technology used. The circuits have to operate close to the beamline for several years without serious degradation of their parameters. The expected total radiation doses are up to 100 Mrad Gamma and 10^{15} equivalent n/cm². We have investigated the suitability of the technology used. The circuits have to operate close to the beamline for several years without serious degradation of their parameters. The expected total radiation doses are up to 100 Mrad Gamma and 10^{15} equivalent n/cm². We have investigated the suitability of this technology before and after irradiation with gammas from Co^{60} for a total dose of 55 Mrad. All devices remained fully functional after irradiation, with no anomalous behaviour.

We have implemented in this technology the front-end readout system for a 22x32 pixel detector array with square pixels of (125 µm)^2. The architecture is identical with the PSI31 chip fabricated in DMILL technology [1].

1. TECHNOLOGICAL ASPECTS

Honeywell has developed 0.65 µm_{eff}, 0.55 µm_{eff} and 0.28 µm_{eff} SOI CMOS technologies called RICMOS IV for radiation hard applications. The 0.65 µm_{eff} process has been optimized for designs operating up to 5 V whereas the 0.55 µm_{eff} process supports low voltage operation up to 3.3 V. The 0.28 µm_{eff} is a brand new development and will not be discussed in this paper. In the technology investigated the transistors are fabricated on full dose SIMOX wafers. The BOX thickness and Epitaxial thickness amount to 370 nm and 230 nm respectively. A schematic diagram of an inverter designed in this technology is shown in Fig. 1. N and P wells are implanted to create a partially depleted polysilicon gate surface channel for NMOS and a buried channel for PMOS. The structure of N and P transistors are identical; they differ only in doping profiles. To eliminate latch-up the N and P transistors are fully isolated using BOX and CVD oxide refilled shallow trenches, which are self-aligned to the active areas and the transistor body. The active area is surrounded by body-tie which prevents the transistor from the kink effect and floating body effects. Improved LDD engineering has also been implemented in order to reduce the lateral drain electric field and to prevent the parasitic bipolar transistor from conducting. The drain and source nodes extend down to BOX to reduce the parasitic capacitance on these nodes. To further reduce the parasitic capacitance on the drain the walled drain option can be used. The body contact can be entirely integrated in the source contact without the need for any additional area. These features increase the density of the circuits. The most significant advantage of the technology over other radiation-hard technologies is the availability of standard 3-layer metal or optional 4-layer metal for interconnections.

For analogue design RICMOS IV offers different passive elements:
- low value resistors with the sheet resistivity of 2.5Ω/sq., 30Ω/sq. and 100Ω/sq.
- high value resistors where the sheet resistivity can be chosen between 1000Ω/sq. and 5400Ω/sq.
- linear capacitors with good voltage coefficient and a high capacitance of 2fF/µm²
- metal fuses for redundancy repair

2. PRODUCTION OF CHIPS

We have submitted two designs in this technology:
- a test chip containing all important building blocks of the pixel detector readout, various transistors and preamplifiers for noise studies and irradiation tests, as well as comparators to study the matching of the transistors before and after irradiation.
We produced the chips in enhanced technology in an engineering run (10 wafers). The runtime was about 16 weeks. The chips were delivered by mid August and they have been under test since then.

3. RADIATION HARDNESS STUDIES

3.1 Irradiation Procedure

To investigate the radiation hardness of SOI technology a Co$^{60}$ source with 1.1 MeV and 1.3 MeV photons was used. We performed two irradiations:

- In '97 several transistors from process monitor bars have been irradiated with different dose rates to obtain total doses of 22Mrad, 40Mrad and 55Mrad. The irradiation was carried out within 99 hours for all transistors simultaneously. (Irradiation tests below 20Mrad were performed by the manufacturer Honeywell [2]). The results of the irradiation showed that the radiation hardness of PMOS should be improved. Honeywell has realised such an improvement.
- In September '98 we irradiated transistors from the latest wafer run, carried out in the enhanced technology. Using again different dose rates over a period of 33 hours. We have obtained total doses of 10Mrad and 20Mrad.

Irradiation to higher doses will be continued. During the irradiation all devices were packed in an aluminium box in an argon atmosphere to avoid chemical reactions with the surfaces by aggressive gases like O$_2$. We irradiated the devices under analogue and digital biasing. In the analogue case the transistors were connected in diode configuration with the drain current density of 300µA/mm. For digital biasing we used the most unfavourable operating conditions: on-gate for n-type devices and off-gate for p-type devices.

3.2 Front Channel Threshold Shift

In Figs. 2 and 3 we have plotted the shift of the front channel threshold voltage as a function of the irradiation dose for PMOS and NMOS respectively. In '97 the transistors were measured directly after irradiation and after 2 months. At that time we observed a large increase of the threshold voltage for PMOS by about 550 mV. Now, for the enhanced technology the threshold voltage increases only by 115mV and 160 mV after 10Mrad and 20Mrad respectively. This shows that the technology has been improved.

For NMOS the shift is even smaller, -30mV, (-60mV) after 10Mrad, (20Mrad). In '97 we observed a positive

- a readout chip for a pixel detector array consisting of 22 x 32 cells.

We produced the chips in enhanced technology in an engineering run (10 wafers). The runtime was about 16 weeks. The chips were delivered by mid August and they have been under test since then.

In production '98 we irradiated transistors from the latest wafer run, carried out in the enhanced technology. Using again different dose rates over a period of 33 hours. We have obtained total doses of 10Mrad and 20Mrad.

Irradiation to higher doses will be continued. During the irradiation all devices were packed in an aluminium box in an argon atmosphere to avoid chemical reactions with the surfaces by aggressive gases like O$_2$. We irradiated the devices under analogue and digital biasing. In the analogue case the transistors were connected in diode configuration with the drain current density of 300µA/mm. For digital biasing we used the most unfavourable operating conditions: on-gate for n-type devices and off-gate for p-type devices.

3.2 Front Channel Threshold Shift

In Figs. 2 and 3 we have plotted the shift of the front channel threshold voltage as a function of the irradiation dose for PMOS and NMOS respectively. In '97 the transistors were measured directly after irradiation and after 2 months. At that time we observed a large increase of the threshold voltage for PMOS by about 550 mV. Now, for the enhanced technology the threshold voltage increases only by 115mV and 160 mV after 10Mrad and 20Mrad respectively. This shows that the technology has been improved.

For NMOS the shift is even smaller, -30mV, (-60mV) after 10Mrad, (20Mrad). In '97 we observed a positive

a readout chip for a pixel detector array consisting of 22 x 32 cells.

We produced the chips in enhanced technology in an engineering run (10 wafers). The runtime was about 16 weeks. The chips were delivered by mid August and they have been under test since then.
threshold voltage shift after irradiation. The discrepancy can be explained with postirradiation effects, namely annealing effects occurring within the 99 hours of the irradiation period. This tendency is also confirmed by the measurements which took place two months later, where the maximum threshold shift amounted to 130mV.

3.3 Back Channel Threshold Shift

Figs. 4 and 5 illustrate the back channel threshold voltage shift for PMOS and NMOS transistors as a function of total irradiation dose. We irradiated the devices with the back gate connected to 0V and to -4V. For PMOS in the new technology the threshold voltage decreases by about 5V independent of biasing during the irradiation. For the old technology the changes were negligible even when irradiated up to 55Mrad so that for PMOS devices this parameter is not critical.

For NMOS the back channel threshold decreases from 25V to about 17V after 10Mrad and 20Mrad, when irradiated with the back gate connected to 0V, but the changes are negligible when irradiated with the back gate connected to -4V. In '97 we observed a large decrease of the back channel threshold voltage to about 7V but even for the highest radiation dose, the back channel threshold is sufficiently high to prevent the transistor from malfunction. For all devices and for all irradiation doses we did not observe irradiation induced leakage current.

3.3 Change of the Transconductance

From the DC measurements we have extracted the transconductance $g_{m}$. Figs. 6 and 7 show the change of the transconductance for PMOS and NMOS transistors measured at the drain current density of 1mA/mm and drain voltage $V_{ds}=-1V$ (PMOS) and $V_{ds}=1V$ (NMOS).

For the enhanced PMOS $g_{m}$ decreases by 6% only after 10Mrad and 20Mrad. The NMOS transistor is more sensitive to gamma irradiation, its transconductance decreases by 16%.

3.4 Noise Behaviour

Fig. 8 shows the ENC measurements for PMOS with a gate width of 1500µm biased with the drain current of 500µA and loaded with the total input capacitance of 10pF. The open circles show the ENC before irradiation, the full circles the ENC after 10Mrad gamma irradiation and the full squares the ENC after 20Mrad gamma irradiation. We observe only a small degradation of the noise behaviour. Fits to the measurements show that the white serial noise increases by about 10% and that the serial 1/f noise contribution is not significant in the interesting range of peaking time (20ns ÷ 50ns). The total ENC increases by 10% at peaking time of 25ns.
In Figs. 9 we have plotted the ENC measurements before and after irradiation for a NMOS with the same gate width of 1500µm and for the same biasing and total input capacitance. The degradation of the noise behaviour is higher. The values of the power densities of each noise source extracted from a fit show that after the total dose of 20Mrad the white serial noise increases by a factor of 1.4 and the 1/f noise increases by a factor of 3. However, the total noise increases by 30% at a peaking time of 25ns. We also observe that there is no significant difference in noise behaviour and in the DC characteristics after 10Mrads and 20Mrad. It seems that radiation induced changes saturate at the latest after 10Mrad.

4. PIXEL READOUT ARCHITECTURE

Fig. 11 shows schematically the architecture of the chip we have translated from DMILL to the RICMOS IV process. The chip consists of 704 pixel cells organized in 11 double columns with 32 pixels in each column. The pixels have a 125µm x 125µm square shape. At the bottom of the chip the double column periphery and time stamps and buffers are located. The overall dimensions of the chip are 5mm by 3mm.

The main purpose of the chip is to implement and test the complete analogue block. The readout logic has a reduced circuit architecture and will be changed for the next generation of chips.

The main features of the architecture are:
- Each pixel is able to detect a hit and to store analogue and digital information.
- The pixels are organized in independent double columns. Information from the pixel cells is transmitted along a double column to logic at the end of the double column.
- The double column periphery allows simultaneous readout and data taking by reading out only column pairs having at least one pixel hit.

The block diagram of the pixel unit cell is plotted in Fig. 12. Each pixel cell contains a preamplifier, shaper, comparator, flag register and shift register controlling the readout. The gain of the preamplifier as well as the time constant of the shaper is controlled by the feedback resistors. The shaper output is connected to a capacitance, which acts as an analogue store, and to the input of a comparator. The threshold of a the comparator is controlled by the 3 bit DAC to accommodate variations of the parameters of the transistors.

The double column periphery is equipped with control logic, which recognizes a hit in a pixel, a twelve-bit buffer for time stamping, and readout logic controlling the data transfer from pixels to the periphery.

5. PHYSICAL IMPLEMENTATION

Fig. 13 shows the layout of the pixel cell in RICMOS IV. The bump bonding pad is the most sensitive part of the pixel electronics since it is on the input of the preamplifier. It is placed asymmetrically in the pixel cell to reduce cross talk from the digital readout lines to the input of the preamplifier. The digital lines are placed in between pixel cells. The third metal layer is used to shield the pixel detector against transients on long digital lines, while the second layer is mainly used for power distribution. The active area consumption in RICMOS IV is 30% lower than in DMILL.
Examples of the layout of the double column logic are presented in Fig. 14. Although the circuit is identical in both cases, the active area used to implement it is a factor of 2 higher in DMILL than in RICMOS IV. Another advantage is due to the availability of three metalization layers. We can completely abandon long polysilicon lines and improve the power distribution.

6. FIRST RESULTS
At the time of the workshop we have performed only some preliminary tests on pixel readout electronics. Fig. 15 shows the pulse at the shaper output for 6250 e⁻ injected to the pixel. The peaking time is less than 22ns for a power dissipation of 35µW. The picture is taken with a picoprobe attached to the shaper output which represents an additional capacitance of 25pF. The gain amounts to 3.9mV/100e⁻.

Fig. 16 shows a threshold scan. Here we have plotted the detection efficiency as a function of the charge injected into the pixel. The slope of the curve is proportional to the noise. The typical noise is 70e⁻ (without detector at the input) for a threshold of about 1400e⁻.

7. CONCLUSION
The threshold voltage and transconductance of the RICMOS IV transistors show low degradation and no increase of leakage current after irradiation with a total dose of 55Mrad (photons from Co⁶⁰).

The noise degradation after 20Mrad is low. It increases by 10% for PMOS and by 30% for NMOS. This demonstrates that the technology is fully suitable for electronics to be used in the LHC environment. The high transistor density and the availability of four metal layers are very advantageous because of better power distribution, lower area consumption, and better shielding of the pixel detector against transients on the digital lines of readout electronics.

8. ACKNOWLEDGEMENTS
We are indebted to Tim Bradow, William Larson and Mike Liu from Honeywell for their excellent support and fruitful discussions. We wish to thank Dr. Henschel from the Fraunhofer Institut für Naturwissenschaftlich-Technische Trend-Analysen for allowing us the use of the Co⁶⁰ source and for his help in carrying out the irradiation.

9. REFERENCES
Radiation hardness. This process has been used to prototype APV chips for microstrip readout in the CMS tracker. Detailed measurements are presented of transistor leakage, transconductance, threshold voltage and noise, and their dependence on dose, for devices from four different processing runs. High temperature annealing studies have been performed to accelerate long-term changes after irradiation. Progress has been made in understanding the radiation tolerance behaviour of the APV6 and subsequent processing runs.

1. INTRODUCTION

The LHC environment will place stringent requirements on electronics used in the inner microstrip tracker regions where ionising doses of up to 10 Mrads will be encountered over the lifetime of the experiments. Low noise and power consumption together with high speed and timing resolution must be maintained. The CMS collaboration has adopted a readout system based around the APV chip series, the first fully functional prototype of which (the APV6 [1]) was fabricated in the Harris process. A previous iteration of the chip (the APV5) has been shown to perform adequately up to 15 Mrad dose levels [2] and more general studies of transistors [3] have demonstrated good performance after 100 Mrad doses.

The first radiation tolerance study of the APV6 [4] exposed some unexpected behaviour with respect to radiation tolerance, where the speed at which the chips could be clocked, the noise and the gain were all significantly degraded after a dose of 3 Mrads. Irradiation studies subsequently performed on Process Control Monitor (PCM) test structures, containing transistors representative of those used in the APV6, gave results consistent with the performance exhibited by the chip.

The APV5 chip was fabricated in the Harris Research Triangle Park (RTP) foundry whereas the APV6 was fabricated after the process had moved to a new foundry in Melbourne, Florida. Assuming that changes in the radiation behaviour have resulted from moving the process it has obviously been of interest to us to study devices fabricated after the move. Two subsequent processing runs at the Melbourne foundry have included PCM test structures, one for MX chips and an additional APV6 run. We have therefore been able to study and compare the individual device radiation hardness on identical devices from different runs.

In this paper we report results from detailed studies of transistor radiation hardness from three Melbourne processing runs, and we have included measurements on identical devices from the APV5 RTP run for comparison. Transistor characteristics, threshold voltages and noise behaviour have been studied and annealing effects have been investigated.

2. EXPERIMENTAL PROGRAMME

The PCM test structure chip contains a number of transistors of varying geometries as well as other structures useful for monitoring process dependent parameters. The test structure is repeated five times at different sites on the 4 inch wafer. In this study we have concentrated on the four transistors listed in table 1.

<table>
<thead>
<tr>
<th>Polarity</th>
<th>Aspect ratio W/L [microns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>2000/1.4</td>
</tr>
<tr>
<td>NMOS</td>
<td>2000/1.2</td>
</tr>
</tbody>
</table>

The 2000 µm wide devices were laid out in the low noise configuration used for amplifier input devices and are thus suitable for measuring noise performance. The 10/10 devices were included to identify any characteristics arising from short channel effects.

Figure 1 shows the circuit used for measuring \( I_{DS} \) dependence on \( V_{GS} \) for NMOS device (polarities reversed for PMOS).

Table 1. Transistors included in this study
source, and the voltage source used for $V_{GS}$ were under computer control, allowing automation of the measurement procedure. Measurements were made under the following bias conditions:

<table>
<thead>
<tr>
<th>VDS</th>
<th>1 Volt</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGS</td>
<td>swept from sub-threshold to strong inversion</td>
</tr>
<tr>
<td>VBS</td>
<td>fixed values of 0 and 2 Volts</td>
</tr>
</tbody>
</table>

Transconductance ($g_m$) dependence on $I_{DS}$ was computed from the $I_{DS}$ vs. $V_{GS}$ characteristics and threshold voltages were extracted from plots of $V_{IDS}$ against $V_{GS}$.

The gate referred noise spectral density for the 2000 $\mu$m wide transistors was measured between 10 kHz and 10 MHz under bias conditions of $|I_{DS}| = 500\mu$A and $|V_{DS}| = 1$ Volt, which are similar to those in the APV6 chip. The PMOS device closely resembles that used for the preamplifier input. The noise measurement system has been previously described [5].

Irradiations were carried out using the Brunel $^{60}$Co source using a silicon photodiode for dosimetry, calibrated using a Farmer air ionisation chamber at a distance of 1 m from the compact cylindrical source. We estimate the accuracy of our dosimetry to be ±10% but relative (device to device) variations should be very small since all devices were mounted in a circular jig with the source located at the centre. Irradiations were performed under bias and devices were kept under bias (as much as possible) between irradiations and afterwards. Irradiations and measurements were performed at room temperature. A dose rate of approximately 30 krads was used which is much higher than that to be found at the LHC where long term annealing over the 10 year lifetime of the experiments is likely to occur. To accelerate these long term changes a high temperature annealing step was performed at the end of the irradiation cycle. Devices were held under bias at 100°C for 7 days.

Four PCMs from each of the APV5 (RTP), APV6 and MX (Melbourne) runs were bonded in 40-pin DIL packages for ease of handling and measurement. Two PCMs/run were irradiated in steps to 3 Mrads and then annealed, the other two in coarser steps to 10 Mrads before annealing. We were particularly interested to study differences between the APV6 and MX runs since changes were made to the processing run to adjust the PMOS threshold voltage between these two. Subsequent to the MX run a further APV6 run was processed and two PCMs from this run have also been studied, though not in so much detail (fewer irradiation steps and no annealing) as the earlier APV6 and MX runs since it was not thought likely that this run would differ significantly from the MX run. This run is referred to here as the APV6c run ('c' here stands for corrected).

### 3. EXPERIMENTAL RESULTS

The detailed nature of this study has yielded a substantial volume of data. For clarity, therefore, we have selected representative data which demonstrate the differences between the processing runs. It was found that the behaviour of the 10/10 devices in table 1 did not differ qualitatively from that of the 2000 $\mu$m wide devices. Although there are some quantitative differences, they are not significant enough to make any difference to the conclusions drawn from the results and hence, for brevity, the results for the 2000 $\mu$m wide devices only are presented.

#### 3.1 Transfer characteristics

Figures 2 and 3 show the dependence of $|I_{DS}|$ on $V_{GS}$ for the widest PMOS and NMOS transistors respectively. A common artefact is apparent where as $V_{GS}$ increases towards threshold the leakage current dips sharply and then begins to rise. This leakage is attributed to the bulk and is observed because we are measuring the current in the source (see figure 1), hence both bulk and drain (or gate) - source leakage currents are summed. Since the bulk-source junction is reverse biased its leakage current would be opposite in polarity to drain-source leakage. The current dip is therefore explained by the current passing through zero as the channel begins to form.

The results in figures 2 and 3 show clear differences between the APV5 and subsequent APV6, MX and APV6c runs. The most obvious effect for the PMOS devices is a more significant shift in the negative direction along the $V_{GS}$ axis. The NMOS devices also show a clear change of sub-threshold current slope after irradiation which is indicative of increasing trapped charge at the gate oxide - silicon interface [6].

#### Table 2. PMOS 2000/1.4 $g_m$ reductions after irradiation, expressed as percentages of pre-irradiation values

<table>
<thead>
<tr>
<th>run</th>
<th>3 Mrads</th>
<th>3 Mrads + anneal</th>
<th>10 Mrads</th>
<th>10 Mrads + anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>APV5</td>
<td>-5</td>
<td>-5</td>
<td>-5</td>
<td>-5</td>
</tr>
<tr>
<td>APV6</td>
<td>-10</td>
<td>-7</td>
<td>-20</td>
<td>-10</td>
</tr>
<tr>
<td>MX</td>
<td>-10</td>
<td>-5</td>
<td>-17</td>
<td>-10</td>
</tr>
<tr>
<td>APV6c</td>
<td>-5</td>
<td>-10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table 3. NMOS 2000/1.2 $g_m$ reductions after irradiation, expressed as percentages of pre-irradiation values

<table>
<thead>
<tr>
<th>run</th>
<th>3 Mrads</th>
<th>3 Mrads + anneal</th>
<th>10 Mrads</th>
<th>10 Mrads + anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>APV5</td>
<td>-16</td>
<td>-15</td>
<td>-19</td>
<td>-</td>
</tr>
<tr>
<td>APV6</td>
<td>-30</td>
<td>-24</td>
<td>-47</td>
<td>-</td>
</tr>
<tr>
<td>MX</td>
<td>-30</td>
<td>-22</td>
<td>-48</td>
<td>-36</td>
</tr>
<tr>
<td>APV6c</td>
<td>-14</td>
<td>-54</td>
<td>-34</td>
<td>-</td>
</tr>
</tbody>
</table>

Tables 2 and 3 show the transconductance $g_m$ (determined at $|I_{DS}|=500\mu$A) dependence on dose for the PMOS 2000/1.4 and NMOS 2000/1.2 devices respectively. The data are expressed as percentages of the pre-irradiation value to indicate relative changes after irradiation. For the PMOS devices in table 2 the APV6 and MX runs show a reduction in $g_m$ of approximately 20% after 10 Mrads,
compared with less than 5% for the APV5 run device. The APV6c run shows better performance than the APV6 and MX runs with a reduction of 10%. Annealing after 10 Mrads has no significant effect on the APV5 run device but a greater beneficial effect on the APV6 and MX run devices, where about half the loss of $g_m$ prior to anneal is recovered.

The NMOS device $g_m$ dependence on dose in table 3 shows a substantial reduction in $g_m$ of almost 50% after 10 Mrads for the APV6 and MX run devices compared with 20% for the APV5 run device and about 35% for the APV6c run device. The APV5 and MX run devices were improperly biased during annealing and so these results are missing. Examining the data for the NMOS 10/10 devices shows no significant annealing for the APV5 run and similar behaviour to the MX run for the APV6 run device.

3.2 Threshold voltages

Figures 4 and 5 show the threshold voltage dependence on dose, for all the 2000 μm wide PMOS and NMOS devices included in this study. The results after annealing, where available, are indicated offset to the right for clarity in the figure but have not actually received a dose beyond 3 or 10 Mrads. Threshold voltages were determined here by extrapolating the linear part of the $\frac{V_{IDS}}{V_{GS}}$ vs $V_{GS}$ characteristics.
characteristic back to the intercept on the $V_{GS}$ axis. For the APV5 run after 10 Mrads threshold shifts of about 100mV and 200mV are apparent for the PMOS and NMOS devices respectively, most of the shifts occurring before the first Mrad. The APV6 and MX run devices show much greater shifts of up to 600 mV after 10 Mrads, which build up gradually with dose. For the NMOS devices the initial shifts with dose are negative but rebound occurs leading to an overall positive shift after 10 Mrads. This threshold voltage behaviour, like the subthreshold current slope behaviour in section 3.1, is indicative of a build up of interface trapped charge. The APV6c run devices show a negative shift of 200 mV after 10 Mrads for PMOS and a positive shift (after rebound) of 50 mV for NMOS.

The annealing results for the PMOS devices in figure 4 show some recovery for the devices irradiated to 10 Mrads, particularly for the APV6 run devices, and no evidence of reverse annealing. The annealing results after 10 Mrads are missing for the NMOS devices in figure 5, but examination of the results for the 10/10 devices shows no significant recovery for the APV5 run devices and results very similar to the MX run for the APV6 run devices, where a small recovery is apparent.

### 3.3 Noise spectral measurements

Figure 6 shows the noise spectral density measurements for representative 2000/1.4 PMOS devices from all runs. The devices were biased to achieve $I_{DS}=$-500µA for $V_{DS}=$-1V and $V_{BS}=$2V which is close to the conditions of operation for the APV6 preamplifier input device. The APV5 run device shows no significant degradation in
4. CONCLUSIONS

We have made a comparative study on a range of transistors included as test structures fabricated on the same wafers as APV5, APV6 (first run), MX and APV6c (second APV6 run) chips. A significant difference is noticeable between the APV5 run which was fabricated in the Harris Research Triangle Park (RTP) foundry and the subsequent runs after the process moved to the Melbourne foundry. After irradiation to doses up to 10 Mrads we have noted greater reduction in transconductance (tables 2 and 3), larger threshold voltage shifts (figures 4 and 5) and increased device noise (figure 6). Transfer characteristics (figures 2 and 3) and threshold voltage behaviour show evidence of a build up of trapped charge at the gate oxide - silicon interface. There are some differences between the Melbourne processing runs, most noticeably for the second APV6 run which showed performance much closer to the very good radiation tolerance exhibited by the RTP process. Some beneficial annealing has been observed using a high temperature annealing step.

Changes to the radiation behaviour of the process after 10 Mrads are of sufficient magnitude to cause concern regarding the performance of front end readout chips for the CMS tracker after this dose. Nevertheless results presented here indicate that the damage builds up gradually with dose and therefore acceptable performance may still be achieved at lower doses, such as are encountered in the outer tracking layers. Variations from run to run indicate the necessity of continued monitoring of the radiation behaviour of future runs.

ACKNOWLEDGEMENTS

We would like to acknowledge technical support at Imperial College, Brunel University and the Rutherford Appleton Laboratory. Particular thanks are due to John Reilly and Sarah Greenwood at IC, to George Ritter at Brunel, and to Jeff Bizzell at RAL. We would also like to thank the UK Particle Physics and Astronomy Research Council (PPARC) for supporting this work.

REFERENCES

[2] Results of irradiating the APV5 chip, M.Raymond and M.Millmore, CMS NOTE/1996-009
Comparative Study of Radiation Hardness of Optoelectronic Components for the CMS Tracker Optical Links

K. Gill\(^1\), C. Aguilar\(^1\), V. Arbet-Engels\(^1\), C. Azevedo\(^1\), J. Batten\(^2\), G. Cervelli\(^2\), R. Grabit\(^1\), F. Jensen\(^1\), C. Mommaert\(^1\), J. Troska\(^2\) and F. Vasey\(^1\).

1) CERN, CH-1211, Genève 23, Switzerland.
2) High Energy Physics Group, Imperial College, London SW7 2BZ, UK.

Abstract

Commercially available semiconductor lasers and p-i-n photodiodes from several different manufacturers have been irradiated with 6MeV neutrons to fluences up to \(10^{15}\)n/cm\(^2\). A comparison of the radiation damage in the lasers is made in terms of the threshold current increase and efficiency loss. In the irradiated p-i-n photodiodes, the damage to leakage current and responsivity is compared. The laser damage was similar overall after normalising the changes with respect to the pre-irradiation values. The p-i-n photodiodes had similar leakage current increases overall. The detectors that were front-illuminated are more radiation resistant than the back-illuminated devices in terms of the photocurrent damage.

I. INTRODUCTION

Optical links will be used extensively in experiments at the Large Hadron Collider (LHC) due to their advantages of large bandwidth, low power requirements, compactness and noise immunity in comparison to copper cables. An analogue optical link system is being developed\(^{[1]}\) at CERN for readout of the Compact Muon Solenoid (CMS) tracking detectors, in addition to a digital link system for transmission of timing, trigger and control signals. Approximately 50000 analogue and roughly 1000 digital fibre channels will be required in total.

By using components already available in the telecommunications market, special custom development can be avoided and the large number of optical links can be constructed on a limited budget. However, all the candidate components have to be tested for sufficient radiation hardness as the radiation environment in the CMS tracker will be severe: total particle fluences over the first 10 year running period will be up to \(-10^{14}\)neutrons/cm\(^2\)(\(-1\)MeV), \(1.6\times10^{14}\)charged hadrons/cm\(^2\)(mainly charged pions, \(-10^{-4}MeV\)), in addition to an ionising dose of up to 70kGy\(^{[2]}\).

For the analogue readout links, and the digital links carrying signals from the tracker, the laser transmitters, optical fibres and connectors will be exposed to high radiation fluences. In the digital links, sending timing and control signals to the tracker, p-i-n photodiode receivers will also be placed in the radiation field. We have already extensively tested\(^{[3]}\) NEC lasers and Epitaxx p-i-n diodes packaged by Italtel\(^{[4]}\) and are confident that these particular components are sufficiently radiation resistant for use inside the CMS tracker. For the fluence/dose levels of interest, ionising damage (from \(^{60}\)Co gamma rays) was determined to be insignificant compared to the effects of displacement damage from 6MeV neutrons, 300MeV pions and 24GeV protons, whose relative damage ratios have been determined\(^{[3]}\). In this study we aim to determine if the levels of 6MeV neutron damage are similar in candidate CMS optical link components from a range of manufacturers.

II. EXPERIMENT

Lasers from 6 manufacturers were tested as well as p-i-n photodiodes from 6 manufacturers. All the components are potentially suitable, in terms of performance and packaging, for use in the CMS tracker optical links. The type and number of each device is summarised in Table 1. All the devices are based on commercially available components, some obtained directly from the manufacturer and others, such as the NEC and Mitsubishi laser die, and the back-illuminated Epitaxx p-i-n photodiodes were supplied in packages by Italtel.

Table 1: Lasers and p-i-n photodiodes irradiated in this study which includes three separate neutron irradiation tests (A, B and C).

<table>
<thead>
<tr>
<th>Laser Manufacturer</th>
<th>NEC (Italtel)</th>
<th>Alcatel</th>
<th>Lucent</th>
<th>Nortel</th>
<th>Mitsubishi (Italtel)</th>
<th>Optobahn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>1310nm, multi-quantum-well, edge-ermitter</td>
<td>8-way</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die</td>
<td>1-way</td>
<td>1-way</td>
<td>1-way</td>
<td>1-way</td>
<td>1-way</td>
<td>1-way</td>
</tr>
<tr>
<td>Package</td>
<td>custom</td>
<td>TO-can</td>
<td>mini-DIL</td>
<td>TO-can</td>
<td>40-pin, chip, 8-way, MPO socket</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4-way DIL, SM fibre ribbon</td>
<td>SM-fibre pigtail</td>
<td>SM-fibre pigtail</td>
<td>SM fibre</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. irradiated</td>
<td>(Test)</td>
<td>(B)</td>
<td>(A)</td>
<td>(B)</td>
<td>(A)</td>
<td>(B)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P-i-n Manufacturer</th>
<th>Alcatel</th>
<th>Nortel</th>
<th>Epitaxx</th>
<th>Firmaconics</th>
<th>Lucent</th>
<th>Epitaxx (Italtel)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>InGaAs/InP planar p-i-n structure</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>p-i-n diameter</td>
<td>n/a</td>
<td>n/a</td>
<td>75μm</td>
<td>80μm</td>
<td>75μm</td>
<td></td>
</tr>
<tr>
<td>Orientation</td>
<td>Front-illuminated</td>
<td>Back-illuminated</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>TO-can, SM fibre</td>
<td>ceramic submount, SM fibre</td>
<td>mini-DIL SM fibre</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. irradiated</td>
<td>(Test)</td>
<td>(A)</td>
<td>(A)</td>
<td>2 (A)</td>
<td>2 (B)</td>
<td>2 (A)</td>
</tr>
</tbody>
</table>

Irradiation was carried out at the SARA neutron irradiation facility\(^{[5]}\). Neutrons with a mean energy of 6MeV are produced by bombarding a beryllium target with a 18MeV deuteron beam. As shown in Table 2, particle fluxes of up to
The light-power versus current (L-I) and voltage versus current at 30-40 minute intervals during irradiation. The threshold current and slope-efficiency were determined by fitting a linear line to the linear region of the L-I characteristic. For the MBI devices, that were packaged in TO-cans without fibre pigtails, ~150V. The photocurrent was measured by monitoring the p-i-n photodiodes at -5V in the idle state. The laser was driven at 1310nm laser situated outside the irradiation zone.

Test A was split into 3 irradiation steps (see Table 2). During these periods some annealing occurred (~14-23% after the first step and 11-17% after the second step). The discontinuities in the data for devices in Test A are due to the gaps between the three separate annealing steps (see Table 2). The devices were annealed in the dark for 30-40 minute intervals during irradiation. The threshold current was determined from the position of the photocurrent and slope-efficiency were determined by fitting a line to the linear region of the L-I characteristic.

Relative threshold increase \( \Delta \text{I}_{\text{th}}(\Phi)/\text{I}_{\text{th}}(0) \)

Across the range of manufacturers, the damage effects are be similar overall to within a factor 2. For the smallest relative increase, the NEC and Lucent lasers have the smallest relative increase and the Optobahn devices have the largest relative increase. The output efficiency is also less than 60% for 4 channels of the Optobahn lasers. This allows us to make a comparison of the efficiency for 4 channels of the Optobahn lasers.

镍的输出效率也低于60%。这使得4通道的Optobahn激光器的效率低于60%。
better comparisons of devices irradiated under different conditions.

The increase in laser threshold and the efficiency loss are both consistent with the effects of displacement damage, normally explained in terms of the recombination lifetimes of injected charge carriers. Radiation damage causes the carrier lifetime associated with non-radiative recombination at defects to eventually decrease to a level similar to the lifetime associated with spontaneous recombination[6]. The resulting competition between these two processes causes the increase of the threshold current. Above threshold however, the stimulated recombination lifetime is much shorter than the lifetime associated with non-radiative recombination at defects and the laser efficiency is less affected by displacement damage (at least until high fluences are reached $10^{14-15}$n/cm$^2$).

The increase in laser threshold and the efficiency loss are both consistent with the expected build-up of radiation induced defects in the bulk leading to the generation of dark current and the trapping/recombination of signal charge[7,8]. Both of these effects are consistent with the effects of displacement damage, as very little annealing occurred after irradiation, the results can therefore be compared directly in terms of the damage after a given neutron fluence.

Fig. 3 shows the leakage current damage (at 5V reverse bias) in all the irradiated devices. The radiation induced leakage current increases to more than 6 orders of magnitude greater than typical pre-irradiation values of ~10pA at -5V and, overall, the increases are similar for all the different devices.

The effect of neutron damage on the p-i-n responsivity is illustrated in Fig. 4, showing the photocurrent at -5V bias for a ~200μW d.c. optical signal, normalised to the pre-irradiation value. The pre-irradiation responsivity was typically 0.9A/W for all the devices. Three distinct types of radiation damage effect occurred: (i) a rapid decrease in response after a certain fluence (Epitaxx/Italtel and Lucent, both back-illuminated),

B) P-i-n photodiodes

The damage effects observed in the p-i-n photodiodes included a large increase in leakage current and a decrease in the responsivity. These effects are both consistent with the expected build-up of radiation induced defects in the bulk leading to the generation of dark current and the trapping/recombination of signal charge[7,8]. Both of these damage effects were generally non-linear with increasing fluence.

**Fig. 2:** Comparison of output efficiency degradation during 6MeV neutron irradiation in lasers from several manufacturers.

**Fig. 3:** Comparison of p-i-n leakage current increases during 6MeV neutron irradiation in devices from several manufacturers.
(ii) a more linear and smaller decrease (Epitaxx TO and Alcatel, both front-illuminated) and (iii) a mixture of both degradation and recovery during irradiation (Nortel and Fermionics, both front-illuminated).

Fig. 4: Decrease in normalised photocurrent at -5V for 200µW optical signal during 6MeV neutron irradiation

Although the mechanisms of the different damage kinetics are not yet understood, it is clear that the front-illuminated devices appear to be more radiation resistant than the back-illuminated devices in terms of the responsivity change. In the case of the two types of Epitaxx devices tested, the p-i-n structures are identical except for the direction of the incident light. The reason for the difference in the radiation damage could be due, for instance, to the effects of introducing mainly acceptor-type defects into the InGaAs layer. After a sufficiently high fluence the low level of initial n-type doping in the InGaAs layer would become fully compensated by the negatively charged defects, which are then expected to be effective trapping centers for signal induced holes. Due to the short optical absorption length of InGaAs at 1.3µm, this situation would be more damaging in back-illuminated p-i-n diodes than in front-illuminated devices because signal induced holes must travel a greater distance through the InGaAs layer in a back-illuminated detector.

IV. SUMMARY

We have found that a variety of commercial 1310nm lasers and InGaAs p-i-n photodiodes should meet the stringent radiation hardness requirements for operation in the CMS tracker over a 10 year period.

The damage effects in the irradiated lasers were relatively similar overall; e.g. after 4x10^{14}n/cm^2 (approximately the highest fluence common to all the types of devices tested), the threshold current increase was 100-200%, relative to the initial value, and the output efficiency was degraded by between 10% and 25%. The p-i-n photodiode leakage current damage was also similar across the range of devices, with ~10µA leakage at -5V after 10^{15}n/cm^2. For neutron fluences in excess of ~2x10^{14}n/cm^2, the front-illuminated p-i-n photodiodes were more radiation resistant, in terms of photocurrent damage, with only 10-35% signal loss after 10^{15}n/cm^2, compared to 60-90% degradation in the back-illuminated devices.

V. ACKNOWLEDGMENTS

The authors would like to thank Bernard Cornet and Loic Baumard for preparing test equipment and Philippe Martin and his colleagues at ISN Grenoble for the neutron dosimetry measurements.

VI. REFERENCES


[4] Photonics Unit, Italtel, 20019 Settimo Milanese, Italy.


RADIATION HARDNESS OF AVALANCHE PHOTODIODES USING CALIFORNIUM-252

Y. Musienko, S. Reucroft, D. Ruuska, and J. Swain
Department of Physics, Northeastern University, Boston, Mass. 02115
and
A. Heering and R. Rusack
Department of Physics, University of Minnesota, Minneapolis, Minn. 55454

Abstract

We describe the use of $^{252}$Cf at Oak Ridge National Laboratory as a neutron irradiation source to test electronics for radiation hardness. We discuss the advantages it provides over reactors and pulsed spallation sources. Some results of radiation hardness tests of avalanche photodiodes using $^{252}$Cf are described.

1 IRRADIATION TESTS REQUIRED FOR AVALANCHE PHOTODIODES AT CMS

The avalanche photodiode (APD) has been chosen as the baseline photodetector for the electromagnetic calorimeter (ECAL) of the Compact Muon Solenoid (CMS) Detector at the Large Hadron Collider (LHC) at CERN in Geneva, Switzerland. The ECAL consists of some 60,000 lead tungstate (PbWO$_4$) crystals, each to be read out by a pair of APD's. Among the reasons for choosing APD's are their insensitivity to high magnetic fields, high quantum efficiency and weak response to charged minimum ionizing particle interactions, otherwise known as the nuclear counter effect. APD's are more resistant to radiation than p-i-n photodiodes and possess an internal gain mechanism. However, like the p-i-n photodiode, the APD does exhibit some degradation of its working parameters as a function of integrated fluence, especially for high hadron fluxes.

At the CMS experiment the ECAL barrel region neutron flux is expected to be $2 \times 10^{12}$ neutrons/cm$^2$/year [1]. Such a high neutron flux will certainly damage the APD structure. As a consequence, a decrease of quantum efficiency is expected as well as increased leakage current. An extensive series of studies of APD resistance to neutron radiation has been carried out by different groups participating in the CMS collaboration. These studies have been performed utilizing different neutron, or equivalent, sources [1]: reactors (Rome, Saclay); a spallation neutron source (RAL); a $^{252}$Cf source (NU); and a proton beam (PSI).

Here we present the results of a recent study of three different APD's and 1 p-i-n photodiode performed by Northeastern University using $^{252}$Cf as a neutron source at Oak Ridge National Laboratory (ORNL) [2].

2 PROPERTIES OF CALIFORNIUM-252 AS A NEUTRON SOURCE

$^{252}$Cf's prolific, isotropic neutron emission rate of $2.34 \times 10^{12}$ neutrons/mg/s is the property that makes it particularly attractive for our purposes. The neutron energy spectrum of $^{252}$Cf has been accurately measured by different groups over a wide range of energies (0.01-30 MeV) [3, 4, 5]. It has been shown to be fitted well with the Watt spectrum model [6]:

$$N(E) = \frac{1}{2\sqrt{\pi} E_w} \left[ \exp \left( -\frac{(\sqrt{E} - \sqrt{E_w})^2}{T} \right) \right. $$

$$- \left. \exp \left( -\frac{(\sqrt{E} + \sqrt{E_w})^2}{T} \right) \right]$$

plotted in figure 1, with $N(E)dE$ the fraction of neutrons in energy range between $E$ and $E + dE$, and the neutron energy, $E$, is given in MeV. The parameters $T$ and $E_w$ are fitted to $T = 1.175 \pm 0.005$ MeV and $E_w = 0.359 \pm 0.009$ MeV.

Important features of this distribution are a peak at approximately 0.7 - 0.8 MeV, close to the most probable energy of neutrons (1 MeV) in the barrel ECAL region of CMS experiment [1], with an average neutron energy ($E$) of around 2.35 MeV. There are energetic neutrons up to approximately 20 MeV, the upper bound for fission product energy from $^{252}$Cf but after 10 MeV or so the fraction of the total becomes insignificant. The half-life of $^{252}$Cf is $2.646 \pm 0.004$ years [7].

![Figure 1: Neutron emission energy spectrum of californium-252.](image-url)
In order to correctly compare the damage caused by different particles having different energies, the Non Ionising Energy Loss (NIEL) of each must be considered [8]. Figure 2 shows the "Energy Dependent Displacement Damage Function" (also called the "KERMA" function), which represents relative damage caused by neutrons in silicon as dependent on their energy [9]. Neutrons with energies below 100 keV produce significantly less damage than that produced by neutrons with energies > 200 keV. Convolution of the KERMA function with the neutron energy spectrum (equation 2) normalised to damage caused by 1 MeV neutrons gives the relative damage caused by $^{252}$Cf neutrons in comparison to 1 MeV neutrons:

$$K^{(252\text{Cf})} = \int_{0}^{\infty} \frac{D(E)}{D(1\text{MeV})} N(E) dE$$

(2)

where $N(E)$ is the neutron energy distribution function plotted in figure 1. Such normalization, here to 1 MeV neutrons, is used to compare silicon damage caused by neutrons with different spectral energy distributions of these sources are known. Taking into account that

$$D(1\text{MeV}) = 95 \pm 4 \text{MeV} \cdot \text{mb}$$

(3)

and calculating the integral in equation 2 we find $K^{(252\text{Cf})} = 1.06$. This means that an integrated $^{252}\text{Cf}$ spectrum causes 1.06 times the damage produced by the same number of 1 MeV mono-energetic neutrons. The KERMA calculations agree to within 10% with direct measurements based on foil dosimetry.

The Radiochemical Engineering Development Center at ORNL is the single production source for $^{252}\text{Cf}$ in the United States and one of only two in the world. To produce this isotope, $^{244}\text{Cm}$ targets (curium oxide) are placed in the High Flux Isotope Reactor at ORNL where they are irradiated for about a year. While in the reactor, they undergo many successive neutron capture/β-decay processes to get to the desired mass and atomic number. The targets are removed and the $^{252}\text{Cf}$ is chemically separated and purified, in a different hot cell environment, from the other transplutonium elements formed. The $^{252}\text{Cf}$ as a powdered oxide is then weighed and welded inside a double stainless steel housing. The total annual yield is 400-500 mg of $^{252}\text{Cf}$ per 90-110 g of target material, and is available for sale at US$56/µg. [10]

The ORNL facilities are ideal for our purposes since the APD's can be placed under bias and monitored, the temperature can be controlled and monitored, and both the neutron flux density and irradiation times can be precisely and accurately adjusted.

Once source delivery has taken place in the hot cell, the only access to the experiment is via remote manipulator arms, or 'waldos'. These waldos are used to place the sources into the desired position and configuration. The hot cell is a 1 inch thick welded stainless steel inner enclosure approximately 20 feet × 30 feet × 30 feet high surrounded by 6 foot thick concrete walls. Visual inspection of the apparatus takes place via a 6 foot thick "fish tank" window of lead glass and water mounted in the concrete wall. The data acquisition, power supplies, and other equipment are located outside the hot-cell, in front of one of these windows.

### 3 EXPERIMENTAL IRRADIATION SETUP

Our experimental setup at ORNL consisted of groups of two APD's placed in a light-tight, aluminum test chamber. The chamber served a number of functions with regard to controlling the APD environment. Constant temperature water pumped through the copper block on which the APD's are mounted provides a means of temperature control. We utilized a Luda constant temperature, recirculating water chiller/pump with a large reservoir.

The APD's could be precisely located with respect to the sources. Provisions were made to monitor the temperature of the APD's with platinum resistive temperature measuring devices (RTD’s).

Moderation of the neutron energy spectrum to bring the average energy down to that expected in the CMS ECAL environment was done using a 1/2 inch thick entrance window of 0.6% carbon filled, high-density polyethylene. The moderation process always produces a thermal neutron component (neutron energies below 1 eV) which we absorb by placing 1 mm of cadmium after the polyethylene, followed by a 1 mm thick lead sheet to stop any recoil γ rays associated with the thermal neutron absorption. Cadmium has a neutron capture cross section of at least $2 \times 10^3$ barns up to 0.2 eV and at least ten barns up to 1 eV. We exclude the possibility of a thermal neutron albedo from the walls of the hot-cell by fabricating an inner enclosure of 1 mm thick cadmium to surround the entire APD volume of the test chamber. Previous exposure dosimetry results indicate that there were no thermal neutrons present in this region, and consequently all of the effects described for these devices were exclusively the result of fast neutrons.

Figure 2: Energy dependent displacement damage (KERMA) function.
The data acquisition system consisted of a 486 PC with software written specifically for the neutron irradiation tests. This was interfaced to a Keithley 485 picoammeter through a Keithley 7001 switching system with a Keithley 7158 ten channel low current scanner card. Communication was via an IEEE-488 GPIB interface. The bias voltage was provided by LeCroy HV supplies in a PC-controlled crate. The software allowed us to monitor the bulk and surface currents where applicable, and temperature for each device. A Caddock high precision, low temperature coefficient 1.0M Ω resistor in the APD circuit provided current limiting protection. We used a feedback loop which read out the voltage drop across this resistor in order to keep a constant bias voltage across each APD corresponding to a gain of 50.

4 AVALANCHE PHOTODIODES STUDIED

Three different types of APD and one p-i-n diode were irradiated in 1997. These APD’s were produced by Hamamatsu and EG&G in the context of the CMS crystal readout photodetector R&D program.

One APD was from Hamamatsu with a p++-p+-n+-n++ structure, produced by epitaxial growth on a low resistivity silicon substrate. The light entry surface of this APD is coated with a thin SiO₂ anti-reflective layer and protected with 0.5 mm of transparent silicone rubber. The package is ceramic with two pins (cathode and anode). This Hamamatsu device has a circular sensitive area 5 mm in diameter and a fully depleted region only 25-30 μm thick.

The two APD’s from EG&G utilized a p++-p+-n+-π-n++ structure produced by ion implantation and diffusion processes on high resistivity (>3 kΩ-cm) thick (196 and 243 μm) silicon. These APD’s are coated with a thin, (10-60 nm) Si₃N₄ anti-reflective layer to enhance the sensitivity of these devices to 450-550 nm light. They are packaged in a ceramic case with 3 pins (cathode, anode and guard ring). The EG&G APD’s have a square 5 by 5 mm sensitive area and depletion regions nearly equal to the thickness of their substrate wafers.

The main junctions of both types of structures are located 4-5 μm from the light entry surface. This junction depth was chosen to optimize the APD’s behavior for such parameters as the excess noise factor, nuclear counter effect response and radiation resistance.

The Hamamatsu p-i-n photodiode was a 200 μm thick, type S3590-01 commercial device. The square 1 cm × 1 cm sensitive area of this diode is protected with transparent epoxy and housed in a ceramic package with two contacts.

Sketches (not to scale) of the structures of both devices are shown in figure 3. A schematic representation of the electric field profile as a function of distance x corresponding to going left-to-right in figure 3 for each is shown in figure 4. The two different EG&G diodes have fields that differ by a stretch along the x-axis.
5 SOME RESULTS ON APD'S

While a full description of the results of the irradiation would require more space than is available here, we present some representative results in this section and refer the interested reader to reference [11] for more details.

Figures 5 and 6 illustrate that one can perform measurements during irradiation as well as "before and after". Tables 1 and 2 show device characteristics before and after irradiation, making it clear that despite damage to APD's after a neutron fluence equivalent to that expected from 10 years of CMS running, the APD's still function as photon detectors. Results on newer APD's are the subject of a paper in preparation [12].

<table>
<thead>
<tr>
<th>Diode</th>
<th>Bias at Gain 50 [V]</th>
<th>$I_{bulk}$ [nA]</th>
<th>Q.E. at 480 nm [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC-16</td>
<td>183.5</td>
<td>6</td>
<td>53</td>
</tr>
<tr>
<td>EG&amp;G-15</td>
<td>365</td>
<td>9.2</td>
<td>78</td>
</tr>
<tr>
<td>EG&amp;G-3</td>
<td>420</td>
<td>16.2</td>
<td>83</td>
</tr>
<tr>
<td>S3590-01</td>
<td>40($M=1$)</td>
<td>0.6</td>
<td>65</td>
</tr>
</tbody>
</table>

Table 1: Parameters of APD's and p-i-n photodiode (last line) measured at 20 C before irradiation.

<table>
<thead>
<tr>
<th>Diode</th>
<th>Bias at Gain 50 [V]</th>
<th>$I_{bulk}$ [nA]</th>
<th>Q.E. at 480 nm [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC-16</td>
<td>183.5</td>
<td>13</td>
<td>51</td>
</tr>
<tr>
<td>EG&amp;G-15</td>
<td>374</td>
<td>30</td>
<td>78</td>
</tr>
<tr>
<td>EG&amp;G-3</td>
<td>450</td>
<td>39</td>
<td>83</td>
</tr>
<tr>
<td>S3590-01</td>
<td>5($M=1$)</td>
<td>13</td>
<td>63</td>
</tr>
</tbody>
</table>

Table 2: Parameters of APD's and p-i-n photodiode (last line) measured at 20 C after irradiation. APD's received $2.33 \times 10^{13}$ n/cm², while the p-i-n photodiode received $2.17 \times 10^{13}$ n/cm².

6 CONCLUSIONS

$^{252}$Cf is a powerful tool for radiation hardness studies, with a spectrum of neutrons very similar to that expected at the back of the CMS ECAL. The spectrum can be modified with various materials, or the effect of another desired spectrum modelled using KERMA functions. Advantages over reactors as neutron sources include the ease with which devices to be irradiated can be biased and held at constant temperature in a dry environment. The simplicity of long irradiations which approximate better the expected exposure at hadron colliders over many years makes $^{252}$Cf an attractive alternative to proton beams and pulsed spallation neutron sources.

An irradiation carried out at ORNL of APD's for the CMS ECAL readout demonstrates the practicality of using this isotope for radiation hardness studies.

7 ACKNOWLEDGEMENTS

We would like to thank the following people for their assistance in this project:

From Northeastern: Steve DiCaccio and Keith Flynn of the Physics Department machine shop for helping get the mechanical portion of these experiments out the door on time. Matt Marcus, an undergraduate who made cables, built circuits, helped drive the truck and generally helped make it all work.

From ORNL: Chuck Alexander for his keen interest and depth of knowledge in things nuclear. Robert McMahon, Ed Smith and Gary Owen for providing source handling expertise and helping provide means to solve the thousand little things that always still need to be done, and always with a welcome sense of friendliness and humour.

We also thank the National Science Foundation and the United States Department of Energy for their support.

8 REFERENCES

Figure 5: APD dark currents as a function of accumulated neutron flux measured during, and few days after, irradiation where the decrease in dark current indicates that annealing is taking place.

Hamamatsu BC-16 (λ=460nm, T=20.0°C)

Figure 6: Photocurrent $I_{ph}$ as a function of bias voltage for the Hamamatsu BC-16 APD measured with the same light intensity before and after irradiation, indicating a radiation-induced loss of quantum efficiency. The dark current after irradiation is shown on the same plot. Photocurrents plotted have the corresponding dark currents subtracted.
TOTAL DOSE AND SINGLE EVENT EFFECTS (SEE)
IN A 0.25µm CMOS TECHNOLOGY
CERN, CH-1211 Geneva 23, Switzerland
T. Calin, J. Cosculluela, R. Velazco, M. Nikolaidis
TIMA/INPG Laboratory, 46 Avenue Felix Viallet, 38031 Grenoble, France
A. Giraldo
University of Padova & INFN, via Marzolo 8, 35131 Padova, Italy

ABSTRACT
Individual transistors, resistors and shift registers have been designed using radiation tolerant layout practices in a commercial quarter micron process. A modelling effort has led to a satisfactory formulation for the effective aspect ratio of the enclosed transistors used in these layout practices. All devices have been tested up to a total dose of 30 Mrad(SiO2). The threshold voltage shift after irradiation and annealing was about +45mV for NMOS and -55mV for PMOS transistors, no leakage current appeared, and the mobility degradation was below 6%. The value of resistors increased by less than 10%. Noise measurements made on transistors with W=2µm and L varying between 0.36 and 0.64µm revealed a corner noise frequency of about 200kHz for the NMOS and 12kHz for the PMOS. Irradiation up to 30 Mrad(SiO2) did not significantly affect the noise performance. The shift registers continuously operated at 1.25MHz during the irradiation, and no error was detected in the pattern propagation. No functional degradation was observed. An irradiation with a heavy ion beam was made on the shift registers to study their sensitivity to Single Event Effects (SEE). No Single Event Latch-up (SEL) was observed up to a LET of 89 MeVcm²mg⁻¹. The register designed using dynamic logic, with a threshold LET lower than 3.2 MeVcm²mg⁻¹, proved to be considerably more sensitive to Single Event Upset (SEU) than its static logic counterpart, which had a threshold LET of about 15 MeVcm²mg⁻¹. A novel SEU-tolerant design was demonstrated to be extremely effective as storage cell.

1. MOTIVATION
In agreement with the first measurements on ultra-thin oxides [1], recent studies confirmed the total dose hardness of the thin oxide of a commercial 0.25µm CMOS technology [2]. The use of radiation tolerant layout practices, based on the systematic use of enclosed NMOS transistors and guardrings, was demonstrated to extend the tolerable total dose level well beyond the inherent technology limit [3].

All these results are extremely promising in view of the possible use of deep submicron technologies for the readout electronics of LHC. In this respect, some important issues not addressed in references [2] and [3] still need to be studied.

How to estimate the correct effective aspect ratio of enclosed geometry transistors, an important parameter entering in the design of a circuit, is not known. The noise of transistors in deep submicron technologies needs to be characterised. Moreover, no investigation of Single Event Effects has been carried out on structures designed in a deep submicron process using radiation tolerant layout practices.

This paper describes the work in progress to study all the above issues.

2. EXPERIMENTAL DETAILS
2.1 Description of the test vehicle
We have designed a test vehicle in a commercial 0.25µm process using three of the five available metal layers. The relevant features of this technology are summarised in Table I.

The test vehicle consisted of a series of individual NMOS and PMOS transistors in both standard linear and enclosed geometry, a ring oscillator, three shift registers and a few logic gates. Also, a prototype front-end readout chip for pixel detectors was integrated, for which results are presented separately at this conference [4].

The standard linear NMOS and PMOS transistors were designed with the same gate width, W=10µm, and with gate length varying between 0.28 and 5µm. All the enclosed geometry NMOS transistors had the same size for the inner diffusion, and gate length varying between 0.28 and 5µm. In this case, two identical transistors for
each gate length were integrated in order to study the matching properties of enclosed devices.

Table 1: technology features.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>2.5V</td>
</tr>
<tr>
<td>Min. L (drawn)</td>
<td>0.24 μm</td>
</tr>
<tr>
<td>t_{ox} (physical)</td>
<td>5 nm</td>
</tr>
<tr>
<td>Vth N/P</td>
<td>550/-450 mV</td>
</tr>
<tr>
<td>Zero-Vt NMOS transistors available</td>
<td></td>
</tr>
<tr>
<td>Shallow trench device isolation (STI)</td>
<td></td>
</tr>
<tr>
<td>2 to 5 levels of global metal (+ M0 for local connect.)</td>
<td></td>
</tr>
<tr>
<td>Stud contact and wiring level vias</td>
<td></td>
</tr>
<tr>
<td>Metal to metal capacitor available</td>
<td></td>
</tr>
</tbody>
</table>

Two zero-Vt NMOS transistors were designed with enclosed shape, with channel length L_{drawn}=0.6μm and L_{drawn}=1μm. Several n-well resistances were integrated.

To study the radiation behaviour of the field oxide, a series of Field Oxide Transistors (FOXFET) has been designed, using polysilicon or metal 1 gates. In some of these devices, the two n+ diffusions constituting the source and drain are separated by a p+ strip. This simulates the presence of a guardring, and allows the direct measurement of its effectiveness in preventing any leakage current.

Three shift registers were integrated to study SEEs on circuits designed in the quarter micron process, each register made up of a number of identical D-Flip-Flop (FF) cells. One of the registers used the standard static architecture for the FFs, another one used a dynamic architecture, and the third one was static but implemented using a dedicated SEU-tolerant (“hard”) design. This design is the successor of other two architectures successfully used to harden memory cells against SEU [5][6]. The size of the FF was 18x16μm for the dynamic, 33x16μm for the standard static and 50x16μm for the “hard”. The number of FFs was 2048 for the two static registers and 1024 for the dynamic design.

All the shift registers used radiation tolerant layout practices: all the NMOS and most of the PMOS were designed with enclosed geometry, and guardrings surrounded all the NMOS devices. All together, the three shift registers contained some 150000 transistors, and occupied an area of about 2.7mm².

2.2 Irradiation conditions

Total dose irradiation tests were performed at room temperature and under bias, mainly using a SEIFERT RP-149 X-ray irradiation facility with a tungsten target for X-ray production (about 10keV fluorescence peak). For individual transistors, worst case bias was applied in all cases. Another set of irradiations was performed on individual transistors using a 60Co γ-ray source. Annealing took place in all cases under bias: at room temperature for one day, to monitor the fast annealing, and then for one week at 100°C following the ESA qualification procedure [7].

Single Event Upset (SEU) and Latch-up (SEL) measurements were performed at the LBL (Lawrence Berkeley Laboratories, California) cyclotron using a heavy ion beam at room temperature. The LET (Linear Energy Transfer) was changed by selecting the ion species (Nitrogen, Neon, Argon, Copper, Krypton and Xenon) and by tilting the device up to 55° relative to the beam line. In this way, LETs varying from 3.2 to 89 MeVcm²mg⁻¹ were obtained.

3. ENCLOSED NMOS: ASPECT RATIO AND OUTPUT CONDUCTANCE

If the use of the enclosed geometry for the NMOS transistors eliminates radiation-induced leakage currents, their special shape does not constitute a common practice in VLSI design. Therefore, no effort has been conducted so far in modelling transistors with such shape. The absence of a convenient model, at least for the effective aspect ratio (W/L), poses a problem especially for analog design. The approximation for the aspect ratio proposed in [3] and based on the assumption of square equipotential lines under the gate might lead to a 30-40% over-estimate. To solve this problem, we have developed a model to estimate the aspect ratio of the enclosed transistors.

![Figure 1: Enclosed transistor shape.](image)

3.1 Transistor shape

There is a wide range of possible enclosed shapes: squared, octagonal, squared with corners cut at 45°, and all of them can have different behaviour and require a separate model. To simplify the problem, we have chosen one specific shape compatible with the design rules of the quarter micron process, and we concentrate our modelling efforts on that. This shape is shown in Figure...
1. The corners of the gate are cut at 45° so that the size of the cut (c in the figure) is constant for all gate lengths. Compared to the octagonal shape, in the chosen geometry the current flows mainly in two orthogonal directions, assuring in general a better homogeneity. This in turn results in better device matching.

3.2 Aspect ratio

A detailed study of the transistors with enclosed geometry has been made, and is described in [8]. This study proposes a model for the effective W/L of enclosed transistors. If applied to the shape of Figure 1, the model leads to the following expression for the aspect ratio:

\[
\frac{W}{L} = \frac{4 \alpha d + 2K (1 - \alpha)}{d - 2a L_{\text{eff}}} \frac{d - d'}{d'^2 - 2a L_{\text{eff}}} + 3 - \frac{d' - 2K}{a L_{\text{eff}}}
\]

In the formula, d is the size of the central drain as shown in Figure 1, \(d' = d - \frac{2.5}{\sqrt{2}}\) is the length of the linear inner side of the gate, \(L_{\text{eff}}\) is the effective channel length, and \(\alpha\) is a constant set to 0.05. \(K = 7/2\) for short channel transistors \((L \leq 0.5 \mu m)\), otherwise \(K = 4\). In our test transistors, d=0.84µm. To derive the above expression, the enclosed transistor is decomposed into three parts. The first part corresponds to the linear edges of the transistor, the second to the corners without the 45° cut, which then is taken into account separately as the third part. The presence of the up-left polysilicon strip, necessary to integrate the gate contact outside the thin gate oxide region, eliminates a part of the corner: this is taken into account in the formula.

<table>
<thead>
<tr>
<th>L_{\text{drawn}} (µm)</th>
<th>(\frac{W}{L})_{\text{est}}</th>
<th>(\frac{W}{L})_{\text{eff}}</th>
<th>(\frac{W}{L})_{\text{extracted}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.28</td>
<td>14.8</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>0.36</td>
<td>11.3</td>
<td>11.2</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>8.3</td>
<td>8.3</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>5.1</td>
<td>5.2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>2.6</td>
<td>2.6</td>
<td></td>
</tr>
</tbody>
</table>

The expression for the aspect ratio can also be used for transistors designed by stretching in one or both directions the shape in Figure 1, provided the corners are not modified. In that case, one just needs to add the contribution of the linear regions generated by the stretching. Transistors with aspect ratio as large as desired can be designed in this way. On the contrary, there is a limitation in the minimum aspect ratio obtainable with enclosed transistors.

As shown in Table 2, the aspect ratio decreases when the gate length is increased. For channel length close to 7µm, the dominant contribution to the transistor current comes from the gate corners. This corresponds to the second term in the above expression, which does not depend on the gate length. Therefore, the aspect ratio reaches a “saturation” value of about 2.3 for \(L_{\text{drawn}} = 7\mu m\). This important limitation for analog design is inherent to the use of enclosed transistor shapes.

3.3 Output conductance

In an enclosed shape transistor, source and drain are not symmetric. The inner diffusion has a much smaller area, hence capacitance, than the outer one. As the gate perimeter is different in the inner or outer side, the transistor output conductance in saturation changes depending on whether the inner or outer diffusion is chosen as the drain. Measurements summarised in Table 3 show that the output conductance is lower when the outer diffusion acts as the transistor drain, and that this asymmetry increases with the gate length. This second trend is easily explained by the fact that the outer gate perimeter increases with the gate length, whilst the inner one does not.

Table 3: Output conductance for enclosed NMOS transistors of different gate length. \(G_{in}\) = inner diffusion as drain, \(G_{dr}\) = outer diffusion as drain. Difference = \((G_{dr} - G_{in})/G_{in}\). Measurements for \(V_{GS} = V_{th} = 300 mV\).

<table>
<thead>
<tr>
<th>L_{\text{drawn}} (µm)</th>
<th>(G_{in}) (µS)</th>
<th>(G_{dr}) (µS)</th>
<th>Difference (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.28</td>
<td>11.09</td>
<td>9.62</td>
<td>19</td>
</tr>
<tr>
<td>0.36</td>
<td>7.17</td>
<td>5.55</td>
<td>23</td>
</tr>
<tr>
<td>0.5</td>
<td>4.10</td>
<td>2.73</td>
<td>33</td>
</tr>
<tr>
<td>1</td>
<td>1.68</td>
<td>0.79</td>
<td>53</td>
</tr>
<tr>
<td>3</td>
<td>0.57</td>
<td>0.17</td>
<td>70</td>
</tr>
<tr>
<td>5</td>
<td>0.41</td>
<td>0.10</td>
<td>75</td>
</tr>
</tbody>
</table>

This characteristic asymmetry of the enclosed NMOS should be taken into account for the choice of which of the two diffusions is the drain. In general, capacitive load and improved output conductance will have to be traded off against each other.

4. TOTAL DOSE RESULTS

In the following all results refer, unless otherwise specified, to X-ray irradiation tests at a dose rate varying...
between 20 and 30 krad(SiO₂)/min. During irradiation and annealing, the bias of the individual transistors was kept in the “worst case” condition. This means $V_{\text{source}}=V_{\text{drain}}=V_{\text{sub}}=0\text{V}$ and $V_{\text{gate}}=V_{\text{ds}}=2.5\text{V}$ for the NMOS, and all terminals grounded for the PMOS transistor.

4.1 Individual transistors using radiation tolerant layout practices

In this paragraph, we group the results concerning enclosed NMOS (including Zero-Vt enclosed transistors) and standard PMOS transistors, which are used together in designs where a high level of radiation tolerance (>100-200krad) is required.

The threshold voltage shift as a function of the total dose is shown in Figure 2 for an irradiation up to 30Mrad(SiO₂). The results refer to transistors with minimum (NMOS and Zero-Vt) or close to minimum (PMOS) gate length. Similar results were obtained for all other channel lengths. Immediately after irradiation (black points), the threshold voltage shift is less than 35mV for the NMOS, and about 70mV for the PMOS transistors. For a total dose of 10Mrad, these values are 15 and 30mV respectively.

![Figure 2: Threshold voltage shift of enclosed NMOS, enclosed Zero-Vt, NMOS and standard PMOS transistors as a function of the total dose. The white points represent the measurement after 24 hours at room temperature (first point) and after final high temperature annealing (last point).](image)

During the annealing (white points), the threshold voltage shift increases to about 45mV for the NMOS and decreases to about 55mV for the PMOS transistors. This is due to the de-trapping of the charge trapped in the oxide and, for the NMOS, to the creation of new interface states. As expected for the thin gate oxide of the quarter micron process, both trapping of charges in the oxide and generation of interface states give contributions of the order of tens of mV to the threshold voltage shift. This is clearly demonstrated by the measurement of the sub-threshold swing (the inverse of the slope), which increases only by about 5mV/dec for the NMOS and 2mV/dec for the PMOS transistors. The change in the swing is directly related to the creation of new interface states.

The mobility degradation is minor as well: we measured a maximum decrease of about 6% for the NMOS (Zero-Vt, devices included) and 2% for the PMOS transistors after 30Mrad(SiO₂) and annealing.

The output conductance of both NMOS and PMOS transistors is practically unchanged after the highest dose irradiation and annealing, as shown in Figure 3 for transistors with gate lengths of 0.28 and 2μm. The dashed lines, referring to the post-irradiation measurements, are practically indistinguishable from the pre-irradiation lines.

![Figure 3: Saturation curves for enclosed NMOS and standard PMOS transistors before (solid lines) and after 30Mrad(SiO₂) and annealing (dashed lines). $V_{GS}=V_{th}$ was about -330mV for the PMOS and 230mV for the NMOS transistors in all measurements.](image)

The enclosed geometry of the NMOS transistors effectively eliminates any source-drain leakage path. This is shown in Figure 4, where the transistor leakage current is plotted as a function of the total dose. The PMOS transistor leakage decreases slightly at high total doses. This is explained by the fact that before irradiation the PMOS transistor is at the very beginning of the weak inversion already for $V_{GS}=0\text{V}$ and $V_{DS}=2.5\text{V}$. As the leakage current is measured under such bias, the weak inversion current is seen as a leakage. With the irradiation, the threshold voltage increases, and this leakage disappears.

![Figure 4: Leakage current for enclosed NMOS and standard PMOS transistors.](image)
Our measurements also confirmed that the systematic use of guardrings around NMOS transistors is effective in preserving the device isolation: no leakage current has been measured in the FOXFETs where a p+ diffusion separated source and drain, even after a total dose of 30Mrad(SiO₂).

4.2 Standard NMOS transistors

For applications where a low level of radiation tolerance is required (10-20krad), our previous study [2] suggested that the quarter micron technology could be used without applying radiation tolerant layout practices. To explore this possibility, we have measured the behaviour of standard NMOS transistors of different channel lengths up to a total dose of 200krad(SiO₂).

The transistor leakage current for NMOS transistors is shown in Figure 5. Up to the total dose of 200krad(SiO₂), no increase of the leakage current is observed on any transistor. The measurement of the integrated FOXFETs showed no leakage between adjacent n+ diffusions. This means that, up to this level of total dose, the electrical isolation between devices is still very effective.

The threshold voltage shift was in all cases less than 2mV, the sub-threshold swing changed less than 1mV/dec, and the mobility was practically unchanged.

4.3 Resistors

Three n-well resistors were integrated in the test vehicle to measure their evolution with the total dose. These resistors had nominal values of 3.3, 1.65 and 0.2kΩ. They were irradiated with X-rays at a dose rate of 30krad(SiO₂)/min and with the two leads grounded. The irradiation results are shown in Figure 6. The maximum variation after a 30Mrad(SiO₂) irradiation is below 10% in all cases.

![Figure 6: Evolution of the resistors with irradiation. Before irradiation, R₁=3.83kΩ, R₂=1.980kΩ, R₃=240Ω.](image)

4.4 Shift Registers

The three shift registers have been irradiated with X-rays up to a total dose of 30Mrad(SiO₂), applying a supply voltage V₆₆=2V. Intermediate measurements were done at 1, 3, 5 and 10Mrad. During the irradiation, performed at a dose rate of 30 (up to 10Mrad) and 40krad/min (from 10 to 30Mrad), the shift registers worked continuously. A pattern of alternate 1s and 0s was circulated at a frequency of 1.25MHz, and the output from the registers was compared with the written pattern to detect eventual errors in the propagation. No error was detected in any of the registers during the irradiation up to 30Mrad.

Our setup only allowed us to establish the functionality, but could not be used for high-speed measurements (>2.5MHz). Functionality was conserved during and after irradiation and annealing. The lower limit of operating frequency for the dynamic register, determined by the transistors leakage current, is reduced by the irradiation below 4.9kHz. This result can be understood from the decrease of the PMOS leakage current shown in Figure 4.

The results obtained on the shift registers demonstrate at the circuit level that, with the use of radiation tolerant layout practices in deep submicron commercial technologies, it is possible to design ICs able to stand high total doses.
5. NOISE

In the design of front-end circuits for the readout of particle detectors, a good understanding of the noise characteristics of the transistors is fundamental as it determines the lowest achievable circuit noise. To study the noise of transistors in the quarter micron process, we have integrated large transistors (W=2000µm) with high transconductance, which offer high drain current white noise density.

The noise measurement chain consisted of a transimpedance amplifier, a voltage gain stage and a spectrum analyser, and is described in detail in reference [9]. With this setup, we could explore the 200Hz-30MHz range. Measurements were performed with the transistors biased in moderate inversion and in saturation (V_{DS}=800mV), and with a drain current of 500µA. Three gate lengths were studied: L=0.36, 0.5 and 0.64µm.

The noise spectra of NMOS and PMOS transistors before irradiation, expressed as equivalent voltage noise at the gate, are shown in Figure 7 for two gate lengths. For the PMOS transistors, no relevant short channel effect is apparent, and the noise scales approximately with the transistor size as expected: the 1/f noise density decreases with the gate area, and the white noise density decreases with the transconductance. The cutoff frequency, where the 1/f and the white noise densities are equal, is about 12kHz.

On the other hand, a significant short channel effect appears in the noise characteristics of NMOS transistors. Both the 1/f and the white noise are higher than expected according to the scaling laws. As a result, the cutoff frequency of the 0.36µm transistor is 1.5MHz, significantly higher than the 200kHz measured for the 0.64µm transistor. These results generally indicate that, in low-noise designs, NMOS transistors with channel length below 0.5µm should be used with care.

![Figure 7: Noise spectra of NMOS and PMOS transistors before irradiation.](image)

The transistors were irradiated with X-rays up to a total dose of 30Mrad (SiO₂) under worst case bias, and the noise measurement was repeated. The measured noise spectra are compared to the pre-irradiation ones in Figure 8 for a channel length of 0.36µm, and similar results were measured for the 0.5 and 0.64µm transistors. Even after such a high total dose, the degradation of the noise characteristics is very limited: the white noise increases by less than 5%, and the cutoff frequency moves only slightly towards higher frequency.

These results indicate that transistors in the 0.25µm process have an excellent noise performance, even after irradiation, and are compatible with the requirements of low noise analog design.

![Figure 8: Noise spectra of NMOS and PMOS transistors with L=0.36µm before and after an irradiation up to 30Mrad(SiO₂).](image)

6. SINGLE EVENT EFFECTS (SEE)

6.1 Single Event Latch-up (SEL)

SEL is a destructive SEE threatening all bulk CMOS and bipolar technologies in a radiation environment. It is triggered by excess current in the base of either a parasitic pnp or npn transistor following the charge deposition from a heavily ionising particle. This switches the parasitic thyristor in a high current self-maintaining state that can cause destructive burnout. Therefore, it can be detected by monitoring the current consumption of the circuit.

During the heavy ion irradiation, we constantly monitored the total current consumption from the three shift registers. The monitoring circuitry also included a block able to inhibit the power supply to the registers for a few ms in case of latch-up detection. This is sufficient...
to break the latch-up condition and bring the circuit back to its normal operating mode.

No SEL was observed during the whole irradiation campaign, at an applied supply voltage of 2.5V, up to the maximum LET available of 89 MeVcm²/kg. Similar results had previously been obtained even on standard (without guardrings) structures integrated in the same technology [10]. This result already pointed to a good robustness of this quarter micron process against SEL. As the systematic use of guardrings decreases the latch-up sensitivity [11], the result obtained on the shift registers was expected.

A recent simulation study [12] has shown that the maximum energy deposition occurring with some probability in the LHC radiation environment will correspond locally to a LET lower than 50 MeVcm²/kg. This will happen in the very rare case of a nuclear interaction in the tungsten, which is often used in ICs for connection purposes between layers. Therefore, the measured threshold for SEL indicates that latch-up will not be a threat in LHC circuits designed using radiation tolerant layout practices.

As the SEL sensitivity is strongly layout-dependent, the same conclusion cannot be generally extended to circuits designed using standard layout. Nevertheless, the results in [10] seem to indicate that, with a reasonable distribution of substrate and well contacts, SEL should not occur even in this case.

6.2 Single Event Upset (SEU)

The charge collection following a heavily ionising particle strike can change the state of the circuit node hit and cause false information to be stored: this phenomenon is called SEU. As the minimum charge collection needed to generate the upset is proportional to the node capacitance and the supply voltage, SEU sensitivity increases with the scaling of VLSI technologies towards smaller device size [13].

SEU sensitivity is also widely design-dependent: dynamic logic is in general considerably more vulnerable than static logic, and the sensitivity can be lowered by increasing the capacitance or the drive capability of the nodes.

To study the sensitivity of circuits designed in the 0.25µm process using layout tolerant design practices, we have irradiated the shift registers with heavy ions under different conditions, applying a supply voltage V[sub]dd=2V. A first set of measurements was performed in what we call “un-clocked mode”. A test pattern was written into the register (at 2.5MHz), then the clock stopped during a time interval ranging from 2 s to a few minutes, and finally the pattern was read out and compared with the original one: each difference was counted as a SEU. In this case, the write and read time was negligible compared to the storing time, and the circuits were working as “memory elements”. Of course, only the two static registers could work in this mode, the dynamic register always requiring a clock to be functional.

During the second set of measurements, in what we call “clocked mode”, the pattern was written and read continuously, and the comparison between data took place all the time. The clock was therefore applied throughout the test, at the constant frequency of 2.5MHz.

1) Un-clocked mode

The result for the standard static register is shown in Figure 9, where the SEU cross-section (σ) is plotted as a function of the particle LET. The cross-section is the number of errors divided by the particle fluence and the number of memory elements, hence it is expressed in cm²/bit. Cross-section curves are a standard practice in SEU testing of circuits, as they give an immediate picture of the upset sensitivity. The cross-section value at high LET, where the curve shows a saturation, is representative of the total sensitive area of each memory cell. It is indicated as σ[sub]sat and, when multiplied by the number of memory elements, it gives the total sensitive area of the chip. The other important parameter visible in the cross-section curve is the threshold LET (LET[sub]th), the value at which the circuit starts to be sensitive to SEU.

![Figure 9: Experimental SEU cross-section for the static standard register.](image)

It is common practice [14] to fit the experimental points with a Weibull curve, using the expression:

\[
\sigma = \sigma_{\text{sat}} \left(1 - \exp \left(-\frac{L - \text{LET}_{\text{th}}}{W}\right)^S\right)
\]

This allows for the extraction of σ[sub]sat and of LET[sub]th. W and S are fitting parameters without physical meaning. The values extracted are shown in Figure 9. It is interesting to note that the saturation cross-section of about 26µm² well matches the integral area of the sensitive node in the circuit layout (about 22 µm²). Also, the critical charge estimated with the SPICE simulation of the cell (170°C) is close to the one approximately extracted from the LET[sub]th (155°C).

The observed threshold at about 15 MeVcm²/kg is considerably higher than what one would expect for
memory designs in the quarter micron technology. In ref. [10], which refers to a different design in the same technology, a LET of about 4 was measured. This difference is attributed to the increased transistor size, typical of the radiation tolerant layout practices, and therefore of the associated parasitic capacitance and drive capability. This translates into a decrease of the SEU sensitivity.

The simulation work reported in [12] shows the probabilities for energy depositions leading to upset in the LHC radiation environment. The probability for an energy deposition higher than 3 MeV in the charge-collecting region (called "sensitive volume") is shown to be practically negligible. The measured LET threshold can be simply translated into energy deposition once the sensitive volume is defined. If we assume (as in [12]) a 1 µm³ sensitive volume, then the threshold energy deposition for upset equals 3.5 MeV. This leads to the first order conclusion that the standard static architecture could be robust enough not to experience a significant rate of SEU in LHC. This should be verified experimentally by a proton irradiation test, which is part of our future work plan.

The static "hard" register began to experience upsets only starting from the highest available LET of 89 MeV·cm²·mg⁻¹. Even at that high LET, the cross-section was measured to be lower than 10⁻⁶ cm²/bit. The proposed architecture is therefore very effective in protecting the content of memory elements not only at the LHC, but also in the radiation environment of Space, where heavy ions are present.

2) Clocked mode

Due to some limitations in our test setup, this measurement was limited to the dynamic and the static "hard" register. Also, it was not possible to precisely draw a cross-section curve, but only to extract the tendency for the SEU sensitivity.

The measurement on the dynamic shift register confirmed the general tendency that dynamic logic is significantly more sensitive to upsets than static logic. A considerable number of SEUs was already observable at the lowest LET available of 3.2 MeV·cm²·mg⁻¹, from which one can deduce a critical charge lower than 35 fC. SPICE simulations lead to an estimated value of about 34 fC. With such a low threshold, the circuit would be quite sensitive to SEU in the LHC radiation environment (especially in the tracker), hence this architecture and more generally all dynamic architecture is not advisable or should be used with great care.

Also the static "hard" register showed a considerable number of errors when the LET was increased to 5.6 MeV·cm²·mg⁻¹. This is due to the particular architecture of the cell, which was designed as a memory cell. During the write phase, the output node does not see any low resistance path towards Vdd or Vss for half of the clock period. Therefore, this node can temporarily change its logic state if hit by an ionising particle. This change does not affect the cell itself, which shows the correct output at the end of the write cycle. Nevertheless, in the specific case of the shift register, the momentary corruption of the output presents the wrong data at the input of the next cell. As this happens during the write cycle, the wrong data is latched into the next cell, originating an upset.

7. CONCLUSION

The use of radiation tolerant layout practices in a commercial quarter micron process has led to the design of devices and circuits able to stand total doses up to 30 Mrad(SiO₂). Enclosed geometry NMOS and guardrings effectively eliminate any leakage current path. Therefore, the total dose limit comes from the radiation tolerance of the thin gate oxide, which is naturally extremely resistant to radiation effects.

As enclosed NMOS transistors are not commonly used in VLSI design, we had to develop a specific model for the evaluation of their effective aspect ratio, which is complicated by the presence of gate corners. The availability of such a model now allows designers to more comfortably deal with such transistor shape.

Standard linear NMOS transistors did not show any leakage current up to a total dose of 200 krad(SiO₂). The transistor isolation was also not affected by such level of irradiation. Therefore this 0.25µm technology could safely be used, without any special layout practice, for designs requiring a low level of radiation tolerance.

The transistor noise in the quarter micron process is compatible with low noise analog design: the corner noise frequency is about 200 kHz for the NMOS and 12 kHz for the PMOS transistor. Irradiation up to 30 Mrad(SiO₂) does not significantly affect these parameters.

The study of sensitivity to Single Event Effects has been performed with a heavy ion beam on shift registers designed using radiation tolerant layout practices. These circuits showed very good performance in terms of immunity to Single Event Latch-up. According to this result, SEL is not going to affect circuits implemented with these layout practices in LHC.

Single Event Upset heavily affects the performance of dynamic logic, but a high SEU threshold of 15 MeV·cm²·mg⁻¹ was measured for the static shift register. An SEU-tolerant architecture has been developed and proved to be very effective in protecting the content of memory elements.
REFERENCES


[4] W. Snoeys et al., “Radiation tolerance beyond 10Mrad demonstrated on a pixel readout chip in standard submicron CMOS”, presented at this LEB98 workshop, to be published in the proceedings


RADIATION TOLERANCE BEYOND 10 MRAD FOR A PIXEL READOUT CHIP IN STANDARD SUBMICRON CMOS

W. Snoeys¹, M. Burns¹, M. Campbell¹, E. Cantatore¹, R. Dinapoli¹², F. Faccio¹, E. Heijne¹, P. Jarron¹, M. Luptak¹, A. Marchioro⁰, P. Martinengo⁰, D. Minervini¹², M. Morel¹, E. Pernigotti¹⁰, I. Ropotar¹ and K. Wyllie¹

¹CERN, Geneva, Switzerland, ²University and INFN Bari, ³INFN Pisa, ⁴Inst. of exp. phys., Kosice.

ABSTRACT

A pixel detector readout prototype has been developed at CERN for the ALICE and LHCb experiments in a commercial 0.25 µm CMOS technology. This technology showed promise at transistor level for high radiation tolerance and provides sufficient density for these applications. The chip is a matrix of two columns each containing 65 identical cells. Each readout cell comprises a preamplifier, a shaper filter, a discriminator, a delay line and readout logic. The chip occupies 10 mm², and contains about 50000 transistors. Electronic noise (~200 e' rms) and threshold dispersion (~160 e' rms) allow operation at 1500 e' average threshold. The radiation tolerance of this mixed-mode analog-digital circuit has been enhanced by designing all NMOS transistors in enclosed geometry and introducing guardrings wherever necessary. The chip was irradiated with X-rays and remains fully functional up to 30 Mrad(SiO₂) with only minor changes in analog parameters and no change in supply currents.

1. INTRODUCTION

Radiation tolerance of integrated circuits is a primary concern in future high energy physics experiments. Although radiation hard technologies exist, they do not always provide adequate density. In particular, pixel detectors are often placed as close as possible to the interaction point and hence require highest radiation tolerance. In addition, the area taken by the readout electronics defines the pixel size, and therefore a high component density is necessary. This was the motivation to also investigate the radiation tolerance of standard submicron technologies.

Irradiation measurements on MOS capacitors [1,2] showed a significant decrease of the radiation induced trapped oxide charge and interface states for oxides thinner than about 10 nm. Gate oxides in present day submicron CMOS technologies are in this range. Recent measurements on transistors implemented in these technologies confirm the significant reduction in radiation induced transistor parameter shifts [3,4].

Ionizing radiation can still lead to source-to-drain and inter-transistor leakage for the N-channel devices. Source-to-drain leakage can be avoided by using a closed gate as shown in fig. 1. The inter-transistor leakage is eliminated by implementing P+ guardrings as also shown. The effectiveness of this layout approach has been extensively proven for transistors in many technologies including the 0.25 µm [4-6]. The achievable density in deep submicron technologies offsets at least partially the loss in area incurred.

Fig. 1. Transistors laid out in enclosed geometry to prevent transistor leakage. The implementation of P+ guard rings prevents leakage between two transistors.

A previous test chip [4] implemented in a commercial 0.5 µm CMOS technology proved the validity of the approach for a full mixed-mode circuit. It withstood ionizing radiation up to a dose of 600 krad to 1.7 Mrad depending on the radiation source. Failure was ultimately caused by the cumulative effect of radiation induced transistor threshold shifts. Transistor irradiation measurements indicate that without special layout precautions the chip would have died at about 50 krad due to excessive power consumption from radiation induced leakage. Although these are very encouraging results, the density penalty of these layout techniques proved to be too large for application in the ALICE pixel detector. Therefore, a new test chip was developed following the same approach in a 0.25 µm CMOS technology. This paper reports on the performance of the new test chip and its radiation tolerance.
3. PIXEL DETECTOR READOUT CIRCUIT DESCRIPTION

The circuit builds on the experience obtained with previous pixel readout chips [4,7-10]. It is a matrix of two columns each containing 65 identical cells, it occupies 10 mm², and contains about 50 000 transistors.

Each readout cell (see fig. 2) comprises a preamplifier, a shaper filter, a comparator, a delay line and readout logic. As this prototype was not intended for bump-bonding to a detector, an input structure has been added to each cell to simulate detector capacitance, coupling between pixels, and detector leakage current.

The circuit can work both with positive and negative input charges. The preamplifier feedback circuit is a modification of a circuit proposed in [11] to allow both polarities of leakage current. The comparator has a three bit threshold fine-adjust. Currently it is controlled by a three bit bus directly linked to the outside. The delay element consists of an 8-bit counter and some control logic. A flag tells the delay control logic which polarity of the comparator output corresponds to a logic one, depending on whether one collects positive or negative input charge. If the comparator fires the counter in the delay is started. The counter can be preset with an arbitrary value prior to counting, and the carry of the most significant bit is used to generate the end of count signal. Therefore the delay can be arbitrarily set. The logic in the delay element is fully static in one column, and dynamic in the other.

The content of the test flip-flop determines whether or not an analog input signal is applied to the preamplifier input across an injection capacitance. A mask flip-flop allows the disabling of a pixel should it be noisy or completely non-functional. If the counter in the delay reaches end of count when the strobe or trigger signal is high a one is written into the data flip-flop.

The layout of the pixel cells are shown in fig. 3. The pitch in the short dimension is 50 µm. The cell layout is based on the previous one implemented in the 0.5 µm technology where the front end occupied 270 µm. The 0.25 µm front end is only 125 µm long. The counter in the delay takes 40 by 60 µm² for the static case and 40 by 35 µm² for the dynamic case. The delay control logic measures about 20 by 25 µm². The rest of the digital part was directly taken from the 0.5 µm chip and still has to be shrunk to 0.25 µm design rules.

Fig. 2. Block diagram of the pixel cell. The delay line in the cell is based on a counter, implemented in a static and a dynamic version.

Fig. 3. Layout of the pixel cells. The top cell contains the delay implemented in dynamic logic, the bottom one contains the static version.
4. Measurement Results Prior to Irradiation

Fig. 4. Distribution of the pixel threshold for all 130 pixels. 1 mV corresponds to 100 electrons input charge. The top two curves show the threshold of the pixels in column 1 and 2 respectively as a function of position (row number). The bottom plot shows the distribution.

The chip has been characterized electrically prior to irradiation using the analog test input and is fully functional. Here some results are summarized.

The injection capacitance could not be calibrated, but only estimated from data on layer to layer capacitances provided by the vendor. All numbers given in absolute electron charge (e) are based on this estimate.

Fig. 4 shows how the threshold in electrons varies across the chip. There is no systematic dependence of the threshold on the position of the pixel within the chip. At this setting the average over all 130 cells is about 1 500 electrons and the spread is 160 electrons rms. The pixel noise is about 220 electrons. Fig. 5 shows how the average pixel threshold can be adjusted from about -20 000 to +20 000 electrons. The roll-up for higher threshold values is due to the clipping of the signal in the preamplifier to avoid circuit saturation and excessive recovery times for large input signals. The minimum threshold without hits due to noise is below 1500 electrons for both polarities of input charge.

In addition, the detector leakage current compensation, the 3 bit threshold adjust circuit, and the dynamic and static counters all work correctly.

Fig. 5. Evolution of the average pixel threshold, the rms variation of this threshold, and the pixel noise as a function of the bias controlling the threshold.

5. X-ray Irradiations

X-ray irradiations were carried out using a dedicated machine (Seifert RP149). The X-ray energy peaked at about 10 keV, and the dose rate was 4 krads(SiO₂)/min. Fig. 6 shows the evolution of the power supply currents with increasing X-ray dose. The absence of any increase in power consumption with irradiation dose confirms on a full circuit scale that enclosed NMOS devices and guard rings prevent radiation induced leakage.

Fig. 6. Evolution of power supply currents with increasing X-ray dose.

Fig. 7 shows the evolution of the average pixel threshold, the threshold dispersion and pixel noise for the same irradiation. For this particular chip a minor bias adjustment was necessary after 30 Mrad to prevent premature signal clipping in the preamplifier. Apart from this minor adjustment all other biases were kept constant. Fig. 7 illustrates that the chip remains fully functional up to 30 Mrad. After 24 hours under bias at room temperature the parameters were unchanged. Following a subsequent anneal for one week at 100°C the
Recent measurements in a high energy proton beam in the NA-50 experiment at CERN confirm the radiation tolerance of this prototype. Detailed results on this will be reported elsewhere after completion of the full data analysis.

6. CONCLUSIONS
The effectiveness of the use of enclosed geometry NMOS devices and guardrings to eliminate radiation induced leakage and increase radiation tolerance has been demonstrated on a pixel detector circuit. This full mixed-mode circuit was implemented in a standard 0.25 μm CMOS process. Measurements established that the circuit tolerated a total X-ray dose of 30 Mrad(SiO₂) and subsequent anneal whilst maintaining full functionality with only minor degradation of analog parameters and practically no change in power supply currents. This result illustrates the promise of these layout techniques combined with commercial deep submicron technologies for applications where a high total ionizing irradiation dose needs to be tolerated. Comparison with the result obtained in a 0.5 μm technology where a similar circuit died after 0.6 to 1.7 Mrad due to radiation induced transistor threshold shifts, illustrates the significance of the improvement for a deeper submicron technology with a thinner gate oxide.

7. ACKNOWLEDGEMENTS
We gratefully acknowledge the collaboration and financial support of our partners in the RD49, ALICE pixel, LHCb RICH, and NA50 projects.

8. REFERENCES


[6] F. Faccio et al., "Total dose and single event effects (SEE) in a 0.25 µm CMOS technology," This conference.


ESTIMATE OF THE SINGLE EVENT UPSET (SEU) RATE IN CMS
F. Faccio, C. Detcheverry*, M. Huhtinen
CERN, CH-1211 Geneva 23, Switzerland

ABSTRACT

SEU error rates in the CMS tracker environment have been estimated with Monte Carlo simulations. The estimated upset rates for a submicron technology are $3 \times 10^7$ upsets/(bit s) at 4.9cm and $1.1 \times 10^8$ upsets/(bit s) at 49cm from the beam line, respectively. Comparison of simulation data with experimental proton irradiation benchmarks points to a tenfold under-estimate of the actual rate. All these results have been obtained under the assumption of a $1\mu m^3$ sensitive volume and 1MeV energy threshold, and are very sensitive to the choice of these two parameters. The simulation indicates that mono-energetic proton beams are an effective tool for the SEU characterisation of ICs for the LHC radiation environment. Thermal neutrons might significantly contribute to the upset rate already in the outer parts of the tracker and in all the other parts of the experiment.

1. INTRODUCTION

In the complex problem of the radiation hardness assurance of electronics in the LHC experiments, the risk associated with Single Event Upsets (SEUs) has not yet been evaluated. To understand whether SEU represents a threat for the performance of the detector systems, it is necessary to estimate an error rate for electronics in the LHC radiation environment. This is the aim of the study presented in this paper. A significantly more detailed description of this study can be found in [1].

Due to the complexity of the problem, this study will be limited to the estimate of SEU rate in the tracker of CMS. These results could nevertheless also be used for the ATLAS tracker, which will have a radiation environment quite similar to the one of CMS. Moreover, we have chosen to deal only with submicron CMOS technologies, which are more likely to be used in the tracker and in the ECAL for ASIC applications.

The radiation environment of CMS is dominated by charged hadrons and albedo neutrons, which can lead to SEU only through nuclear (inelastic or elastic) interaction in the materials. Only alpha particles and recoil nuclei produced by the interaction can locally deposit enough energy to provoke an upset. As these particles generally have short ranges, the nuclear interaction has to occur in the material surrounding the sensitive point for SEU.

This implies that, to estimate the error rate, one should pass through the calculation of the probability of nuclear interaction of the primary hadrons with the target nucleus. This is clearly manageable only with the help of a powerful Monte Carlo simulation code, which has all the necessary interaction cross-sections as an input, and is able to transport both the primaries and the interaction products in the material.

2. THE SEU PHENOMENON

SEU is a non-destructive phenomenon, which concerns in general every memory element temporarily storing a logic state. It corresponds to a soft error (data corruption) appearing in a device due to the energy deposited in Silicon by an ionising particle. In the following description, we will consider an SRAM memory cell composed of two cross-coupled inverters. The same architecture is often used for static memory cells in ASICs, as local registers. We will suppose a particle struck at the drain of one of the four transistors of the memory cell.

Ionising particles, both primaries and secondaries generated by nuclear interactions in the material, create electron-hole pairs in the silicon device. The created carriers drift in the local electric fields and are collected at the different electrodes of the target transistor. Part of the charge collected at the drain accumulates on the capacitive load of the struck node, hence changing its state. This capacitor is mainly represented by the input of the second inverter. If the collection process is fast and the collected charge is large enough, the potential of the struck drain changes. The second inverter then switches and reinforces the change of state at the output of the struck inverter: the content of the memory cell is upset.

Therefore, SEU vulnerability is described in terms of a critical charge, i.e. the amount of collected charge required to produce a transient voltage sufficient to cause the non-struck inverter to switch. The critical charge corresponds to a critical energy that has to be deposited in the silicon by the ionising particle to provoke SEU. As the critical charge is actually collected at the sensitive node, the energy deposition should occur in a silicon volume in the proximity of the collecting node. This volume is called the sensitive volume (SV).

* On leave from University of Montpellier, now with Philips Research Laboratories Eindhoven
The evaluation of SEU sensitivity is carried out by placing the device under a beam of particles and measuring its cross-section \( \sigma \), defined at normal incidence as:

\[
\sigma = \frac{N_{\text{events}}}{\Phi} \text{ (cm}^2) \quad (1)
\]

where \( \Phi \) is the total particle fluence, and \( N_{\text{events}} \) is the number of events (SEU) counted during the test. Cross-section curves typically represent the \( \sigma \) of the device as a function of either the Linear Energy Transfer (for heavy ion experiments) or the energy (for proton experiments) of the incoming particles.

3. ERROR RATE PREDICTIVE MODEL

In order to predict the SEU rate in the CMS tracker environment, we used the following approach:

1) Definition of a sensitive volume SV.
2) Definition of a critical energy \( E_{\text{crit}} \) which, if deposited in the SV, will lead to a charge collection greater than the critical charge and provoke an SEU.
3) Simulation of the radiation environment. The output of the simulation is the number of times a given energy has been deposited in the SV. This number is divided by the particle fluence in the simulation to obtain the probability for each energy deposition.
4) The integration of all the probabilities for energy deposition equal or greater than \( E_{\text{crit}} \) gives the SEU probability. As this is the number of upsets divided by the fluence, this probability also represents a cross-section. This number, multiplied by the particle fluence expected for a given position in the CMS tracker and divided by the LHC operating time (about 5 \( 10^7 \) s), gives the upset rate.

The first three points will be discussed in more detail:

1) The sensitive volume is defined by a sensitive area and a sensitive depth, corresponding to the depth up to which the deposited energy creates charges that can be collected fast enough to provoke SEU. Actually, as suggested in previous work [2], both the sensitive area and depth increase with the energy deposited by the incident particle. However, in the practical simulation case, the sensitive volume cannot be changed with the deposited energy, but it must be set to a constant value. In this work, the sensitive volume is set to a region surrounding the drain of the “Outside the well” transistor turned OFF, which is the most sensitive point of the cell. The size of this region has been chosen on the basis of experiments and simulations referring to a specific device: a 64 Kbit SRAM circuit manufactured in a 0.6\( \mu \text{m} \) technology [3]. For this device, the SV has cubic shape and a volume of 1\( \mu \text{m}^3 \). As our prediction of SEU rate concerns submicron technologies, this choice represents a reasonable approximation.

2) The critical charge can be obtained by simulating the memory cell with a SPICE-like circuit simulator. The current spike resulting from the charge collection following the energy deposition can be simulated with a current generator. The critical charge is the integral of the smallest current pulse leading to an upset. The critical energy can be estimated from the critical charge (about 3.6 eV need to be deposited to generate an e-h pair). As the critical charge depends on the node capacitance, it changes with the technology used as well as with the memory cell design. Again, the value we have chosen is based on the specific device of reference [3], which had \( E_{\text{crit}} = 1 \text{ MeV} \).

3) The simulation of energy deposition in the SV was performed in several phases. The core of the simulations is the generation of the inelastic hadronic events, which has been done with the event generators of the FLUKA cascade simulation code [4][5]. The fragments produced by the FLUKA event generators have to be transported in the silicon until they enter the SV. During the transport the energy loss, due to ionising and non-ionising effects, has to be taken rigorously into account. This is done with the TRIM code [6], which has been modified such that atomic scattering can be taken into account in order to explicitly follow the whole atomic cascade. Only the ionisation deposition of fragments in the SV is counted.

The primary input used when generating the events in the case of the LHC environment was the hadron spectrum in the lower part (r=20-40 cm) of the CMS barrel silicon tracker [7]. For the proton beam simulations, it was the proton energy. In this work we did not simulate the interactions of neutrons with energy lower than 20 MeV. Such neutrons might lead to a non-negligible SEU rate, and this issue will be discussed in section 6.

4. COMPARISON OF SIMULATED AND MEASURED DATA FOR A PROTON BEAM IRRADIATION

In order to verify the capability of our simulation approach to produce reliable results, we applied it for a radiation environment for which experimental data are available: mono-energetic proton beams. We therefore ran the simulation for 20, 30, 60 and 200\( \text{MeV} \) protons, using a sensitive volume of 1\( \mu \text{m}^3 \) and setting an energy threshold of 1\( \text{MeV} \). As for the experiment, in the simulation the proton beam was unidirectional and normally incident on the surface of the silicon.

Figure 1 compares the simulation result with a set of experimental data for SRAM circuits from different manufacturers. The experimental data refer to several 0.5\( \mu \text{m} \) and one 0.25\( \mu \text{m} \) technologies, and are normalised to one bit of memory. The wide variation of SEU cross-section indicates that it is difficult to estimate the sensitivity from such general considerations as the technology generation and the memory size.

In Figure 1, the shape of the experimental curves is well reproduced by the simulation, but the absolute value
for the cross-section under-estimates all the experimental points. This might well be explained by our choice for the SV, and will be discussed in the following paragraph.

4.1 Effect of SV size and energy deposition threshold

The SEU probability (or cross-section) obtained from the simulations depends strongly on the assumptions made for the size of the SV and for the critical energy. In order to quantify this dependence we repeated the simulation for two increased sizes of the SV, and we analysed the results using different assumptions for the energy threshold.

An increase of the SV size has two effects, both increasing the SEU probability. First the probability for a fragment to hit the SV will increase according to its size. This is a simple geometrical effect which just scales the probability, preserving the dependence on the proton energy. But an increased size of the SV will also allow for longer path-length of a fragment in the SV and thus for a larger energy deposition. This comes close, but is not equivalent, to the effect of lowering the threshold.

Figure 2 shows the simulation data (cross-section) for different SV sizes. First, only the surface of the SV is increased (2x2x1µm). In this case, most of the effect of increasing the size is explained by the increased probability that the fragment hits it. Then, also the sensitive depth is increased to 2µm. Especially at low energies the effect is larger than the simple geometrical factor and the curve becomes somewhat flatter. This additional increase and the flattening are explained by the increased energy deposition of fragments due to the longer path-length.

The sensitive depth depends in first approximation on technology parameters such as doping profiles and thickness of the epitaxial layer. On the other hand, the surface of the SV changes with the circuit architecture, the sizing of the devices and the layout. Therefore the under-estimate of the experimental cross-sections in Figure 1 can be explained by an under-estimate of the SV surface. This is reasonable because the 1x1µm surface chosen refers to the sensitive area corresponding to the drain of the NMOS device, the most sensitive point, but neglects the contribution of the drain surface of both the PMOS and the (N or PMOS) access switch. This contribution might well increase the SV surface by a factor of 3 or more. In Figure 2, a fourfold increase in the surface brings the cross-section much closer to the experimental points.

A lowering of the energy threshold means that fragments with smaller LET or shorter pathlength will be able to trigger a SEU. Since the p-Si cross-section actually rises towards lower energies, it can be expected that the energy dependence of the SEU probability would be reduced at lower thresholds or even turn into a higher probability at low energies.
5. ESTIMATE FOR THE CMS TRACKER ENVIRONMENT

5.1 Results for the tracker

The described procedure has finally been applied to derive an estimate of the upset rate in the CMS tracker environment. We used a SV of 1μm³ and set the critical energy to 1MeV, and obtained an SEU probability equal to about 1.7 × 10⁻¹⁴. The estimated rate in the tracker, at different distances from the beam line, can easily be calculated by multiplying this probability with the fast hadron flux (charged hadrons plus neutrons above 20MeV) at every point. This is possible because the energetic distribution of fast hadrons in the tracker is to a fairly good approximation position independent, hence the flux only scales with the distance from the beam line. Table I summarises the result of this calculation for increasing distances in the tracker. These results do not significantly change when we repeat the simulation adding a tungsten pillar on top of each SV. This additional structure was added to evaluate the impact of the presence of heavy nuclei in the close vicinity of the SV. Tungsten was chosen because it is the heaviest and most frequently met element in the general CMOS technology.

Table I: Estimated SEU rate, expressed in upsets/(bit s), at increasing distances from the beam line in the CMS tracker. The particle fluxes include all charged hadrons as well as neutrons with E > 20MeV.

<table>
<thead>
<tr>
<th>Distance from beam line [cm]</th>
<th>Particle flux [cm⁻²s⁻¹]</th>
<th>Estimated SEU rate [upsets/(bit s)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3</td>
<td>4.9 × 10⁶</td>
<td>8.3 × 10⁻⁷</td>
</tr>
<tr>
<td>7.1</td>
<td>1.9 × 10⁷</td>
<td>3.2 × 10⁻⁷</td>
</tr>
<tr>
<td>11</td>
<td>8.6 × 10⁶</td>
<td>1.5 × 10⁻⁷</td>
</tr>
<tr>
<td>22</td>
<td>2.7 × 10⁶</td>
<td>4.6 × 10⁻⁴</td>
</tr>
<tr>
<td>32</td>
<td>1.4 × 10⁶</td>
<td>2.4 × 10⁻⁴</td>
</tr>
<tr>
<td>41</td>
<td>9.0 × 10⁵</td>
<td>1.5 × 10⁻⁴</td>
</tr>
<tr>
<td>49</td>
<td>6.2 × 10⁵</td>
<td>1.1 × 10⁻⁴</td>
</tr>
<tr>
<td>58</td>
<td>4.2 × 10⁵</td>
<td>7.1 × 10⁻⁹</td>
</tr>
<tr>
<td>75</td>
<td>2.2 × 10⁵</td>
<td>3.7 × 10⁻⁹</td>
</tr>
<tr>
<td>83</td>
<td>1.6 × 10⁵</td>
<td>2.7 × 10⁻⁹</td>
</tr>
<tr>
<td>91</td>
<td>1.2 × 10⁵</td>
<td>2.0 × 10⁻⁹</td>
</tr>
<tr>
<td>99</td>
<td>8.7 × 10⁴</td>
<td>1.5 × 10⁻⁹</td>
</tr>
<tr>
<td>115</td>
<td>4.7 × 10⁴</td>
<td>8.0 × 10⁻¹⁰</td>
</tr>
</tbody>
</table>

5.2 Influence of the particle composition of the radiation environment

The comparison of the simulation results indicates that the SEU probability in the LHC environment is only about 60% higher than the one for the mono-energetic 60MeV proton beam. Despite the great difference of the two radiation environments (presence of other hadrons, energetic spectrum of all particles extending into the GeV region for the LHC), the estimated rate is less than a factor of 2 different.

Some incompleteness in the FLUKA model for pion interaction might have led to an underestimate of the probability for the LHC environment (we believe this effect to be limited to a factor of 2 or less). Nevertheless, it seems that the estimated rate is not extremely sensitive to the particle composition and energy distribution.

This has two important consequences, which have not to be taken as “exact”, but as approximations for practical purposes:

1) To estimate the upset rate in regions of the experiment other than the tracker, one can simply use the probability of energy depositions higher than 1MeV obtained for the tracker environment (1.7 × 10⁻¹⁴) and multiply it by the total particle flux of the relevant region. As discussed below, this flux should not include the contribution from low energy neutrons.

2) Monoenergetic proton beams with energy up to 200-300MeV, normally used for SEU characterisation of devices in space applications, are a very effective tool to estimate the SEU susceptibility of ICs, and can lead to the evaluation of upset rates in the LHC environment.

These approximations can be useful to estimate the order of magnitude of the upset rates.

6. NEUTRON-INDUCED SEU

Neutrons with energy lower than 20MeV are not taken into account in our calculations. This is a practical limit for the intranuclear cascade model used to simulate nucleon-nucleus interactions.

The major unknown, preventing a simulation of low-energy neutron induced SEU, is the boron concentration and distribution in the devices. Moreover, the fluxes of low energy neutrons in the different parts of the experiment cannot always be precisely estimated, because they are often dependent on the materials locally used, and all designs are not yet final. Nevertheless, the simulation data in our possession quite reliably indicate a maximum thermal neutron fluence of 5 × 10¹³ n/cm² over 10 years in the CMS tracker. In the experimental hall this value is reduced to 3 × 10¹⁰ n/cm² in the forward direction (5 × 10⁹ n/cm² in the barrel).

If predictions of the upset rate coming from the calculation are not available now and would require intensive work, useful indications may come from available experimental data. A recent experimental study
on commercial SRAMs [11] has shown a sharp increase in the upset rate (a factor varying with the component from 2 to 100) when neutrons below 1eV are present in the irradiation spectrum. The 6 types of memories tested present a wide variability of SEU sensitivity; the observed upset rate, normalised to a fluence of $10^{16}$ n/cm$^2$, was in the range $7 \times 10^{-8}$ - $2 \times 10^{-6}$ errors/(bit s).

Knowing the number of upsets observed for the most and least sensitive SRAM tested for a given experimental neutron fluence, we can extrapolate these data to approximately evaluate the number of errors the same circuits would experience in the CMS radiation environment. To do so, we use the above given predicted fluence of thermal neutrons in the tracker and in the experimental hall, and we assume that thermal neutrons are responsible for all the observed upsets. We then divide the obtained errors in CMS by its foreseen activity time ($5 \times 10^{17}$ s) to get an upset rate. Table II shows the result of this extrapolation.

From this speculative exercise, and comparing the rates to those in table I, the conclusion is that already in the outer parts of the tracker, thermal neutrons could significantly contribute to the upset rate. According to this result, thermal neutrons might be the dominant cause of SEU in all other parts of the experiment.

Table II: Upset rates that the least and most SEU-sensitive SRAM circuits in reference [11] would experience in the low-energy neutron radiation environment of CMS.

<table>
<thead>
<tr>
<th>Least sensitive</th>
<th>Most sensitive</th>
</tr>
</thead>
<tbody>
<tr>
<td>[upsets/(bit s)]</td>
<td>[upsets/(bit s)]</td>
</tr>
<tr>
<td>Tracker</td>
<td>$10^9$</td>
</tr>
<tr>
<td>Exp. hall</td>
<td>$6 \times 10^{13}$</td>
</tr>
</tbody>
</table>

7. CONCLUSION

With the help of Monte Carlo simulation methods, an approach has been proposed leading to the estimate of upset rates in the CMS radiation environment. The need for the approximate definitions of a sensitive volume and a critical energy represents the dominant source of uncertainties of our predictions.

The comparison of simulated SEU cross-sections with experimental data of submicron circuits irradiated with mono-energetic proton beams indicates that the shape of the cross-section curve is correctly reproduced. The under-estimate of its absolute value might be attributed to an under-estimate of the sensitive volume size.

The calculation for the CMS tracker radiation environment gives estimated upset rates varying from $8.3 \times 10^7$ to $8 \times 10^{16}$ upset/(bit s) depending on the distance from the beam line. These results were obtained under the assumption of a $1 \mu m^3$ sensitive volume (SV) and 1MeV critical energy. Simulations showed that all these results are very sensitive to the size of the SV and the critical energy chosen.

In the outer parts of the tracker and in all other parts of the detector, thermal neutrons might significantly contribute to the SEU rate.

The comparison of the simulation results indicates that the SEU probability in the LHC is only about 60% higher than the one for mono-energetic proton beams. Therefore, 50-300MeV proton beams can be effectively used to evaluate circuit SEU susceptibility in the LHC radiation environment, and usefully used to correlate simulation results and experiments, hence validating the estimated upset rates.

All the results presented are valid for static memory elements, but not for dynamic logic. In that case, the critical charge for upset, hence the critical energy, is lower. Therefore, the SEU rate is higher for dynamic logic circuits.

REFERENCES

STATUS OF THE RD48/ROSE COLLABORATION

S. J. Watts, Brunel University, Uxbridge, UB8 3PH, UK. (email: Stephen.Watts@brunel.ac.uk)

Abstract

The status of the RD48 or ROSE (R&d On Silicon for future Experiments) Collaboration is described.

1. INTRODUCTION

This paper describes the work of many groups working within the RD48 or ROSE Collaboration with the specific objective of defect engineering more radiation tolerant silicon detectors [1]. Defect engineering involves the deliberate addition of impurities to silicon in order to effect the formation of electrically active defect centres and thus control the macroscopic parameters of devices. If current models are correct, then the key ingredients to change are oxygen and carbon. Oxygen and carbon capture silicon vacancies and interstitials respectively. The carbon is converted from a substitutional to an interstitial position which is mobile at room temperature. It eventually forms stable defects with oxygen and substitutional carbon. Diffusing silicon interstitials and vacancies escape from a region of silicon where an intense concentration of Frenkel pairs are produced by a Primary Knock-On Atom (PKA). The PKA is produced by the incident radiation. Vacancies can react with one another to form multivacancy defects. This leads to clustering of intrinsic defects around the PKA production point. This so-called “cluster” region controls many of the electrical parameters of irradiated silicon.

Various types of silicon are being evaluated with resistivities above 500 Ω cm. These are high resistivity epitaxial, FZ Si-Ge, FZ Si-Tin, carbonated FZ and oxygenated FZ. Oxygenated FZ has been grown using gas doping by Polovodie in Prague. However, oxygen concentrations greater than about 10^{16} cm^{-3} are not possible with this method. ITME in Poland have recently grown highly oxygenated FZ using a “jet” technique - this involves a quartz ring plus oxygen gas jet around the float-zone. ITME in Poland have also grown high resistivity epitaxial layers as thick as 200 μm. MACOM in the USA have grown epitaxial layers up to 150 μm thick. CZ material has also been studied. Tin doped material is important to study. Ref. [2] shows that tin highly suppresses divacancy production. Both Topsis and ITME have grown Si-Tin FZ. In both cases, the tin concentration was about 2 to 3 \times 10^{17} cm^{-3}. Figure 1 shows that most of the oxygen/carbon concentration variants have been made.

2. MACROSCOPIC EFFECTS

Four main macroscopic effects are seen in high-resistivity diodes following irradiation by MeV neutrons. The diodes are usually processed on 300 μm thick n-type material with a resistivity of around 4 kΩ cm. Similar effects are also seen following GeV proton and pion irradiation which also create cluster type damage. Macroscopic changes are found to scale with the Non-Ionising Energy Loss (NIEL). This has been calculated and can be used to relate the damage caused by particles of different types and energies. Thus, one needs only to refer to an equivalent 1 MeV neutron fluence. For brevity, this paper will use the term “fast neutrons” rather than “1 MeV equivalent neutron” when quoting fluences. A compilation of recommended NIEL values to use for various particles over a wide range of energies is given in reference [1].

![Figure 1 Oxygen and carbon concentrations in substrates investigated by the ROSE Collaboration.](image)

2.1 Effective Doping Changes

In a non-irradiated diode the space-charge results from shallow dopants in the silicon. Irradiation results in a build-up of negative space-charge in depletion regions due to the introduction of deep levels. The effective...
doping concentration, \( N_{\text{eff}} \), is inferred from the voltage required to obtain full depletion, \( V_{\text{FD}} \), which is,

\[
V_{\text{FD}} = \left( \frac{\text{Diode Thickness}}{2 \varepsilon_0 \varepsilon_s} \right)^2 e |N_{\text{eff}}| \quad \text{(1)}
\]

In equilibrium - no external bias - both n-type and p-type material become almost intrinsic after around \( 10^{13} \) cm\(^{-2} \) fast neutrons. However, under bias, the effective doping concentration is entirely controlled by radiation induced deep levels for fluences beyond \( 10^{13} \) fast neutrons cm\(^{-2} \). In an n-type diode, deep acceptors eventually cause the depletion region to grow from the n+ rather than p+ contact. The fluence at which this occurs is referred to as the "inversion fluence". Figure 1 illustrates that a detector which starts with a positive space charge - point B - has a negative space charge following irradiation - point A. The inversion point is marked as \( N_{\text{eff}} = \text{Zero} \).

It is important to note that CMS have found that heavily irradiated detectors must be biased by about twice the depletion voltage to give maximal signal to noise performance.

\[
\Delta I/\text{Volume} = \alpha f \quad \text{(2)}
\]

\( \alpha \) is around \((4 - 9) \times 10^{-17} \) Acm\(^{-1}\) immediately after irradiation.

2.3 Reverse annealing of the effective space-charge

Following irradiation to high fluences, the build-up of negative space-charge is seen to increase dramatically after several months for diodes kept at room temperature. This can be suppressed by keeping the diodes at about -5 °C. This is called "reverse annealing". The best fit to the data is found using a second-order process parameterisation [1]. However, the rate constant has been found to be fluence dependent. This means that a first-order disassociation or re-ordering process is responsible. The activation energy is 1.31 ± 0.04 eV. It takes several years for the process to saturate at room temperature. It can be accelerated by heating samples at 100 °C. The amount of reverse annealing is proportional to the irradiation fluence.

2.4 Charge collection efficiency

Silicon detectors are used to detect charged particles. These traverse the silicon producing about 24,000 electron-hole pairs in a 300 μm thick detector. At room temperature, about 10% of the charge is lost per \( 10^{14} \) fast neutrons cm\(^{-2} \). Recent experimental measurements [3] find that for temperatures below 100K fifty percent of the charge is recovered in detectors irradiated to \( 2 \times 10^{15} \) neutrons cm\(^{-2} \). The charge collection efficiency is still poor at 195K. This has been referred to as the Lazarus effect. In effect, the defects are frozen out. What is surprising is that there is still charge loss at 4K.

2.5 Annealing effects

Both the leakage current and the effective space charge anneal at room temperature following irradiation by fast neutrons. There is a beneficial recovery which occurs over about two weeks followed by the reverse annealing stage referred to above. The beneficial annealing stage affects both the leakage current and effective space charge. Reverse annealing only occurs to the effective space charge. The leakage current continues to anneal for years after irradiation. On can write the effective space charge in an initially n-type substrate as,
\[ N_{\text{eff}} = N_{\text{eff,0}} - N_S - N_{\text{BA}} - N_{\text{RA}} \]  

(3)

where \( N_{\text{eff,0}} \) is the starting doping concentration, \( N_S \) is the stable concentration of radiation induced defects, \( N_{\text{BA}} \) is the concentration of radiation induced defects that anneal out over a two week period at room temperature, and \( N_{\text{RA}} \) is the concentration of radiation induced defects that anneal over several months at room temperature. The fast neutron introduction rate for these concentrations are roughly 0.025, 0.015 and 0.06 cm\(^{-1}\) for \( N_S \), \( N_{\text{BA}} \) and \( N_{\text{RA}} \) respectively. The introduction rate for \( N_S \) is referred to as the \( \beta \) parameter. Some confusion can arise because the depletion voltage depends on the magnitude of \( N_{\text{eff}} \) and not its sign - note equation (1). This is illustrated in Figure 2. Take point B. This corresponds to a material which is initially n-type and has not been irradiated beyond the inversion point. Beneficial annealing will cause the depletion voltage to increase. If one now takes point A which corresponds to a material that has been irradiated past the inversion point, the same annealing process will cause the depletion voltage to decrease. Similar comments also apply to the effect of the reverse annealing process on the depletion voltage.

2.6 The Bottom Line

Four key parameters describe the behaviour of the irradiated silicon detectors and determine their lifetime and operating conditions in high radiation environments. These parameters are:

a) The leakage current parameter, \( \alpha \).
b) The introduction rate for stable acceptors, \( \beta \). This controls the operating voltage after the inversion fluence leading eventually to breakdown.
c) The inversion fluence. This is proportional to the initial doping concentration, \( N_{\text{imp}} \).
d) The introduction rate for the space-charge responsible for reverse annealing. This process can be inhibited by cooling the detector.

Finally, the charge collection efficiency is degraded for fluences beyond about a few \( 10^{14} \) n cm\(^{-2}\) due to trapping.

3. RESULTS

Progress has been made in two areas – new materials and in operating conditions. These are discussed in the following sections.

3.1 Material Development

With the important exception of the \( \beta \) parameter, it has proven difficult to achieve major changes to the fast neutron induced macroscopic parameters by altering impurity levels. However, substrates with high oxygen content are considerably less affected by gamma irradiation [4] compared to standard float-zone material. In this case no cluster region is formed. This means that the behaviour of neutron irradiated silicon is dominated by defect clusters. Silicon-tin should perform much better. The material tested to date only shows a small effect. However, it is likely that there is a threshold to the tin concentration before a dramatic reduction is seen in the divacancy production. In reference [2], the tin concentration was at least 1018 cm\(^{-3}\).

Some substrates show important differences compared to standard Float-Zone material. For instance, some MACOM epitaxial material shows effective doping changes after inversion that are a factor three better than normal – i.e. the \( \beta \) parameter is substantially lower. This is a significant improvement and is being studied further. The most probable explanation for the improvement is due to the fact that the material is highly compensated; boron is removed at a faster rate than phosphorus resulting in a positive space charge that balances the radiation induced negative charge. There is also clear evidence that high carbon concentrations make the material less radiation tolerant. Finally, in CZ material, reverse annealing changes are a factor two less, [5]. However, higher resistivity material is needed for detectors and this is being pursued.

The leakage parameter, \( \alpha \), has been found to be material independent, [6]. Defect clusters appear to be the main microscopic cause of the leakage current.

As mentioned earlier, the one parameter that can be altered, and ultimately controlled, is the \( \beta \) parameter. This parameter for various substrates is shown in Table 1. Note that this parameter scales with NIEL for standard material. It does not for some substrates. This is being studied further.

| Table 1: The \( \beta \) parameter in various substrates, [7]. |
|-----------------|-----------------|-----------------|
| Material        | \( \beta \) (cm\(^{-3}\)) | \( \beta \) (cm\(^{-3}\)) |
|                 | 1 MeV neutrons  | 24 GeV/c protons |
| Standard FZ     | 0.028           | 0.016           |
| ITE processed   |                 |                 |
| Standard FZ     | Not Available   | 0.012           |
| SINTEF processed|                 |                 |
| Oxygen Jet FZ   | 0.020           | 0.005           |
| MACOM           | 0.007           | 0.006           |
| Epitaxial       |                 |                 |
| Carbon enriched FZ | 0.028       | 0.033           |

Note that diodes processed on the same material by ITE and SINTEF show different values of \( \beta \) although results from more diodes are needed. Defect concentrations
after proton irradiation in similar SINTEF diodes are also lower, [8]. Some process dependence appears probable.

3.2 Operating Conditions

It should be noted that improved tolerance to radiation effects has been achieved due to the use of multi-guard structures. These allow much higher operating voltages to be applied. In addition, there have been two recent developments in this area, both aimed at operating silicon detectors after heavy neutron irradiation - beyond few $10^{14}$ n cm$^{-2}$. These developments are:-

a) To operate heavily irradiated detectors under forward bias, [9]. The I/V characteristics of heavily irradiated silicon are almost ohmic - it is similar to GaAs in that it becomes a relaxation rather than a lifetime material. At 250K the forward current is no worse than the radiation induced generation current. As a rule of thumb, the voltage required to obtain the same charge collection efficiency (CCE) under forward as compared to reverse bias is about a factor ten lower.

b) To cool the detector to below 100K, as noted in Section 2.4. The CCE improves dramatically. This behaviour has been broadly understood but further work is needed. Operation up to fluences of $10^{16}$ n cm$^{-2}$ may be possible under these conditions.

4. CONCLUSIONS

The following conclusions can be drawn from the data that has been collected over the last year or so:-

a) The $\beta$ parameter can be reduced by at least a factor of 2 to 3. If this can be achieved reliably then this will provide safe operation of the detectors in the LHC experiments over a ten year period. The reason for the lower $\beta$ parameter, in most cases, is thought to involve the compensation level of the material and the oxygen and carbon concentrations. To oversimplify the recipe for such a material, it needs to be suitably compensated and the oxygen/carbon ratio must be greater than one.

b) The compensation level of the starting material is important for all silicon substrates and should be checked before it is used for detector production. This is possible using photoluminescence.

c) Low resistivity (1 K ohm cm) material should be used. This inverts at a higher fluence and reduces the final operating voltage after 10 LHC years, [1]. Recent results from CMS, [10], confirm this conclusion. ATLAS, [11], find no improvement. This may be due to the compensation level in the material and needs further study.

d) Some possible process dependence has been observed. The reason for this is not clear. It may be difficult to elucidate the reason due to commercial considerations.

e) Oxygenated FZ made using the jet technique performs better than standard FZ if irradiated with protons. The material needs to be studied with charged pions and the reason for the NIEL violation (compared to neutrons) needs to be understood. Diffused oxygen material has been tested using neutrons and showed no improvement. This material will be tested using protons.

f) Silicon-tin has yet to prove itself. Tin concentrations beyond $10^{14}$ cm$^{-3}$ at least are needed. It is not trivial to make such material with the required resistivity.

g) CZ material looks promising and higher resistivity substrates are being investigated – e.g magnetic CZ. The reduction of the reverse annealing by a factor 2 is not understood, but gives some hope that this process may be understood and controlled.

h) Cryogenic operation looks to be a very promising way to operate silicon detectors after very high neutron fluences. Further work is needed to understand such operation and develop low mass cryogenic systems. Forward operation also needs further investigation. Both the RD39 and RD48 collaborations are investigating this operational mode in more detail. Various silicon substrates will be tested at cryogenic temperatures - some may perform better if used at 100K.

Table 2 provides a simplified overview of various choices for silicon detectors in high radiation environments.

<table>
<thead>
<tr>
<th>Material or Operation</th>
<th>Maximum Fluence ncm$^{-2}$</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard High Resistivity FZ (4 kOhm cm)</td>
<td>Strips $10^{14}$, Pixels $10^{15}$ (with partial depletion).</td>
<td>Guard Ring and high voltage operation needed. Operation marginal at the maximum fluence quoted.</td>
</tr>
<tr>
<td>Standard Low Resistivity FZ (1 Kohm cm)</td>
<td>Strips $10^{14}$, Pixels $10^{15}$</td>
<td>Operational safety margin to these fluences</td>
</tr>
<tr>
<td>$\beta$ controlled material</td>
<td>Strips Few $10^{15}$, Pixels $&gt;10^{15}$</td>
<td>CCE will limit maximum fluence.</td>
</tr>
<tr>
<td>Cryogenic Operation (100K)</td>
<td>Up to and beyond $10^{14}$</td>
<td>More studies required.</td>
</tr>
</tbody>
</table>
Note that pixel detectors can withstand higher fluences as the leakage current and noise levels per element are lower.

5. ACKNOWLEDGEMENTS

I am grateful to the other co-spokesmen of the ROSE Collaboration, Gunnar Lindstrom (Hamburg University) and Francois Lemeilleur (CERN) for their advice and help. The ROSE Collaboration consists of over 30 institutions worldwide. Without the efforts of these institutions, this paper would not be possible. In addition, the efforts of the various silicon wafer producers mentioned above, as well as diode processing by ITE, Poland, DIOTEC, Slovak, Canberra, Belgium, SINTEF, Norway and Micron Semiconductor, UK, were vital for this work. Support from the UK Particle Physics and Astronomy Research Council (PPARC) is acknowledged.

6. REFERENCES

3. V. Palmieri et al., Preprint BUHE-98-06.
7. A. Ruzin et al., Paper to be presented to the 6th Int. Conf. On Advanced Technology and Particle Physics, Como, Italy, October 5-9 1998. To be published in NIM A.
11. P. Allport, Private Communication.
ELECTRONICS FOR TRACKERS
ELECTRONICS FOR TRACTORS
Dead-time Free Pixel Readout Architecture for ATLAS Front-End IC

Lawrence Berkeley National Laboratory
1 Cyclotron Road, Berkeley, California 94720

Abstract

A low power sparse scan readout architecture has been developed for the ATLAS pixel front-end IC. The architecture supports a dual discriminator and extracts the time over threshold (TOT) information along with a 2-D spatial address of the hits associating them with a unique 7-bit beam crossing number. The IC implements level-1 trigger filtering along with event building in the end of column (EOC) buffer. The events are transmitted over a serial data link with the protocol supporting buffer overflow handling by appending error flags to events.

This mixed-mode full custom IC is implemented in 0.8μm HP process to meet the requirements for the pixel readout in the ATLAS inner detector. The pixel array and the EOC have been tested and the test chip meets the ATLAS specifications of ambiguity free data readout at 40MHz data rate with a 3V supply.

SUMMARY

The LHC beam crossing rate of 40MHz requires a balance among many conflicting front-end requirements like low power, fast readout, dead-time-less operation, good noise isolation in a large array of about 3000 pixel channels[1]. The column architecture with distributed intelligence and the data bandwidth shrinking from the leaf nodes (pixels) to the root of the tee (serial data out) meets the high data rate ATLAS requirements. The pixel readout chip is based on the column architecture with 18 columns (organized in pairs) containing 160 pixels. This massive parallelism provides over 2Gb/s data bandwidth between pixels and EOC, minimizing the pixel dead-time. Data from a column pair is transferred into an EOC buffer location using a handshake implemented by the column-EOC-arbitration unit (CEU), as shown in Figure 1. The 20-deep EOC buffer locations receive data from a pixel column pair within a cycle of hit detection, implementing a dead-time-less system.

The analog front-end consists of a preamplifier-shaper and a dual discriminator [2]. The digital back-end of the pixel associates hits with a unique beam crossing and extracts TOT information from the level (high threshold) and time outputs (low threshold) of the discriminator. This is achieved by distributing a 7-bit gray coded time-stamp to the pixel array which latches the leading (LE) and trailing edge (TE) of the discriminator pulse in a pixel RAM. In addition to the time information the pixel provides an ID in the form of a 8 bit ROM address. The pixel supports a sparse scan readout (zero suppression) to optimize the data bandwidth usage between the columns and EOC. A provision to vary the handshake rate is implemented for dead-time and clock frequency tradeoff. A fast priority scan path is implemented by having a low delay in the critical data path. Other enhancements like priority look ahead, to enhance the readout speed and data driven self-timed logic for low power, are also implemented to achieve dead-time-less low power operation.

The CEU transfers event data from a pixel column pair to EOC buffers. It implements left-right column priority arbitration and a first level of data sparsification by a zero suppression readout of columns. A single 4-phase clock is generated to synchronize multiple simultaneous tasks like data sparse scan, bit line pre-charge, reading data from pixel memory, writing data into EOC buffer locations. The clock frequency is determined by the worst case timing of the above activities and is tunable in 4 discrete steps between 5MHz and 40 MHz. This programmable feature helps
maintain pessimism while minimizing pixel dead time and optimizing column-EOC data bandwidth. The 4 phases help reduce the risk of skew in the 8mm long handshake distribution.

The EOC consists of a 20 deep memory to read data out of every pixel column pair. The EOC implements second level of data sparsification by buffering data and making level-1 trigger coincidence. An EOC word contains RAM and CAM (content addressable memory) memories for data storage, data driven addressing for filtering and data retrieval. The data associated with a trigger is retained until readout. During the readout phase event building is implemented by retrieving data from EOC buffers using a 2-D sparse scan. The EOC implements a number of critical activities in parallel including pixel data transfer using a 5-40 MHz clock, trigger filtering and data rejection with a 40MHz signal and data readout with a 10MHz handshake.

The readout control unit (RCU) consists of a state machine that generates timing signals for trigger filtering and data rejecting. The 7-bit variable-latency time stamp is generated by a pair of variable offset gray code counters. The latency (LAT) can be varied between 25ns and 3.2us by downloading a configuration into command registers. The time stamp index is distributed to the pixels and a time stamp compare code, offset by a latency period, is used for trigger filtering the EOC. A 16-deep FIFO (first-in first-out static memory) implements a trigger memory to buffer up to 16 active triggers on the chip and also generates trigger accept index and trigger accept stamps. A 7-bit modulo-subtractor is implemented to extract the TOT from a 7-bit wrapped around gray code time-stamp. The RCU implements a data push architecture. As soon as a triggered event is buffered, the RCU initiates a readout sequence by transferring data from EOC to a 26-bit data serializer which transmits data over a serial data link using LVDS (low voltage differential signaling) drivers. The data is formatted into events by appending a header and a trigger number to the 2-D spatial address and TOT information of each HIT. In addition an end of event word is transmitted when all data associated with an event is read out of the EOC locations. An error flag handling capability is also built into this serial data protocol to handle EOC buffer overflow and to indicate possible data corruption.

The pixel column and the EOC have been tested and the test chip meets ATLAS specifications of ambiguity free data readout at 40MHz beam and trigger rates with a 3V supply. The digital pixel logic is implemented in 50µ x 150µ area while the analog front-end with the bump bond pad also occupies a similar geometry. The design uses 0.8µ HP 3-metal process with one of the metal layers used to shield fast digital signals from the sensitive analog front-end. The 160 pixel x 18 column die area is approximately 80 mm² with less than 25% inactive (area excluding the pixel elements).

II. REFERENCES


MAREBO, A FULL RADHARD PIXEL DETECTOR PROTOTYPE FOR ATLAS

L. Blanquart*, D. Calvet
IN2P3 / CPPM, Case 907, 163 Avenue de Luminy, F-13288 Marseille Cedex 9, France

P. Fischer
Physikalisches Institut der Universität Bonn, Nussallee 12, D-53115 Bonn, Germany

ABSTRACT: MAREBO is a radhard pixel front-end chip for ATLAS designed in the DMILL radhard BiCMOS technology. The chip is the latest generation of the ATLAS pixel chips of the FE-A prototyping programme. It has been submitted in June 1997 and received in November 1997. It contains 12 columns of 63 pixels each. The main goal of this chip is to reach LHC requirements in terms of electrical specifications and radiation tolerance. The pixel size has been extended in order to fit with existing n+/n and diamond detectors. MAREBO has been intensively measured in lab and without n+/n sensors and has been successfully tested in beam before and after irradiation. All these results have demonstrated that the chip meets analog electrical requirements for the ATLAS pixel detector at LHC. Irradiation measurements of the analog section are also discussed.

I. INTRODUCTION

For many experiments, silicon pixel detectors, featuring high spatial resolution and real two-dimensional reconstruction, are of considerable interest. This interest has been recently focussed by the successful implementations of the CERN Omega [1,2] experiment and the DELPHI [3,4] detector at LEP.

In the foreseen ATLAS[5] and CMS[6] detectors at the future CERN collider (LHC), a high radiation level [7] is expected. Electronics for vertex detectors, especially for the pixel detectors which can be placed very close to the interaction point (4cm, 11cm and 14cm), requires radhard technologies. DMILL is a new radhard technology developed at CEA-LETI (Grenoble, France) and industrialized since mid 1997[8] at TEMIC/MHS (Nantes, France). It can accommodate these severe constraints along with high speed operation, mixed analog-digital implementation and low noise needs[9,10]. It integrates monolithically PPFET, vertical NPN and CMOS devices on a thick silicon film on insulator (SIMOX plus epitaxy). The SOI substrate, along with insulating trenches, ensures complete dielectric isolation.

The very encouraging results obtained with the ATLAS pixel prototypes during the development of the DMILL technology[11,12,13] have demonstrated that the severe demanding LHC requirements can be reached. In parallel, in order to optimize the learning, time and financial contraints, 2 Front-End designs have been submitted in the AMS BiCMOS 0.8um technology: Beer&Pastis[14,15] and the real scale FE-A demonstrator (PIRATE)[15].

The MAREBO chip is the latest generation of the ATLAS pixel chips of the FE-A prototyping programme. The main goal of this chip is to meet the ATLAS pixel requirements for the analog section in a radiation hard technology. It has been designed in the DMILL rad-hard BiCMOS process and was submitted in the first Multi-Project run (MPW) offered by TEMIC/MHS in 1997. MAREBO has been successfully bump-bonded to n+/n and diamond sensors and has been tested in the lab as well as in beam at CERN before and after irradiation.

II. THE MAREBO CHIP

The chip has a size of 7.3mm*5.5mm with an active area of 5.2mm*3.2mm. It contains 12 columns of 63 pixels each with a layout area of 50um*397um. The actual pixel pitch is slightly larger (433.4um) in order to fit existing n+/n as well as diamond detectors. Every pixel cell contains an analog part with a preamplifier/comparator circuit for negative input polarity, a 3-bit DAC for threshold fine adjust, a readout section for time tagging and analog information using the Time-Over-Threshold technique[16], and a control section which allows to inject and mask pixels, load DAC values and to monitor the discriminator signals through the hitbus (fastOR).

The circuits of the analog part and of the control section are nearly identical to the circuits implemented in the ATLAS pixel FE-A demonstrator (PIRATE) such that a comparison of the level of integration in DMILL and the AMS BiCMOS 0.8um technology (Austria Mikro Systeme) is possible: the size of the analog parts is almost identical (144 um for DMILL and 141 um for AMS including the bump bond pad) while the control logic takes 20% more space in DMILL. Every transistor is isolated by insulating trenches in DMILL but the «trench to trench» rule is half as stringent as the «well to well» or «active to well» rules in a standard technology. The transfer to DMILL has nearly no impact on the analog layout size because transistors in analog designs have usually dedicated substrate connections. In digital layouts, which are principally larger in DMILL than in AMS, the wells can be merged to avoid the «well to well» rule so that they can be shrunk by about 20% with respect to standard DMILL layouts. Nevertheless the size of the DMILL design is only slightly larger than the present AMS design.

The Fig. 1. depicts the layout of the pixel cell.

---

* Corresponding author: Tel +33 4 91827243, fax +33 4 91827299, e-mail: blanquart@cppm.in2p3.fr
III. CHIP PERFORMANCE

The amplifier is a folded cascode charge sensitive amplifier with a feedback capacitance of 3 fF buffered by a nMOS source follower. These two full-CMOS stages are fed back by an improved version of the DC feedback circuit already proven in the previous chips[13]. Special attention has been paid to simulate the cell with worst case models which include process variation and parameter shifts after high levels of irradiation.

![Fig. 2. Output signal of the MAREBO preamplifier without detector: Input charges of 5, 10, 15, 20 and 25 ke (horiz. scale: 200 ns per div., vert. scale: 200 mV per div.).](image1)

![Fig. 3. Output signal of the MAREBO preamplifier with detector: Input charges of 6, 8, 10, 12 and 14 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).](image2)

![Fig. 4. Output signal of the MAREBO preamplifier without detector: Feedback current of 1, 2, 3, 4 and 8 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).](image3)

Fig. 2 to Fig. 5. show the output of the MAREBO charge sensitive amplifier monitored through an on-chip buffer with a gain of about 0.95 for various input charges, feedback currents with and without detector. Charge is injected by applying a voltage step to a capacitor in the pixel cell. All measurements are taken at the nominal power consumption of 40 µW for the analog part of the pixel.

![Fig. 5. Output signal of the MAREBO preamplifier with detector: Feedback current of 0.25, 1, 2, 3 and 5 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).](image4)

Fig. 2 to Fig. 5. show the output of the MAREBO charge sensitive amplifier monitored through an on-chip buffer with a gain of about 0.95 for various input charges, feedback currents with and without detector. Charge is injected by applying a voltage step to a capacitor in the pixel cell. All measurements are taken at the nominal power consumption of 40 µW for the analog part of the pixel.

![Fig. 5. Output signal of the MAREBO preamplifier with detector: Feedback current of 0.25, 1, 2, 3 and 5 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).](image5)
The width of the discriminator output signal increases when very high leakage currents are injected, and tests to a 200 fF test capacitor and a threshold of 2900 e for an amplifier connected to a sensor diode. As depicted in Fig. 9., the behavior of the charge sensitive detector. The time walk decreases even further which is more than expected after 10 years of LHC operation.

This technique allows the minimum charge to be reduced to 500-600 electrons above the threshold for a pixel cell with leakage currents of 100 nA shows that the shaping time is slightly decreased but tends to saturate after 50 nA. This effect is clearly demonstrated when very high leakage currents are injected, and tests show that the threshold is only slightly increased even after values greater than 200 nA.

The cell-to-cell threshold mismatch is a crucial point for realizing an accurate pixel detector. In particular, it determines the minimum threshold that can be set. Pixels with thresholds much lower than the average value would produce too many noise hits. Although good dispersion results were obtained without independent pixel adjust on the previous Beer&Pastis chip (σ = 90e, [14,15]) and on the MAREBO chip (σ = 93e, see Fig. 10.), a 3-bit DAC for threshold fine tuning has been implemented in each cell in order to eliminate tails in the dispersion distribution and to adjust the thresholds after high level of irradiation when random parameter shifts of detector and electronics may occur and the available charge will be smaller. This fine-tuned threshold is based on a network of switched pMOS resisters which locally control the comparator bias system. The 3 bits are statically stored in registers in the control logic part of every pixel. They are loaded via a shift register which runs across all pixel cells. A control current Itrim is used to set the range of thresholds covered by the DAC. i.e. the threshold shift per LSB (least significant bit). Fig. 11 shows the response of the same pixel for increasing input charges for the 8 possible DAC settings. The threshold change by about 100 e per LSB for Itrim = 1μA is in accordance with the simulation. The threshold change per LSB is a linear function of Itrim and the DAC itself has a differential non-linearity of 14% which is better
than required for this application. No extra noise is induced by the adjustment circuit. Fig. 10. depicts the distribution of the thresholds of a complete chip before and after threshold tuning. The tuning is performed in a two step operation, First, the Itrim value is determined by searching for the largest variations, second the DAC bits are calculated. The spread after adjustment is reduced to 40 e.

![Fig. 10. Distribution of the array threshold before and after adjustment](image)

Fig. 10. Distribution of the array threshold before and after adjustment

![Fig. 11. Discriminator response for increasing input charge for the 8 possible DAC settings for Itrim = 1 µA.](image)

Fig. 11. Discriminator response for increasing input charge for the 8 possible DAC settings for Itrim = 1 µA.

The cross-coupling between pixels with bump bonded sensor is defined as the ratio of the signal induced on one neighbour and the signal on the central pixel. Note that the pixels of the MAREBO chip have a length of 433.4 µm so that an increased cross coupling compared to 300 µm is expected. The method for measuring crosscoupling is described below. Using the on-chip injection circuitry, the threshold of an arbitrary pixel is determined. The pixel is then pulsed together with one or two neighbours. Due to cross coupling, a smaller injected charge is enough to fire the central pixel in 50% of the injections so that effectively, a threshold reduction is observed. For thresholds of typically 3000 e, 5000 e and 9000 e, shifts are observed when one neighbour is also injected. This leads to a cross coupling of 2%.

IV. IRRADIATION OF MAREBO

MAREBO has been irradiated in a 24 GeV proton beam at PS (CERN). The maximum flux was 2.00 × 10¹³ p cm⁻² h⁻¹ (note that this flux was reached by performing a complete beam)

![Fig. 12. Output signal of the MAREBO preamplifier after dose/fluence of 0, 4 Mrad(SiO₂)/1.14·10¹⁴ p/cm², 10 Mrad(SiO₂)/3.10¹⁴ p/cm² and 24 Mrad(SiO₂)/7.10¹⁴ p/cm² with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.)](image)

Fig. 12. Output signal of the MAREBO preamplifier after dose/fluence of 0, 4 Mrad(SiO₂)/1.14·10¹⁴ p/cm², 10 Mrad(SiO₂)/3.10¹⁴ p/cm² and 24 Mrad(SiO₂)/7.10¹⁴ p/cm² with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.)

The peaking time is increased due to extra-load presented during irradiation.

![Fig. 13. Measured leakage current of the sensor versus the fluence (the detector voltage has been increased from -150V to -600V during irradiation).](image)

Fig. 13. Measured leakage current of the sensor versus the fluence (the detector voltage has been increased from -150V to -600V during irradiation).

![Fig. 14. Measured Equivalent Noise Charge versus fluence for 2 different feedback current, i.e. 2 different recovery time.](image)

Fig. 14. Measured Equivalent Noise Charge versus fluence for 2 different feedback current, i.e. 2 different recovery time.
profile using one pixel of a MAREBO chip connected to a sensor) and the nominal temperature during and after irradiation was -7°C. In total, 4 MAREBO chips connected to a sensor and 2 MAREBO chips without detector have been irradiated and out of these 6, one MAREBO chip with detector and one without detector have been tested on-line.

V. TEST BEAM BEFORE AND AFTER IRRADIATION

MAREBO has been tested in beam at H8 (CERN). As several chips were tested before irradiation during the May-June 1998 programme, the August-September 1998 period was used to test irradiated chips (kept at -7°C). The threshold was 3500e.

Fig. 15. Measured threshold variation of the pixel cell versus fluence.

Fig. 16. Correlation between pixel position and telescope prediction for MAREBO 2 before irradiation.

Fig. 17. Efficiency versus trigger delay for MAREBO 2 before irradiation.

Fig. 18. Analog information using the TOT technique for MAREBO 2 before irradiation (for a single hit pixel or 2 adjacent hit pixels).
Fig. 16. to 18. are issued from data taken on MAREBO before irradiation. Fig. 16. shows the perfect correlation between telescope prediction and pixel position for one of the MAREBO chip. Fig. 17. depicts its efficiency versus trigger delay. As the incoming particle is not synchronized to the 40MHz clock used to transfer data out the chip, the «In-Time» efficiency depends on the delay between the generated trigger with respect to the rising edge of the clock signal[17]. Fig. 17. has been reconstructed using a Time to Digital Convertor (TDC) and shows an efficiency of more than 99% along with a large plateau (which will drastically ease the time of the trigger delay for a huge number of chips at LHC). Fig. 18. shows the analog information and the MIP is clearly visible (typ. 27 bunch crossing periods).

Fig. 19. to 21. depicts the same measurements on the same MAREBO chip after 24Mrad(SiO2)/7 10^{14}p.cm^{-2}. A perfect correlation between telescope prediction and pixel position is observed (Fig. 19.) as well as an efficiency of more than 95% (Fig. 20.). The change (before and after irradiation) between the absolute trigger delay is due to different Lemo cables. A time reduction of the TOT is observed (Fig. 21.) after high level of irradiation. This effect is due to the faster shaping time of the preamplifier output signal (see chapter IV.) and the reduction of created charges in the sensor (At this point, the detector is partially depleted).

VI. CONCLUSION

Lab tests as well as beam tests before and after irradiation have demonstrated that the MAREBO chip meets the demanding LHC requirements for the analog section in a radiation hard technology. This is the first radhard package (electronics+sensor) for the ATLAS pixel detector which remains fully functional in beam after very high level of irradiation.

The analog front-end of the MAREBO chip will be implemented in the DMILL full scale demonstrator by the beginning of 1999.

MAREBO chips connected to diamond detector are currently under test and will be tested in beam in the very near future.

VII. ACKNOWLEDGMENT

The authors wish to thank the ATLAS pixel community, particularly:
- Thierry Moutuy and Francesco Ragusa for their work on the testbeam analysis on the MAREBO chip.
- Pierre Delpierre for his work on the testbeam organization of the MAREBO chip.
- Yves Gally, Patrick Breugnon and Jean-Claude Clemens to have developed the MAREBO acquisition.
- Jens Wuestenfeld for his precious help during the irradiation period.
- The sensor community to have produced the MAREBO silicon sensor in the frame of the ATLAS sensor development programme.
REFERENCES

Abstract

The CMS pixel detector will be equipped with analogue readout of moderate accuracy (3-4 bits). The analogue front-end consists of a charge sensitive preamplifier and shaper. A comparator with programmable pixel threshold trimming identifies hit signals within one bunch-crossing. The readout is organized in a double column of pixels. A column drain architecture has been chosen which can cope with the large amount of data. In the present design a double column of pixels is searched for hits after receiving a valid hit signal. We have implemented a token-bit mechanism to skip non hit pixels. Using an active bypass circuit a skipping frequency of up to 1.6 GHz has been verified. We have measured a low cross-talk of 750 electrons from the digital signals to the preamplifier input which is far below the anticipated operating threshold of 2500 electrons. The hit data are stored in the column periphery of the front-end chip waiting for the level-1 trigger confirmation.

1 INTRODUCTION

The main purpose of the pixel system (see Fig. 1) is to provide unambiguous three-dimensional tracking points. In order to allow an efficient tagging of jets as well as of other objects the tracking must extend as closely as possible towards the reaction vertex. The CMS pixel system [1] will have two barrel layers and two end disks on each side of the barrel. The layers are composed of modular detector units which consist of the Si-sensors bump-bonded to the readout chips. The final readout chip will cover 53x52 pixels with a square pixel size of 150x150 μm². Table 1 summarises the main parameters of the barrel. The pixel system envelope extends from 3.7 ≤ r ≤ 21 cm and for −50 ≤ z ≤ 50 cm.

At radii smaller than 10 cm the hostile radiation environment will reduce the lifetime of both sensors and readout chips below the expected lifetime of the experiment. Therefore the pixel detectors placed closest to the beam must be replaced at least once during the experiment. To profit from the improved secondary vertex resolution at very small radii, it is proposed to build the pixel barrel system in two stages. For the initial low luminosity period of LHC, radial positions down to 4 cm will be covered. When the luminosity reaches the design value the innermost sensors will be removed and modules added at larger radii.

Table 1: Parameters of CMS Pixel Barrel. Layer 1 and 2 form the low luminosity configuration, layer 2 and 3 will be used at high luminosity.

![Figure 1: Perspective view of the CMS pixel detector (high luminosity configuration).](image-url)
lifetime of the detectors. To profit from analogue interpolation, the readout should have a hit threshold not larger than 2000 - 3000 electrons. With the threshold at 5 $\sigma$ noise, the equivalent noise charge should remain below about 400 - 600 electrons. Leakage currents of up to 100 nA must be absorbed by the preamplifiers. In order to limit reverse annealing and the leakage current, the sensor temperature during running should be below -5 °C.

The position resolution has been calculated as a function of analogue pulse height granularity (number of ADC-bits) with a Monte Carlo simulation. The results indicate that a 4 bit digitisation of the analogue signal is sufficient to obtain most of the resolution that is possible.

2 FRONT-END ELECTRONICS

A schematic view of the pixel readout is shown in Fig. 3. Each sensor pixel is connected via a bump bond to its own readout circuit on the readout chip (Pixel Unit Cell, PUC). Two PUC columns form a double column, which represents an independent readout unit controlled by a circuit sitting in the column periphery (see Fig. 3). Local bus lines connect all PUC’s of a double column with the column periphery, one of them being the Column OR which combines all PUC’s in the double column into a global OR.

The circuit of each PUC can naturally be separated into two functional blocks. The analogue block amplifies the signal charge from the sensor. If the signal is above a tunable threshold, the periphery is notified via the Column OR. The column periphery registers the associated bunch crossing number (time stamping) and sends a token signal up and down the double column, bypassing empty pixels. In the readout block of the hit pixels the token signal initiates the transfer of pixel address and analogue signal, which are stored in a data buffer located in the periphery, waiting for the first level trigger (1LT). The confirmed time-stamps with their associated signals and addresses are transmitted directly from the periphery through analogue optical links to the front-end driver in the counting room, where digitization is performed. In the next sections we will describe the performance of the testchips, which were developed at PSI in the radiation hard DMILL technology [3].

2.1 Analogue Front-End

Fig. 4 shows a pixel unit cell (PUC) with separate analogue block and digital readout block. As a general strategy we try to keep the number of transistors in the PUC as small as possible. This can be achieved in transferring many tasks of the readout to the column periphery.
For signal amplification we use a charge sensitive preamplifier and shaper configuration. The leakage current from the DC coupled silicon pixel is automatically absorbed through an additional resistor in the feedback path of the preamplifier. A number of different preamplifier circuits have been implemented in order to study their speed and noise performance before and after irradiation [4]. Fig. 5 shows the output pulse shape with a cascode circuit used for the preamplifier. This circuit uses a p-FET input transistor. After irradiation with 100kGy 1.1 MeV Photons and with a 45 fF capacitance at the input we measured a noise of 190 erms. This is expected to increase to ~ 250 erms with a detector bump bonded to the input (~ 80 fF total capacitance).

One of the most critical elements in the pixel analogue block is the comparator stage which must be as robust as possible against irradiation effects. Fig. 6 shows the simplified schematics of such a comparator stage. The basic idea is to stabilise its working point through a forward diode characteristics expected to be rather invariant under irradiation. Since the comparator is AC coupled a constant output offset is fixed by the forward voltage drop of the diode used as a feedback element. This voltage drop is generated by bleeding a small bias current into the input node. Due to the very steep diode characteristics, one expects only small changes in the comparator output offset even for rather large irradiation induced variations of the bias current. The diode stabilised comparators have been irradiated to 100 kGy. Operating at a threshold of ~ 1950 electrons we observed a rms spread of about 200 electrons after irradiation. A time-walk curve of this comparator with the preamplifier and shaper chain explained above is shown in Fig. 7.

![Figure 6: Basic schematics of a diode stabilised comparator circuit.](image)

2.2 Column Drain Architecture and Hit Search Logic

The level 1 trigger latency time in CMS will be 3.2 µs (128 bunch crossings). With the expected hit frequencies the probability of a pixel being hit again at another bunch crossing within 3.2 µs will be 2 - 4 \%. In the architecture chosen for the CMS pixel readout, the basic idea is to copy all pixel hits occurring in a pixel double column into the column periphery as soon and as fast as possible in order to free the pixels for the next hit (Column Drain Architecture). If this can be accomplished within typically 7 - 8 bunch crossings following the hit, then the probability of having a second hit in the pixel reduces to 0.14 \%. The bunch crossing number association to the pixel hits (time-stamping) can be done very efficient in the column periphery.

Without any extra measures the double column will suffer a dead time of about 10 \% during the draining of the hits down to the periphery. With relatively little increase in complexity the column drain mechanism can be made doubly buffered, i.e. during a token-bit scan, which on average will take several bunch crossing cycles, an additional time-stamp can be recorded. Its associated pixel hits are read out immediately after the readout of the previous hit is finished. This reduces

![Figure 7: Time-walk curve of the complete analogue block with diode](image)
the dead time to the 0.5 % level.

The test of a high speed bypass mechanism is crucial for the Column Drain Architecture operation. In the DM.PSI32 chip (DMILL) we realised a pixel unit cell with the full architecture that was used in various column configurations for tests of speed and crosstalk behaviour to the analogue block [5].

The crucial part in the pixel readout block is an active bypass circuit that allows a fast token bit transfer skipping empty pixels. Fig. 8a shows the transistor schematic of the basic circuit idea. For empty pixels the hit flip-flop leaves the bypass switch of the token line closed. The circuit is based on a precharge logic with positive feedback for speed acceleration. The transistors used for load operation are shown in grey. In the stand-by mode, the token line and the load line are high, waiting for the skipping readout procedure to start. Just before the column drain readout begins, the load line goes low. In Fig. 8b a reduced circuit drawing shows the crucial elements taking part in the token bit propagation. The bypass transistor is closed, representing a serial resistance that for long skips quickly becomes the speed limiting factor in a purely passive token bit bypass mechanism. As the token line (n-1) from the previous pixel goes low, the two transistors become conducting, discharge their node capacitances and therefore further accelerate the high to low transition for the next pixel. The discharge current of the token line capacitance during this very fast wave transition flows locally to the capacitance ground. The wave will propagate through all empty pixels at maximum speed until it reaches a hit pixel where the bypass switch has been opened. The running up wave is sensed and used to put the pixel data onto the column readout bus. After acknowledgement by the column periphery the bypass switch is closed, allowing the token wave to continue to the next pixel hit. We have measured the token wave delay time for different long pixel skips. The result is shown in Fig. 9a. A pixel delay time of 620 ps has been measured for a digital supply voltage of 4.5 V. The dependence of the skip frequency on different supply voltages is shown in Fig. 9b. The precise propagation speed is not critical, since the whole column drain system is based on a handshake mechanism. With the measured 1.6 GHz skipping speed a full column skip takes 65 ns. After irradiation with 100 kGy Photons from a $^{60}$Co source the skipping frequency is slightly reduced (1.2 GHz).

Great care has been taken to measure the crosstalk of the token wave mechanism onto the analogue pixel block. By lowering the comparator threshold of pixels while a token wave was propagated through these pixels a column internal crosstalk of 700 - 750 electrons was measured. Between columns an upper limit of $<450$ electrons could be measured [5]. With a foreseen pixel threshold of 2500 electrons there should be enough margin to tolerate this crosstalk.

3 CONCLUSIONS

The results obtained from the radiation hard prototype chips indicate that we are well within reach of the performance required at LHC. In particular the studies of crosstalk from the digital block to the analogue block show that this problem is less severe than previously feared. This is attributed to the excellent properties of the SOI CMOS process and to special precautions taken in the layout and circuit concept.

A pixel threshold of 2500 electrons will be used which is far above the crosstalk level. With a minimal 5 $\sigma$ requirement this implies a maximal allowed noise level of 500 electrons after irradiation. It is possible to stay within the required limits unless there are unexpected high pixel capacitances way beyond 100 fF.

The time-walk should stay below 25 ns for the same pixel threshold in order to have a correct bunch crossing identification. In any case the analogue pixel readout offers a backup solution in case an unexpected system degradation (e.g. by heavy irradiation) would shift.
the small pixel hits into the next bunch crossing. They could be recovered by an off-line time-walk correction, provided the next bunch crossing is read out as well. With the foreseen number of fibre links this extra data transfer rate could be handled.

The adjustment of the pixel thresholds or the masking of very noisy pixels is indispensable for a large pixel system. If the variation after irradiation of the analogue block can be kept small (e.g. by the diode stabilised comparator) a reduction from 3 trim-bits to 2 bits (3 trim steps and pixel mask) could be envisaged.

All prototype results shown have been obtained with a power dissipation that is within the analogue power budget of 40 μW per pixel.

4 REFERENCES

Abstract

The effects of radiation induced faults in an analogue CMOS I.C. have been investigated by applying a testing method formerly developed to detect hard and soft faults in linear analogue circuits. The test is performed on the analogue front-end of a test circuit for silicon pixel detectors employed in high energy physics experiments. Accessibility to the internal nodes of the circuit has been provided so as to make the output observable, in compliance with the standard P1149.4. Experimental results show that after different doses of expositions a higher sensitivity to the test method compared with the simple pulse response is achieved. Considerations about checking the chip functionality through the measure of the dynamic current power consumption are provided.

1. INTRODUCTION

A technique formerly developed for the diagnosis of single-input, single-output linear time-invariant analogue circuits [1], has been applied to the testing of a variety of contemporary analogue I.C. structures [2-6].

Essentially, the test methodology is based on the excitation of the circuit under test (CUT) by a suitable input stimulus consisting of a piecewise constant signal, referred to as Complementary Signal (Compsig) [1], whose characteristics are obtained from the knowledge (analytical or experimental) of the circuit singularities, and on the observation of the CUT response to this input in a well defined time instant where this response should vanish. A deviation from the nominal expected behaviour reveals the presence of a faulty condition either induced by a possible physical defect originated by the manufacturing process or caused by particular environmental or operating conditions such as nuclear radiation.

In general, the approach may be developed in either a specification driven or a fault driven stile. In this latter case, the starting point is the derivation of a "realistic" fault list from the knowledge of the circuit structure (technology and layout) on the basis of the "a priori" fault analysis [7] methodology. Then, a suitable fault simulation is set up [8] to check for the fault coverage of the given stimulus. Experimental results have proven the applicability of this methodology to a variety of circuits including simple time-continuous structures, switched capacitor filters and even complex mixed signal I.C.'s [6, 9].

Recently, an extension of this technique has been applied to test for malfunctions which may arise from high energy radiation induced degradation. In fact, when nuclear or space applications are concerned, some anomalous behaviours are frequently observed depending on the irradiation dose. In particular, in the field of nuclear applications, circuits are usually classified into rad-tol and rad-hard classes on the basis of their ability to tolerate radiation levels up to few Mrad, without apparent damage.

However, usually the characterisation of such damages is either carried out at single device level or for the whole circuit which often is a mixed signal one [8]. In this way, it is not possible or, at least, not easy to achieve a clear understanding of the effects of radiation damage on the single analogue sub-circuits, which would provide an essential information from the perspective of subsequent redesign actions.

For this reason, with reference to a typical high energy nuclear experiment [10, 11], we developed a way to provide access to internal nodes of a front-end circuit for silicon detectors [12], and applied the Compsig approach to detect possible anomalous behaviours in both DC and AC performances of the analogue part of the circuit.

Some experimental results clearly show the potentiality of this methodology.

The paper is organised as follows: first some considerations about the typical radiation damages in CMOS irradiated circuits are presented together with their implications at circuit level; successively it is explained how the test is organised in practice and the experimental results are reported for the analogue section of the pixel front-end. Then, the additional circuitry
needed to perform the test in practice is shown, and finally a possible test strategy which relies on the monitoring of the transient supply current (IDDQ) is presented.

2. TESTING FOR RADIATION DAMAGES AT CIRCUIT LEVEL

2.1 Radiation effects on CMOS IC's.

Bulk and surface effects are usually observed in a CMOS IC as a consequence of exposition to nuclear radiation.

In particular, the electrons and holes created by ionizing radiation have a high probability for immediate recombination, especially if no electric field is applied. With higher electric field strength the number of free charges increases. Because of their high mobility electrons are swept out almost immediately leaving the much slower holes behind [11]. Depending on the direction of the electric field, more or less holes move to the Si/SiO₂ interface where they are trapped, causing essentially an increase of the oxide charge Qox.

This positive oxide charge causes an electron accumulation underneath the Si/SiO₂ interface and therefore a higher voltage is needed to achieve the flatband condition, leading to a shift of the flatband voltage of:

\[ \Delta V_{FB} = \frac{q t_{ox}}{\varepsilon_0} \Delta N_{ox} \]

with \( t_{ox} \) the oxide thickness, \( \Delta N_{ox} \) the increase of the number of oxide charges and \( q \) the elementary charge.

This change in the flatband voltage causes a shift of the device threshold for both n-channel and p-channel MOSFETs. This, in turn, causes a variation of the devices transconductance.

Besides the above effect, the hole trapping in lateral and field oxides is at the origin also of the leakage paths between source and drain of n-channel transistors and between ground and VDD biased diffusions. The source-to-drain leakage which occurs at the edges of the n-channel transistor (in the direction parallel to the source-drain channel) prevents it from being completely switched off, and this can already happen after a total dose as low as 20krad. The easiest way to solve this problem is to eliminate the edges, and this is possible by using edgeless (or “gate-all-around”) n-channel transistors in which the gate is disposed all around the drain so as to eliminate the interface between thin and thick oxide. p-channel transistors do not need this care, as they typically do not exhibit appreciable leakage after irradiation.

Thus, in conclusion, one should expect that, at circuit level, both static (leakage, gain reduction, etc.) and dynamic (poles and zeroes location) performances of an analogue IC are affected by exposition to radiation.

2.2 Testing the pixel analogue front-end by a voltage pulse.

The circuit under test used for the experiments (LHC2Test) has been manufactured in a commercial 0.5μm technology and makes use of edgeless n-channel transistors. It has two columns of 64 replicas of the same channel, which can be selected by a test and mask shift register. Each channel comprises an analogue front-end for the read-out of the signal coming from the pixel detector which is directly bump-bonded at the input of the charge sensitive amplifier (CSA). The CSA is a n-MOS cascode stage with a gain of 40mV/μC. The supply voltage is 3.3 V, the charge time constant is 5ns. The second stage is a 2nd order shaper amplifier with a shaping time of 23 ns.

Four test chips were used to study the damages of irradiation. Chip 1 was not exposed to irradiation, chip 2 was exposed to an irradiation of 200krad, the chip 3 of 800krad and the chip 4 of 2Mrad.

All the chips were at first tested by applying a single pulse of T=10ns and an amplitude of 80mV at the input of the CSA. The measured pulse responses for the four chips at the output of the CSA and the shaper are shown in the figures 1-4.

From these figures it is apparent that the pulse response of chip 2 (200krad) does not deviate from the response of the non-irradiated one, the chip 3 (800krad) deviates only slightly from the response of the non-irradiated. In contrast, for higher dose irradiation (chip 4), the deviation of the pulse response for both the charge sensitive amplifier and the shaper is evident [12].

![Figure 1: CSA pulse response for three different chips: Chip 1 (not irradiated) has the higher amplitude and a faster return to zero, chip 3 (800krad irradiated) has soft amplitude reduction and slower discharge time. The chip 4 (2Mrad) has a strong increase in the discharge time.](image-url)
In the CSA the deviation of its response could be explained by considering that the charge trapped in both thin and field oxides of the transistors of the active feedback resistor causes an increment in the time constant responsible for the discharge time.

The same effect could be recognised at the output of the shaper (figures 3, 4) with a well defined reduction of the gain for high dose of irradiation. This is due to the fact that transistors in the shaper are no more in the saturation region, because of an increase threshold due to the trapping of the charge and are now working in triode region.

The figures 2 and 4 where chip 1 and chip 2 (200krad) are compared, show that the parametric changes induced by low dose of irradiation cannot be detected by using the pulse response.

Figure 2: CSA pulse response comparison between the chip 1 (unexposed) and the chip 2 (200krad).

In contrast, the use of the complementary signal as input stimulus, appears to be more sensitive to parametric perturbations induced by a soft radiation dose (figures 5 and 6). The compsig is a piece-wise constant signal obtained from the circuit singularities and is used as input stimulus to check whether the output goes to zero when the stimulus vanishes. Figure 5 shows the results of the test, comparing the compsig response of chip 1 with chip 3 at the output of the shaper. It is apparent that, the irradiated chip has a response which doesn’t vanishes with the input since oscillations persist after the end of the test stimulus.

For the low dose (200krad) irradiated chip (figure 6) the exact time point at which its response goes to zero cannot be easily distinguished from that of the unexposed one.

Figure 4: Shaper pulse response comparison between chip 1 (unexposed) and chip 2 (200krad).

Figure 3: Shaper pulse response for three different chips: Chip 1 (unexposed), chip 3 (800krad irradiated) with soft amplitude reduction. Chip 4 (2Mrad) has a strong decrease in the amplitude.

Figure 5: Compsig response at the shaper output of chip1 and chip3. The compsig scale factor is 50mV/div, 10ns/div, the shaper output scale factor is 5mV/div.
Therefore the radiation effects result more evident by observing the whole shape of the compsig response than the simple pulse response (figure 4).

Fig. 7 shows a possible solution to these requirements. In test mode, the switch S1 is closed and S6 is open and the response to the test signal is put on the bus. In the normal mode S1 is open and S6 is closed, thus the current signal can be injected into the discriminator.

Figure 6: Comp sig response at the shaper output of chip1 and chip2. The comp sig scale factor is 50mV/div 20ns/div, the shaper output scale factor is 5mV/div.

2.3 Testing requirements at circuit level.

To apply in practice the proposed testing method, it is needed to observe the output of the shaper without applying an appreciable capacitive loading on this node. Moreover using the comp sig as a test stimulus, means to check that the output in a predefined set of time points assumes well defined values. This calls for the use of a clocked comparator to be connected at the shaper output, in compliance with the standards IEEE1149.1-4.

Digitizing Ricever

A digitizing receiver is used to compare the output voltage with a reference. This may be a fixed reference, or a variable reference may be supplied via AT1 or AT2. The digitizing receiver may even be the logic input to the capture flip-flop, though this requires careful design. The digitizing receiver can be a subtle source of difficulty. In CMOS, the most obvious digitizing receiver is a simple inverter, but these are not suitable because of their interaction with analogue signals. Normally, an analogue signal on the input to such a circuit would keep both the p- and n- channel transistors in the inverter turned on, resulting in an undesirable standing current between the power supplies. Further, if the inverter is biased near its threshold, Miller capacitance from output to input will 'kick back' charge into the input, causing noise and signal distortion.

A possible scheme is also shown in fig.8 which makes use of a "zero static power analogue comparator" consisting of input switches, a switched cross-coupled pair, and output isolators to balance the load on the cross-couple and isolate the analogue signals on it from the digital circuitry downstream.

This circuit drains current from the supplies only during the transitions from follower to latching mode.

Also, the input switches will inject some charge into the input when the cell is latched. After latching, some time is required to settle from sampling to latched mode, or offset may occur. This comparator may develop offsets from charge trapping in the cross-coupled transistors, so a third precharge state may be desirable for highest accuracy. The four isolation transistors
minimize output loading effects when the comparator is near balance [13].

3. BUILT-IN DYNAMIC CURRENT TESTING

A more general information on the status of the whole chip could in principle be achieved by observing the transient power supply absorption (IDDT).

The basic idea is to analyse the dynamic current transients to detect anomalous circuit behaviours from the shape of the supply current during the circuit excitation [14].

As defects typically change internal capacitance either by shorts or bridges, the transient behaviour is likely to change and to be observable in the time domain. A simple current mirror offers one of the easiest ways to observe the current just by copying it in the sensor and measuring it.

Even for radiation induced damages, the main effects in the analogue side affect the dynamic behaviour of the CUT and therefore they are evident during the transients.

In the case under consideration, measurements were performed to check the sensitivity of the supply current transients monitoring to the radiation effects.

Figure 9 shows the circuit arrangement used for the measures. A resistor of 10Ω is inserted between the analogue supply (VDDA) source and the chip under test. In this way it is possible to monitor the current absorbed by the whole chip, when a pulse test is applied, by reading the differential voltage at the resistor ends (CH1-CH2).

The results are reported in figures 10-12.

![Figure 9: Measurement setup](image)

Figure 10 shows the spike during the transients on the chip 1 (unexposed), chip 3 (800krad) and chip 4 (2Mrad), when a pulse is applied as test stimulus. There is a decrease of the spike amplitude, that means a reduction of the consumption during the transients, when the chip is strongly irradiated: this is due to a reduction of the gain and to a slower transition time.

![Figure 10: The dynamic current test on the chip 1, chip 3 (800krad) and chip 4 (2Mrad).](image)

![Figure 11: Chip 1 and chip 3 current transients.](image)

![Figure 12: Chip 1 and chip 4 current transient.](image)
For the chip 4 the signal is severely corrupted by noise, as it is more evident in figure 12. Figure 11 shows a zoom of the comparison between the current transient in chip 1 and chip 3.

4. CONCLUSIONS

The effects of radiation induced faults in the analogue front-end of a pixel detector employed in high energy physics experiments has been investigated. A testing strategy formerly developed to detect hard and soft faults in linear analogue circuits has been successfully employed to detect most of specification deviations on test chips irradiated with 800krad and 2Mrad dose and the results are here reported. The results show that, even for the 800krad dose, the test devised is able to detect the degradations of the amplifier performances. These modifications become more evident by applying the complementary signal approach.

Also, the results show that hardened devices do not necessarily produce high circuit immunity to radiation and the proposed test method provides a mean to detect these performance deviations and to monitor them during the operating life of the chip.

Finally, an alternative approach has been explored which makes use of a current sensor to monitor the supply current absorption during transient excitation. This technique, which is becoming very popular in the test community also because of the negligible electrical loading on the CUT and consequent absence of frequency limiting effects, still needs of further investigation to be advantageously employed in the pixel electronics.

5. ACKNOWLEDGMENT

The authors are indebted to M. Campbell, F. Formenti, E. Hejine, W. Snoeys (CERN labs.) for providing the test chips and supporting the measurements.

6. REFERENCES

2. F. Corsi, D. De Venuto, C. Marzocca, et al., 1995, in Proc. of 2nd Advanced Training Course: Mixed Design of VLSI Circuits, Krakow, Poland.
3. D. De Venuto, F. Corsi, et al., 1996, in Proc. of MELECON'96; Bari, Italy.
4. D. De Venuto, E. Cantatore, F. Corsi, 1996, in Proc. of European Test Workshop 96; Sete, France.
6. F. Corsi, D. De Venuto, C. Marzocca, 1997, in Proc. of European Test Workshop 97; Cagliari, Italy.
THE SILICON DRIFT DETECTOR READOUT SCHEME FOR THE INNER TRACKING SYSTEM OF THE ALICE EXPERIMENT

G. Alberici, INFN sez. di Torino, Torino, Italy (email: gianluca@tot2xs.to.infn.it)
G.C. Bonazzola, Università di Torino, Torino, Italy (email: bonazzola@to.infn.it)
D. Cavagnino, Università di Torino, Torino, Italy (email:davide@di.unito.it)
P. De Remigis, INFN sez. di Torino, Torino, Italy (email: deremigi@to.infn.it)
P. Giubellino, INFN sez. di Torino, Torino, Italy (email: giubellino@to.infn.it)
R. Hernandez, INFN sez. di Torino, Torino, Italy (email: hernandez@to.infn.it)
G. Mazza, INFN sez. di Torino, Torino, Italy (email: mazza@to.infn.it)
D. Nouais, INFN sez. di Torino, Torino, Italy (email: nouais@to.infn.it)
A. Rivetti, Politecnico di Torino, Torino, Italy (email: rivetti@polgen1.polito.it)
F. Tosello INFN sez. di Torino, Torino, Italy (email: tosello@to.infn.it)

for the ALICE collaboration

Abstract

The Silicon Drift Detectors (SDD) provide, through the measurement of the drift time of the charge deposited by the particle which crosses the detector, information on the impact point and on the energy deposition. Therefore their readout is characterised by a very large amount of data that has to be readout with very low power consumption, due to the strong temperature sensitivity of the drift velocity.

The foreseen readout scheme is based on a single chip implementation of an integrated circuit that includes low noise amplification, fast analog storage and analog to digital conversion, thus avoiding the problems related to the analog signal transmission. A multi-event buffer that reduces the transmission bandwidth and a data compression/zero suppression unit complete the architecture.

In this paper the system components design is described, together with the results of the first prototypes.

1. SYSTEM REQUIREMENTS

The ALICE Inner Tracking System (ITS) is made of 6 silicon detector layers, as summarised in table 1. This paper refers to the layers 3 and 4, that consists of Silicon Drift Detector (SDD).

The layers have cylindrical shape and are formed of linear structures called ladders. The SDD ladder organisation is shown in table 2. The total number of anodes is 61440 for layer 3 and 98304 for layer 4. The maximum power dissipation allowed by constraints on the amount of material for cooling system is around a total of 0.8 kW for the two layers.

Table 1: Inner Tracking System dimensions

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>R (cm)</th>
<th>z (cm)</th>
<th>Area (m²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pixel</td>
<td>3.9</td>
<td>12.25</td>
<td>0.06</td>
</tr>
<tr>
<td>2</td>
<td>Pixel</td>
<td>7.6</td>
<td>16.3</td>
<td>0.17</td>
</tr>
<tr>
<td>3</td>
<td>Drift</td>
<td>14</td>
<td>21.1</td>
<td>0.37</td>
</tr>
<tr>
<td>4</td>
<td>Drift</td>
<td>24</td>
<td>29.6</td>
<td>0.89</td>
</tr>
<tr>
<td>5</td>
<td>Strip</td>
<td>40</td>
<td>45.1</td>
<td>2.27</td>
</tr>
<tr>
<td>6</td>
<td>Strip</td>
<td>45</td>
<td>50.4</td>
<td>2.85</td>
</tr>
</tbody>
</table>

Table 2: ALICE SDD layers organisation

<table>
<thead>
<tr>
<th>Layer</th>
<th>Ladders</th>
<th>Detectors/ladder</th>
<th>Anodes/ Detector</th>
<th>Anodes/ladder</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>20</td>
<td>6</td>
<td>2x256</td>
<td>3072</td>
</tr>
<tr>
<td>4</td>
<td>24</td>
<td>8</td>
<td>2x256</td>
<td>4096</td>
</tr>
</tbody>
</table>

The SDD structure is shown in fig. 1. When a particle crosses the detector a charge cloud is generated. Due to the electric field, the cloud drifts toward the anodes. At the collection anodes the cloud has a gaussian-like shape; during the drift the cloud becomes larger, due to the charge carrier diffusion, but maintains its shape.

For particle tracking and identification it is necessary to know:
- The cloud position projected along the anodes
- The charge cloud arrival time (related to the distance from the particle crossing point to the anodes)
- The amount of charge collected by the anode(s)
2. READOUT ARCHITECTURE

2.1 General Scheme

A general scheme of the proposed architecture for the SDD readout is shown in fig. 2. The readout chain is divided in two major units:

- Signal amplification and A/D conversion
- Data compression and transmission

The first unit is distributed on the ladder near the detectors, whereas the second unit is concentrated at both ends of the ladder itself.

Key points of the proposed architecture are:

- To avoid any on-line analysis. In a detector like ALICE an early failure detection is very important and it is safer if raw data are sent to the acquisition system. Moreover, data analysis requirements can change during the experiment and a system with hardwired analysis would be less flexible
- To minimise the power consumption near the detector, in order to decrease the amount of material needed to implement the cooling system.

2.2 Signal amplification and A/D conversion unit

The basic idea is to amplify the detector output current, sampling it and performing an A/D conversion. As a good tradeoff between power consumption and time resolution a sampling frequency of 40 MHz has been chosen. Such sampling rate allows to obtain at least 3 samples of the signal shape from an anode, even at minimum drift time. However, it is not possible to design an A/D converter at this conversion frequency that satisfies the space and power requirements (the power limits mentioned above allow a maximum power consumption of ~5 mW/channel); it is then necessary to implement a temporary analog memory to allow the A/D converter to work only when the external trigger is received. This indeed allows the conversion frequency to be reduced by more than one order of magnitude.

Each half detector (256 anodes) will be connected with 4 chips of 64 channels. Each channel consists of a preamplifier, a 256 cell analog memory, and an half 8-bit A/D converter (i.e. one converter per 2 channels). The chip, named PASCAL (see fig. 3), consists also of a multiplexer, a set of digital buffers and drivers for data transmission and a control unit.

The circuit works as follows: the SDD output is continuously amplified and sampled at 40 MHz. Samples are stored in the analog memory while waiting for a trigger signal. ALICE detector will produce three useful triggers, namely the first level trigger (L0), with a fixed latency of 1.2 μs, the second level trigger (L1) with a fixed latency of 2.4 μs and the third level trigger (L2) with a variable latency (≤ 100 μs). The chosen trigger signal freezes the analog memory (after an additional delay related to the drift time) and starts the A/D conversion phase, dealt in parallel with the data transmission to the end of the ladder. During the conversion time any signal from the detector is ignored.

The preamplifier is a transimpedance amplifier with an input range of a couple of μA and an output range of about 1 V. The bandwidth has to be around 10-12 MHz, that is a reasonable bandwidth at the chosen sampling frequency. In order to decrease the A/D resolution from 10 to 8 bit without affecting the SNR, a non linear transfer function is required. The upper limit for power consumption is 1 mW/channel.
maximum drift time, a write frequency of 40 MHz and a read frequency of 3 MHz. It must dissipate less than 2 mW/channel during the write phase at 40 MHz. Its power consumption during the read phase, when also the ADC works, has to be lower than 5 mW/channel.

The A/D converter requirements are: 8-bit resolution and power consumption below 10 mW/channel during conversion. Since both the ADC and the analog memory read amplifier are triggered, they work only around 10% of the time, then the average power dissipation satisfies the overall requirements for one channel. The conversion time depends on the dead time that is tolerable: around 3.5 μs/channel for 1 ms dead time and 400 ns/channel for 200 μs dead time.

More than 90% of data are baseline samples, so a strong data reduction is possible. Two types of algorithms have been studied and implemented:

- Lossless algorithms: the idea is to obtain data reduction avoiding cluster analysis and loss of information. The principle is to calculate the differences between consecutive samples and to apply a Huffman coding to the values, this algorithm is able to get compression using the spread in result probability. This solution needs a very simple on-line processing, but produces a smaller reduction compared with a raw zero suppression.
- Loss algorithms: in order to increase the compression ratio of the previous algorithm, it is possible to fix thresholds on both absolute values (threshold) and on differences (tolerance). The thresholds can be modified during normal operation through the slow control system.

After the reduction, the data are sent to the SIU (Source Interface Unit) board for the transmission of data to the DAQ.

The data compression and transmission unit and the SIU are part of the End Ladder Board (see fig 4), located at both ends of the ladder. This board has two main purposes:

- Receives the data from the detectors front-end; reduces it through the previous algorithms and sends it to the DAQ.
- Manages the slow control system.

2.3 Data compression and transmission unit

At the end of the ladder power and size requirement are less stringent, so it is possible to reorganise the data in order to reduce the output bandwidth.
The slow control system is based on the IEEE 1149.1 standard interface port (JTAG) and is used for both test and configuration purposes. Using a standard interface for slow control reduces the number of control lines required and greatly simplifies the chips and boards testing before and during the experiment activity.

### 2.4 Transmission between the two units

The amount of data that has to be transmitted between the two units is very large: in the worst case (layer 4) there are 4096 anodes with 256 8-bit samples each. The compression and transmission chips will be placed on both sides of the ladder; anyway for each side 512 Kbytes have to be transmitted. Two possible scenarios has been studied:

- After the ADC no buffer is used. In this case the transmission time must be equal to the conversion time; this means a bus bandwidth of around 512 Mbytes/s in the case of 1 ms transmission time and 2560 Mbytes/s for 200 µs transmission time. Supposing to transmit at 40 MHz (the same frequency of the analog memory clock) the number of 8-bit buses will be 13 for the first case and 64 for the second one. A more practical number for the first case is 16 buses (one every 128 channels), while 64 buses is exactly one bus for every 32 channels. This leads to a number of cables that is very difficult to manage, especially if the case of 200 µs transmission time will be chosen.

- After the ADC two or more 256 bytes/channel digital buffer are implemented. In this case the event is stored locally and can be transmitted at lower speed. An analysis made for the ALICE TPC detector (see [3]) shows that with 2 event buffers and a readout time of 2 ms the dead time to the buffer saturation is only 0.1%; the dead time increase to 9.1% with a 10 ms readout time. Supposing to have an 8-bit bus for each 256 channels (half detector) the readout time is around 1.6 ms, with only 8 buses for each ladder side.

The second solution greatly simplifies the cabling between the two units; moreover, even in the 1 ms case, a fast readout of the analog memory relax the requirement on the discharge time of the capacitor, and ultimately on the capacitor size. Reduced capacitor sizes means, in turn, reduced size and power requirements of the PASCAL chip.

On the other side, analog and digital memories cannot be integrated on the same chip (for size and noise reasons) and extra chips (see fig 5) have to be put on the ladders, where the space and power consumption requirements are more strict. Nevertheless, the second solution seem still easier to implement.

### 3. REFERENCES

[1] ALICE Technical Proposal -- CERN LHCC 95-71
ALICE Detector Data Link (DDL) -- Interface Control Document
ALICE Internal Document, INT-96-43
[3] F. Formenti, L. Musa
FEE architecture for the ALICE TPC
Slides presented on the ALICE technical board, May 1997
Switched Capacitor Arrays Analog Memories for Sparse Data Sampling

D. Lo Presti(2), S. Panebianco(1), G. V. Russo(1), S. Reito(2)

(1) Dipartimento di Fisica dell'Università and Sezione INFN, Catania, Italy
(2) Sezione INFN, Catania, Italy

ABSTRACT

Two full custom Analog Memories for sparse data sampling have been designed as arrays of switched capacitors. While the first one (ADeLine1) is only one channel of 8 cells, the second one (ADeLine2) is organized as 8-channel, 256-cell. Both the devices use only one operational amplifier to read the cells. The control part of the ADeLine chip is full custom designed for size reduction, high speed performance and low power dissipation. The cells are addressed in a sequential mode during the write phase, writing all the channels of one column simultaneously, but in a random mode, only one cell at a time, during the read phase. The memories have been integrated in double poly, double metal AMS 0.8 µm CMOS. The memories have 3.5V input and output swings, a linearity beyond ±6 mV in a 2 V range and 11 bits of resolution. New designs of the ring shift register, the sampling capacitors and the read-out amplifier have been made. A new chip, ADeLine3 with 3 channels and 64 cells is presented.

1. Introduction

Many High-Energy Physics Experiments require the simultaneous and high rate storage of the information from several hundred thousand analog signals. This is generally accomplished by a temporary storage until a trigger decision is made. Then the signals are digitized, processed and sent to an acquisition system.

A traditional solution of this problem involves the use of a Flash Analog to Digital Converter followed by a digital memory. A valid alternative is to store the analog signals in a Switched Capacitor Array (SCA). The capability of this solution has been demonstrated in a number of designs [1]-[6]. These SCA circuits show very good performances as regard cost, density, dynamic range, power dissipation and speed.

In this paper we describe two prototypes of analog memories realised in view of the design of the readout system for the Silicon Drift Detectors (SDDs) [7]-[10] that will be used at LHC in the ALICE (A Large Ion Collider Experiment) detector as Inner Tracker. The main aim of the two designs is to study the properties of the basic cell of the memory and to design a layout with the minimum size, very low crosstalk and power dissipation, a very good linearity, high input/output swings and a remarkable resolution.

2. Adeline Design

For our purpose the more pressing requirements are [1]-[2].

1. very low power dissipation due to thermal constraints on the nearby detector;
2. very small silicon area to diminish cost and to have little matter across the particle trajectories in order to reduce multiple scattering;
3. a good reconstruction of the input shape to obtain the desired precision in the determination of the particle impact point.

A SCA memory like the Haller one, with some suitable modifications, is enough to fulfil our requirements. The main variations are:

1. the sampling frequency must be relatively small (40 MHz) compared to the Haller one (900 MHz);
2. the read frequency must be higher (1 MHz) compared to the Haller one (100 kHz);
3. instead of two switches for the selection of the sampling capacitor, only one is used. The desired bandwidth can be reached with a switch having a small parasitic capacitance. It is used for the read phase too;
4. as a consequence only one addressing system is required;
5. data in the SCA memory are sparse and only one data is read at a time. This means we can use only one OA for the whole device: the matching between channels improves and power dissipation and silicon area decrease;
6. two Ring counters are used for the addressing of the cells. In the write phase only a Column Up/Down Ring Shift-Register (U/D R-SR) works, while in the read phase a Row U/D R-SR is used too;
7. the technology used is AMS CMOS 0.8 µm double-poly double-metal for size, power reduction and very good performances. Using 500 fF sampling capacitors the matching is better than 2%.

We have designed two different memories on this basis on the same chip. The first one, ADeLine1, is a 1-channel, 8-cell; the second one, ADeLine2, is an 8-channel, 256-cell. The final version will be four times the latter: 32-channel, 256-cell.

A simplified scheme of one channel of the ADeLine memory is shown in Fig.1. The kth cell of the jth row consists of a NMOS transistor Sk and a poly-poly storage capacitor Ckr (0.5 pF, 8.2 x 33.2 µm²). V_a and V_b are suitable DC reference voltages.

During the write phase the CMCS switches S_w and S_w are turned ON, connecting the signal V_i to the input busses and the common node of all the switches S_k.
to a $V_a$ reference voltage, while CMOS switches $S_{ij}$ and $S_{ib}$ are maintained OFF. An analog signal applied to the circuit’s input is sampled onto the cell capacitors $C_{ik}$ by sequentially turning ON and OFF switches $S_{ij}$ to $S_{256}$ by means of the column U/D R-SR that works in UP mode. During the whole write phase the CMOS switch $S_e$ (erase switch) is ON to keep the output to a defined potential $V_b$.

During the read phase, $Sw_i$ and $Sw_b$ are turned OFF, disconnecting the signal $V_i$ from the input busses. By means of an appropriate control to the row U/D R-SR we turn ON the switches $S_{iq}$ and $S_{ib}$ of the selected row. Other controls to the column U/D R-SR turn ON all the switches $S_{jk}$ of the column selected. In this way, only one cell at a time is inserted in the feedback loop of the OA. The function of the erase switch $S_e$ is to fix the output to $V_b$ before each read phase. Between two readings $S_e$ is turned ON and $S_{iq}$ is turned OFF. After $S_e$ is turned OFF the selected cell is read and the voltage stored in the sampling capacitor plus a $V_b$ voltage that is present at the output of the amplifier. This operation is repeated for all the cells to be read. The input bus must be forced back to $V_b$ before each cell reading, otherwise the charge sharing and the parasitic capacitances shall seriously degrade the circuit’s performances.

The performances of SCA memories are strongly affected by parasitic capacitances. All the 256 $C_{ik}$ sampling capacitors of the same $j$th channel are connected to the same top line. The total capacitance of this line in respect to the ground is $C_i$. Analogously all the 256 $S_{jk}$ column selection switches of the same $j$th channel are connected together to the same bottom line.

### 1.1 The Addressing System

The two U/D R-SRs have been designed full custom to match the column pitch and to reduce power dissipation and the number of transistors for each cell. One of the registers, 256 cells wide, is dedicated to the column addressing. The other one, 8 cells wide, is for row addressing. They operate with two-phase clocks. The shift direction depends on the U/D input level. The output voltage is stored in the parasitic capacitance of the gate of the next cell without the use of static latches.

### 2. Results

A picture of the ADeLine chip is shown in Fig. 2. You can see in the upper part ADeLine1 (2.3 x 4.5 mm$^2$), and in the lower part two replies of ADeLine1 (1.2 x 0.8 mm$^2$). The channel pitch of ADeLine2 is 210 um (depending on the application) and the column pitch is 13.2 um.

At the moment we have measured only the performances of ADeLine1. To measure ADeLine2 a more complicated measurement set-up must be acquired.
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.

The measurement of the pedestal fluctuation was
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.

The measurement of the pedestal fluctuation was
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.

The measurement of the pedestal fluctuation was
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.

The measurement of the pedestal fluctuation was
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.

The measurement of the pedestal fluctuation was
accomplished writing and reading alternatively all the
cells of the channel with a fixed input signal. The fluctua-
tions of the value between the different cells of the chan-
nel were measured. If we take into account the difference,
for all the cells, between the mean output and the input of
the same cell building an overall spectrum we achieve
the compactness of the cell, the linearity in a large dy-
amic range.
A new design of the sampling capacitor to improve the dynamic range and the resolution. All of them were reached. The next step has been a new prototype of the ADeLine with a better performance readout operational amplifier in order to achieve the read frequency of 1 MHz, a new R-SR to further reduce the die size and to obtain the desired write frequency of 40 MHz and with 32 channels to reduce power dissipation. A more accurate design of the sampling capacitor could give a better resolution.

4. ADeLine3.

A new design of the analog memory has been developed. Taking into account the test results, several modifications have been introduced to optimise the whole system performance:

1. New compacted unidirectional ring shift register with better speed performance. Every 16 cells a system composed of a couple of inverters is introduced to regenerate the clock signals which drive the shift register. In this way the control clock signal presents the same phase to every switch. Wider metal2 wires have been used to transmit the two clock phases. The equivalent resistance of these wires is in this way reduced and reduces the effects on the signal propagation (RC effects). Post layout simulations of the shift register with 64 cells show a maximum write frequency equal to 230 MHz.

2. A new design of the sampling capacitor to improve the matching has been made. The shape of the 0.5 pF capacitor is showed in fig. 9. Using an octagon of superimposed poly1 and poly2 layers instead of a rectangle, avoiding the 90° corners, results in a better matching for the dimensions of the capacitor. In this way a better resolution in the sampled voltage is achieved.

A new readout operational amplifier has been designed. The choice of the folded cascode consents wider output and input swing, about 3 V. The amplifier is able to drive a load capacitance of 15 pF (the foreseen ADC input capacitance) at a read frequency of 1 MHz. The low power consumption consents the use of one amplifier for each channel, avoiding the use of the row-shift register.

POSTLAYOUT SIMULATIONS RESULTS

In fig. 10 the layout of the AdeLine 3 chip is shown. The chip has 3 channels (two with the optimised sampling capacitor and one with the old ones) and 64 cells. In fig. 11 the output of the 3 channels is shown. The write frequency is 40 MHz and the readout frequency is 4 MHz.

REFERENCES


S.Panebianco - Ph. D. Thesis, Catania University, 1998

[14] B.J.Sheu, Chenming Hu - IEEE J.SS Cir, V.SC19,
ELECTRICAL CHARACTERIZATION OF ALICE128C : A LOW-POWER CMOS ASIC FOR THE READOUT OF SILICON STRIP DETECTORS

Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux 
LEPSI - IN2P3/CNRS - ULP 
23, rue du Loess - BP 20, 67037 Strasbourg Cedex 02 - France 
Email : hebrard@lepsi.in2p3.fr

J.R. Lutz and al. - ALICE/STAR group from IReS (Strasbourg - France) 
and 
S. Bouvier and al. - ALICE/STAR group from Subatech (Nantes - France)

ABSTRACT

ALICE128C is a new low-power CMOS ASIC dedicated to the readout of Silicon Strip Detectors (SSD) for the ALICE [1] and STAR [10] experiments. The architecture of the circuit and the main simulation results have been presented already [2]. This paper presents the electrical characterization results according to the procedure used to test the circuit. All functional blocks were tested with success, and all electrical specifications are satisfied. Especially, in the case of a 10MHz readout rate with a mean readout cycle every 1ms, i.e. for typical conditions of use, the mean power dissipated per channel is kept very low, around 340µW/channel. Specific functionalities were added in ALICE128C to control, to test and to characterize the circuit [2][3]. They have been used extensively during the characterization and they will provide efficient testing capabilities after mass production and during the ALICE and STAR experiments.

I. INTRODUCTION

ALICE128C is a 128 channels chip designed with the AMS1.2µm CMOS technology (die size 6mm x 8.5mm) [2]. Each channel amplifies, shapes and stores as a voltage signal onto the capacitance C_held the charge deposited on a strip of the detector. This storage is triggered by the external HOLD logic signal which arises τ_c seconds after the radiation event. The shaping time (τ_c) is adjustable from 1.4µs to 2µs. An analog multiplexer allows a sequential readout of the data at a rate up to 10MHz through a tristate output buffer shared by the 128 channels. The output buffer has been designed to drive an external link with a 100Ω characteristic impedance in parallel with a capacitance up to 20pF. The tristate property of the output buffer allows a daisy chain of several ALICE128C chips connected onto the same external link. A slow control mechanism compatible with the << JTAG IEEE1149.1 >> standard [4] has been added to accurately bias the different analog blocks and to tune the shaping time. It also controls an internal test pulse generator which provides a variable current pulse emulating a deposited charge up to ±11MIPs (MIP : Minimum Ionizing Particle; 1MIP = 25000 electrons).

The next section develops the specific testing functionalities added to ALICE128C. Then, a short description of the test set-up used to characterize the circuit is given. Section IV describes the procedure used to test the circuit and gives the main results of characterization. Finally, section V concludes the paper.

II. CIRCUIT TESTABILITY

ALICE128C is mainly an analog circuit since the digital part includes only the JTAG module and the readout controller. Testing efficiently such a circuit is a challenge. So one of our efforts in designing ALICE128C was to add specific testability features into the chip. These features address three goals : the circuit electrical characterization, the circuit test after mass production and the on-site circuit test during the experiment.

After prototyping, the circuit has to be electrically characterized. In particular, the amplifying channel gain is measured by injecting a calibrated current pulse at the input. But it would be very tedious, time consuming and error prone to connect every 128 channels, or successively each channel, of a prototype to an external charge injection system in order to measure the corresponding gains. So, in front of each channel, a current pulse generator has been integrated (figure 1). It switches a current, I_pulse, from one branch of a differential stage to the other one, to produce a step
voltage across a double polysilicon capacitance $C$, connected to the input of the preamplifier [3]. Such a system emulates a charge $Q$, deposited on the detector by a radiative particle which value is $Q=I_{\text{pulse}}R.C$. By writing into a 8 bits current D/A converter, $i_{\text{pulse}}$ is then varied to set the test pulse level.

![Diagram of current pulse generator](image)

Fig. 1: Current pulse generator

The channels where the pulse has to be injected are selected through a shift register. At the output, depending on the kind of test to perform, it is possible to read sequentially all the signals stored on the $C_{\text{readout}}$ capacitances (normal readout cycle) or to select one particular channel through the output shift register. In this later case, the external HOLD logic signal is set to 0 and we see through the corresponding channel from the input to the output. This allows for example to visualize the shape of the signal at the output of the shaper in order to measure/set the shaping time. Of course, to be used for characterization, the pulse generators have to be calibrated. We will see how it is done in section IV. All the different testing configurations and the pulse level, thus all the registers, are addressed by means of the JTAG controller.

After mass production, the circuits are sorted in order to throw out the possible wrong products. This sorting is based on simple trials which involve the measurement of some power supply DC currents for example. But more complicated measurements can be considered. In this case, one can take advantage of the specific testing functionalities of ALICE128C. A channel out of order can be easily detected by using the internal pulse generator. Of course, these kinds of test have to be performed before bonding the silicon strip detector to the chip, and the use of TAB bonding [5] can also become an advantage.

During the long range experiment (around 10 years), it could be essential to check periodically the functionality of the circuit, to adjust the analog parameters in case of harmful deviations, and also to disconnect an ill circuit from the readout daisy chain. The specific testing and control functionalities of ALICE128C are mainly added for such a purpose. Furthermore, these controls and tests must be done remotely and without requiring a lot of links since the circuit is situated into the heart of the spectrometer. Thus, in order to minimize the number of interconnections, all the chips are connected serially according to the JTAG.IEEE1149.1 protocol [4]. In the normal mode, the analog readout of the 128 channels is done sequentially, activated by a token from the previous chip. In order to disconnect a chip out of order, the readout register is bypassed by connecting the token input to the token output. Note that on reset, the token is bypassed and a JTAG instruction has to be sent to enable the readout.

III. TEST SET-UP

The test set-up used to characterize ALICE128C is presented on figure 2.

![Test set-up diagram](image)

Fig. 2: Test set-up

On one side, a HP82000 IC evaluation system is used to generate specific digital stimuli as the Read-Out-Clock, the external HOLD signal, the Test Pulse Request and some configuration signals (Reset,...). On the other side, a home data generation/acquisition system (a Siroco) [6], dedicated to Strip Detectors Read-Out Systems, is used to send the JTAG sequences and to acquire the analog output signal provided by ALICE128C. This hardware testing system is controlled by means of a unix workstation with specific softwares written in C to drive the Siroco and in HP Vee to drive the HP82000. Finally, the digital stimuli and the resulting analog signals are stored in ASCII or MATLAB files which can be analyzed through PAW [7] or MATLAB [8]. Thanks to this set-up the different
testing configurations can be selected very fast and many electrical measurements were performed to characterize ALICE128C.

IV. TEST RESULTS

IV.1 Internal Pulse Generator Calibration

Prior to stimulating the circuit by means of the internal pulse generator, one must calibrate the generator. The ALICE128C prototype was mounted on a specific PCB with an external current pulse injection system connected on channel 39. This external generator is made up of a capacitance which value is accurately known, a voltage pulse generator, and a 50Ω resistor in order to adapt the voltage generator output impedance. By tuning the voltage amplitude, the injected charge can be varied accurately. In order to calibrate the internal pulse generator, one must calibrate the internal pulse generator, the transfer characteristic has to be shifted by a certain amount. This external generator was compared with the characteristic obtained using the internal injection system, this former characteristic has to be compared with the characteristic obtained using the internal injection. Due to parasitics added by the external injection system, this former characteristic has to be measured after disconnecting the external system. Nevertheless, this is mechanically too complicated and the transfer characteristic of channel 39, obtained with external injection, was compared with the characteristic obtained by internal injection on another channel, here channel 63. As we will see later, this approximation is good since the channel to channel gain dispersion is small, less than 1%.

![Image](https://via.placeholder.com/150)

**Fig. 3**: Pulse generator calibration

The measurements performed on channels 39 and 63 are shown on figure 3. For the external injection system, the MIP is taken equal to 25000 electrons. In this case, the amplifying channel begins to saturate over ±12 MIPS, so the amplitude of the curve was restricted to ±12 MIPS. A linear fitting performed on the full input range gives a gain of 62.56mV/MIP which is also the actual gain of channel 63! By means of the 8 bits D2A current converter, the internal generator is assumed to be able to provide ±14 MIPS. In this case, the linear fitting of the transfer characteristic gives a measured gain of 50.97mV/MIP. Assuming that the internal generator actual amplitude is of ±11.4 MIPs (1MIP = 25000 electrons). From now, 1 MIP will be assumed equal to 25000 electrons!

This is a good calibration procedure only if the 8 bits D2A input range gives a gain of 62.56mV/MIP which is slightly higher than the gain required by the specifications [2].

IV.2 Amplifying channel gain and linearity

![Image](https://via.placeholder.com/150)

**Fig. 4**: Transfer characteristic non linearity

Setting all the biasing currents at their nominal values (values obtained by simulation), the transfer characteristic of channel 63 was measured by performing a typical readout cycle (internal current pulse injection + HOLD signal after 1.5μs + readout) every 10ms with a readout rate of 10MHz. In order to remove harmful noise, the measurement is performed thousand times and the average value is retained. At each new readout cycle, the injected current pulse level is increased by 1 MIP. This measurement procedure provides the transfer characteristic of figure 3. The actual transfer characteristic has to be shifted by the output DC level, here 288mV since the base line has been removed for convenience. As mentioned before, the linear regression performed on the full input range gives a gain of 62.56mV/MIP which is slightly higher than the gain required by the specifications [2] (50mV/22000.e^c = 56.8mV/MIP).
The deviation from the fitted linear curve is presented on figure 4. It was calculated as the ratio of the difference between the measured and the fitted values at the corresponding point with the fitted value. As expected from simulation [2], the non linearity is lower than 2% in the range of ±4 MIPs and 8% over the full range.

**IV.3 Channel to channel gain dispersion**

Using the same measurement procedure, but injecting the internal pulse at the same time into 32 adjacent channels, the gain and the base line of each channel were measured. The choice of injecting simultaneously on 32 channels was taken to save time during the test (each measurement is performed thousand times and its average value is retained as the right measurement 1). Figures 5 and 7 show the resulting distributions.

Figures 5 and 7 show the resulting distributions. Using the same range. The deviation from the fitted linear curve is presented than 2% in the range of ±4 MIPs and 8% over the full range. It was calculated as the ratio of the difference between the measured and the fitted values at the internal pulse at the same time into 32 adjacent channels, the gain and the base line of each channel were measured. The choice of injecting simultaneously on 32 channels was taken to save time during the test (each measurement is performed thousand times and its average value is retained as the right measurement 1).

Figures 5 and 7 show the resulting distributions.

**Fig. 5 : Channel to channel gain**

Two channels, channels 23 and 33, are out of order. This is certainly due to ESDs (ElectroStatic Discharge) which have destroyed the gate oxide at the input of the charge sensitive amplifier (CSA) during the bonding of the chip on the test PCB. Note that the channel input nodes have no protection diodes since noise has to be kept at a minimum level on these nodes. The gains of channels 32 and 34 are slightly higher than the mean gain. This must be again due to damage occurred during the bonding. Furthermore, the gain of channel 39 is higher than the other gains because of the parasitics induced by the external injection system connected to this channel.

By looking at the global channel to channel gain distribution (figure 5), a cluster phenomenon is clearly observed. The gains are clustered by sets of 32 corresponding to the 32 channels where the pulse is injected. On the other hand, the gain seems to increase inside a cluster from the first to the thirty second channel! An accurate analysis has to be carried out in order to explain in details this phenomenon. Nevertheless it is due to small resistive voltage drops occurring on the Vss power line and resulting in a discrepancy between the reference current provided by the internal 8 bits D2A current converter and the pulse copy of this current into each current pulse generator.

Since these generators are equally spaced in front of the chip, the small voltage drops are linearly distributed over the 32 channels, resulting in the observed cluster phenomenon.

The mean amplifying gain, 57.61mV/MIP, is reduced in comparison to the gain measured on channel 63, 62.56mV/MIP, when only one pulse is injected (figure 3). This comes again from the same cause acting globally on the 32 current pulse generators and resulting in a decrease of the mean gain.

**Fig. 6 : Gain distribution**

![Gain distribution](image)

Figure 5 shows the gain distribution. It can be seen as a gaussian distribution with a 57.61mV/MIP mean value and a standard deviation of $\sigma=0.71$mV/MIP. The two channels out of order were removed and channels 23, 33 and 39 were not considered in calculating the distribution gaussian fitting. The channel to channel gain dispersion $\sigma$, is then of the order of 1.2%. On one hand, this dispersion comes from the dispersion of the integrated component electrical characteristics. On the other hand, it comes from the clustering phenomenon described previously. One can expect that the main source of dispersion is due to the clusters. So the 1.2% dispersion can be seen as a pessimistic value.

This result shows that our assumption on gain dispersion in performing the pulse generator calibration was justified.

**IV.4 Base line distribution**

The base line is distributed randomly with a mean value of 296mV and a 7mV standard deviation, i.e. only 11.2% of one MIP as base line dispersion. Note that the
base line is not disturbed by the cluster phenomenon since it is determined for 0MIP injected.

For such front end amplifying system, the Equivalent Noise Charge (ENC) at the input is proportional to the detector capacitance. So the ENC was measured with the SSD bonded to the chip [9]. A value of 300 electrons was obtained for a detector capacitance around 5pF. This is in the range of the specifications. So the ENC was measured with the chip [9]. A value of 300 electrons was obtained for a detector capacitance around 5pF. This is in the range of the specifications.

V. CONCLUSION

This paper has presented the electrical characterization of ALICE128C. Thanks to the specific testability features added to ALICE128C, the characterization procedure was made easier and a lot of measurements possible. The main results are given and show that all required electrical specifications are satisfied. ALICE128C has been mounted with success into a global detecting prototype system and is expected to be used for the ALICE and STAR experiments [9].

REFERENCES

[10] Star Technical Proposal, « Proposal for a Silicon Strip Detector for STAR (SSD) », SUBATECH (Nantes), IReS (Strasbourg), LEPSI (Strasbourg), Physics Department of Wayne State University (Detroit - USA), 1998

where $T_c$, the period between two readout cycles is expressed in milliseconds and $\langle P \rangle$ is expressed in microwatts. For a typical readout cycle every 1 ms, the mean power consumption per channel is then kept to the very low value of 340µW/channel.

IV.5 Noise

For such front end amplifying system, the Equivalent Noise Charge (ENC) at the input is proportional to the detector capacitance. So the ENC was measured with the SSD bonded to the chip [9]. A value of 300 electrons was obtained for a detector capacitance around 5pF. This is in the range of the specifications (<400 electrons) [1][2].

IV.6 Power consumption

Until now all the measurements were carried out after biasing the circuit by the nominal currents obtained by simulation. So, for a 10MHz readout rate, the mean power consumption per channel is given by [2]:

$$\langle P \rangle = 328 + 10.53 \times T_c$$
FRONT-END ELECTRONICS FOR THE ALICE TPC -DETECTOR


CERN, Geneva (Switzerland)


University of Frankfurt (Germany).

P.Donni, D.La Marra, L.Rosselet.

University of Geneva (Switzerland).

Abstract

The front-end electronics for the Time Projection Chamber (TPC) for the ALICE experiment consists of 5x10^5 channels. A single readout channel is comprised of three basic units: a charge sensitive amplifier/shaper with a fast tail cancellation; a 10 bit 10 MSPS low power ADC; a digital ASIC which contains the zero suppression circuit and a multiple-event buffer. Data from a number of channels (4096) are multiplexed into an optical link (DDL) by means of a local custom bus which can support a data throughput of 2 MByte/event at a trigger rate of 50Hz. The construction of a prototype of this electronics is presented in this paper.

1. INTRODUCTION

ALICE [1] is A Large Ion Collider Experiment now being built to study high energy heavy ion collisions at the Large Hadron Collider (LHC). LHC will collide several species of ions, ranging from protons up to lead, at centre-of-mass energy of about 5.5 TeV/nucleon.

ALICE is scheduled for initial operation in 2005. It will be composed, from the inside out, of an inner tracking system, based on six layers of high-resolution silicon tracking detectors (ITS), a cylindrical TPC, a time of flight system (TOF), an electromagnetic calorimeter and an array of counters optimised for high-momentum particle identification (HMPID). This is the central part of the detector, which covers ±45° over the full azimuth, embedded in a large magnet with a weak solenoidal field. The detector is completed by a forward muon spectrometer.

The relativistic ions collisions at LHC will have an extremely high charged particle multiplicity. For the central events in Pb-Pb running, for instance, about 3x10^7 tracks will be produced in the detector acceptance. In such an environment, to achieve a good two-track resolution, is required a three-dimensional space point readout with a very high spatial granularity. ALICE uses a TPC as main tracking system.

The use of a TPC for tracking reconstruction in such high particle density environment has been shown to be possible by NA49 in the lead runs at the SPS. However, a number of ALICE-specific requirements, make new designs indispensable.

The ALICE TPC [1], of cylindrical shape, will be 500cm long, subdivided into two drift spaces of 250cm by a central high voltage plane, and extends in the radial direction from 90cm radius out to 250cm. The image charge is detected by 5x10^5 pads located on two readout planes at the cylinder end-caps. The readout planes are based on a new concept, the Ring Cathode Chamber (RCC) [2], which makes use of a pad structure that surrounds almost completely the sense wire. In ALICE, the TPC will be used for tracking reconstruction, momentum measurement and particle identification by dE/dx.

2. ELECTRONICS REQUIREMENTS

In a TPC, the drift velocity, drift length and diffusion constant determine most of the parameters for the front-end electronics. For the ALICE TPC a cool gas mixture with a drift velocity of 2.5cm/µs and a diffusion constant of 250µm^2/µs has been chosen as the most probable candidate.

The average longitudinal diffusion determines a shaping time of 240ns, which is comparable to the diffusion width of the detector pulse in the time domain. From the shaping time, a sampling frequency of approximately 10MHz can be derived. Thus, the total drift space of 250cm is divided into about 1000 time slots. Each of the 1000 slots corresponds to a 2.5mm drift distance.

Diffusion and electron statistics limit the resolution both in the drift and azimuth directions. Monte Carlo studies indicate that to reach the detector resolution limit, a 40:1 signal-to-noise ratio is required. The dynamic range is set by the requirement that the electronics accommodate a 280 MeV/c proton, which is about 10 times a minimum ionising signal. To allow for
Landau fluctuations, the electronics must not saturate for signals up to 20 times minimum ionising. The pad capacitance is of the order of a few pF and can integrate a maximum charge of 0.2pC (1.25x10^6 electrons), leading to a maximum acceptable noise (r.m.s.) of about 1500 electrons.

To achieve the necessary rate capability the zero suppression will be done in the front-end before the data is transferred to the DAQ system. Owing to the high channel occupancy, in order to minimise pile-up effects, a very precise tail cancellation in the front-end stage is required. To be compatible with the dE/dx resolution, a channel occupancy, in order to minimise pile-up effects, a maximum charge of 0.2pC (1.25x10^6 electrons), is transferred to the DAQ system. Owing to the high temperature stability, which influences the drift velocity.

In Pb-Pb running, event rates will reach 10^5 minimum bias events per second; in p-p running, the maximum interaction rate will be of the order of 10^3 interactions per second. A few percent of these rates correspond to central collisions that will be trigger selected. The large granularity of the TPC (5x10^5 pixels) leads to event sizes of 0.6 GByte/event. Zero suppression at the front-end will reduce the data throughput by a factor of 10; data compression at the front-end and at the DAQ will further reduce the data to the order of 2.5 GBytes/s, with about 50 events/s written to permanent storage.

In proton-proton mode the detector will produce a data volume smaller of a factor 5.

A critical aspect in the TPC operation is the temperature stability, which influence the drift velocity. A temperature stabilisation of about 0.1°C over the whole volume, corresponding to a variation of the z-(drift) co-ordinate of 1mm in the worst case is necessary. This stability can be achieved by operating the TPC at a working temperature of 25°C and cooling the readout modules with a traditional water cooling system if the power dissipated by the front-end electronics is below 25kW (50mW/channel).

The radiation load on the TPC is low, with a total dose received over 10 years of less than 300 rad and a neutron fluency of less than 10^11 neutrons/cm^2.

3. READOUT COMPONENTS

The front-end electronics for the ALICE TPC consists of 5x10^5 channels. A single readout channel is comprised of three basic units: a charge sensitive amplifier/shaper with a fast tail cancellation; a 10 bit 10 MSPS low power ADC; a digital ASIC which contains the zero suppression circuit and a multiple-event buffer.

3.1 Preamplifier/Shaper

The charge collected on the TPC pads is amplified and integrated by a low input impedance preamplifier (Fig.1).

The pulse shape of the pad signals in a TPC geometry is rather complex. It depends on the details of the chamber and pad geometry. For the RCC structure, the time dependence of the induced signal changes from the substantial undershoot behaviour [3], due to the motion of positive ions relative to the pad and the wire planes, observed in flat cathode arrangements, into 1/t tail typical of proportional tubes. This tail has to be cancelled to 1% or better of the maximum pulse height in about 1μs.

These analogue functions have been implemented in a custom integrated circuit, named CALICE. This circuit, that is produced in a bipolar technology (HARRIS SEMICONDUCTOR UHF1X), contains in a silicon die of 7mm^2 the preamplifier and shaper circuits for 4 channels with a power consumption/channel of 5mW.

The CALICE circuit has an input impedance ranging from 60 Ω for the dc components up to 200 Ω for the highest frequency in the range of interest, a conversion gain of 5mV/IC, an output dynamic range of 2V with a linearity of 1%. It produces a pulse with a rise time of 120ns, a shaping time (FWHM) of 240ns and a tail cancellation at the ~1% level after 700ns.

The single channel has a noise value (r.m.s.) below 1000 e and a channel to channel cross-talk below -60dB. The chip is supplied with 3V/-2.5 V.

3.2 A/D Conversion

Fast-conversion ADCs of the required dynamic range and precision are commercially available. Conversion times of the order of 100ns (required in our case) can be achieved with flash-ADCs or with successive approximation pipelined ADCs.

The power budget of 50mW/channel calls for low power ADCs. Fortunately, due to the explosive growth of wireless communication systems and portable devices, where the power consumption is a major problem, 10 bit 10 MSPS ADCs with low power consumption are now widely available. Fig.2 shows the trend in the reduction of the power consumption, for 10 bit ADCs, during the last 10 years. From Fig. 2 we can see that, starting from 1996, several commercial ADCs with a power consumption below 100mW are commercially available. Furthermore, most of them feature a stand-by power consumption below 10mW. In this aspect it should be noted that the ALICE TPC has a duty cycle of 10%. The digitisation occurs during the
detector drift time (100 µs), triggered by the L1 decision (1KHz).

of the baseline, allows the subtraction of time dependent pedestal values from the ADC samples values. Alternatively this LUT, addressed by the ADC data, can be used to perform the corrections for the non linearity of the input signal during the pedestal subtraction. Finally the same LUT can be used to generate a test pattern. That is an important feature that allows complete test of the overall digital readout chain.

Fig. 2: power consumption versus year.

A study of 3 commercially available ADCs has been completed. Fig. 3 shows the ENOB versus the frequency of the input signal. We conclude that all three fulfil the ALICE TPC requirements in terms of performance and power consumption in the frequency range of interest.

3.3 Baseline subtraction, zero suppression and multiple-event buffering

The ALTRO (ALice Tpc ReadOut) chip is a custom VLSI integrated circuit. It contains the digital circuitry, for 8 channels, to perform pedestal subtraction, zero-suppression, formatting and buffering. In the block diagram of the ALTRO, shown in Fig. 4, the main logical units can be distinguished.

In the Pedestal Subtraction Unit (PSU) the lookup table (LUT) corrects any possible systematic instability

Fig. 3: ENOB versus input signal frequency

Another interesting option would be the use of a non-linear ADC. A candidate would be the CRIAD [4]. The CRIAD is a multiple-range linear ADC with 4 ranges. In each range the resolution is defined by an 8-bits linear conversion performed between two references, the upper one being the high end of the range, the lower one being ground (0V). The commutation of ranges is automatic with the signal amplitude.

Fig. 4: ALTRO block diagram.

In the Zero Suppression Unit (ZSU) the basic pulse detection scheme implemented is based on a fixed threshold, where samples of a value smaller than some constant decision level above the baseline (threshold) are rejected. To reduce the noise sensitivity, a glitch filter checks for a consecutive programmable number of samples above the threshold. In order to keep enough information for further feature extraction, a programmable sequence of pre-samples and post-samples are also recorded. Finally, the merging of two subsequent sets, closer than 3 samples, is foreseen. The implementation of this zero suppression scheme requires 16 pipeline stages. With this pipeline a programmable number (up to 16) of samples before the trigger (pre-trigger samples) can be stored. This feature allows the compensation of the L1 to L0 trigger latency (1.6 µs).

The zero suppressed data is formatted into 32 bit words according to a back linked data structure. L1 related data is stored in a multiple-event buffer. The Event Buffer Unit (EBU) can work both either as a fixed-length event buffer or as a variable-length event one. In the first case, a programmable amount of memory is allocated to each event independently of the event size; while in the second configuration each event occupies the memory space necessary to store the zero-suppressed event data. The first configuration clearly uses the data memory space inefficiently, while it has the advantage that front-end electronics does not need to propagate a "busy" signal to the TRIGGER/DAQ system.

The ALTRO chip interfaces to the external world through 4x10 bit ports, for the data coming from 8 dual ADCs, and a 40 bit control bus based on an asynchronous handshake protocol which can support a data transfer of 100 Mbytes/sec.

In order to have an estimation of the size and the power consumption, this circuit has been studied using the standard cell library of a 0.5µm CMOS process, leading to a die size of 8mm²/channel and a power
consumption of 8mW/channel. The production of a prototype in a MPW run is foreseen for the near future. An FPGAs implementation of the same circuit has been designed and is now used for the readout of the TPC prototype.

4. SYSTEM DESCRIPTION

A schematic diagram of the system components and their interconnection is shown in Fig. 5.

![Fig.5: System block diagram.](image)

The CALICE chips are bonded directly onto the backside of the readout plane, which houses the pad structure on its front side, using the Tape Automated Bonding (TAB) process [5]. The rest of the readout chain is contained in the front-end cards (FECs), which are plugged in crates, attached to the detector mechanical structure. Fig. 6 shows the configuration used for the prototype described in the next section.

![Fig.6: System mechanical structure.](image)

Each FEC contains 128 channels. 32 FECs are controlled by a "data routing module" (DRM), which interfaces the FECs to the DAQ, the Trigger and the Detector Control System (DCS). The DRM broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via a custom bus, based on the LVDS technology. The transfer of data words is synchronous and modules containing valid unread data are enabled to assert data on the bus by individual addressing. The interfacing of the DRM modules to the Trigger and to the DAQ follows the standard data acquisition architecture of the experiment [6]. The DRM modules also provide buffering of data and word counts. Data are finally moved via the LVDS bus to the FIFO driver of the optical link.

The readout of one event is performed in two separate phases, which are consecutive for a given event, but can otherwise be activated concurrently. In a first phase the trigger information is received by the TTC system [7] and broadcast to all modules in the subsystem starting the digitisation of each channel which lasts for the detector drift time. During this phase pedestal subtraction and zero suppression are performed. In the second phase, information is moved from the output buffers to the DAQ readout receiver cards via the optical link. The time needed to complete the second phase depends on the size of the event, but other triggers can be processed during the readout of previous event, as long as the multiple-event buffers in the FEC are not "nearly" full. Dead time can be generated (by sending an "XOFF" signal to the trigger in the variable length scheme) only when this condition occurs.

5. A 2000 CHANNELS PROTOTYPE

An important milestone in the design of the large TPC is the construction of a small prototype (~2000 channels) which will be installed in the NA49 experiment during '98. The front-end electronics for the prototype TPC is designed to incorporate the main features of the electronics for the full-size detector.

![Fig.7: FEC implemented as VME board.](image)

The realisation of the final set-up structure will be accomplished in two phases. In a first phase only the amplifier/shaper (PASA) chips will be installed close to the detector, directly mounted on the back-side of the
TPC PC board, using the Tape Automated Bonding (TAB) process. The rest of the readout chain will be housed in VME units (Fig. 7) (large format) 3 meters away from the detector (Fig. 8).

This has been done to allow the testing, during the first phase, of the detector and the new electronics chain, with the standard VME.

![Diagram of FEE for the Alice TPC prototype](image)

**Fig. 8: FEE for the Alice TPC prototype**

That has been considered as very important during the debugging phase of the prototype. In the second phase, the VME crates will be removed and new FECs will be placed close to the detector.

The amplifier/shaper chip used in the prototype is a version preceding the one above described. The main difference concerns the rise time that is of 50ns instead of 120ns [8]. For this rise time value the bandwidth limitation at about 4MHz, shown by one of the ADCs studied (Fig. 3), becomes important [9].

The ADC used in the prototype is the AD9200 (Analog Devices). The digital readout, including the pedestal LUT and the data memory, is implemented in the FPGA EPF10K20-TC144 (ALTERA). The board control logic, the VME interface and the LVDS bus interface are implemented in the FPGA EPF10K20-RC240 (ALTERA).

### 6. CONCLUSIONS

The ALICE TPC Front-End Electronics requires the development of two ASICs: a preamplifier/shaper circuit; a digital circuit to perform the pedestal subtraction, zero suppression and event buffering. The two ASICs, which fulfill the specifications, have been developed. ADC's according to the ALICE-TPC requirements are commercially available; however, a custom CMOS ADC, such the CRIAD, might represent an interesting solution to be further investigated. The multiplexing of a high number of front-end channels is achieved via a custom bus based on the LVDS technology. Test of a sizeable amount of this electronics in the NA49 (SPS) environment is underway.

### 7. REFERENCES


---

**Note:** The image and text provide a comprehensive overview of the ALICE TPC Front-End Electronics, detailing the processes, components, and developments involved in the project. The text emphasizes the importance of testing during the debugging phase and highlights the role of ASICs and custom buses in achieving high multiplexing capabilities. The references at the end of the document provide further reading material for those interested in the technical details of the project.
Abstract

Detector modules consisting of Silicon Strip Detector (SSD) and Front End Electronics (FEE) assembly have been designed in order to provide the two outer layers of the ALICE Inner Tracker System (ITS) [1] as well as the outer layer of the STAR Silicon Vertex Tracker (SVT) [2]. Several prototypes have been produced and tested in the SPS and PS beam at CERN to validate the final design. Double-sided, AC-coupled SSD detectors provided by two different manufacturers and also a pair of single-sided SSD have been associated to new low-power CMOS ALICE128C ASIC chips in a new detector module assembly. The same detectors have also been associated to current Viking electronics for reference purpose. These prototype detector modules are described and some first results are presented.

1. INTRODUCTION

The ITS includes 1706 SSD modules, i.e. about 2.6 Millions analog channels for 5.4 m² of surface and the SVT 320 SSD modules, i.e. about 0.5 Million analog channels for 1 m². All modules are identical in size and characteristics.

The 75x42 mm double-sided SSD includes 768 AC-coupled strips on each side. Global tests on leakage current and capacitance are performed on a probe station, as well as coupling capacitance measurements for each strip.

The analog readout of the detectors is performed by means of the ALICE 128C readout chips designed by the LEPSI at Strasbourg [3], [4]. The specific characteristics of this chip relate to a very low power consumption, on-chip control and remote tuning facilities. Its specifications have been presented earlier and the measured electrical characteristics are presented in another paper [5] in this workshop. Automatic analog and digital testing of this chip is performed at each assembly step. Statistical information is subsequently provided.

The prototype modules used for the tests are equipped with standard hybrids, fan-in on glass, and wire bonding. Signal/Noise ratio (S/N), resolution and charge matching are measured. The proposed final connection and packaging technique using TAB is presented in another paper by S.Bouvier [6].

2. SILICON STRIP DETECTORS

Three supplies of detectors have been tested. They have the same 75x42 mm overall size and the same 300 µm thickness for double-sided SSD or twice 150 µm for a pair of single-sided SSD. They have also the same general geometric layout: 768 strips on each side, no floating strips, 95 µm pitch, 25 µm to 30 µm strip width, stereoscopic angle of ±17.5 mrad, guard ring width ≤ 1 mm, double bonding pads on each strip end. Thus, they can be used with the same fan in, the same hybrids and the same connections (figure 1).

Figure 1: P side of the detector (simplified layout in full size).

They have also the same polarization technique (punch thru on both sides) and the same electric specifications: depletion voltage ≤ 60 V for 300 µm bulk thickness and, at depletion voltage, detector leakage current ≤ 5 µA, strip leakage current ≤ 5 nA and guard ring leakage ≤ 5 µA.
Differences between detectors relate to the resistivity of the material (≥ 6 kΩ.cm), the inner design techniques, the manufacturing processes, and the strip width which is defined as to provide a "coupling capacitor / parasitic capacitors" ratio ≥ 20 for each strip in order to limit the crosstalk. Typical coupling capacitor value is 150 - 200 pF as on figure 2. One can notice a shortened capacitor on the left, and a slope on the very right side corresponds to the shorter strip area.

![Fig. 2: Measured strip coupling capacitance side P/N](image)

### 3. READOUT CHIPS

Reference readout electronics use standard IDEA hybrids equipped with standard VA2 chips. Peaking time is tunable around 1.6 μs, dynamic range is 4 MIPs and nominal ENC is 135 e + 12.3 e/pF [7].

The new readout electronics uses the ALICE128C 128 channels chip designed with the AMS 1.2μm CMOS technology. The die size is 6 mm x 8.5 mm [3]. Each channel amplifies, shapes and stores as a voltage signal onto the capacitance \( C_{\text{HOLD}} \), the charge collected on a strip of the detector. The shaping time \( t_s \) is adjustable from 1.4 μs to 2 μs. The dynamic range extends to more than ±12 MIP. Nominal ENC is 290 e + 8 e /pF. Power supply is ±2 V. Special attention has been taken to power consumption which is always below 850 μW/channel and drops down to 340 μW/channel for a 1 ms readout cycle. An analog multiplexer allows a sequential readout of the data at a rate of up to 10 MHz through a tristate output buffer shared by the 128 channels. The output buffer has been designed to drive an external link with a 100Ω characteristic impedance in parallel with a capacitance of up to 20 pF. A slow control mechanism implementing the "JTAG IEEE1149.1" protocol biases the different analog blocks and tunes the shaping time [8]. It also controls an internal test pulse generator which provides a variable current pulse emulating a deposited charge up to ±11 MIP. The channels, where the pulse has to be injected, are selected through a shift register. At the output, one can read sequentially all the signals stored on the \( C_{\text{HOLD}} \) capacitances in a normal readout cycle or select one particular channel through the output shift register to visualize, in "transparent" mode, the shape of the signal at the output of the shaper in order to measure/set the shaping time. Of course, the pulse generators have to be calibrated for characterization use. All the different testing configurations and the pulse level, i.e. all the registers, are addressed by means of the JTAG controller.

### 4. HYBRID

The prototype hybrid has been made by a set of two thick printed circuit boards (PCB) which provide electrical connections and mechanical support for chips, detector, fan in, external components and connectors to link it to the outside world for signals and power supply. It is presented in figure 3.

![Fig. 3: Hybrid assembly](image)

All the PCBs are identical. Each PCB holds six ALICE128C chips for the readout of the 768 strips located on each detector side. Each board operates one detector side. Thus, two boards are needed for each double-sided detector or for a pair of single-sided detectors. They face each other in a symmetric way but they are completely electrically insulated in order to be floated. Even with the very high coupling capacitor yield of the detectors (≥ 99%), we chose to float one side of the double-sided detectors in order to avoid depletion voltage to be applied across the capacitors. We can float any P or N detector side in order to evaluate the noise added by the opto-insulation (≥ 100 e⁻). External components relate mainly to decoupling capacitors and current reference resistors.

### 5. BEAM TEST SETUP

The beam tests have been performed over three runs in May and June 1998 at CERN on the SPS accelerator with 125 GeV pions, and in August 1998 on the PS accelerator mainly with 10 GeV pions.

Figure 4 presents the detectors under test (DUT) placed into a submicron precision silicon telescope for beam test purpose [9], [10], which provides geometric and timing reference information for charged tracks. The detector frame is equipped with 4 single-sided
reference detector pairs having a readout pitch of 50 µm. They provide a spatial resolution of 1.4 µm per detector and a track extrapolation error lower than 1 µm in the center of the telescope.

The data acquisition frame located in the control room includes essentially the trigger electronics, a data acquisition VME crate with the Eurocom CPU, VME Sirocco ADC boards, and an acquisition sequencer board. Data are recorded on Exabyte cassettes. The acquisition program OS9DAS which runs under control of a terminal is based on Microdas software [11].

A PC running a LabView control program is interfaced with the DUT by means of a JTAG interface. It performs the detector control, i.e. it stores the operating FEE parameters (biasing, shaping time a.s.o.) and initializes the detector assembly. It is also in charge of hardware tests.

6. TEST RESULTS

For the detectors provided by two manufacturers C and E, the analysis is focused on signal over noise ratio on both sides, on charge matching result for the double-sided detectors and on geometric resolution. The S/N of the detector C with Alice128C readout is shown in figure 5 and the corresponding charge matching in figure 6. The S/N of the detector E with Alice128C readout is represented in figure 7 and the corresponding charge matching in figure 8. The pulse height ratio P/N is displayed in figure 9. For all detectors, the results correspond to side N floating.

6.1 ALICE128C chip on detector C

6.2 ALICE128C chip on detector E
6.3 VA2 chip on detector C

The S/N of the detector C with VA2 readout is shown in figure 10 and the corresponding charge matching in figure 11.

![Fig. 10: S/N detector C](image)

![Fig. 11: Charge matching detector C](image)

The nearly rectangular shape can be explained by the geometric characteristics of the detector which has a 95 µm wide pitch and no intermediate floating strips. The number of strips involved in a cluster is below 2. Thus, the distribution of perpendicularly arriving particles provides a resolution of 22 - 25 µm. This is slightly better than the geometric resolution value of the pitch over the square root of 12.

![Fig. 12: Resolution P side detector C](image)

6.4 ALICE128C chip on SS detector

A set of two single-sided 150µm SSD has been glued back to back in order to provide a detector assembly with the same layout, size and total thickness as the double-sided SSDs. The front end electronics is equipped with ALICE128C chips. This option was considered earlier in order to avoid floating electronics. The main expected difference in characteristics besides the half depletion voltage is the S/N ratio of about 20 shown in figure 14. It is directly related to the thickness of each SSD. This measurement provides a valuable information on the possibility to reduce the thickness of the chosen double-sided SSD for the ALICE and STAR experiments.

![Fig. 13: Resolution N side detector C](image)

![Fig. 14: S/N single-sided detector 150µm thick](image)

6.5 S/N DATA SUMMARY

The maxima of the S/N ratio distribution for double-sided detectors from the two different manufacturers (C and E) linked to either ALICE128C chips or VA2 chips are summarized in table 1.

| Table 1: Signal / Noise summary for double-sided SSD |
|-----------------|--------|--------|
| S/N             | P side | N side |
| Detector C + VA2| 55     | 40     |
| Detector C + ALICE| 45    | 40     |
| Detector E + VA2| 65     | 35     |
| Detector E + ALICE| 55    | 30     |
The N side S/N ratio is lower than the P side for two main following reasons: the strip insulation technique on the N side of the detector made by P spray and the need for floating electronics on one readout side. This latter request requires opto-insulation of the readout electronics on the chosen N side which adds some noise and thus reduces the S/N ratio.

ALICE128C chips provide S/N ratio lower by 10 units than VA2 chips. This must be related to the 3 time larger dynamic range and to a 4 time lower power consumption.

One can also notice that the detector of the manufacturer C provides a medium S/N, nearly balanced on both sides, whereas the detector of the manufacturer E provides a generally higher S/N ratio on side P and lower on side N.

7. TOTAL DOSE EFFECT AND LATCHUP

The total dose effect has been tested on the detector as well as on the ALICE128C chip on the Viviron tandem accelerator with 20 MeV protons. These irradiation tests will be pursued soon. Preliminary results reveal an increase of the detector leakage current of 14 nA/krad whereas the ALICE128C chip shows a decrease of the pedestal voltage.

The latchup cross section of the ALICE128C chip has been defined. This cross section has a threshold at 5000 MIP and the overlapping area between the cross section and the expected energy loss spectrum in the chip is about to be evaluated by simulation.

8. CONCLUSION

The present results relate to several detectors of different kinds. All detectors were working. They provide interesting information but the statistics is too low to enable a reliable technical discrimination between the two manufacturers.

The difference between the two readout chips was expected and corresponds to a different design goal. Roughly, compared to the VA2 chip, the ALICE128C chip provides a 3 time expansion of the dynamic range and a much lower power consumption (down to 1/4) for a S/N ratio of less than 20% lower.

One concludes that the chosen detector layout and biasing technique provide a space resolution below the 27 μm recommended in the ALICE technical proposal.

The double-sided technique allows charge matching selection for ambiguous hits.

The ALICE128C chip demonstrates its ability to provide good data with reasonable S/N ratio. It allows drastic reduction in power, in cooling and in material by reducing the external components.

ACKNOWLEDGMENTS

We are greatly obliged to Ogmundur Runolfsson, Robert Hammarstrom and Kaspar Muhlemann for their determinative help in bonding the detectors onto the hybrids.

REFERENCES

THE ABCD BINARY READOUT CHIP FOR SILICON STRIP DETECTORS
IN THE ATLAS SILICON TRACKER

W. Dabrowski
Faculty of Physics and Nuclear Techniques,
UMM, Cracow, Poland (email: W.Dabrowski@ftj.agh.edu.pl)
F. Anghinolfi, P. Jarron, J. Kaplon, C. Lacasta, P. Weilhammer
CERN, Geneva, Switzerland
D. Campbell*, W. Gannon, P.W. Phillips
Rutherford Appleton Laboratory, Didcot, UK
A. Clark, D. LaMarra, D. Macina, A. Zsenei
University of Geneva, Switzerland
D. Dorfan, T. Dubbs, A. Grillo, E. Spencer
Santa Cruz Institute for Particle Physics, UCSC Santa Cruz, CA, USA
N. Kundu
University of Oxford, Oxford, UK
G. Meddeler*
NIKHEFF, Amsterdam, The Netherlands
P. Staaf
University of Uppsala, Sweden
M. Wolter, R. Szczygiel
Institute of Nuclear Physics, Cracow, Poland

Abstract

The ABCD chip is one option for the front-end readout architecture for silicon strip detectors in the ATLAS Silicon Tracker. The chip comprises all functional blocks required for the binary readout architecture. Two batches of 8 wafers have been manufactured successfully while the DMILL process was still in the stabilisation phase in the Temic foundry.

An overview of the design architecture and expected performance is presented along with the test results obtained from the first prototype batch. Some preliminary results from the second batch are reported as well. Full required functionality has been achieved although some analogue parameters are not fully satisfactory. The problems recognised in the present prototype are discussed.

1. INTRODUCTION

The ABCD design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker [1]. The design follows previously developed prototype, the SCTI28B chip [2]. Functionally it is fully compatible with another technological option being developed for the SCT and employing two separate chips: CAFE-M [3] - a front-end chip realised in the MAXIM bipolar process and ABC [4] - a binary pipeline chip realised in the Honeywell bulk CMOS process. The DMILL technology [5] in which the ABCD chip is fabricated, being a BiCMOS one, offers a possibility to implement the complete binary architecture as required for the ATLAS SCT in a single chip. Two versions were designed and manufactured, for the p-side and for the n-side readout of silicon strips.

* presently at Oxford Instruments
* presently at LBNL, Berkeley, CA, USA
2. THE ARCHITECTURE

Only a short overview of the architecture of the ABCD design is reminded here since it has been presented and described before [6]. The block diagram of the chip is shown in figure 1. It comprises all blocks of the binary readout architecture, the front-end circuitry employing a bipolar transistor in the input stage, discriminators, binary pipeline, derandomizing buffer, data compression logic and the readout control logic.

The main blocks of the SCT128B prototype, the front-end circuits and the pipeline, have been implemented in ABCD with some minor changes. Compared to the SCT128 architecture [2,6] some new features have been introduced in the ABCD design. The most important one is the sparse readout logic which allows performing zero suppression on the chip so that only addresses of hit channels can be read out.

3. SINGLE CHIP TEST

Detailed evaluation of the chip performance has been performed separately for the analogue parameters and for digital parameters using dedicated single chip test set-ups.

3.1 Front-End Performance

In order to measure in detail the analogue performance of the ABCD front-end circuitry a dedicated evaluation board has been designed. A standard set of measurements as described in [2] was performed. The extraction of basic parameters, i.e. gain, noise and offset spread was obtained form a number of discriminator threshold scans. The results presented here are from chips fabricated in the first ABCD batch.

Figure 2 shows an example of the so-called S-curve which represents the probability of firing the discriminator as a function of threshold for a given input signal of 3 fC. The wide spread of the S-curves illustrates the main problem of the present prototype: a large spread of the effective offset across the 128 channels of a given chip. By fitting the measured S-curve to the error function one obtains the rms value of noise at the input of the discriminator. The distribution of noise for 128 channels in one chip is shown in figure 3. From the threshold scans for several input charges one obtains the gain of the front-end circuitry and the discriminator offset. Taking into account the average gain of 112 mV/fC, as shown in figure 4, the equivalent noise charge of 760 eV rms is measured which is about 20% higher than the expected value.
3.2 Digital Performance

For detailed evaluation of the digital part of the ABCD design a general purpose mixed signal tester at CERN was used. The tester allowed for a direct comparison of VERILOG simulations and functionality of the device. Additionally it allows to test the digital functionality with increasing clock to determine speed margins for various digital blocks.

The test vectors were extracted from the VERILOG models. In total about 100,000 test vectors were run for the complete digital test of the chip. The data test patterns were generated randomly to simulate all possible configuration of hits in the chip. For the chips which passed all the tests the output data was required to be identical with the simulated/expected results. The test were run at various (increasing) clock frequencies up to the point where the chip failed to respond correctly. Two test modes were applied: A - L1 and BC counters excluded from data comparison, and B - full data comparison. A typical example of test results is shown in table 1.

Table 1. Maximum clock frequency in MHz achieved for various digital tests of the ABCD chip.

<table>
<thead>
<tr>
<th>Test description</th>
<th>Mode A</th>
<th>Mode B</th>
</tr>
</thead>
<tbody>
<tr>
<td>SendID, address decoding</td>
<td>66.7</td>
<td>50.0</td>
</tr>
<tr>
<td>BC reset test</td>
<td>x</td>
<td>52.6</td>
</tr>
<tr>
<td>DTM mode, no hit</td>
<td>62.5</td>
<td>50.0</td>
</tr>
<tr>
<td>DTM mode, single hit</td>
<td>58.8</td>
<td>50.0</td>
</tr>
<tr>
<td>DTM mode, multiple hit</td>
<td>58.8</td>
<td>47.6</td>
</tr>
<tr>
<td>Accumulator test</td>
<td>52.6</td>
<td>50.0</td>
</tr>
<tr>
<td>Data Compression logic test</td>
<td>45.4</td>
<td>45.4</td>
</tr>
</tbody>
</table>

The obtained results confirm that the chip meets the basic requirements of operation at 40 MHz. Comparing results for the two test modes A and B it is clear that some speed limitation is introduced by the first level trigger (L1) counter and the bunch crossing (BC) counter. The most critical block, however, appears to be the Data Compression Logic, as was expected during the design phase because it uses some asynchronous logic circuitry which is sensitive to parasitic components in the layout.

4. WAFER SCREENING

4.1 Test Set-up

An automatic wafer test system has been developed to test digital functionality as well as to measure basic analogue parameters of the front-end circuit at the wafer level. The system is based on a Karl SUSS PA200-II probe station with a fully motorised chuck stage. The schematic diagram of the test system is shown if figure 5. The chip control and data acquisition is based on VME modules: a sequencer (SEQSI) which provides clock and control signals for the chip, and a data receiver (DRAFT). The probe station movement is controlled via a GPIB interface. For measurement of characteristics of the digital-to-analogue converters on the chip an HP voltmeter with an analogue multiplexer is used, interfaced to the system via the GPIB bus.

![Automatic wafer test setup](image)

Fig. 5. Schematic diagram of the wafer test system.

Our aim was to test the digital functionality of chips on the wafers at the nominal operating clock frequency of 40 MHz and also to measure basic analogue parameters. This has been achieved first of all by implementation of some testability functions in the ABCD design, notably internal calibration circuitry which generates test pulses for the front-end with controllable amplitude and timing. In this way no analogue signal is required to be provided to the chip for measurements of analogue parameters. Because of the binary architecture the output data is delivered also in the digital form.

The probe card is made in a standard technology with 62 needles and a typical pitch of 200 µm. In order to cope with 40 MHz digital signals, custom designed buffering and terminating circuitry has been implemented on the PCB in a close distance about 2 cm to the needles. The photo of the chip under test is shown in figure 6.
4.2 Test Procedures

Each chip on the wafer is tested in four basic steps, starting from a simple test of digital functionality and ending with a basic characterisation of analogue performance. The four steps are:
- basic digital test
- advanced digital test
- threshold scans
- DAC measurements.

Presently the test is continued through all 4 steps regardless of the result of each step.

In the basic digital test the operations of write/read the status register is performed. The contents of the status register is checked for various chip addresses. In the advanced digital test the testability implemented in the design is used. First the operation of writing and reading the mask register is performed for 4 different mask patterns and 2 sets of the clock and command inputs. Subsequently test vectors are loaded into the mask register in the test mode and the data is read out at the output. This way all the digital circuitry starting from the mask register up to the output is exercised. The qualification of the chips for correct digital functionality is based on a comparison of the output pattern with the input test vector.

In order to extract basic analogue parameters of the front-end the discriminator threshold scan is performed for 3 different levels of calibration pulses, corresponding to 2, 3 and 4 fC of the input charge. From this data we can extract the gain and noise of the front-end circuit and effective offset of the discriminator for each channel according to procedures described in ref. [2]. In the last step the characteristics of the data-to-analogue converters on the chip are measured over full range of operation.

4.3 Test Results

Concerning the digital functionality the chips are qualified as good ones if they pass 100% of basic and advanced digital tests performed at the nominal clock frequency of 40 MHz. The yield evaluated on the basis of the digital test was between about 30% for the first batch of wafers and about 90% for the wafers from the second batch delivered.

A set of typical results of analogue tests performed for a wafer from the second batch is shown in figure 7. The plots show the distributions of gain and offset for 128 channels in one chip. Figure 8 shows the distributions of mean values of gain and offset for 131 chips from one wafer which passed before the digital test. At this point it should be noted that during wafer testing the front-end circuit is biased below the nominal conditions so that we have a lower gain which helps to keep the chips in stable operation. For the nominal bias conditions the gain is about a factor of 2 higher (see figure 4).
Although the measurement conditions on the wafer tester are not sufficient to extract precisely the analogue parameters of the front-end, we have found that the measured parameters correlate well with those obtained later on from modules equipped with the tested chips. Based on the parameters measured on the wafer level we can assign an analogue quality factor for each chip taking into account the gain value, spread of gain and spread of offset. In our present wafer probe system the typical noise level measured on the wafers is about 1700 el rms compared to the typical value about 600 - 800 el rms measured for a single chip operated on the dedicated test board or on the ceramic hybrid. On the other hand we observe a quite consistent level of noise for all chips independently of the gain and offset spread.

5. SCT MODULE

The ABCD chips have been used successfully to build a full size SCT detector module formed by 2 daisy chained silicon strip detectors of dimensions 6.4 x 6.4 cm². The effective length of strips is 12.6 cm resulting in the total capacitance load at the preamplifier input of about 20 pF. The pitch of strips is 80 µm and the total number of 768 strips are read out by 6 ABCD chips via the token ring system implemented in the ABCD architecture. The chips are placed on the ceramic hybrid providing the power supply connections, control signal and data connection as well as a mechanical support.

A standard set of measurements was taken for the fully populated hybrid before detectors were connected and subsequently for the complete module. Figure 9 shows the distributions of noise for 6 chips operated on the hybrid without and with the detector connected. On average noise is about 900 el rms for the chips with zero input capacitance and 1600 el rms with full length strip detectors. Assuming the total detector capacitance of 20 pF one obtains the noise slope of 35 el/pF which is close to the expected value. The baseline noise of 900 el rms measured on the fully populated hybrid is substantially higher compared to the noise measured for a single chip and this effect has to be investigated further.

6. CONCLUSIONS

The prototype readout chip for the ATLAS semiconductor tracker has been developed and manufactured successfully in the DMILL technology being transferred to the TEMIC foundry. Full digital functionality of the prototype has been obtained at the nominal operating clock frequency of 40 MHz. The analogue performance is mostly satisfactory although the variation of some parameters across the chips, notably the effective offset at the discriminator, has to be reduced.

An automatic wafer test system has been developed and proved to be useful for qualification of chips.

Fig. 9. Distribution of noise for 6 chips on the module without detectors connected (hybrid) and with detectors connected (module).

including the analogue performance. The 8 wafers from the first batch have been tested and chips delivered to the collaboration for building prototype SCT modules.

The chips from the two batches manufactured during the phase of process stabilisation exhibit a consistent improvement of device parameters as well as improved yield.

REFERENCES

PERFORMANCE OF A CMOS MIXED ANALOGUE-DIGITAL CIRCUIT (APVD) FOR THE SILICON TRACKER OF CMS


1 IPNL Lyon France, 2 IReS Strasbourg France, 3 IC London UK, 4 LEPSI Strasbourg France, 5 CEA Saclay France, 6 RAL Didcot UK

* corresponding author: E-mail: philippe.schmitt@ires.in2p3.fr
IReS, 23, rue du Loess, B.P. 28, F-67037 Strasbourg, Tel: 33 3 88 10 66 24, Fax: 33 3 88 10 62 34

Abstract

The APVD is a rad-hard front-end readout integrated circuit in the DMILL technology for the silicon tracker of CMS.

The circuit contains 128 identical analogue channels, each one composed of a low noise preamplifier, a CR-RC shaper, a 160 cells deep analogue pipeline and a signal processing stage. A deconvolution filter at this point recuperates the initial fast response function of a silicon detector and confines it to one LHC bunch crossing. The 128 analogue channels are read-out by a serial output via a high-speed analogue multiplexer. Slow control is implemented on the chip using an I2C serial bus interface, which configures the chip and runs the internal calibration system. A dedicated block generates all the biases.

This paper presents the measured performance of the first APVD prototype.

1. INTRODUCTION

The CMS inner tracker contains approximately 19' channels from both silicon detectors and Micro-Strip Gas Chambers (MSGC). The main target is to build a system with minimum power consumption, minimum material and sufficiently low noise. An analogue readout system has been chosen for the following reasons: robustness, better resolution and easiness of testability. Existing rad-hard technologies have to be employed to meet the LHC time schedule.

The APVD is the first prototype for CMS of a rad-hard front-end readout chip developed in the DMILL process. It has been designed by a French-British collaboration of several laboratories. The design of the APVD is based both on the topology of the front end chip APV6 [1] fabricated in the Harris AVLSIRA technology and the design experience of the front-end chip FILTRES [2] developed in the DMILL process.

The DMILL technology uses an SOI substrate and integrates monolithically rad-hard, low noise, analogue-digital CMOS, JFET and bipolar transistors. This technology allows the design on the same chip of both analogue and digital fast circuits.

Submitted in summer 1997, the prototype of the APVD has been received in the beginning of 1998. Due to unexpected high values of one resistor type, the chip has been re-fabricated in a second run and has been received in September, two weeks before this conference. After a brief introduction of the main design features of the APVD, this paper will present the measured performance of the first run.

2. APVD DESIGN FEATURES

The block diagram of the APVD [3] is shown in Figure 1.

Fig. 1 APVD block diagram

The 128 analogue input pads are situated on the left-hand side of the chip. The silicon strip detectors are connected to the input pads by ultrasonic wire bonding. Standard DMILL ESD (Electro-Static Discharge)
In the VME LabVIEW, who drives a VME instrument via a GPIB bus. This characterise the chip (Figure 2). An electronic test bench has been added to the input pads. The current pulse is transformed into voltage by a charge preamplifier and then amplified and filtered by a CR-RC shaper. The signals are buffered by a source follower connected to the analogue pipeline ADB (Analogue Delay Buffer), where the signals are sampled and stored at 46 MHz. On receipt of a first level trigger, the signals are read and processed by the APSP (Analogue Pulse Shape Processor). The analogue output current signal is read-out serially at 20 MHz. The control of the circuit is provided by several blocks. On the right-hand side, the I2C interface allows programming of the main parameters of the circuit for the slow control and also generates the signals to cycle the APSP. The pipeline control logic controls the writing and the reading sequences of the analogue pipeline. The addresses of the tagged cells are stored in a FIFO. Further on the left, there is a pulse generation unit that internally generates calibration pulses for testing the analogue chain. The bias generator block is a set of RAM based registers and DAC’s, and generates all the bias currents and control voltages for the analogue blocks and some digital patterns for the calibration pulse generator. It is programmed through the I2C controller. All digital processing of the chip and its pad layout are identical to the APV6.

3. TEST BENCH DESCRIPTION

An electronic test bench has been developed to characterise the chip (Figure 2).

A precise electric charge is sent to a selected input channel of the chip by a pulse generator, whose delay is controlled via the GPIB. After trigger reception, the APVD chip sends serially an output frame containing 128 multiplexed analogue values to an oscilloscope or to an ADC board [4] located in the VME crate for measurement. The data are then read and treated by the PC.

Several test programs developed under LabVIEW allow a complete characterisation of the chip.

4. BIAS AND INTERNAL CALIBRATION

There are seven analogue biases (4 currents and 3 voltages) to control the analogue chain (preamplifier, shaper, source follower and analogue processor). These currents are obtained in the bias generator by mirroring a reference current with different ratios controlled by the I2C interface. For the voltages, an internal conversion resistor is added. The reference current can be generated via an internal or an external resistor. The value of the internal resistors on the first run of the APVD was out of specification; an external reference current has to be used.

Test pads on the chip permit the measurement of the biases sent to the analogue chain. Figures 3 and 4 show respectively current and voltage biases as function of the slow control I2C code. These biases cover the whole application range with good linearity and the spread from chip to chip is below 2%.

![Fig. 3 current biases linearity](image)

![Fig. 4 voltage biases linearity](image)
The internal calibration system can inject calibration charges up to 10 MIPs to all inputs of the chip through eight calibration lines. This allows the measurement of the amplifier pulse shape on the chip. A request pulse sent by the APVD sequencer via chip sequencing link sets a calibrated pulse to selected channels. A trigger with an appropriate latency starts the read-out of the chip. Moving the calibration request by steps of 25 ns, a coarse reconstruction of the shape can be made. In order to obtain a better resolution, the calibration pulse can be delayed by steps of 3.125 ns by controlling the I2C programmed internal delay line.

A trigger with an appropriate latency starts the read-out of the chip. Moving the calibration request by steps of 25 ns, a coarse reconstruction of the shape can be made. In order to obtain a better resolution, the calibration pulse can be delayed by steps of 3.125 ns by controlling the I2C programmed internal delay line.

5. ANALOGUE PERFORMANCES

Operating at 20 MHz, a 128 to 1 three-level multiplexer drives the analogue output current of the chip. The analogue data are preceded by a 4-bit header where the third bit indicates an internal logical error and an 8-bit address corresponding to the triggered pipeline column. Although it is impossible to totally suppress the coupling between the analogue output frame and logical signals in the analogue multiplexer, precise sampling in the ADC reduces additional noise contribution.

The difference in rise time between the two curves is typically due to the electronic response time of the chip. An undershoot of a few per cent has also been observed. An adjustment of the shaper parameters is needed to suppress this phenomenon in the next design. Nevertheless the shape is close to an ideal CR-RC.

The linearity tested in peak mode over a dynamical range of ±6 MIPs is shown in figure 8.
Figure 9 shows a typical measurement from a set of different channels in the six modified chips. In peak mode the gain is 95 µA/MIP and the non-linearity is less than 8 % over ±5 MIPs range. The peaking time varies slightly between 47 and 50 ns in the ±5 MIPs range.

Fig. 9 Linearity in peak mode

It should be noted that the amplifier pulse shape depends slightly on input capacitance. A gain variation less than 5% with a loss of 9 ns in peaking time is observed when a capacitance of 15 pF is added to a PCB line capacitor around 5 pF.

Fig. 10 Amplifier shapes versus input MIPs in deconvolution mode

Figure 10 gives the average shape of the deconvolution filter. The small undershoot is due to sensitivity of the deconvolution method to a non-ideal CR-RC amplifier response. A gain of 90 µA/MIP over ±5 MIPs is obtained. The non-linearity is less than 10 % with correct rise time (Fig. 11).

Fig. 11 Linearity in deconvolution mode

6. NOISE PERFORMANCE

Two different noise measurements have been performed in peak and deconvolution modes. Using an oscilloscope to read-out the analogue pedestal of a selected channel in several thousand samplings with a precision of 100 ps, a Gaussian distribution of amplitude can be collected. The ENC of the APVD can then be calculated from this distribution. This method allows an accurate measurement of ENC. Figure 12 shows a typical noise performance of the APVD in peak mode and deconvolution mode respectively.

Fig. 12 APVD noise performance

The average values of the measured noise figures are:
- Peak mode: 505 ± 45 e/pF
- Deconvolution mode: 870 ± 53 e/pF

The noise measurement in peak mode agrees with our simulation. In deconvolution mode the noise is higher than in peak mode mainly due to multi-sampling. The APSP enters three times in this mode is also a possible noise source[5].

7. PIPELINE AND PROCESSOR PERFORMANCE

By changing the T1 trigger timing in 25 ns steps, a complete scan of the pipeline can be obtained. A typical outcome of this test is shown in figure 13 where the pedestal is plotted as a function of both the channel and the cell number.

From this measurement, three points can be verified:
- Firstly, defective cells of the pipeline, caused by the technology problems or the sensibility of our design to the technology, can be correctly defined. We also observe a dispersion of pedestals from channel to channel.
- Secondly, the contribution of the cell to cell fluctuation to the total noise can be measured and is less than 200 rms electrons. This value is negligible when added in
quadrature to the input noise obtained for a realistic detector capacitance.

Finally, by subtracting two measurements with and without input internal calibration pulse, channels can be identified in which preamplifier or shaper have a problem. This measurement allows also a check on the uniformity of the gain from channel to channel. From nearly 3000 channels in all tested chips, around fifteen preamplifier-shapers were defective. A good uniformity has been obtained.

Figure 14 represents the Analogue Pulse Shape Processor (APSP) performance. There are two curves on the figure. The first is directly obtained by using the deconvolution mode. Using the three-deconvolution weights and the amplitudes of three corresponding points measured in peak mode, the second curve was obtained. We can see that the APSP works correctly.

8. CONCLUSIONS

The APVD is a 128-channel front-end readout integrated circuit in the rad-hard DMILL technology for the silicon tracker of CMS. The first version of the chip has been evaluated. The internal control system works correctly and a good analogue performance of the chip has been found. This version of the APVD is now under beam test at CERN for silicon detector. In spite of good functionality of the APVD, several potential problems, such as instability in certain bias conditions, sensitivity to technology variation, have been found. Further studies will be made to improve the APVD performance. Evaluation of the chip in its environment will give us more conclusive information. A temperature test as well as an irradiation measurement will be performed as soon as possible. In order to evaluate large quantities of chips an automatic on wafer test bench will be developed.

ACKNOWLEDGEMENTS

We would like to thank the technical staff of our laboratories for their continuous and valuable support. In particular, we thank O. Runolfsson for his kind and very professional support of bonding many chips on their respective test-boards.

REFERENCES


A 128 Channel Analogue Pipeline Chip for MSGC Read-out at LHC

L L Jones, M J French, Rutherford Appleton Laboratory, UK
M Raymond, G hall, F G Sciacca, Imperial College, London, UK

Abstract

A 128 Channel analogue pipeline chip has been made for the read-out of CMS MSGC detectors at the LHC. Developed from the APV series, it features slow shaping and a deconvolution-type algorithm optimised for MSGC signals. Leakage current compensation has been employed, and leakage current monitoring provides warning of possible MSGC breakdown. The first version of the circuit has been fabricated using Harris AVLSI-RA radiation hard technology.

1. INTRODUCTION

Over the last few years, a series of CMOS chips, the APV circuits [1], has been developed to read out silicon microstrip detectors for the CMS. This architecture has been further developed and modified to optimise it as far as possible for MSGCs whilst minimising the circuit changes required.

The CMS MSGCs have lower capacitance than the silicon strips which has implications on the noise performance, and they are required to be DC coupled to the front-end, so the chip must be immune to leakage currents. MSGC strips are also prone to breakdown causing discharges which may damage the strips and the electronics. Warning must be given so that damage can be avoided. In addition the weights of the deconvolution algorithm have been modified to achieve sufficient timing resolution for the expected MSGC signal shape.

The chip has three modes of operation. One mode, Deconvolution, is used in normal operation when data rates are sufficiently high such that the effects of pile-up are significant. The second, Peak, is used when pile-up is not significant and a larger signal to noise ratio is required. The third, Multi, is a test mode which allows multiple consecutive pipeline columns to be triggered and read out.

Additional features include a dedicated calibration circuit for fine timing resolution, programmable pipeline latency, and an on-chip bias generator, all of which are programmable through a Philips PC compatible interface, and apart from the current monitoring outputs the pin-out is fully compatible with the silicon version.

2. CHIP OVERVIEW

The APV-MSGC (figure 1) is an analogue pipeline ASIC intended for read-out of MSGC detectors in the CMS tracker. The architecture of the CMS tracker read-out system is based on analogue processing of data in the detector prior to transmission in analogue form to the DAQ.

Figure 1 APV-MSGC chip

The chip contains 128 channels of preamplifier and shaper driving a 160 column analogue memory into which samples are written at the LHC 40MHz frequency. The memory always contains a record of the most recent beam crossing that the chip has sensed, and data access mechanisms allow the triggering and queuing of data in the memory for output. Triggered data are then processed with a deconvolution-type filter (APSP) - a switched capacitor network which deconvolves the shaping function of the preamplifier and shaper stages to give a pulse shape with sufficient timing resolution for MSGC signals. Following the APSP, data are held in a further buffer until they can be read out serially through an analogue multiplexer at 20MHz. The APV-MSGC also contains features required for eventual use in CMS including a programmable bias generator, an internal test pulse generation system, and a slow control communication interface.

The APV-MSGC is developed from the APV6 - the silicon microstrip read-out chip - but has been redesigned to optimise it for MSGC signals. To achieve this several modifications have been made to the APV6.

1. Front-end modified to optimise for MSGC capacitance
2. Addition of a leakage current compensation circuit
3. Addition of leakage current monitor circuit to warn potential detector breakdown
4. Additions to bias generator for biasing above circuitry
5. Deconvolution algorithm changed to optimise for MSGC signal shape
6. New mode of operation for reading out consecutive triggers
At this stage it was not thought practicable to include a baseline restoration circuit for each channel. This would have been used to ensure that the preamplifier and shaper recovered quickly following saturation by very large signals. Inclusion would have meant increased chip size due to the additional circuitry required in each channel and the modifications necessary to the bias generator.

3. FRONT END

The front-end electronics of the APV-MSGC chip (figure 2) are essentially the same as that for the APV6, but with slight modifications for noise optimisation and pulse shape adjustment, and additional circuitry for detector leakage current compensation and monitoring. In addition the input protection diodes have been increased in size to make them comparable with those found in the PreMux128 - a 128 channel preamplifier-shaper chip which has been extensively used in the characterisation of the MSGC detectors.

3.1 Preamplifier

The preamplifier is a charge amplifier made from a single-ended folded cascode amplifier with a 250fF feedback capacitor and a long channel nfet feedback transistor. The pfet input transistor has a size of 400/1.4 and is biased at 400µA. Its source is connected to GND to reduce power consumption. The gain of the preamplifier is 15.4mV/silicon MIP (where a silicon MIP = 24000 electrons). The output is buffered by a source follower which also provides the level shift required for DC stability through the feedback transistor. The feedback transistor also provides a discharge path, in order to avoid pile-up in the preamplifier, and is usually set to give a resistance in the order of 100MΩ.

The transimpedance gain of the preamplifier is

\[ V_{\text{out}}(s) = \frac{R_{\text{fp}}}{sR_{\text{fp}}C_{\text{fp}} + 1 + sR_{\text{fp}}C_{\text{fp}}} \]

\[ \text{Pip} = \frac{R_{\text{fp}}C_{\text{fp}}}{2} \]

\[ V_{\text{peak}} = \frac{2C_{e}V_{\text{in}}}{eC_{f}} = 5.3 \times V_{\text{in}} \]

3.2 Shaper

The shaper is derived from the same folded cascode amplifier architecture as the preamplifier with a 250fF feedback capacitor but a shorter nfet feedback transistor. The input coupling capacitor is of magnitude 1.8pF. The pfet input transistor has a size of 400/1.4 and is biased at 88 µA.

The voltage gain of the shaper is given by

\[ V_{\text{out}}(s) = \frac{\frac{sR_{\text{fp}}C_{\text{fp}}}{1 + s^2C_{\text{tp}}R_{\text{fp}} + 1 + sC_{\text{tp}}R_{\text{fp}}} \left( C_{\text{fp}} + C_{\text{sh}} \right)}{sR_{\text{fp}}C_{\text{fp}}} \]

This is equivalent to a CR-RC shaper with a peaking time

\[ t_{\text{peak}} = \frac{R_{\text{fp}}C_{\text{fp}}}{2} \]

and a peak voltage given by

\[ V_{\text{peak}} = \frac{2C_{e}V_{\text{in}}}{eC_{f}} = 5.3 \times V_{\text{in}} \]

The total gain due to both the preamplifier and shaper is therefore 81.5mV/Silicon MIP. Perfect CR-RC shaping is not achieved since the output of the preamplifier has a finite rise time (in the order of 10ns). Therefore to achieve an overall peaking time of 50ns, the shaper must be adjusted to have a shaping time of around 40ns.

3.3 Leakage Current Compensation

Current from an MSGC comprises two components - the signal due to ionising particles passing through the chamber, and a DC leakage current. Leakage would
cause a voltage to form across the feedback transistor of the preamplifier. The preamplifier would be able to cope with very small leakage currents, however increasing radiation damage to the MSGC may cause the leakage current to increase to such a point that the preamplifier is pushed out of its optimum operating point. Such a situation is undesirable.

To overcome the problem of leakage current, the preamplifier has been modified to include a leakage compensation circuit. This consists of a voltage controlled current source which senses the voltage at the preamplifier output. If a leakage current causes the preamplifier output voltage to change then sufficient current is supplied to the MSGC strip such that none is drawn across the feedback transistor. The circuit has been implemented using an nfet as the current source (figure 2) whose gate is connected directly to the preamplifier output. A long channel nfet forms part of an RC time constant (adjustable using $V_{cmp}$) that ensures only the leakage current, and not the signal, is compensated.

The sourcing current is mirrored out from the front end to the leakage current monitoring circuit which will be described later.

3.4 Noise

By far the largest contribution to the front-end noise comes from the input transistor in the preamplifier. The input transistor is half the size of that in the APV6 since the lower capacitance of the MSGC strips means the transconductance and gate capacitance of the input transistor can be reduced.

4. ANALOGUE PIPELINE

The analogue pipeline buffers data coming from the detectors for sufficient time until the level1 trigger is processed. The trigger latency is $3.2\mu s$ equivalent to 128 pipeline columns.

4.1 Analogue Memory

The pipeline consists of an array of 128 X 160 switched capacitor elements. One side of each capacitor connects to VSS and the other to the write and read switches. The capacitor has a size of 250fF.

4.2 Control

The pipeline control is required to have the following functions:

- Sequence the writing of data into the analogue array.
- Mark useful (triggered) data.
- Remember which elements contain triggered data.
- Avoid writing over triggered data until they have been read out.
- Sequence the retrieval of data.

A write pointer continuously circulates the pipeline sampling the shaper output from each channel at intervals of 25ns. A trigger pointer follows behind the write pointer, separated by the trigger latency. When a trigger is received, depending on the mode of operation, either one, or three consecutive columns (figure 3) within the pipeline, are reserved for reading out. Once reserved these columns cannot be overwritten until the data have been read out. Therefore, on their next pass the write and trigger pointers will skip the reserved columns.

![Figure 3 Sampling of shaper output signal.](image)

Columns within the pipeline are grouped in pairs. This was done to reduce the amount of control logic required. The column pairing means that for each column triggered, both it and its pairmate are reserved and both are skipped over until the triggered column has been read out. If a number of consecutive column-pairs are reserved in the pipeline then the pointers must skip all of these in one 25ns interval. Each pair introduces a 2ns delay which means only 12 consecutive column pairs can exist before the delay is such that the pointers disappear or are delayed by one clock cycle. The separation between write and trigger pointers is monitored so that if it deviates from the programmed latency an error flag is set.

The addresses of triggered columns are stored in a FIFO which has a depth of 20. Therefore, depending on the mode of operation, either 20 or 6 triggers can be buffered in the pipeline before the FIFO overflows. If an overflow does occur an error flag is set.

5. ANALOGUE PROCESSING

The previous version of this chip, the APV6, was designed for read-out of silicon strip detectors. Signals from silicon strip detectors come as single impulses of current which can be integrated in a charge amplifier and shaped using a CR-RC shaper into a well defined voltage pulse. Deconvolution can then be performed on the sampled signal in order to recover the original impulse signal, thus confining it to one beam crossing interval. In the APV6, this deconvolution was performed using a switched capacitor filter with a three weight algorithm. The weights of the capacitors were determined from theory due to the well defined shape of a CR-RC signal.

Signals from MSGC detectors, however are not so well defined as their silicon counterparts. A simulation study...
was undertaken at Imperial College [2] in order to determine the optimum algorithm for processing MSGC signals to give sufficient timing resolution for CMS purposes. Good results were achieved using 50ns CR-RC shaping of the MSGC signal, a sampling interval of 25ns and a three weight signal processing algorithm. This has the advantage that these functions are already implemented on the APV6 chip and minimal effort would be required to convert it for MSGC use. Another advantage in keeping the algorithm logically compatible with the silicon version is that synchronisation is maintained between read-out of silicon strip detectors and MSGC detectors. This reduces the cost and complexity of the data acquisition electronics.

5.1 APSP Weights

The new APSP (Analogue Pulse Shape Processor) uses the three weight deconvolution optimised for MSGC signals (figure 4). The weights are:

weight 1 = -1.202 (applied to sample 1 in figure 3)
weight 2 = 0.172 (applied to sample 2 in figure 3)
weight 3 = 0.858 (applied to sample 3 figure 3)

These have been translated into capacitor weights of

\[ C1 = -2pF \]
\[ C2 = 0.286pF \]
\[ C3 = 1.428pF \]

Capacitor \( C1 \) has been divided into a capacitor of size 1.667pF and a capacitor of size 0.333pF. This is so that the output signals are of roughly equal magnitudes (per MIP) when operating in either Peak or Deconvolution modes. When in Deconvolution mode switch \( \text{dec mode} \) is closed to give a capacitance of 2pF, and in Peak mode the switch is left open, giving 1.667pF.

5.3 Operation of APSP

In Deconvolution mode, the three samples (figure 2) are read in sequence from the pipeline and written onto \( C1, C2 \) and \( C3 \) by closing and opening switches \( \text{ri1}, \text{ri2} \) and \( \text{ri3} \) in turn. They are then simultaneously read out through the amplifier by closing switches \( \text{ro} \) and \( \text{ro dec} \). To achieve the negative weight for \( C1 \), the capacitor is written onto one side and read out from the other.

In Peak mode, the single sample (from the peak of the signal) is read from the pipeline and written onto \( C1 \) by closing and opening switch \( \text{ri1} \). This is then read back out through the amplifier by closing only switch \( \text{ro} \).

In both cases the gain for the last read operation is reduced by closing switch \( \text{last cycle} \). The resulting voltage is then sampled on a 1.77pF buffer capacitor before it is read out through the analogue multiplexer. There are two buffer capacitors which alternate every read-out cycle. This is so that APSP can process and store a data set while the previous data are still being read out through the multiplexer.

![Figure 4 APSP circuit.](attachment:image)

A third mode of operation called Multi-mode allows triggering of consecutive pipeline columns and read-out of each sample separately. Modes are selected by programming a dedicated mode register

6. LEAKAGE CURRENT MONITORING

One indication that an MSGC strip is about to break down is a continuous increase in the leakage current of that strip. To avoid a discharge, the power to the faulty strip must be switched off, however, it is not practicable to address each channel individually.

The MSGCs have therefore been arranged into groups of 32 channels, where the power to any one group can be switched off. Within the chip the leakage current to each channel is mirrored out of the front-end by a factor of

![Figure 5 Current Monitoring Circuit](attachment:image)

two, and then summed for groups of 32 channels (i.e. for channels 0-31, 32-63, 64-95, 96-127). These four
summed currents then form inputs to current comparators, where they are compared with a reference current (figure 5) which has been programmed using an on-chip register. A latch is set for each of the currents exceeding the reference value. The latched outputs then drive four open-drain output pads which are used to switch off the power to the group of 32 MSGC channels containing the faulty strip. The reference current is defined using one channel of the bias generator programmable over the I\textsuperscript{C} interface with 8 bit resolution. The bias generator channel provides a maximum of 127.5\mu A output current which is mirrored down by a factor of 0.4 to give 51\mu A. The summed currents are multiplied by a factor of 10 giving a total multiplication factor - from the initial leakage current value - of 20. The leakage monitor range is therefore from 0-2550 nA in steps of 10 nA. A second channel of the bias generator is used to define a bias current for the monitor circuit electronics and a third channel is used to store information concerning the states of the 4 comparators and latches, which are then accessible over the I\textsuperscript{C} interface. Once any of the latches has been set, it can only be reset by resetting the whole chip, or by using an I\textsuperscript{C} command to the bias generator channel.

7. PRELIMINARY TEST RESULTS

Preliminary tests have been carried out at Imperial College. However, the leakage current compensation and monitoring circuits have not yet been fully tested so no results are available for these at present.

![Figure 6 Pulse Shape Adjustment](image)

The pulse shape can be observed at the output of the chip following analogue processing (figure 6). The case when VSHA=110 provides the optimum performance when the signal is closest to the ideal CR-RC shape. For this case the signal is 70\mu A for a 1MIP input. Adjusting VSHA above and below this value lengths or shortens the peaking time.

Figure 7 shows the pulse shapes obtained in both peak mode and deconvolution mode. This shows that the deconvolution algorithm is functioning correctly and that the gain in either modes is almost the same.

8. CONCLUSIONS

A CMOS mixed signal analogue pipeline has been designed and manufactured. Based on the APV6 it has been optimised for read-out of CMS MSGC detectors, and preliminary test results show the circuit to be working. The next version of the chip will be designed on a 0.25\mu m process which can be made radiation hard by careful circuit design techniques.

9. ACKNOWLEDGEMENTS

We would like to acknowledge technical support at the Rutherford Appleton Laboratory and Imperial College. Particular thanks are due to Jeff Bizzell at RAL and Sarah Greenwood and John Reilly at IC. We would also like to acknowledge the financial support provided by PPARC.

9. REFERENCES


Readout of Micro Strip Gas Chambers for the CMS Central Tracker with the APV6 Front-end Chip

F.G. Sciacca  
Blackett Laboratory, Imperial College, Prince Consort Road, London, UK, SW7 2 BZ  
and CERN, CH-1211 Geneva 23, Switzerland  
G. Hall, M. Raymond  
Blackett Laboratory, Imperial College, Prince Consort Road, London, UK, SW7 2 BZ  
M. French, L. Jones  
Rutherford Appleton Laboratory, Chilton, Didcot, UK, OX11 0QX

Abstract

It is foreseen that all the microstrips of the Silicon and MSGC tracker in CMS will be read out by the same front-end electronics. The APV6, a 128 channel pipeline chip developed and optimized for silicon detectors, has been used for the first time to instrument one prototype MSGC built and operated according to CMS specifications. The low noise amplifier is identical to the one included in the version of the chip optimized for MSGC which has recently been prototyped. In their low luminosity operation mode (peak mode) the two chips behave in identical way. Some results are presented of the performance of the system stimulated by a Sr source and operated in peak mode.

1. INTRODUCTION

The CMS central tracker contains 5.6x10^6 channels implemented as silicon microstrips and 6.4x10^6 channels in gas microstrip (MSGC) technology. Analogue readout without data sparsification at the front-end has been chosen in order to achieve robustness of the system against common mode noise effects, to simplify debugging and ultimately to improve the overall performance for physics. Analogue data will be transmitted optically to the external digitizing stages. Detector and electronics control and monitoring will be implemented digitally and will make use of similar optical technologies.

Because of similarities in detector capacitance and signal sizes it is foreseen to employ the same front-end electronics to readout both kind of detectors. Some inevitable differences, however, dictate modifications.

The APV series is the result of the efforts of the RD20 collaboration which have culminated in the APV6 [1], the final prototype of the readout chip optimised for silicon microstrips in CMS. It is a radiation hard CMOS circuit which consists of 128 amplifier, pipeline and signal processing stage inputs, includes an analogue signal processing stage for MSGC signals [3, 4] and the on-chip capability to generate an alarm in case of an imminent discharge in the detector. Test structures of a circuit meant to quickly restore the baseline level following the very large pulses generated by heavily ionizing particles have been prototyped as well.

Two modes of operation are possible for both chips: in deconvolution mode the analogue signal processing stages will be used to achieve optimal bunch crossing identification during high luminosity running; in peak mode no signal processing takes place and the behaviour of the two chips is identical. This paper presents some results of the performance of a system which makes use for the first time of one APV6 chip operated in peak mode to readout a prototype MSGC built and operated according to CMS specifications.

2. CMS TRACKER READOUT SCHEME

A block diagram of the CMS tracker readout scheme is shown in figure 1. On each of the Front End Modules the data from a pair of APVs are multiplexed onto one line by one APV MUX chip. Multiplexing is done at 40 MHz, therefore the APV output multiplexing stage must run at 20 MHz. The analogue signals are subsequently transmitted optically to the barracks for digitization and sparsification on a Front End Driver (FED) module. The Front End Module receives from a Control Module the slow control signals on a 2-wire bi-directional bus conforming to the commercial I²C standard. The 40 MHz clock and T1 trigger signals are transmitted differentially and are recovered on the front end Module by an additional chip.

The tracker target performance can be summarised as follows:

- Low noise (CMS goal: <2000 e⁻ during the full operational lifetime).
• Low power consumption at the front end (CMS goal: ~2mW/channel)
• Adequate Bunch Crossing (BC) Identification (CMS goal: 1 BC (silicon) - 2 BC (MSGC))
• Synchronization desirable through the whole tracker

However it has been gradually understood that the BC identification issue is much more challenging than originally thought. This is discussed later.

A nested multiplexer architecture [5] allows some power saving and causes the analogue data to be output in a non-consecutive channel order.

Slow control of the APV is implemented using the 2-wire I²C serial bus. The master in the system is located in the Control Module (figure 1) and up to 15 APVs individually addressable can be connected to one bus and will always act as slaves. It is thus possible to access individually all the internal registers of the APV for appropriate setup, control and monitoring. Table 1 shows a list of the registers. All can be written to and read from except for the error and the I-threshold registers which can only be read from.

### Table 1: APV6 internal registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>latency</td>
<td>distance between write and trigger pointers to pipeline. Value up to 160</td>
</tr>
<tr>
<td>analogue bias</td>
<td>4 currents and 4 voltages. Programmed values converted by on-chip DACs</td>
</tr>
<tr>
<td>mode</td>
<td>peak/deconvolution multi-sample (APVM only) bias ON/OFF power up/down) internal calibrate ON/OFF</td>
</tr>
<tr>
<td>cal pulse amplitude</td>
<td>programmable in ~625 electron steps up to ± 6 MIPs</td>
</tr>
<tr>
<td>cal skew</td>
<td>8 steps of 3.125 ns</td>
</tr>
<tr>
<td>cal mask</td>
<td>which of 8 cal lines to drive</td>
</tr>
<tr>
<td>error (read only)</td>
<td>latency error bit set if value read on chip • programmed value. FIFO overflow bit set if too many triggers in too short a time</td>
</tr>
<tr>
<td>I-threshold</td>
<td>threshold for current sensing (APVM only)</td>
</tr>
</tbody>
</table>

The APV6 and APVM have identical dimensions and pad layout thus allowing the development of common front-end sub modules both at prototyping and construction stages.
3.2 APV6 and APVM differences

The deconvolution operation is described in detail in [6]. In the case of silicon detectors, whose signals resemble delta impulses very well, the pulse produced by the preamp/shaper stage approximates very well an ideal CR-RC shape which is uniquely defined and can be described analytically. Inverting the transfer function of the shaper it is possible to calculate a set of three weights which, applied to three consecutive samples, ideally confine the signal to one bunch crossing only. This set of weights has been implemented in the APV6.

In the case of MSGCs, signals from the detector have a complex time structure which fluctuates greatly with an average charge collection time of 50ns. Consequently the pulse resulting from the preamp/shaper suffers from fluctuations in peaking time and amplitude. It is impossible in such a case to use the deconvolution method to obtain single bunch crossing identification. Even the CMS goal of two bunch crossings is hard to achieve and it has been shown [4] that an inevitable compromise between time tagging capabilities and signal size/noise performance must be reached. A set of three weights optimized according to these considerations for use with MSGC detectors has been defined [4] for implementation in the APVM. They are applied, as in the APV6, to three consecutive samples, so synchronization is trivially achieved across the whole microstrip tracker.

Another feature of the APVM dictated by necessities of operation in conjunction with a gas detector is a current sensing circuit at the input. Leakage current from groups of 32 adjacent channels is summed and compared against a threshold programmed via slow control. In case the threshold is exceeded, which can be a symptom of an imminent discharge in the gas detector, an alarm bit is set which can be transmitted to the control system for triggering a precautionary procedure to avoid the discharge.

4. LAB SYSTEM CALIBRATION

A Sr90 collimated source is placed in front of the detector, a 100mm x 100mm x 3mm chamber filled with Ne(33)/DME(66), and a scintillator behind for triggering purposes. Simple NIM logic vetoes triggers in a 7μs window following a T1, the time needed to read out a complete data frame. It also provides synchronization to the DAQ. A prototype of the CMS Front End Driver (figure 1) module is used for digitization, and the slow control is implemented via a simple VME I2C interface card. The system can be remotely controlled via VME and the control and DAQ software are developed in LabView running on a PowerPC.

The system calibration procedure included the tuning via I2C of the pulse response of the preamp/shaper to approximate the ideal CR-RC shape, characterisation of the response of the 128 amplifiers and pedestal/noise measurements to identify channels behaving incorrectly. These procedures have been carried out before and after the bonding of the detector. Figure 3 shows the pulse shape of a typical channel bonded to the detector after tuning. The on-chip internal calibration system has been used for this purpose. Eight calibrate lines feed groups of 16 channels individually selectable via I2C (cal mask, table 1). Following a Calibration Request pulse (two consecutive T1 pulses), a voltage step is applied to a capacitor and the charge injected into the preamp. There is a capacitor for each channel whose value is known to within 20%. A T1 pulse is sent at the appropriate time to perform readout. Fixing the latency and T1 and moving the calibrate request in steps of 25ns, a coarse mapping of the pulse shape is possible at 25ns intervals. The cal skew register (table 1) can be used to delay the calibration pulse in fine steps within the 25ns intervals, thus achieving finer time resolution (3.125ns). The amplitude of the pulse can be programmed via I2C (cal pulse amplitude in table 1).

Using this procedure the impulse responses of the 128 channels have been measured and are shown in figure 4.

Figure 3. Impulse response of a typical channel tuned to approximate CR-RC shape.

Figure 4. Impulse response of the 128 channels bonded to the detector.
Figure 6 illustrates their distribution. A conversion after baseline subtraction, while figure 5 shows the values of the peak of the pulse for the 128 channels in the order in which they come out from the chip and figure 6 illustrates their distribution. A conversion constant of 1 ADC channel $\times$ 200e$^-$ can be calculated for the system. This value is consistent with other cross-check measurements performed. Typical channels exhibit a channel-to-channel gain spread consistent with the differences between the internal capacitor values. Incorrect behaviour of channels showing lower gain has appeared only after bonding to the detector.

Figure 7 shows a typical noise measurement before and after the bonding of the detector. Values are common mode subtracted and reordered to the correct channel sequence. Noise figures are consistent with expectations from previous measurements [1] for a strip capacitance of 5pF (0.4pF/cm, 12.5cm) but in this case anomalies in the noise performance of some channels have also appeared after detector bonding. This clearly indicates that anomalous behaviour is related either to the detector or the bonding. The gain values normalised to the most probable value of 163ADC counts and reordered are superimposed in figure 7. A one-to-one correspondence between channels exhibiting anomalous values of noise and gain is clearly visible. In particular, the channels whose noise is lower than expected show minimal response to the calibration pulse. Channels with conspicuously higher noise show lower gain. A number of channels have gain slightly lower than the typical values (>0.8) while their noise values are as expected.

Looking at figure 5 it can be noted that these channels precede or follow in the readout sequence other channels with much lower response, which thus appear to be responsible for this effect.

Going back to figure 7 it can be observed that channels showing anomalous behaviour are never physically isolated, but always come in groups of at least two adjacent. One possible explanation of this effect could be found in the bonding. The procedure is in fact quite laborious, involving two bonds per channel and rather long wires. Since bonding pads are laid out in a double row on the chip and on the intermediate pitch adapter, the bonding wires of adjacent channels stay on two different levels; they could touch each other shorting the inputs of the corresponding amplifiers, which could result in the anomalies observed. A couple of channels began showing higher noise and lower response only after several weeks of testing. This observation could support the hypothesis, in that mechanical stress could have lead to a contact between the two bond wires. A closer inspection under the microscope supports this hypothesis as well, although does not provide definitive confirmation.

5. LAB SYSTEM PERFORMANCE

The amplifier response to detector currents generated by B's traversing the detector has been investigated. Given the nature of MSGC signals it is impossible to map the amplifier pulse shape for a single event using the APV6. A facility has been implemented as a testing tool on the APVM, in which, following a single T1, it is possible to send out 3 samples. With a sequence of 6 T1 separated by 75ns intervals it is therefore possible to readout up to 18 consecutive samples stored in the pipeline. It is however possible with the APV6 to perform a pipeline scan fixing the T1 time and changing the latency value in steps of 25ns. Acquiring a statistically significant number of events per step, it
is possible to reconstruct an average pulse shape. Figure 8 shows the result of such measurement.

![Figure 8. Average amplifier response to MSGC currents](image)

The chamber is operated at the nominal CMS working point (Vcath -520 V, Vdrift -3.5kV) and 10000 events acquired at each latency value; the averages of the charge spectra obtained after off-line cuts are then plotted (solid line). The dotted line corresponds to the average response of an ideal CR-RC amplifier with 50ns time constant to 10000 detector current generated with a Monte Carlo program [6]. The agreement with the measurement is excellent, especially on the rising slope, where are located the samples used in the APSP filter optimized for MSGC. Figure 9 shows the pulse height spectrum measured at the latency which ensures maximum efficiency. The noise of a typical channel is superimposed. S/N is in excess of 25, again in good agreement with simulation predictions.

![Figure 9. Pulse height spectrum with the trigger timed at the peak of the amplifier response.](image)

Figure 10 shows the result of a cathode voltage scan. Even when a large voltage is applied to the chamber, no appreciable distortion from the logarithmic behaviour is visible. This shows that the dynamic range of the amplifier is suitable for application in CMS MSCGs.

![Figure 10. Average response of preamplifier at different cathode voltages of MSGC.](image)

6. CONCLUSIONS

An APV chip operated in its low luminosity peak mode has been used for the first time to instrument a portion of a gas detector prototype for the CMS detector at the LHC. Even if optimized for readout of silicon detectors, the APV6 has been shown to be suitable to reading out gas detectors.

All the on-chip system features have been successfully used to tune-up and calibrate the system. The average amplifier response to detector signals has been reconstructed showing excellent agreement with predictions from simulations. The noise performance is as expected from previous measurements.

The APV6 design has been modified for optimal performance in conjunction with MSGC, resulting in the APVM chip, recently prototyped. It features an analogue pulse filter optimized for MSGC signals and a current sensing circuit at the input able to issue an alarm in case of imminent discharge in the detector. An additional operation mode has been implemented which allows multi-sample output for testing purposes. However, when operated in peak mode the chip should behave as the APV6. In this sense the measurements described in this paper are an indication of the suitability of the APVM for reading out MSGCs.

APVM prototypes have recently been shipped and are currently under test. Figure 11 shows the impulse response of the newly implemented APSP filter as measured in early tests at IC. Agreement with expectation from simulation is excellent. Noise figures are in agreement with expected values as well. When the testing procedures will be complete, the APVM will replace the APV6 in the lab setup described in this paper. Once correct functioning is demonstrated, studies will concentrate on the performance of the APSP filter.
Figure 11. Impulse response of the APSP filter in the APVM chip

ACKNOWLEDGMENTS

Thanks are due to PPARC for financial support of the APV development. We would like to thank J. Bizzel, S. Greenwood, J. Reilly, J. Martin and C. Bastie for important contributions to assembly.

REFERENCES


[2] A 128 Channel Analogue Pipeline Chip for MSGC Read-out at LHC. L. Jones et al., these proceedings.


[6] Electric Field, Avalanche Growth and Signal Development in MSGCs, R. Bellazzini, M.A. Spezziga, INFNPI/AE-94-02
The microstrip tracker for the CMS experiment at the LHC will be read out using radiation hard APV chips. During the production phase large numbers of die must be screened while still on the wafer using an automatic test facility. A high level of confidence is required in identifying good die on the wafer so that yields for subsequent production stages can be maximized. This has to be balanced with time constraints, which limit the amount of testing which can be performed on a single die. The design, performance and results for a prototype wafer probe system are presented.

1. INTRODUCTION

1.1 Front-end System

The CMS microstrip tracker readout system has been described in detail elsewhere [1]. The principal front end components are the APV chips, of which ~100,000 will be required, whose purpose is to sample, amplify and store, for up to 3.2 µs, the signals from their associated detectors. Upon external triggering, the APV will send data via an analogue optical link to a receiver module.

The system design goals - analogue readout with minimal power, material, cost and sufficiently low noise - are strongly constrained by the requirement to use existing technologies which can be demonstrated to allow production of the system in the relatively short time available until CMS operation is scheduled to start. In addition, the requirement for radiation hardness led to the adoption of the Harris AVLSI-RA bulk CMOS process, which uses 4-inch diameter wafers, for APV development.

An approximate time scale for the production and large scale testing of the APV is shown in fig. 1.1. The APV6 is the final prototype, in which only a small number of design faults remain. These have been identified and will be removed in subsequent runs.

1.2 Time considerations

If all front end chips are produced on 4-inch diameter wafers and assuming a reasonable fabrication yield, the tracker construction will require the testing of up to ~5000 wafers on a three-year time-scale.

Assuming standard working hours of 40 hours/week and 44 weeks/year for three years, one arrives at the available testing time of 5280 hours. To test 5000 wafers in this time would require an average testing time per wafer of about 1 hour, including wafer loading and unloading.

<table>
<thead>
<tr>
<th></th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final prototype fabrication</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Testing of final prototype</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full scale production</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Production testing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assembly of tracker</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig 1.1: Approximate time scale for production and testing of the APV chips

Testing of one wafer currently requires approximately 2 hours. If we are not able to significantly reduce this time, further testing centres will be necessary to meet our procurement schedule. Two to three testing centres would allow us to meet our testing demands comfortably.

1.3 The APV6

The APV6[2] front-end chips consist of 128 channels, each of which contains a pulse amplifier and shaper that feeds a 160 deep analogue pipeline capable of storing input pulses for up to 3.2 µs. On an external T1 trigger the data is retrieved from the pipeline and then output, via a 128 : 1 multiplexer, in one of two modes: peak or deconvolution. Peak mode transmits the pipeline data stored at the peak amplitude of the pulse, while in deconvolution mode, the full output pulse duration is restricted to only two beam-crossing intervals, thus enabling pulses in consecutive beam crossings to be resolved.
The output stream consists of a digital header, containing information on the status of the chip and the pipeline location from which the data was retrieved. This is followed by a set of analogue levels retrieved from all 128 channels. Control of the various chip operation modes and bias settings is achieved via a standard \( I^2C \) serial bus link[3]. Each APV6 has an address that can be set to enable the \( I^2C \) bus to communicate with individual chips. Another important feature is the internal calibrate system. This generates a signal at the input amplifier whose response can be stored in the pipeline. All 128 channels can be driven to enable testing of amplifier gain and pulse shaping uniformity. This feature is used extensively in testing.

2. TESTING THE APV6

2.1 Criteria for automated wafer screening

The APV6 chips are manufactured on wafers (fig. 2.1), which contain 61 individual chips. Before die can be sawn from the wafer and distributed for assembly on front-end hybrids, the degree of functionality must be established. They are classified in three categories: 1) Fully functional, 2) Partly functional or 3) Useless. The inclusion of category 2 is intended to maximize the yield, since some, but not all, of these chips will be failed after further inspection of the test data.

![Fig. 2.1: Map of a wafer containing 61 APV6 chips.](image-url)

The yield must be maximized to minimize fabrication costs. Therefore, it is important that wafer screening be accurate to ensure that no possibly useful chips are failed unnecessarily. Conversely, it is important that no bad chips are passed and then found to be faulty after distribution, where packaging costs and loss of time would be incurred.

It is essential that the information gathered during testing is stored for future reference. Certain chips may contain acceptable errors, such as bad channels or pipeline locations. To make the best possible use of these chips it will be necessary to provide detailed information of any chip faults. Therefore, along with a fully automatic testing procedure, there must be a complete data logging system.

![Fig. 2.2. Schematic of the probe-station test setup](image-url)

2.2 Setup and Apparatus

Fig. 2.2 gives a schematic representation of the test setup. All control and testing is performed by a Macintosh using LabView software. The clock and trigger signals to the APV6 are provided by the SEQSI (sequencer) module. They are buffered by optical relays on the card interface board. The analogue output from the APV6 is taken directly to the ADC, and may also go to a scope. An OUTE signal is taken to a discriminator to provide a fast pulse (~5ns) representing the leading edge of the data stream. This signal is used to start the logic that triggers the ADC. Data are read from the APV6 into the computer at a typical trigger rate of 20kHz.

The \( I^2C \) signals and addressing are provided within the setup by the SEQSI. The SEQSI can presently run the \( I^2C \) interface at a bit rate of a few kHz, although the APV6 can accept data at about 400 kHz. Significant improvements in speed will be achieved using a faster \( I^2C \) driver. All \( I^2C \) transactions are software generated.

2.3 Test Procedure

The total number of individual tests and checks that are presently included in the procedure is 18. Before any of them are carried out a looping trigger sequence is sent to the chip which causes it to reset and then read out the data from one pipeline location. This provides a continuous
output stream of pedestal values from all 128 channels which are later subtracted from the channel values during the retrieval of pulse data.

There are two types of tests: terminal and non-terminal. Terminal tests must be passed for the chip to be marked as good; non-terminal test can be failed and will be noted for the benefit of the chip recipient.

Each of the 61 sites on a wafer is numbered in a particular order (from bottom left to top right). These die numbers are then used to identify the output data. Table 2.1 gives a brief description of each of the 18 tests.

To accompany the error list and site number for each chip, a data sheet is also produced. This sheet includes seven plots, which are valuable information for anyone who will be using the chip. The raw data are also saved to file in binary form. If a situation arises where the data sheet does not clearly show the required information, then the raw data can be retrieved.

<table>
<thead>
<tr>
<th>Test</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. No probe contact</td>
<td>A sensor checks for good contact between the probe needles and the chip.</td>
</tr>
<tr>
<td>2. I²C write</td>
<td>The I²C bus is tested to see if the chip is receiving and acknowledging the intended data.</td>
</tr>
<tr>
<td>3. I²C read</td>
<td>The I²C bus is tested to see if the chip is sending the expected data.</td>
</tr>
<tr>
<td>4. No OUTE</td>
<td>The Out Enable (OUTE) is a pulse synchronized with the output analogue data. Its presence is tested for.</td>
</tr>
<tr>
<td>5. No AOUT</td>
<td>No analogue output stream, identified if data for every digitized channel are zero.</td>
</tr>
<tr>
<td>6. Stuck bits in I²C registers</td>
<td>Some bits in the I²C registers may be stuck either high or low, which may not be picked up in an I²C read test.</td>
</tr>
<tr>
<td>7. I²C read-write compare</td>
<td>Data written to the chip are compared with data received from the chip.</td>
</tr>
<tr>
<td>8. Bad currents</td>
<td>The APV should draw specified currents during normal operation, which should lie within a defined range.</td>
</tr>
<tr>
<td>9. Failed some addresses</td>
<td>All possible chip addresses are tested. If one or more fail then error 9 is produced</td>
</tr>
<tr>
<td>10. Failed all addresses</td>
<td>As test 9, but if all addresses fail then error 10 is produced.</td>
</tr>
<tr>
<td>11. Can’t set VADJ</td>
<td>The analogue data baseline is controlled by the chip register VADJ. If the analogue level cannot be set then error 11 is produced.</td>
</tr>
<tr>
<td>12. Some bad pedestals</td>
<td>Set if any channels have a pedestal value outside a predetermined range.</td>
</tr>
<tr>
<td>13. Excess bad pedestals</td>
<td>Set if more than an acceptable number of channels are outside the required range.</td>
</tr>
<tr>
<td>14. Noisy analogue output</td>
<td>The RMS noise on the analogue output is compared with an acceptable value</td>
</tr>
<tr>
<td>15. Some bad cells</td>
<td>All cells in the 128 x 160 analogue pipeline are tested for abnormal levels.</td>
</tr>
<tr>
<td>16. Channels with low gain</td>
<td>Pulse heights in peak and deconvolution mode are recorded for all channels using a calibrate signal. An error is set if the result is outside an acceptable range.</td>
</tr>
<tr>
<td>17. Some bad pipeline addresses</td>
<td>Each pipeline address is read from the digital header and checked.</td>
</tr>
<tr>
<td>18. Failed all pipeline addresses</td>
<td>Set if test 17 reveals more than an acceptable number of discrepancies.</td>
</tr>
</tbody>
</table>
Fig. 3.1. Data sheet from APV6 chip 40, wafer 14.
3. EXAMPLE WAFER MAP AND DATA SHEET

For every tested wafer a map displaying the recommended chip failures and passes is produced. Fig. 2.1 shows the result of a full wafer scan.

Each of the sites contains a summary of the information gleaned during testing. The failed sites contain the number of the terminal test. The good sites contain a list of the non-terminal test that they failed. The availability of this information is helpful in speeding up the process of selecting chips for distribution and also for passing on the information to the recipient of the chip.

An example data sheet for one chip from an APV6 wafer is shown in fig. 3.1. The data sheet contains four plots: “Pedestals” shows the average channel pedestals. “Channel Cross-section” contains 160 plots showing the channel output values after pedestal subtraction, one for each pipeline location. “Pipeline Cross-section” contains 128 plots of the pipeline pedestals, one for each channel. The combination of these two provides a simple way of looking at the two-dimensional array which contained this data. In the ideal case, with no amplifier noise, both of these plots would exhibit only zero values since these data are taken after pedestal subtraction. “Pulse Heights Peak Mode” and “Pulse Heights Deconvolution Mode” contain one plot showing the calibration pulse heights in the two modes of operation. “Pulse Shapes Peak Mode” and “Pulse Shapes Deconvolution Mode” show the shape of the maximum, minimum and average pulses taken from every channel in both modes. The time scale is in ns and from this plot one can inspect the peaking time and pulse width.

The data sheet is representative of a fully operational chip with fairly normal channel pedestals. The spread of the pipeline pedestals can be seen clearly on this plot, i.e. each channel bin contains all 160 pipeline locations. The full spread can be seen to be less than 10 ADC counts. Comparing this to the size of an average pulse height, roughly 110 ADC counts, one can see that there is a maximum deviation of ~5%. There are three channels of interest: 111, 112 and 113. These channels appear to have a less uniform pipeline. The effect that this would have on data must be investigated and some threshold must be set which puts an upper limit on the allowable spread throughout the pipeline. The plot of the pipeline shows that there are no outstanding bad locations but one is able to see that the non-uniformity of channels 111, 112 and 113 is spread throughout the pipeline. The spread of the pulse heights can be seen to be acceptable, at roughly 10%. The pulse shapes are also clearly within acceptable limits.

6. CONCLUSIONS

We have developed a wafer screening setup capable of automatically testing all chips on a wafer and making a comprehensive study of the digital functionality and characterization of the analogue components. All data retrieved during the test procedures are stored and a map of the wafer, indicating the good and bad sites and the degree of their functionality, is produced.

As yet no real work has been done on developing a comprehensive data storage and recovery system, which will be required later. All data are presently saved in binary format and hard copies of all the data sheets and wafer maps are printed out and filed. The development of a database for the test data is an important task and will commence soon. The exact format of this database and the media which it could employ are under discussion.

It is important that careful consideration of the test threshold settings is made in order to ensure the optimization of chip performance and minimization of production costs. A full investigation into the exact effect of threshold variation on yield for all the tests should be undertaken. which will provide solid information to define failure criteria and ensure confidence in the testing procedure.

Investigation into the cost, availability and feasibility of industrial involvement to sub-contracting the testing work is being seriously considered.

7. ACKNOWLEDGEMENTS

We would like to thank Martin Millmore for his considerable contribution to the initial probing setup, John Reilly for technical help and PPARC and RAL for financial support.

8. REFERENCES


DEVELOPMENT OF A READ-OUT CHIP SUITABLE FOR THE LHCb EXPERIMENT

Martin Feuerstack-Raible, Ulrich Straumann
University of Heidelberg

Edgar Sexauer, Michael Schmelling, Ulrich Trunk
Max-Planck-Institute for Nuclear Physics, Heidelberg

Ruud Kluit
NIKHEF, Amsterdam

Jo van den Brand
Free University of Amsterdam

Abstract

For the LHCb experiment a dedicated analogue pipeline chip will be developed. To fulfill the time schedule of the LHCb experiment for detector prototyping testing but also to have a long-term solution, development will be made in two branches.

The already existing SCT128A design from CERN, which is implemented in the radiation hard DMILL process, will be adapted to the LHCb requirements.

In parallel, a new design will be made in a deep submicron process. These processes recently showed very good results concerning radiation hardness and their availability will grow in future.

Existing analog circuits from e. g. 0.8µm CMOS processes can not be ported easily to deep submicron processes. Also, to fully exploit the radiation hardness of this technology, special layout considerations must be taken into account. Thus existing digital standard cell libraries can no be used but must be constructed anew to be radiation hard. Such libraries would be interesting beyond the scope of the LHCb project.

THE ANALOGUE PIPELINE CHIP IN THE LHCb DATA ACQUISITION SYSTEM

As described in [1] the LHCb data acquisition system has four trigger levels. Here we discuss only the topics relevant to this subject. Electronics for level zero resides on the detectors and consist of pipeline buffers with a storage capacity of approx. 3µs. The buffers take data with the LHC bunch crossing clock of 40MHz and are read out concurrently with the level zero trigger rate of 1MHz, which makes it impossible to use existing LHC pipeline chips without changes. After a level zero trigger, data must be driven electrically to the next pipeline buffers, which reside in a distance of approx. 10m outside the detector.

Subdetector frontends

The Silicon Vertex Detector (SVD) [2], the Inner Tracker (IT), which most likely will be realized with Microstrip gaseous Counters (MSGCs) [2], and the RICH, in case it is implemented with Pad Hybrid Photo Detectors (Pad-HPDs) [2] or multianode Photo Multipliers, could make use of the same multi channel analogue pipeline chip. Table 1 summarizes the
requirements of the different detectors. For the RICH, only the Pad-HPD case is shown since the signal of the multianode PMT can easily be downscaled to a level comparable to the other cases.

Because of the large number of channels and because of space constraints in the SVD and the RICH, a 128 channel chip will be used.

The signal of the Inner Tracker’s MSGC is a statistical distribution of charge pulses over a drift time which is longer than the LHC bunch crossing time. A detailed model of that process with parameters of a chamber suitable for LHCb has yet to be developed. Thus the preamplifier/shaper for the MSGC might differ from the one for the silicon microstrip detector and the Pad-HPD, which have similar characteristics.

**Pipeline and read-out architecture**

The maximum required latency is, as with any similar chips developed for LHC experiments, up to 3.2µs, including all signal delays and all trigger processor computation times. Thus a pipeline of 128 stages plus space for multi-event buffers is needed.

Because of the level zero trigger rate of 1MHz the read-out speed is critical for the event loss rate. Hence a serial read-out of 32 channels at 40MHz is foreseen. A 128 channel chip will then have four 32 channel ports running in parallel. To detect synchronisation errors, data will be prepended by a header of two clock cycle length. The four channels can then code the 8bit pipeline column number which was read out. In case of an internal error, numbers larger than the maximum column number can code information about the error condition.

Two bits of the pipeline column number

\[ 34 \times 25\text{ns} = 850\text{ns} < 1/(1\text{MHz}) \]

![Fig. 3: The analogue output data format](image)

**Control interface**

The chip will be programmable and monitorable via the standard I2C[3] interface. All clock and trigger signals are received via Low Voltage Differential Signal (LVDS) receivers.

**IMPLEMENTATION**

Due to the radiative environment of the Vertex Detector and the Inner Tracker „standard“ CMOS technology, like 0.8µm CMOS processes, can not be used, though they were still interesting for the RICH detector. Thus it only remain two technology choices: the radiation hard DMILL technology from Temic or the newer deep submicron technologies from various suppliers.

Apart from the questionable future availability of the single vendor DMILL process, the cost disadvantage is especially evident for the RICH application, where essentially no radiation hard technology is needed.

Modern deep submicron processes have recently been shown to be radiation hard[4] (at least with respect to total dose effects) and their availability will grow in future. The main disadvantage is that few existing analogue CMOS designs can be ported to these processes, because the maximum supply voltage is typically limited to 2.5V and the process parameter spread is large. When radiation hardness is required,

<table>
<thead>
<tr>
<th></th>
<th>SVD</th>
<th>RICH</th>
<th>IT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>233.000</td>
<td>500.000</td>
<td>70.000</td>
</tr>
<tr>
<td>Occupancy (%)</td>
<td>0.5</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>Min. signal (electrons)</td>
<td>12,000</td>
<td>5,000</td>
<td>~30,000</td>
</tr>
<tr>
<td>Detector capacity</td>
<td>4pF</td>
<td>4pF</td>
<td>12pF</td>
</tr>
<tr>
<td>Required S/N</td>
<td>&gt; 8</td>
<td>&gt; 8</td>
<td>&gt; 15</td>
</tr>
<tr>
<td>Radiation</td>
<td>1Mrad/y</td>
<td>&lt;100kRad/y</td>
<td>&lt;1Mrad/y</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;4mW/channel</td>
<td>&lt;2mW/channel</td>
<td>&lt;4mW/channel</td>
</tr>
</tbody>
</table>

Table 1: Detector requirements on the read-out chip
special layout techniques, like enclosed MOSFETs have to be used. Thus all analogue circuits have to be designed anew and even existing digital standard cell libraries can not be used for radiation hard designs.

Consequently, any read-out chip for LHCb in these technologies will be a complete new design, which is no short-term solution. To fulfill the time schedule of LHCb detector prototyping under these circumstances a two-way strategy must be followed.

**Implementation based on the SCT128A**

For having a short-term solution for the radiative environment of the SVD, the SCT128A[5], which is a DMILL design from CERN, will be adapted to the LHCb specification. Since the SCT128A already fulfills the requirements on the frontend, solely the read-out multiplexer has to be split into four parts which run in parallel and which also output the header containing the column number, which was read out. The output driver is already able to run at 40Mhz and the chip is also programmable via an I2C interface.

**Implementation in deep submicron technology**

The development of a new preamplifier/shaper in deep submicron technology which is suitable for the LHCb SVD is the first item to be addressed. First results on that are expected in the mid of next year.

In parallel, a digital standard cell library will be developed which obeys radiation hard design rules. This library will then be the basis for implementing all digital parts of the LHCb read-out chip, like the pipeline control logic or the I2C interface, for which well tested synthesizable Verilog code already exists from the Helix128[6][7] and the follow-on project CIPix.

**REFERENCES**


[3] Philips semiconductors: „The I2C bus and how to use it (including specifications)


ELECTRONICS FOR CALORIMETERS
THE FRONT-END BOARD FOR THE ATLAS LIQUID ARGON CALORIMETER.

Etienne Augé, Dominique Breton* (corresponding author), Philippe Cros, Gisèle Martin-Chassard, Vanessa Tocut, Jean-Jacques Veillet.

*LAL ORSAY, 91405 Orsay cedex, France

Jaroslav Ban, Nicolo Cartiglia, Herbert Cunitz, Al Gara, John Parsons, William Sippach.

Nevis labs, Columbia University, Irvington, NY 10533, USA

Douglas Gingrich, J Hewlett, Lars Holm, S Mullin, James Pinfold.

CSR, University of Alberta, Edmonton, Alberta T6G 2N4, Canada

Eric Delagnes.

CEA-DSM-DAPNIA Saclay, 91191 Gif sur Yvette, France

ABSTRACT

The very high collision rate and the scarcity of interesting events foreseen at the future Large Hadron Collider at CERN require the development of new types of readout electronics structures. Among those, the dual port analog memories provide the possibility to decrease the high rates of incoming data. These memories allow indeed to perform the analog to digital conversion only after the level 1 trigger, thus dividing by at least a factor 100 the amount of samples to digitise, and to use much slower ADCs. Nevertheless, this induces that they are able to sample the incoming analog signal at high frequency (40 MHz for the LHC) and to store it waiting for the level 1 trigger latency. Moreover, the very high dynamic range of the detector signal requires the analog memory to cover at least 12 bits of resolution, even with a multigain system.

The Laboratoire de l’Accélérateur Linéaire (LAL) from Orsay, the Nevis Laboratories from Irvington, the University of Alberta from Edmonton and the CEA-DAPNIA from Saclay have developed a complete readout solution to fit the requirements of the ATLAS liquid argon calorimeter system. The upstream part of the chain consists in warm preamps followed by tri-gain bipolar shapers, dual port analog memories (also named “analog pipelines” or “Switch Capacitor Arrays”), and 12bit-5MHz ADCs. All these components are gathered on a large board, which provides the readout of 128 calorimeter channels. The first prototypes of the board give entire satisfaction.

1. REQUIREMENTS

The basic requirements for the readout system are the following:

- Amplify and shape the signal coming from the detector with an optimisation of the signal to both electronics and pile-up noise ratios.
- Sample at 40 MHz the signals coming out of the shapers.
- Store data during the level 1 trigger latency ($\geq 2us$).
- Read several samples (typically 5) per event accepted by level 1 (the maximum rate should be 75 kHz and could raise up to 100 kHz) and perform the analog to digital conversion.
- Format and transmit the data to remote DSP boards (“R.O.D”) which will provide on the fly feature and energy extractions before sending data to the level 2 event buffers.
- Operate fully simultaneous write and read operations and deal with interleaved events.
- Cover a dynamic range of 16 bits without degrading the calorimeter resolution (0.7% for the largest signals).
- Feed the level 1 trigger system with analog sums of the input signals.

The total number of channels to be equipped is very high (~200,000) and the electronics has to fit in a limited volume with stringent constraints on power dissipation and accessibility. Furthermore, the radiation level to deal with is at the level of 100 krad per year, including a safety margin of a factor 5.
2. SYSTEM DESIGN

The front-end electronics of the liquid argon calorimeter is located directly on the detector. There are around 60 crates, which house four different types of boards (see Fig. 1).

The idea to design a 128-channel readout board arose at the end of 1996. To match the above requirements, the following solutions were chosen (see Fig. 2):

- The signal shape is bipolar with a rise time of 40ns to optimise pile-up versus electronics noise.
- The detector signals dynamic range of 16 bits outgoing the preamplifiers is divided in three linear ranges of 12 bits. This operation, performed by tri-gain shapers (gains of 1, 10, 100), allows to split the dynamic range without degrading the intrinsic detector resolution (~7 bits).
- Each signal coming out of the shapers is send to analog memories. Inside each memory, the signal is sampled at 40 MHz and stored until a level 1 trigger is received.
- Then only the interesting data is converted by the ADC (1% of the total input rate) with all samples on the same gain and sent serially to the output drivers.

Then the interesting data is converted by the ADC (1% of the total input rate) with all samples on the same gain and sent serially to the output drivers.

3. FRONT-END BOARD SPECIFICATIONS

This board treats the 128 channels coming from the detector in 16 groups of 8 channels (see Fig.2). Each block includes:

- two 4-channel tri-gain shapers [2].
- two 4x3-channel analog memories or SCA (Switched Capacitor Arrays).
- one 12bit / 5MHz ADC.

There is also a large amount of digital components to ensure all the functionalities:

- 8 Altera FPGAs for gain selection and output data formatting (each for 16 channels).
- 2 Xilinx SCA controllers (each for 64 channels) which provide write and read addresses to the SCA and perform the synchronisation for all the read operations [9].
- A summation block for the first step of level 1 trigger analog sums.
- The TTC interface for the fast signals (CLK, L1, INIT).
- The interface for the new fast serial link (SPAC) which allows the downloading of all electronics sited on the detector.

The signals coming out of the shapers are sent to the analog memories. Inside each memory, the signals are sampled at 40 MHz and stored until the SCA controller receives a level 1 trigger. Then the five samples corresponding to the selected event will be driven sequentially towards the output of the chips. At this point and for each sample, the 2x4 internal channels of two associated chips are multiplexed at a 5 MHz rate.

For each channel, the peak sample (the third sample) is first read. It is compared on the medium gain both to saturation and to a low threshold. Depending on the result of the comparison, one of the gains is chosen and stored. Then the same sample is read once again on the right gain, and sent to the output. All the four other samples are also read on the same gain as the peak sample. The total time needed for reading a group of 8 channels with 5 samples is thus 9us.

Event output data is formatted in a block of 50 16bit-words and sent serially on two lines (one for each byte) towards the R.O.D boards [10].

On the Front-end board, special care has been taken to avoid as much as possible the crosstalk between the digital part running either at 40 or at 5 MHz and the
analog signals. This implied the use of common ground planes covering the complete board, special routing of critical signals, and strong decoupling and filtering of power supplies. All the perturbative digital lines are transmitted in differential analog signals. This implied the use of common ground and an external resistor is needed in series in both applications. All chips have weak and strong technologies. In the chips without input switching, it is inadvisable for a high reliability of l.2um or less which also suffers from analog crosstalks, but only due to small layout imperfections.

Two teams (Nevis and Orsay/Saclay) have then combined their experience and efforts to design new circuits fitting exactly the requirements.

In this experiment, the electronics will have to withstand a total ionizing dose higher than 100krad. The last chip, dedicated to the final application, uses the DMILL CMOS 0.8um rad-hard technology [7].

Each of the 16 SCA channels consists in:
- 144 storage cells in which the signal is sampled at 40Mhz
- a write amplifier
- a return path amplifier
- a read-out amplifier

The noise, the switching charge injection dispersion and the sensitivity to digital perturbation scale at first order as 1/Cs. Thus a high value (1pF) has been chosen for the storage capacitor. The timings of the read, reset, and write operations, optimised for linearity, dynamic range and sampling time precision are shown in Fig. 3, and are described in detail in [5].

The connection between the shaper and the pipeline is a critical point of the system. Consequently, in order to keep this connection short and to simplify the board layout, the two chips have the same modularity and use the same PQFP100 package.

Each gain of the four calorimeter channels treated by a shaper is stored in a pipeline channel. A 'slave' channel is connected to the reference output of the shaper. Its output is subtracted externally during read to the selected gain channel output. This pseudo-differential operation reduces drastically the coherent part of the noise induced within and in front of the pipeline. Unlike in [5], each slave channel corresponds to a different calorimeter cell. To limit a potentially catastrophic coupling from high gain to low gain, the channels are arranged as shown in Fig. 4.

The digital part of the SCA has been designed to ensure the minimum digital activity. All the digital input signals are differential low level (LVDS or PECL). The write addresses, sent in parallel, are decoded using the power efficient scheme described in [4]. The read addresses are sent bit serially at the rate of the read clock before the read signal initiates the decoding of this channel.
address. Then the read-out and multiplexing operation is sequenced by the read clock. This sequence depends on a 'parity' static bit indicating whether the SCA is the first of the second one multiplexed toward the bottom read bus parasitic capacitance. The write and return busses are large to lower their resistivity whereas the bottom read bus is very thin to lower the noise which is proportional to its capacitance [6].

The performances of both the HP and DMILL chips are summarised in Tab.1. They have both been characterised on the same dedicated test bench performing simultaneous write/read operation. All the present results have been measured with the chips mounted on sockets. Thus all are worst case and the values measured when mounted directly on the board are still better, especially for noise and crosstalk. The dynamic range is then close to 14 bits.

## 5. SPAC BUS SPECIFICATIONS

The aim of this protocol is to provide the loading and reading of all registers and memories located on the calorimeter of the ATLAS detector [8]. It has been designed to be fast (10MBit/s), reliable (integrated error detection) and cheap. The slave interface fits in an unique circuit and offers several facilities (SPAC -> VME transcoder to drive a VME bus thus allowing crate interconnections, JTAG outputs for on board FPGA programming, ...). The SPAC bus can use PECL or BTL levels and be uni or bidirectional. User’s software is written in C, and graphic interfaces are running on UNIX and MacIntosh. The SPAC bus induces small power consumption and is totally mute when not used. The protocol is simple and powerful, and allows an immediate understanding of data transfers with an oscilloscope.

### SPAC general view

![SPAC general view](image)

**Fig. 5 : SPAC system architecture**

The main points of this one-master n-slaves bus are described below (see Fig. 5). The following definitions allow any kind of transfer, including as many words as desired, in each direction between the master and the slaves. The specific adaptations for custom applications are left to the choice of the users.
Here follow the main features of the SPAC bus:

- The protocol requires only two bidirectional wires with BTL levels: SCL for clock/strobe, SDA for data (see Fig. 6). But it can be used identically with four unidirectional wires, in BTL or PECL technology. The master and slaves can either be considered as emitters or as receivers on the line.

- There is no problem of master arbitration as this bus is single-mastered by definition. Nevertheless, to prevent any collision, each emitter watches over the line before and while taking hand on it. Moreover, the protocol forbids the broadcast reading command.

- Each slave connected to the bus is addressable by a unique 7-bit address. One address is reserved for the global broadcast mode, which allows the addressing of all the slaves. Moreover, 15 other addresses are reserved for local broadcast modes, which allow the addressing of various groups of slaves, defined by the users. These groups realise a partition of the totality of the slaves (each slave belongs to one group). The broadcast modes are only available for write commands coming from the master.

- The data always travel in the same direction as the clock. Data is transferred at 10Mbit/s. The slaves use their local 40MHz clock to generate the 10MHz return data clock, so no additional clocks are needed. The slave interface clocks are internally resynchronised during each transfer from the master.

- The data packets are 9bit long (see below) with always exactly one missing clock period between packets. This allows to separate clearly the packets for simplicity purpose and gives time for data transfer within the receiver (this will help to simplify the receiver electronics). The 9bit words are transferred with LSB first (this allows the checksum to be calculated sequentially).

- The SDA and SCL lines follow the start and stop conditions of the I2C protocol. Conversely, there will be no acknowledgement from the slave during a data transfer as this is the limiting point for the bus speed. In a general way, all the timings are secure as long as several conditions about the board distances are respected. This makes this system very safe.

- To prevent the collisions, the emitter always checks that the line is not busy before taking hand on it. Moreover the open collector structure protects the bus against any short.

- The format of the response to a read request is the same as the format of the request except for the direction bit in the first word. This means that the data contained in the two first words is a copy of the one received from the master. This allows crosscheck and makes the control software more convenient.

**Fig. 6 : SPAC bit streams**

- The slave provides a JTAG output in order to program any other FPGA on the host board.

- There is a possibility for any slave to send an interruption to the master when the line is idle. This command has a special format (both lines pulled to zero during 10 clock cycles).

The SPAC is currently being used intensively and successfully in beam test at CERN. As its possibilities are wide, it may also be used for many other applications, as test benches in the lab. That is the case of the SCA test bench which provided all the previous results.

6. PERFORMANCES OF THE FRONT-END BOARD

Most of the original requirements have already been reached with the first 128-channel prototype. Five of these boards are currently used at CERN on test beam. The following results have their origin both in lab test benches and in beam tests.

- The total power dissipation is 96W per board, i.e. 750mW per channel.

- The dynamic range is in excess of 18 bits without preamps. It is calculated by dividing the maximum output signal on the low gain (2500 ADC counts) by the noise in the high gain (0.8 ADC count). When connected to the detector, it goes down to 16 bits. The noise is indeed strongly depending on the cell capacitance and on the preamp input impedance (see Tab. 2).

- The integral nonlinearity stays below 0.2% over the full range with real signals (see Fig. 7).

- The noise distribution is gaussian. Its characteristics depend on the gain:
  - On the high gain, it is totally dominated by the preamp input, what is in respect with the requirements. The ratio between shaper and input noise is around 1/10 and between SCA and shaper around 1/2.5.
- On the medium gain, it is still dominated by the input noise. The resolution is good (over 8 bits) as the noise amplitude is around 1 ADC count.
- On the low gain, it is dominated by the last stages (shaper + SCA + ADC) but the value is nevertheless around 0.5 ADC count.

The noise is distributed into two major contributions: incoherent and coherent. The latter can also be divided into two terms: one corresponding to groups of four channels that can be found everywhere on the board, and the other to the term common to all channels on the board. The major source of coherent noise is the pickup at the board input.

### Tab. 2: noise results on the Front-end board

<table>
<thead>
<tr>
<th>Noise/channel</th>
<th>Incoherent</th>
<th>Coherent/4</th>
<th>Coherent/board</th>
</tr>
</thead>
<tbody>
<tr>
<td>High gain</td>
<td>3.5 to 7.8</td>
<td>1.3</td>
<td>1.2</td>
</tr>
<tr>
<td>Medium gain</td>
<td>1.2</td>
<td>0.2</td>
<td>0.3</td>
</tr>
<tr>
<td>Low gain</td>
<td>0.6</td>
<td>0.03</td>
<td>0.3</td>
</tr>
</tbody>
</table>

The sum over 128 channels is dominated by the noise contribution which is coherent per board in the high gain. This is therefore one of the main points to focus on. However, it appears currently not to be shared between two neighbouring boards, even without lateral shieldings.

### 7. CONCLUSION

Six 128 channel front-end boards have already been produced and tested in beam tests at CERN. The performances measured proved the validity of the technical choices. Most of the original requirements have already been reached. The main remaining difficulty is the coherent pickup at the board input. Thus the input connector shielding will be improved. Moreover, the current prototype is not radiation tolerant, what is a mandatory requirement at the level of 100krad for the production. However, some components as the analog memory designed in DMILL technology are already rad-hard and their performances could qualify them for the final run.

### REFERENCES

PERFORMANCE of the ATLAS LAr CALIBRATION BOARD

J. Colas, M. Moynot, P. Perrodo, G. Perrot, I. Wingerter-Seez

Laboratoire de Physique des Particules, IN2P3-CNRS
Chemin de Bellevue
B.P. 110 - 74941 ANNECY-LE-VIEUX, FRANCE.

J.P. Coulon, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau, L. Serin

Laboratoire de l'Accélérateur Linéaire, IN2P3-CNRS et Université Paris-Sud
B.P. 34 - 91898 ORSAY CEDEX, FRANCE.

ABSTRACT

The ATLAS Liquid Argon electromagnetic calorimeter needs a very accurate calibration system in order to fulfill its physics requirements. Calibration boards have already been produced to test the calorimeter modules in electron beam. These boards contain a logic to load a full run (various DAC and patterns) and provide 128 signals which are injected on the electrodes with precision resistors. Measurements have demonstrated a good linearity over a 16 bits dynamic range and a good uniformity (0.2%).

1. INTRODUCTION

The precision in physics aimed in ATLAS requires a good energy resolution over the full acceptance and thus a small overall constant term, better than 0.7%. Part of this constant term is related to the ability to calibrate 200000 channels with a good accuracy [2].

Due to the fast shaping times used at LHC experiments, the readout electronics is current sensitive and thus the traditional charge calibration through a precision capacitor is no longer valid. Moreover, the parallel noise is smaller at these shaping times and thus it is possible to use a current calibration with precision resistors.

2. REQUIREMENTS

- Signal : it should be as close as possible to the real signal which has a triangular shape. The initial current must be very precise and injected close to the electrodes. The rise time must be about 1 ns and the decay time 450 ns.
- Dynamic range : from 200 nA (noise level) to 10 mA (nearly 3 TeV in one cell).

- Non uniformity between channels : 0.25% including the board itself and the signal distribution (cables, mother boards).
- Linearity : the integral non linearity must be less than 0.1% for each of the 3 gains of the shaper [1].
- Timing between the real physics signal and the calibration pulse : within ±1 ns to keep the sensitivity to any jitter as small as possible
- Radiation hardness : the board must tolerate radiation fluxes of gammas (20 Gy/yr) and neutrons ($10^{12}$/cm$^2$/yr).

3. CALIBRATION PULSER DESIGN

3.1 Principle :
The calibration pulses are generated by pulsers the principle of which is described on figure 1.

![Figure1: Principle of the pulser](image-url)

The fast output voltage pulse is obtained by interrupting a precise DC current $I_1$ that flows in the inductor. When a command pulse is applied on $Q_1$, $Q_2$ is cut off and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay across the parallel
combination of the cable characteristic impedance \( Z \) and a termination resistor \( R_0 \) of the same value. This pulse is propagated inside the cryostat through a 7 m long 50 \( \Omega \) cable and is applied across a precise injection resistor \( R_{in} \) (0.1\%) in the cold, directly to the electrodes. The resulting current is given by:

\[
I_{cal} = -\frac{R_0}{2R_{in}} I_p \ e^{-t/\tau} \quad \text{with} \quad \tau = 2L/R_0
\]

An amplitude up to 10 mA can be achieved by applying a 5V pulse in a 500 \( \Omega \) injection resistor.

The main difficulty of this calibration system is to distribute uniformly throughout the calorimeter a very precise voltage pulse. To minimize the attenuation due to skin effect, the pulsers are located close to the feedthrough.

### 3.2 Complete design

The current \( I_p \) is generated from a 18 bits DAC voltage through a voltage to current converter. The current in the output branch is \( I_1 = V_{DAC}/R_{in} \), as negligible current flows in the gate of the JFET transistor. A low offset op amp as OP 07 must be used, as \( V_{offset} = 100 \mu V \) corresponds to 1.5 LSB. This can be seen as a pedestal, but it is not likely to be stable.

To ensure good linearity, the base current of Q, which varies non linearly with I, (\( \beta \) varies with the collector current and the temperature) is measured and added to \( I_p \). Q is made of 4 transistors in parallel to share the large DC current for \( I_p \) (up to 200 mA) and to keep a low \( R_{in} \) necessary for the wide dynamic range.

Five precision resistors (0.1\%) determine the calibration pulse accuracy.

### 3.3 Digital part

Calibration parameters are loaded using the SPAC protocol [3]. The digital functions are integrated in FPGAs. A full run is loaded at the beginning and contains:

- DAC values (ramp for linearity measurements)
- Delay values (for timing studies)
- Pattern values (to select channels and enable crosstalk measurements)
- Number of triggers
- No access to the board is necessary during one run, but all the parameters can be read back for each trigger if required.

![Figure 2: Schematics of the analog part](image-url)
4. PRACTICE REALISATION

A board with 128 pulsers has been realised (Figure 3). The size of the board (490 mm x 410 mm) is determined by the front end crate dimensions [2].

The analog part contains 64 pulsers on each side of the board. The pulsers are aligned in a single row close to the output connectors to ensure good uniformity. As the density is very high, surface mounted components have been used (9000 components). The distance between the inductors which make the signal shape is large enough to minimize the mutual coupling between channels.

The digital part is located on the top of the board, on both sides, inside 13 FPGAs.

The layout has been realised with a special care to avoid coupling between digital signals and the analog part which is connected directly to the electrodes.

5. EXPERIMENTAL MEASUREMENTS

5.1 Sensitivity to $Z_c$:

The cable characteristic impedance $Z_c$ is usually specified within ±10%. When a cable is terminated at both ends, the signal amplitude depends only to a second order on $Z_c$. Thus, if $Z = R_c (1 + x)$

$$V = \frac{V_0}{1 + x} \left( \frac{1 + x/2}{2} \right)^2 = \frac{V_0}{2} \left( 1 - \frac{x^2}{4} \right)$$

Figure 4

Thus a 10% error on $Z_c$ results in a -0.25% error on $V$. A very good agreement between the calculation and the measurement has been obtained.

The uniformity has been measured after a 64 channels 50 Ω cable with $Z_c$ varying within ± 5%. The absence of correlation with $Z_c$ shown in Figure 4 demonstrates that the sensitivity to $Z_c$ is not a dominant contribution. The loss of signal by skin effect in the cables is around 5% and will be divided by 3 in the cold. The r.m.s of the dispersion is 0.13% including the variation of $Z_c$ AND the skin effect.

5.2 Signal shape:

A signal measured at the output of one pulser is shown in the following plot. The pulse shape nicely follows an exponential decay as shown by the fit and the rise time is 1 ns.
5.3 Uniformity:
Measurements have been performed on one board (128 pulsers) after a CRRC\textsuperscript{2} shaper ($t_r = 45$ ns). The raw dispersion between channels is 3.5\%.
The following sources of non uniformity have been found:

- The different stripline length between the output of each channel and the output connector. It is corrected for by a small current increase, realised with a calculated resistor in parallel with $R_{20}$.

Figure 6 shows the dispersion before and after correction. It is reduced from 2.3\% to 2\%.

- Part of the non uniformity is also coming from the dispersion of the inductor value (±5\%), which determines the exponential decay. After correction, the r.m.s is reduced from 2\% (dashed line) to 1.3\% (plain line). This number corresponds to the statistical dispersion of the five 0.1\% precision resistors ($rms = 0.2\%\sqrt{5/12} = 1.3\%$).

In the next boards, inductors within ± 2\% precision will be used.

5.4 Linearity:
The linearity has been measured with a 12 bits ADC, sampling the signal at the peak, over the 3 gains of the ATLAS shaper ($t_r = 45$ ns). The integral non linearity is within ± 0.1\% for the low and medium gains. It is slightly worse for the high gain, due to the injected charge discussed below.

![Figure 6]

![Figure 8]

5.5 Injected charge:
Figure 9 shows the signal obtained for various small DAC settings.

The first positive lobe is due to the capacitive coupling of the command pulse (CMD) through the $C_c$ capacitor of $Q_5$, whereas $Q_5$ is still on.

![Figure 7]

![Figure 9]
The second negative lobe corresponds to the injected charge. Indeed, when $Q_i$ is cut off by the command pulse, the very fast voltage variation on its collector, 3V in 1 ns, results in a charge which is injected in the output through a $= 1$ pF parasitic capacitor between the emitter and collector of $Q_i$. This could be reduced in a next iteration using a specially designed PMOS transistor [4].

5.6 Crosstalk:

The crosstalk over one output connector has been measured in the ATLAS configuration (a warm cable followed by a pin carrier, a vacuum cable, a second pin carrier and a pigtail [2]).

The sign of the crosstalk depends on the position (lateral or opposite neighbour) but remains always lower than 0.1% at the signal peak, dominated by cable crosstalk.

5.7 Timing:

To keep the sensitivity to any jitter as small as possible, the real physics signal and the calibration pulse must be aligned within ± 1 ns. Two delay chips [5] are implemented on the board to perform this tuning. The delay chips have been measured linear to ± 0.2 ns over 0 to 25 ns range with a 0.996 ns step.

The jitter dependence with the delay value has also been measured and is slightly worse than the 200 ps required. A new version of the chip will be soon tested.

6. RADIATION TOLERANCE

Several components of the pulsers have been irradiated to neutrons ($10^{13}$n/cm$^2$) in Grenoble and gammas (20 hours with 10 krads/hour) in Saclay, and the most sensitive elements have been found to be low offset op amps. Many commercial op amps have been tried but died after neutron irradiation. The OP177 resists to neutrons and gammas, but the increase of the offset voltage from 10 μV to 100μV seems not acceptable for the calibration board.

A commercial dual 18 bits DAC (PCM 1700P Burr Brown) has been irradiated, but the offset voltage drifted to 1 mV after irradiation.

All other semi conductors exhibited satisfactory behaviour (small β drop).

7. CONCLUSIONS

Experimental measurements on the 128 channels calibration board with final ATLAS density have given good results and fulfill the calorimeter requirements.

One board is used on the test beam at CERN and 10 boards are in production to equip the module 0 of the ATLAS calorimeter. This pulser design is also used in other experiments (NEMO and D0).

The next step is to ensure that all elements on the board exhibit satisfactory radiation tolerance, in particular the low offset op amps, the DAC and the digital part.

REFERENCES

"A fast monolithic shaper for the ATLAS E.M. Calorimeter".
ATLAS internal note LARG-No-092

CERN/LHCC/94-43 LHCC/P2, December 1994, 15

A. Gara (NEVIS)
"SPAC : Serial Protocol for the Atlas Calorimeter"
ATLAS internal note LARG-No-93

University of Mainz
"An integrated calibration system for Liquid Argon Calorimetry" (DRAFT)

"A PLL-Delay ASIC for clock recovery and trigger distribution in the CMS tracker"
ANALOG SIGNAL PROCESSING FOR THE CMS ELECTROMAGNETIC CALORIMETER.

Jean-Pierre Walder

Institut de Physique Nucléaire de Lyon, IN2P3-CNRS et Université C. Bernard LYON-I
43 Boulevard du 11 novembre 1918 69622 Villeurbanne Cedex France
Walder@in2p3.fr

I INTRODUCTION.

To accommodate the 16 bits dynamic range of the PbWO₄ crystal calorimeter of CMS in the 12 bits of a digital readout, a multi-gain switching topology is used along with a wide dynamic range transimpedance amplifier in front to convert capture the photocurrent signal of a pair of avalanche photodiode as shown in figure 1. As the trigger algorithms are digital, the readout chain must provide each 25 ns quantized data and therefore, sampling, switching and multiplexing process must be performed at a 40 MHz speed. As a result, the bipolar transistor device, known for its high performance in terms of speed and gain, seems suitable to implement such functions. In addition the level of radiations (up to 2MRad and 5E13 n/cm²) undergone by the electronics imposes the use of radiation hard technology containing bipolar devices.

II DESIGN OF THE BICMOS MULTI-GAIN PREAMPLIFIER.

As shown in figure 1, scintillation light from the crystal is converted into a photocurrent by the photodetector, and into a shaped voltage pulse by the preamplifier. The preamplifier has several outputs, each with different gains (1,4,8,32) and a constant bandwidth in order to keep the same delay at all outputs. A second circuit receives the four preamplifier outputs. A voltage value for each of the four inputs is captured every 25 ns by sample-and-hold circuits. Every 25 ns, voltage comparators and digital logic determine which of the "held" voltage values is the largest (highest gain) below a certain 'saturation threshold'. This value is multiplexed and digitized by a 12-bits ADC.

II.1 The preamplifier.

The schematic of the preamplifier [1] is shown in figure 2. This transimpedance amplifier design targets BiCMOS technology. As seen from the schematic, the passive RfCf network associated with the compensation capacitance Cc, along with the detector capacitance Cd and the transconductance gM1 of the input stage performs the (RC)² shaping of the output pulse; therefore no additional shaping stage is needed. In addition, the compensation resistor Rz is used for internal pole-zero cancellation. Design modifications from the preamplifier presented in [1] were performed concerning the maximum input charge. In order to improve the photostatistic and the signal to noise ratio (degraded by leakage current of the photodetector) two avalanche photodiodes (APD) are put in parallel instead of one. Therefore, both the input charge, provided to the preamplifier, and the source capacitance Cd are doubled. The feedback resistor Rf should be halved and other passive components modified accordingly compared to the previous version.
The full scale input charge is 64 pC, corresponding to a 2 TeV event and the source capacitance $C_d$ is 250 pF (cable capacitance included). The main sources of noise come from the thermal noise of the input transistor M1, which gives an equivalent noise slope of 16e/pF, the feedback resistor $R_f$ with a noise contribution of 2700 electrons, the thermal noise of the amplifier labelled A, with an equivalent input noise resistor of 200Ω, and the class A/B stage (M2, M3, Q4, Q2, Q3) with an equivalent input noise resistor of 50Ω. All these contributions give a total noise of about 10000 electrons, referred to the input.

II.3 Sample and hold and multiplexer stages.

In CMOS switches, charge injection hampers the performance at these speeds, so the sample/hold and multiplexing functions are performed with current-switched amplifiers as shown in figure 4.

These amplifiers are configured as OTAs, with an NPN differential pair. The differential pairs are mirrored with PMOS transistors and the mirrored outputs are mirrored with NPN transistors. The amplifier output then charges the hold capacitor (5pF) not shown in this figure. The use of NPN transistors in the pair and mirror ensures that the amplifier switches off gracefully, so that the held signal is not perturbed. In addition, clamping transistors are connected on gates of MOS current mirrors to bleed off charge when switching.

II.4 Clocks and digital logic.

Two clocks, each at 40MHz are employed. The sample/hold clock controls the sample/hold transitions, and a second clock controls the logic which determines the multiplexer output. All clock input circuitry is implemented with ECL logic cells, while conventional CMOS logic is used for the remaining digital functions.
III RESULTS OBTAINED ON PROTOTYPES.

Both transimpedance amplifier and multi-gain switching circuit, called floating point unit (FPU) were produced in AMS BiCMOS 0.8µm technology [2]. The layout of these circuits are respectively shown in figure 5 and figure 6.

Figure 5: Layout of the preamplifier (AMS).

Functionality tests were performed both in lab and in test beam. Figure 7 shows the measured noise dispersion of 40 transimpedance amplifiers for a total input capacitance of 250 pF. The mean value of 11600e is a bit higher than simulated because the value of the resistor Rz (see figure 2) was higher than expected. The total power consumption of the preamplifier is 80mW.

Figure 6: Layout of the FPU (AMS).

Figure 7: Noise dispersion on 40 preamplifier prototypes.

Figure 8: Non linearity of the FPU.

Figure 8 shows the linearity tested in lab of the FPU, using a 40 MHz clock and a low frequency ramping signal at the input (<100KHz). A non linearity of 0.08% was measured. Preamplifier and FPU were also tested in H4 beam at Cern on a 36 channels crystal matrix (proto 97). Chip-on-board technology was used to realise this prototype along with encapsulated AD 9042 ADC for analog-digital conversion. Figure 9 shows the digitized output pulse for a 120 GeV electron beam. The upper part corresponds to raw data showing a change in range from the X32 gain output to the X8 gain output. The lower part shows the reconstructed pulse. The total power consumption for both analog and digital part is 150mW each. Test chips in BiCMOS DMILL technology containing a transimpedance amplifier matched for one APD (120pF) along with a FPU test slice (the complete analog chain for one channel) were submitted in 96. Both the preamplifier and FPU functionality have been tested to doses exceeding $2 \times 10^{14}$n/cm² and 100 kGy with no observed detrimental effects (no statistically significant change in noise or peaking time in the preamplifier or sample/hold performance in the FPU).

New versions of preamplifier and a complete FPU (6 analog channels and digital part) were submitted in March 98 and will be tested soon. Two supplementary analog channels were incorporated to readout the APD leakage current and temperature through the FPU data channel.
Present rad-hard bipolar technologies (up to 3MRad and $3 \times 10^{10}$h/cm$^2$) offer the possibility of designing analog circuits with high $f_T$ NPN and PNP transistors along with integrated high performance passive components. Consequently, we have also undertaken the design of a complete floating point preamplifier in UHFLX process of Harris. We kept the same topology as shown in figure 1 and the following subsections will describe the main part of this design.

**IV.1 Transimpedance amplifier.**

The schematic of the bipolar transimpedance amplifier is depicted in figure 10. The topology is similar to the BiCMOS counterpart. The input PNP transistor was chosen to have a low base resistor value (rbb') and the highest current gain $\beta$. Degenerating resistor $R_d$ was added to improve linearity. Compared to the BiCMOS preamplifier, the input PNP transistor exhibits two main sources of noise, one due to the base current $I_b$ and the other due to collector current $I_c$. The contribution of them to the total noise is given by:

$$ENC^2 = \frac{2qI_c \tau}{\beta} \cdot \frac{4kT}{\tau} \frac{kT}{2qI_c} \left( \frac{kT}{q} \right) (C_d + C_f)^2$$

where $\tau$ is the shaping time constant, $C_f$ and $C_d$ are respectively the feedback and detector capacitance. By taking the derivative of the previous equation with respect to $I_c$, the optimal collector current is obtained:

$$I_{opt} = \left( C_f + C_d \right) \frac{kT}{q} \frac{1}{\beta} \approx 1.4mA$$

for $C_d = 250pF$, $C_f = 22pF$, $\beta = 60$, $\tau = 40$ns.

As a result, a total noise of 9000 electrons is obtained (simulation) including the contribution of all sources of noise. The emitter follower Q4, used as level shifter, also increases the input impedance of the class A/B stage.

**IV.2 Voltage amplifiers.**

In order to benefit from the high performance of NPN and PNP, a symmetrical architecture like the one used in current feedback amplifier was chosen to implement voltage amplifiers providing the X1, X4, X8, X32 gains (figure 11). As a constant bandwidth is required (see II.2), the same technique of capacitor ratios was adopted. The bandwidth of this current feedback amplifier is given by [3]:

$$BW = \frac{1}{2\pi R_2 C}$$

As the resistor $R_1$ should have a low and fixed value to lower the noise, the resistor $R_2$ and the loading capacitor $C$ is changed accordingly in order to have a constant bandwidth (~50MHz) and four different gains. The simulated noise level is 20$\mu$V at the output and remains negligible compared to the total noise of the preamplifier except for the X1 amplifier with a noise level of 45$\mu$V. This higher value does not degrade the performance since the resolution of the system is independent of electronic noise for high energy signals. A clamping circuit was also added to prevent saturation and long recovering time for high level signals.
IV.3 Sample/hold and multiplexer stage.

The schematic of the sample/hold and multiplexer stage is shown in figure 12. A symmetrical switched emitter follower architecture was employed to realise both functions. Digital controlled differential pairs turn on and off unity gain transistors, each 25 ns. A non-linearity of 0.1% is achieved for signal swing equals to power supply rails minus 5V. In addition, clamping transistors were incorporated to improve speed. As a result, figure 13 shows a full scale simulated sample/hold signal superimposed with the continuous signal coming from the preamplifier. As the 12 bits ADC [4], connected at the output of the chip, require a 1V swing within a 1.9V to 2.9V voltage range and is DC coupled, a on-chip buffer, implementing a 0.5 gain function and capable of sinking 2mA in quiescent condition, was designed, based on symmetrical current feedback followed by emitter followers architecture [5].

REFERENCES


DIGITIZIATION AND DATA TRANSMISSION FOR THE CMS ELECTROMAGNETIC CALORIMETER

P. Denes, Physics Department, Princeton University, Princeton NJ 08544, USA
(email: peter.denes@cern.ch)

Abstract

The CMS Electromagnetic Calorimeter front-end readout consists of a photodetector, floating-point preamplifier, ADC and fiber-optic transmitter. The (commercial) ADC has undergone a wafer lot qualification process that is the model of how the on-detector electronics will be qualified. The fiber-optic transmitter is based on a full-custom, low power serializer developed for the ECAL. The first version of the serializer has been successfully realized in CHFET technology, consumes 60 mW (<100 mW with integrated driver and VCSEL) and has been verified for radiation hardness.

1. INTRODUCTION

The CMS Electromagnetic Calorimeter [1] will consist of 82 728 lead tungstate (PbWO₄) crystals arranged in a barrel and two endcaps. The scintillation light from the crystals is captured by a photodetector (two 25 mm² avalanche photodiodes in the barrel and one 170 mm² vacuum phototriode in the endcaps), amplified, digitized and transported by high-speed fiber-optic links off of the detector. The digitizing electronics must survive a total absorbed dose of up to \( 10^5 \) (10⁵) Gy in the barrel (endcaps) along with a fluence of \( 2 \times 10^{11} \) n/cm² in the barrel over the lifetime of the detector, which is defined to be the amount of time required to obtain an integrated luminosity of \( 5 \times 10^9 \) pb⁻¹. The endcap photodetectors must operate up to \( 10^4 \) n/cm², however the digitizing electronics will be placed in such a way as to limit the total fluence to \( 5 \times 10^9 \) n/cm².

The signal capture electronics consists of a custom monolithic wide dynamic range preamplifier [2] and gain-multiplexing circuit [3] followed by a 40 MHz 12-bit ADC (Analog Devices AD9042). The preamplifier converts the photocurrent into a voltage with a dynamic range of around 16 bits. This voltage is then amplified by four clamping amplifiers with gains of 1, 4, 8, or 32. The gain-multiplexing circuit simultaneously samples each of these four voltages at the LHC bunch crossing frequency of 40 MHz. Voltage comparators and digital logic in the circuit then determine which of the four voltage samples is the largest (corresponding to the highest gain) below a certain threshold. This (quasi-static) voltage is multiplexed and digitized by the ADC.

The output data consist of a floating-point representation of the voltage in the form

\[ G_0 \ [D_1 \ldots D_{12}] \]

where \( G_0 \) is a data type flag, \([G_{1..G_0}]\) is a 2-bit code representing the gain range used (1, 4, 8, 32) and \([D_{11..D_0}]\) is the 12-bit ADC mantissa. In this way, the 12-bit ADC covers the full -16-bit dynamic range.

Following the ADC, a high-speed fiber-optic transmitter (one per crystal) transports the digitized data off the detector to the counting room. Readout units of 10 channels are serviced by a 12-fiber optical ribbon cables with 10 high-speed transmission links to the control room as well as an LHC clock and serial command line towards the detector.

2. ADC PILOT PROGRAM

Radiation hardness is a key concern for electronics at the LHC, and the custom circuits being developed for the CMS Electromagnetic Calorimeter are fabricated in radiation-hard processes. The ADC is fabricated in Analog Devices' XFCB 1.0 (eXtra Fast Complementary Bipolar) process. Although the intrinsic properties of the process and the design techniques used in the ADC result in a radiation-hard part, the part is not formally guaranteed to be radiation hard. In order to ensure that the ADCs for CMS meet the radiation hardness requirements listed above, CMS and Analog Devices (ADI) have defined a process flow which includes a validation phase. Since the first definition of this flow, the ability to use parts packaged in standard 44-pin quad flat packs, rather than die, has simplified this process.

In the planned flow, ADI produces isolated wafer lots of (on average) \( N \) ADCs. If the lot yield is below a certain threshold it is scrapped. One percent of the \( N \) ADCs would be designated as qualification samples, and a fraction of those would be tested under irradiation to validate the lot. The qualification ADCs are pulled at random during the testing of packaged devices. Fifteen to twenty lots would be required for the CMS ECAL.

In order to test this procedure, and verify that the wafer-to-wafer performance of the ADCs are consistent, we have performed an irradiation of \( 5 \times 10^{10} \) p/cm²/s over a 10 cm. At these energies, the proton energy deposition is five times greater than for minimum ionizing particles. Similarly, the damage induced by one
72 MeV proton is equivalent to that of two 1 MeV neutrons. Calorimeter electronics in CMS will be subjected primarily to ionizing and neutron radiation, thus exposure to this beam simulates the radiation cocktail at LHC. At OPTIS then, $10^3$ p/cm$^2$ is the equivalent of $2 \times 10^{13}$ n/cm$^2$ along with a simultaneous 10 kGy (1 MRem).

Results from the irradiation of the roughly 500 ADCs is presented in detail elsewhere [5]. Measurements were made at four frequencies (1.2, 2.5, 5.0 and 9.6 MHz) at a number of amplitudes. The test set-up, due to its location directly at the exit of the beam and the use of sockets, can not achieve the ultimate ADC performance, but it is nonetheless sensitive to very small changes.

Table 1 Worst spur (largest harmonic) for the ADCs before and after irradiation. $10^3$ p/cm$^2$ is the equivalent of the lifetime dose in the ECAL electronics at $\eta = 1.4$.

<table>
<thead>
<tr>
<th>Dose (p/cm$^2$)</th>
<th>Frequency (MHz)</th>
<th>Worst Spur dBFS Before</th>
<th>After</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^3$</td>
<td>1.2</td>
<td>-78.8$\pm$2.6</td>
<td>-79.0$\pm$2.7</td>
</tr>
<tr>
<td>$2 \times 10^3$</td>
<td>1.2</td>
<td>-79.6$\pm$1.7</td>
<td>-79.2$\pm$2.7</td>
</tr>
<tr>
<td>$4 \times 10^3$</td>
<td>1.2</td>
<td>-80.1$\pm$2.6</td>
<td>-75.2$\pm$3.6</td>
</tr>
<tr>
<td>$10^3$</td>
<td>2.5</td>
<td>-77.8$\pm$2.6</td>
<td>-78.1$\pm$2.5</td>
</tr>
<tr>
<td>$2 \times 10^3$</td>
<td>2.5</td>
<td>-78.9$\pm$1.7</td>
<td>-78.1$\pm$3.1</td>
</tr>
<tr>
<td>$4 \times 10^3$</td>
<td>2.5</td>
<td>-78.2$\pm$2.7</td>
<td>-75.4$\pm$3.7</td>
</tr>
<tr>
<td>$10^3$</td>
<td>2.5</td>
<td>-77.8$\pm$2.8</td>
<td>-76.1$\pm$3.2</td>
</tr>
<tr>
<td>$2 \times 10^3$</td>
<td>5.0</td>
<td>-77.7$\pm$2.6</td>
<td>-75.9$\pm$2.8</td>
</tr>
<tr>
<td>$4 \times 10^3$</td>
<td>5.0</td>
<td>-78.4$\pm$3.1</td>
<td>-74.9$\pm$3.4</td>
</tr>
<tr>
<td>$10^3$</td>
<td>9.6</td>
<td>-79.1$\pm$2.9</td>
<td>-76.7$\pm$1.9</td>
</tr>
<tr>
<td>$2 \times 10^3$</td>
<td>9.6</td>
<td>-79.7$\pm$2.8</td>
<td>-76.6$\pm$1.7</td>
</tr>
<tr>
<td>$4 \times 10^3$</td>
<td>9.6</td>
<td>-78.9$\pm$2.4</td>
<td>-75.7$\pm$3.8</td>
</tr>
</tbody>
</table>

Dynamic performance of the ADCs was not affected at doses up to $2 \times 10^3$ p/cm$^2$ (equivalent to 20 kGy along with $4 \times 10^3$ n/cm$^2$). This is illustrated in Table 1, which shows the largest harmonic as a function of dose and frequency before and after irradiation. The values are averaged over the ADCs tested, and the error bar is the rms dispersion of the ADCs. Furthermore, both pre- and post-irradiation behavior showed no wafer-to-wafer variation, so that no special sample selection is required: validating the lot, with random samples is sufficient, a large number of samples from each wafer is not required.

3. FIBER-OPTIC BIT SERIALIZER

3.1 Introduction

The use of digital pipelines with digital trigger sums is a key feature of the CMS detector. At the time of the Technical Proposal [6], it was imagined that digital pipelines would be placed on the detector directly after

the ADC, and that these pipelines would be followed by trigger summation and readout electronics. In such a scenario, several thousand high-speed, radiation-hard fiber optic data links would have been employed to transport the trigger data and main readout data off the detector.

In 1997, after reflection, the collaboration felt that such a system, while fully in the spirit of the CMS design, presented two drawbacks: First, trigger filtering and readout data selection intelligence would be buried in the detector, thus making any modifications extremely difficult. Second, the implementation of such a solution requires a very large quantity of radiation-hard digital electronics, which implies a large cost (and design effort, as almost all would have to be semi-custom design). For these reasons, we are pursing an approach where data are transported off the detector directly after digitization. This maintains the functionality of the previous scheme, but with simplified requirements on the digital readout.

The electronics layout is dictated by the detector modularity (see [1]). With ten-channel readout units and one fiber-optic link per channel, a total of twelve fibers are used per ten-channel unit. On the detector are ten high-speed transmitters (with corresponding receivers in the control room, out of the radiation environment) and two low-speed (40 MHz) receivers for the clock and serial command line (with the corresponding transmitters in the control room). In addition to radiation-hardness, a key requirement for the transmitters is low power consumption (in order to remain under 1.5W/channel, a design ceiling of 300 mW for the complete transmitter was required).

The transmission link consists of four components:

1. The protocol encoder (which takes an incoming parallel stream and adds formatting to maintain an overall DC offset-free data pattern)
2. The parallel-to-serial converter (which takes the encoded parallel stream and creates a high-speed serial bitstream)
3. The optical driver (which drives the optical emitter with the serial bitstream)
4. The optical emitter

Commercial devices typically integrate the encoder and serializer, and have ECL outputs to allow electrical or optical transmission. Similarly, commercial optical transmitters typically integrate the optical driver (with ECL inputs) and the emitter in one package. Most commercial serializers use logic in high-speed bipolar processes, and thus consume considerable power, and are not designed to be radiation hard. To meet the radiation-hardness and power requirements for the CMS ECAL, a custom development was required.

3.2 CHFET Serializer

Principle design considerations for the ECAL include
- Radiation hardness: The transmitter should withstand the $2 \times 10^4$ Gy and $5 \times 10^5$ n/cm$^2$ expected over the life of the detector (at largest $\eta$).
- Power consumption < 300 mW
- Synchronous 40 MHz data transmission (to avoid any noise introduced by clocks beating against each other)
- Lowest possible cost due to the large number of links

The ECAL data consists of 15-bit words every 25 ns. To maintain compatibility with existing serial formats, this 15-bit word will be transmitted as 16 bits embedded within a 20-bit frame. In this way, the serial data rate is 800 MB/s. The protocol selected to prove the principle of operation is compatible with the CIMT (Conditional Invert Master Transition) protocol. Here, 4 control bits are added to the 16 data bits (thus making 20 bits). In order to maintain a DC free line, depending on the number of ones and zeros in the frame, the frame is transmitted as is or inverted. The protocol logic ensures that over time, by inverting frames when required, the number of ones and zeros is balanced. The central two control bits are always 0 and 1 (or 1 and 0 in the inverted case) so that there is always a clock transition in a known place on every frame. This is convenient for error detection, as synchronization errors are immediately detected (which is not the case for packet-oriented transmission).

The IC technology chosen for serializing must possess sufficient rapidity to shift out the stream at 800 MB/s and sufficient drive capability to launch this signal off-chip. For the ECAL, the protocol encoding, serializer and driver are all in the same chip, so that the off-chip drive is a current rather than a differential voltage signal. Based on previous investigations, CHFET technology [7] was chosen. CHFET is a complementary GaAs radiation-hard technology characterized by
- 0.6 $\mu$m minimum size n-channel FETs and 0.7 $\mu$m minimum size p-channel FETs
- Typical digital operation voltage of 1.3V
- Typical threshold voltages of 0.2 V (nFET) and -0.3 V (pFET)
- Much higher nFET gain than pFET gain ($\beta_{n}/\beta_{p} \approx 10$)

The availability of complementary enhancement-mode transistors allows logic similar to CMOS to be constructed (i.e. no static power consumption). Further, as dynamic power consumption is proportional to $CV_{dd}^2$, where $C$ is the effective input capacitance and $V_{dd}$ is the power supply voltage, the low CHFET device capacitance and low operating voltage result in a large power savings. In addition, as nFETs have higher $\beta$ than their silicon counterparts, high speed and drive are possible with nFET configurations (see [8] for a discussion of FFL logic).

In order to minimize cost, use of 850 nm VCSELs with multi-mode fiber was selected. Radiation-hard VCSELs from several manufacturers are available. (In our tests and irradiation studies, the baseline VCSEL used was the Honeywell HFE4080.)

3.3 Serializer Layout

In order to keep power consumption to an absolute minimum, and simplify clocking, a DLL-based rather than PLL-based approach has been selected. In a PLL-based serializer, the frame clock (40 MHz in our case) is multiplied up to the bit rate (800 MB/s in our case) and a series of D flip-flops shifts out the data at the full bit rate. In the DLL-based approach, copies of the frame clock, delayed by 0, 1, 2, ..., 19 bit widths (1/800 MB/s = 1.25 ns bit width) are used with combinatorial logic to create the serial bit stream. Unlike the PLL approach, there are no high-speed clocks and no high-speed flip-flops (although fast transitions are required to produce the bit stream). Further, the DLL is inherently easier to synchronize than the PLL [9], because the DLL involves a first-order capture (only the bit width is adjusted) whereas a PLL is a second-order capture problem (both frequency and phase must be adjusted).
A first version of serializer (along with VCSEL driver) has been fabricated. The architecture, shown in Figure 1, consists of four main blocks:

1. The input flip-flops that hold the 20-bit parallel input stream. This section consists of CMOS-like logic operating at $V_{DD} = 1.3$ V.
2. The high-speed combinational logic that creates the serial bit stream. This section consists of high-speed nFET logic operating at $V_{DD} = 1.3$ V.
3. The clock input and error amplifiers that provides the reference voltage for the DLL. This section consists of analog logic operating at $V_{DD} = 5$ V. (The 5 V supply is for compatibility with the rest of the system, 2 V is sufficient.)
4. The VCSEL driver, which also consists of high-speed nFET logic operating at $V_{DD} = 1.3$ V, as well as the VCSEL bias $V_{DD4}$.

![Figure 2 Voltage-Controlled Delay Element](image)

The clock is differential ECL, AC-coupled to $V_{DD}/2$. Internally these are converted to rail-to-rail signals. These signals differentially drive a series of identical delay elements as shown in Figure 2. The voltage-controlled delay is formed by the cross-coupled inverters operated at $V_{DD}$. The control voltage has been designed to nominally be 1.3 V, with a slope (in the vicinity of 40 MHz) of 15 mV/MHz. Process variations in transistor gain (and capacitance) are easily taken care of with the higher analog supply voltage ($V_{DD}$). To ensure that the outputs are rail-to-rail, the bottom stage (at $V_{DD}$) buffers the delayed signals. A phase detector, consisting of cross-coupled flip-flops, compares the incident clock and the output after all of the delay stages, and produces "UP" or "DOWN" current impulses. These current impulses are integrated on an external capacitor, whose voltage is used to generate $V_{DLL}$. Additional digital logic is employed in the phase detector to prevent locking onto harmonics.

The parallel to serial conversion is conceptually accomplished by using the overlap of the clock at bit i ($C_{k_i}$), the data value of bit i ($D_i$) the inverse of the clock at bit i+1 ($C_{k_{i+1}}$). To eliminate the glitches that would be produced by unequal rise and fall times, the logic of Figure 3 is used. Here, in addition to the $C_{k_{i}}$, $C_{k_{i+1}}$, and $D_i$, a look-ahead function is performed on $D_{i+1}$ and $C_{k_{i+1}}$. Note that although the logic is drawn as a series of gates, the logical function is implemented in a single cell.

The logical OR of these pulses generates the input to the VCSEL driver. The OR output passes though a series of successively larger inverter stages and drives an open-drain output. A digital input allows extra open-drain input stages to be switched in if more optical output is required. The VCSEL anode is connected to $V_{DD}$, and the cathode to the open-drain output. An internal current source generates the static threshold bias current. As the VCSEL is already forward biased, the voltage swing at the cathode is thus minimized.

![Figure 4 CHFET Serializer and VCSEL Driver](image)

The serializer and integrated VCSEL driver, shown in Figure 4, occupy 6.4mm². The VCSEL driver was designed to operate with the HFE-4080, and provides a pre-bias of 5 mA and switches 10 mA of current. Total power consumption under normal operating conditions (800 MB/s) including VCSEL is 90 mW, shared among the different sections as follows:

- $V_{DD_1}$, 40 MHz logic: 10 mW
- $V_{DD_2}$, high speed core: 40 mW
- $V_{DD_3}$, clock input level adapter and DLL analog amplifiers: 10 mW
- $V_{DD_4}$, VCSEL (average current through VCSEL via VCSEL driver, including pre-bias): 30 mW

Operation of the serializer is illustrated in Figure 5. Here, alternating frames with hexadecimal values 7FC01 and 3FC01 are transmitted. The least significant bit is
transition rate is illustrated by the alternating penultimate "1"/"0".

The serializer (with HPE-4080 VCSEL), as well as CHFET process test chips, have been tested under irradiation at the OPTIS facility (described in Section 2). During the irradiation, random synchronization patterns were transmitted by the serializer and optically captured by a Finisar FRM-8510 followed by an HDMP-1024 G-Link receiver. Supply voltages, bias currents and DC operating points were also continuously monitored during the irradiation. The total proton fluence was 3.5×10¹⁶ p/cm², which is equivalent to 7×10¹⁵ n/cm² along with 35 kGy (3.5 MRad). No significant changes were observed, and the only measurable voltage shift was an increase in the PLL operating voltage of ~7 mV. This shift is consistent with a very slight β change (< 1%) and V T shift (< 10 mV) in the transistors of the delay chain. The effect is reproduced under irradiation in ring oscillators (fabricated in the same run as the serializer on the process test chip) where in order to maintain a constant oscillation a slight increase in V DD is observed with dose is required.

As the core circuitry of the serializer has been validated, the next version will include a demonstration of line encoding protocol. In order to maintain DC line balance, the disparity (number of "1"s - number of "0"s) per frame is integrated, and the frames are inverted as required to maintain an integrated disparity of zero. Owing to the high speed and low power consumption of CHFET, it is possible to perform this operation in a fully digital fashion. The digital disparity integrator is constructed with a bit-disparity adder tree (which computes the disparity of the frame). This operation requires about 12 ns (half of the 25 ns frame interval).

The second operation consists of adding the frame disparity to the integrated disparity, and deciding the frame polarity. Although the complete operation could be accomplished in one frame, in order to absorb any possible process variations, an extra pipeline stage has been added, thus during clock N, frame N's disparity is computed, and frame N-1 is serialized. The total front-end latency is thus 4 clock cycles, 3 for the ADC and 1 for the serializer, which is well within the requirements of the CMS trigger.

4. CONCLUSIONS

The Analog Devices AD9042 12 bit, 40 MHz ADC has demonstrated sufficient radiation hardness for use in the ECAL. Further, the standard plastic device package shows no significant signs of degradation after irradiation, simplifying its implementation in the detector. An irradiation test of devices distributed from all wafers in a lot showed extremely uniform performance, as well as behavior under irradiation. A first production batch has just been qualified.

A low power, radiation-hard bit serializer has been constructed in CHFET technology. The serializer converts parallel 20 bit input words at the LHC bunch crossing frequency of 40 MHz into 800 MB/s serial streams. The bitstream is transmitted via optical fiber by use of an on-chip VCSEL driver. The serializer consumes 60 mW when operating, and with VCSEL driver and VCSEL total power consumption is 90 mW.

The serializer and VCSEL have been tested under proton irradiation and show no significant degradation in static or dynamic performance. A second version of the serializer with on-chip protocol implementation will be submitted at the end of 1998, and work on an integrated package (serializer with protocol, driver, VCSEL and fiber pigtail) is commencing.

REFERENCES

6 AD9042 ADC for use in the CMS Electromagnetic Calorimeter
7 CHFET is produced by Honeywell SSEC, Plymouth, MN USA.
8 D. E. Fulkerson et al., Complementary heterostructure FET technology for low power, high speed digital
AN ELECTRONIC CALIBRATION FOR
THE ELECTROMAGNETIC CALORIMETER OF CMS

Jean Pierre Mendiburu
LAPP, Annecy-le-Vieux, France
(email: mendibur@lapp.in2p3.fr)

1. INTRODUCTION AND REMINDER

The crystal electromagnetic calorimeter of CMS (ECAL) is foreseen to measure the electromagnetic particles in a range of 50 MeV to 2.5 TeV with the ambitious challenge of a stochastic term • 2%, a calibration term • 0.5%, and a noise term • 150 MeV.

A calibration of 0.5% on a detector of 10^5 channels is a challenge that has never been archived; it certainly needs several redundant methods of evaluation. In our case, apart from the standard methods based on W’s and Z’s, we foresee a calibration by light injection at the front face of the Crystal and an independent calibration of the electronic chain by charge injection.

We describe here the charge injection for the barrel as developed by LAPP. The end caps will have their own system, probably close to this one.

At the present time, some options are still open and described so.

The ECAL of CMS is segmented in 18 "supermodules" in Φ and each supermodule is composed of 4 "modules" aligned in Z. The module is the basic unit for the construction and the supermodule is the basic unit for the assembling. Each supermodule is made of one module M5 which contains 500 crystals and 3 modules M4 of 400 crystals.

The electronic calibration addressing system is based on the same geometrical modularity.

2. DESCRIPTION OF THE SYSTEM

The charge injection calibration is foreseen to inject at the input of each preamplifier a pulse having a shape identical to the AFD’s one.

The requested performances are:

- The complete coverage of the dynamic range as expected at LHC physics, with an error (distance to the linearity) • 0.1 %
- The addressing system as flexible as possible.
- All the electronic imbedded in the detector has to be rad hard up to an integrated dose of 30 K rads and 2 10^15 neutrons.

The project relies on two main topics: the incorporation of linear injectors in the preamplifier chips design and the command circuits that order the amplitude and the channels to be calibrated.

The command station, situated in the control room consists of a computer linked to a VME crate. Two sets of 3 optical fibbers link the station to the detector. They pass at the left and right side of the barrel and link by daisy chains the supermodules and the calibration towers.

3. THE ANALOG PART

The preamplifier ASIC has been modified to integrate, a Calibration Signal Injector (CSI). When ordered by the control room, this circuit injects at the input of the preamplifier a calibrated pulse of current which amplitude is determined by an analog voltage level preselected by the addressing system. This part has to be designed in the same technology as the preamp. (both DMILL and Harris technologies are under study).

The analog current pulse has to have a the dynamic range of 16 bits, from 40 nA to 4 mA with an absolute precision of 10^-3 (10 bits) reproducible in time and between channels. The noise (in particular the correlated noise) and the cross talk induced by the calibration system on the preamplifiers have to be as low as possible.

The pulse generation is based on a bipolar pair of transistors Q1-Q2.

In a previous step, Q1 is blocked, and the current Ik, fixed by the DAC, flows through Q2 to Rk. The trigger changes the state of the bipolar pair: Q1 becomes conductive and Q2 is blocked. This induces the discharge of the capacitance Ck (about 30 pF) through Rk (about 500 Ω) and the preamplifier.

The pulse received by the preamplifier has an exponential shape with a decay constant of τ=Rk*Ck. (the preamplifier input impedance is negligible in comparison with Rk).

The precision of the injected current relies on the precision of Ik and on the values of Rk and Ck. We will pre-measure each circuit in order to know the exact characteristics of each generator.
The current generator feeding this pulse generation, on which relies the precision and the linearity is actually developed on two versions (A and B) as seen in figure 1. In version A the reference resistor R0 is installed on the collector of the driving transistor, whereas in version B, it is installed on the emitter part. The version A requests to add one amplifier and this drives to a circuit that is more flexible but more power consuming.

5. NEXT STEPS AND CONCLUSION

We have sent an AMS version of injector B in September and will send a DMILL version in October. We foresee to send a Harris version before December. A new version DMILL version of Injector A will be sent in December (if any). We also foresee to have a new irradiation runs with new ACTEL circuits in November.

The overall aim is to make the choice of command circuits at the end of the year and of the injectors for spring, to be on the "module 0 " of the ECAL for the end of 99.

In our ECAL project we think that the calibration at the level of the precision requested to follow the crystals one, will a long, delicate procedure where all the information will be useful and it will be a great help to have the independent measurement of the electronic chain produced by our electronic calibration.

4. THE ADDRESSING SET-UP

The calibration is controlled through two VME cards, one per half barrel, each feeding a set of three fibbers.

Each fibber set arrives in the detector on a half barrel receiver that drives the 17 other supermodules through SuperModule Units (SMU) linked by a daisy chain. Each SMU drives Tower Calibration Units (TCU); each CTU contains the DAC system, that governs the common calibration voltage amplitude and the trigger.

We have based the command system on commercial circuits. The basic elements have been chosen in the list of circuits tested as rad tolerant by the CNES and powered on 5 Volts only.

For test irradiation, we have mounted the circuit shown in figure 2 based on following elements:

- a/ The differential line transceiver for bi-directional data communication ADM 1485, in B CMOS technology.
- b/ The DAC AD 8582 in B CMOS technology
- c/ We have also tested the non volatile FPGA ACTEL 1020 B in 1m technology.

We first have irradiated the circuit on the nuclear plan ULYSSE at Saclay up to $10^{15}$ neutrons/cm$^2$ and 20 Krad of $\gamma$.

The result is that all the circuits survived. The offset of the DAC has moved by -850 $\mu$Volts (but this could be due to temperature hazards) and output Voltage has shifted by .2%.

In a second irradiation run, at SIN (Grenoble), we have irradiated a set of these 3 chips up to $3 \times 10^{14}$ n/cm$^2$ and a test circuit up to $2 \times 10^{14}$ n/cm$^2$. The circuit was powered and measured during the irradiation.

In both cases the ACTEL PGA is dead after $2 \times 10^{10}$ n/cm$^2$. The results are shown in figure 3 up to $3 \times 10^{14}$ n/cm$^2$ and figure 4 shows measurements made in lab on the DAC after $2 \times 10^{10}$ n/cm$^2$.

We have investigated with the constructor and found that the ACTEL 1020 is not protected from latch up and we are going to test other FPGA's of the market in next irradiation runs.
Figure 1  Principle of injector A

Figure 1  Principle of injector B
Figure 2 Principle of the test circuit for irradiation tests
Fig 3 Result of DAC irradiation at $10^{13}$ n/cm$^2$

Fig 4 Dac irradiation after $10^{14}$ n/cm$^2$
Front-End System for the ATLAS Hadronic End-Cap Calorimeter

J. Ban, W. D. Cwienk, J. Fent, L. Kurchaninov, A. Kiryunin, H. Oberlack, P. Schacht

H. Brettel, Max-Planck-Institut for Physics, Munich, Germany (email: brettel@mppmu.mpg.de)

Abstract
For the ATLAS hadronic end-cap calorimeter a monolithic Gallium Arsenide front-end chip has been developed. About 800 prototypes have been produced and tested at room temperature. Detailed investigations of several chips have been carried out both at room and cryogenic temperatures. Repeated warm-cold shock tests of a board, equipped with these chips, proved excellent reliability. 10 preamplifier and summing boards were applied to beam runs at CERN in October-97, April-98 and August-98.

1. INTRODUCTION

The hadronic end-cap calorimeter (HEC) of ATLAS [1] is a liquid argon (LAr) sampling calorimeter with copper plate absorbers. Signals from two consecutive gaps are fed into one preamplifier, and signals from a number of preamplifiers (2, 4, 8, or 16 for different regions of the calorimeter) are actively summed to form one output signal.

The front-end electronics is placed on the outer radius of the calorimeter wheel (inside cryostat) in order to minimize the length of the cables from signal pads to preamplifiers. Five „preamplifier and summing boards“ (PSB), equipped with 12 to 15 front-end chips each, process signals from one HEC module (1/32 of the wheel). Output signals from PSBs are rearranged according to requirements of later trigger tower building and arrive via feedthroughs at the external electronics. HEC uses the same front-end boards as other liquid argon calorimeters of ATLAS. The only exception is the replacement of the (warm) preamplifiers by pole-zero cancellation circuits.

As technology for the front-end ASIC the GaAs TriQuint QED-A PROCESS has been selected because it offers excellent high frequency performance (resulting in low noise), stable operation at cryogenic temperatures, and radiation hardness. The circuit described in this paper is the recent outcome of prototyping made during several years in the framework of the RD33 experiment [2] and later for tests of the HEC prototype modules. The final version of this chip was successfully used in tests of the HEC Module-0 during October-97, April-98 and August-98 beam runs at CERN.

2. CHIP ARCHITECTURE

The block diagram of the front-end chip is shown in fig. 1. It consists of 8 identical preamplifiers and 2 drivers that give the possibility to sum signals according to physics requirements. The summing resistor Rs, the driver feedback loop, as well as input and output decoupling capacitors are external components, mounted on the PSB.

Figure 1: Block diagram of the front-end chip.

PA - preamplifier, DR - driver circuit.

The preamplifier scheme is given in fig. 2a. The input stage is a cascode X1, X2, biased by two current sources X3, X4 and X7, X8. The diodes Xd1 - Xd3 protect the input transistor against possible high voltage discharges in the LAr gaps. The first transistor has the effective width of 10 mm (100 gates of 100 μm in parallel) in order to optimize the signal to noise ratio. Its forward conductance g_m can be adjusted by applying an additional current through resistor R_p. The feedback loop is formed by the combination R_s - C_i. Together with the open-loop gain it’s value determines the input impedance, close to 50 Ω. The last stage X5, X6 has high output impedance, so current signals can be summed at a load resistor. Actually it consists of the parallel circuit of the external bias resistor Rs and the input impedance of the driver stage. The combination of three diodes Xd4 - Xd6 and resistor R_1 is introduced for the level shift and temperature stabilization.
3. DYNAMIC CHARACTERISTICS

3.1 Input impedance

The preamplifier circuit was designed to match 50-Ω cables from the detector to the PSB in the frequency range 1 - 20 MHz. In order to make the signal rise time faster, the input impedance was chosen lower than 50 Ohm, tolerating a slight mismatch for the short cables. Fig. 3 shows the measured input impedance as a function of frequency. In the working range it is around 40 Ω and it varies from chip to chip between 40 and 50 Ω.
3.2 Time response

The time response of the chip to the exponential input current pulse is shown in fig. 4 together with a fit by two exponential functions. It was measured with a digital oscilloscope for 100 μA input current when a capacitance of 220 pF and a 1 m long cable were connected to the input.

The rise time of the output pulse is an important characteristic defining the final pulse shape and transfer coefficient. It depends on the detector capacitance and intrinsic frequency band of the circuit. It was measured for the HEC range of capacitances and is shown in fig. 5. It can be seen that the real shape is reasonably described by an integration time constant corresponding to a resistivity of 48.4 Ohm and an offset time of 5.83 ns.

3.3 Linearity

The expected range of ionization signals in the HEC is up to 250 μA per preamplifier and 1000 μA per driver. The non linearity in these ranges was found to be less than 1.4 % for preamplifiers and 1.6% for the complete channel, well within specifications.

4. NOISE PERFORMANCE

The electronic noise has a strong impact on the energy resolution of the calorimeter and limits the possibility to detect minimum ionizing particles (muons). For current sensitive preamplifiers the noise is usually characterized by the input equivalent noise current (ENI), that is the noise to signal ratio for unit input current. To describe the noise performance of the detector one has to know the ENI as a function of detector capacitance, cable length, and shaper parameters.

The capacitance of the HEC channels varies from 50 to 400 pF and the cable lengths - from 50 to 200 cm. A RC2-CR shaper is to be used with peaking time 30 - 50 ns depending on the HEC region. A wide set of ENI measurements was done for various shaper time constants and input capacitance - cable length combinations. Fig. 6a shows a typical dependence of ENI on the shaper time constant for a fixed cable length of 150 cm and for three values of detector capacitances. Measurements were done for 8 preamplifiers connected to one driver. A fit by a power function (curves in fig. 6a) is used to reconstruct the ENI value for a given peaking time. A result of such a reconstruction is demonstrated in fig.6b for peaking times 30 ns and 40 ns. As expected, the ENI has a linear dependence on the input capacitance.
In order to compare the results with the theoretical thermal noise, the noise spectrum density was measured for short cables (since a long cable on the preamplifier input makes the spectrum shape very complicated [3]). The noise spectrum recalculated to one preamplifier input is given in fig. 7. A fit by model function (curves in the figure) shows that the chip has three noise sources - white serial with equivalent resistance 35 Ohm, white parallel with equivalent resistance 800 Ohm, and flicker parallel with corner frequency 1.5 MHz. The last parameter varies widely for different chips from 0.5 to 5 MHz.

![Figure 7: Measured and calculated input noise spectra for three input capacitors (numbers at curves).](image)

During investigations at cryogenic temperatures excess noise was detected, when the supply voltages \( V_{\text{cm}} \) and \( V_{\text{sd}} \) were increased above certain thresholds. The source could be located to the first transistor of the preamplifier [4].

The presence of excess noise restricts the supply voltage range of the front-end electronics. Based on the measurements of more than 150 chips we conclude that the best operational point is \( V_{\text{cm}}=+3.0 \, V \), \( V_{\text{sd}}=+7.0 \, V \), and \( V_{\text{cm}}=-1.5 \, V \) (range -1V to -1.9V) for LN and LAr temperatures. At this point not a single chip delivers excess noise. On the other hand the linearity, input impedance and timing are still good.

### 5. QUALITY CONTROL

The HEC is designed to operate reliably with full precision over a period of at least 10 years. This requires qualification and tests of all items.

The PSBs and their components are submitted to an extended procedure that is described in the production readiness review [5].

As the front-end chips are the heart of the electronic chain, the QC concerning them is treated in detail by the following chapter.

### 6. CHIP TESTS AND SELECTION

Up to now we use chips from a pre-series of 4 GaAs wafers fabricated by TriQuint. After visual inspection of the wafer by GIGA, suspicious chips were sorted out.

Results of pre-series: We started with amplitude measurements of chips as they came from the factory (not previously tested). Based on the results, selections were taken after each step: gain variation, peaking time (after RC²-CR shaper, \( RC=25\,\text{ns} \)) and noise. Good chips were dropped 5 times into liquid nitrogen and then the test procedure was repeated.

Table 2 presents a summary of the results. About 72% of the delivered chips from all wafers were good. There was a different yield from wafer to wafer, well correlated with technology parameters measured by TriQuint. We lost about 4% of all chips by the cold treatment. A negligible number was lost during the assembly and tests of the PSBs.

<table>
<thead>
<tr>
<th>Delivered by factory</th>
<th>ALL</th>
<th>WAF 14</th>
<th>WAF 15</th>
<th>WAF 6</th>
<th>WAF 17</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>797</td>
<td>200</td>
<td>191</td>
<td>204</td>
<td>202</td>
</tr>
<tr>
<td>Bad</td>
<td>159</td>
<td>33</td>
<td>31</td>
<td>33</td>
<td>62</td>
</tr>
<tr>
<td>Big gain variation</td>
<td>67</td>
<td>17</td>
<td>31</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Good</td>
<td>573</td>
<td>151</td>
<td>129</td>
<td>164</td>
<td>129</td>
</tr>
<tr>
<td>Yield</td>
<td>71.8%</td>
<td>75.5%</td>
<td>67.5%</td>
<td>80.4%</td>
<td>63.9%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>After 5 cool downs</th>
<th>ALL</th>
<th>WAF 14</th>
<th>WAF 15</th>
<th>WAF 16</th>
<th>WAF 17</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>571</td>
<td>151</td>
<td>127</td>
<td>164</td>
<td>129</td>
</tr>
<tr>
<td>Bad</td>
<td>5</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Big gain variation</td>
<td>20</td>
<td>13</td>
<td>0</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>Good</td>
<td>546</td>
<td>134</td>
<td>126</td>
<td>159</td>
<td>127</td>
</tr>
<tr>
<td>Yield</td>
<td>95.6%</td>
<td>88.7%</td>
<td>99.2%</td>
<td>96.6%</td>
<td>98.5%</td>
</tr>
</tbody>
</table>

Table 2: Summary of measurements

Based on large statistics (more than 4000 preamplifier channels) we could precise the test specifications for the mass production. In order to reduce cost, only chips that have successfully passed a full electrical test on the wafer - we expect about 70% - will be packed. Probably after cold treatment, assembly and tests of PSBs about 5-10% of the chips have to be rejected.

QC-Procedure: GIGA checks the wafer parameters and proceeds an electrical test of our circuits. At MPI all chips are dropped 5 times into liquid nitrogen. Then each chip is measured at room temperature (gain, variation of gain, risetime and noise).
7. PSB FRONT-END BOARDS

The GaAs chips are mounted on the PSB front-end boards together with passive components for interconnections, feedback of driver stages and line filtering.

![Graph](image1)

Figure 8: Output amplitudes of 1 PSB (after shaping) in warm and cold. Each input channel is pulsed separately.

![Graph](image2)

Figure 9: Linearity of PSB channels (after shaping) in warm and cold. Each input channel is pulsed separately.

During the design of the 8-layer boards care has been taken to separate the signal lines and make them as short as possible. Interleaved ground and supply voltage plains are segmented, thus avoiding uncontrolled current flow resulting in cross talk or oscillations.

The layout of the 5 types of front-end boards is similar, differing in number of chips and arrangement of summing only.

A full electrical test of the printed boards is foreseen by the producer (shorts etc.). The PSBs will be assembled and all channels checked at room temperature, in liquid nitrogen and finally at room temperature again. If just a single channel fails, suspected components are replaced and the entire test procedure is repeated.

Finally reference data are taken from warm and cold precision measurements (gain, variation of gain, rise time, linearity and cross talk). Full information of 5 prototype boards is documented in [6] and [7]. The fig. 8 and 9 show a small change of amplitudes only, but better linearity in the cold, an indication for higher open loop gain at cryogenic temperatures.

8. RELIABILITY

The application of warm/cold shock treatments on a PSB delivered a surprising good result [8]. We intended to destroy one board by repeated temperature stresses and thereby detect weak points like bad soldering or break of components. All channels were measured at room temperature, then liquid nitrogen was poured over the board until it was completely covered and measurements were made again. The board was pulled out of the container and, due to the humid surrounding air, covered itself by ice which we then removed by a pressured air jet. This action has been repeated 20 times within one week and no single channel failed.

9. REFERENCES

[5] MPI, „Quality assurance for the cold Front-end System of HEC“, PRR-HEC-Elec-C4
[6] MPI, „Design of the HEC PSB Boards“, PRR-HEC-Elec-B1
[7] MPI, „Results of Mass Measurements of Complete PSB Boards“, PRR-HEC-Elec-B3
[8] MPI, „Results of Multiple Cold Shock Tests of a Complete PSB Board“, HEC-PRR-Elec-B2
Front-end Electronics for the ATLAS Tile Calorimeter

K. Anderson, J. Pilcher, H. Sanders, F. Tang
Enrico Fermi Institute, University of Chicago, Illinois, USA

S. Berglund, C. Bohm, S-O. Holmgren, K. Jon-And
Stockholm University, Stockholm, Sweden

G. Blanchot, M. Cavalli-Sforza
Institute de Fisica d’Altes Energies, Universitat Autonoma de Barcelona
Bellaterra, Barcelona, Spain

September 6, 1998

Abstract

The ATLAS Tile Calorimeter readout is designed to measure energy depositions in a single cell from ~30 MeV to 2 TeV. Signals up to 800 pC must be processed over a dynamic range of 16 bits. More than 10,000 channels of front-end readout electronics are needed for this detector. This paper presents the design of the front-end readout electronics and its test results.

1. Introduction

The ATLAS Tile Calorimeter (TileCal) must measure signals from energy depositions in a single cell which range from ~30 MeV to 2 TeV[1]. This corresponds to signals up to 800 pC from each of the two photomultipliers associated with a cell. In addition, the calorimeter response and electronics gain must be calibrated and monitored with a precision of better than 1%. This paper deals particularly with the pulse shaping, calibration and control electronics for the version of the electronics used in test beam running in 1998 (Version 2.3). It is very close to the final one.

2. Front-end Electronics Design

Most analog functions of the front-end electronics are contained on a 7-cm by 4.7-cm printed circuit board, called the 3-in-1 card, located inside the steel shield of each PMT block[2].

The 3-in-1 card provides the following functions:

• shaping of the PMT pulse to match the requirements of the 10-bit 40MSPS digitizers
• production of two linear outputs with relative gain of 64 to achieve an overall dynamic range of 16 bits
• production of an analog signal for the Trigger Summation Card of the Level 1 trigger
• charge integration for monitoring and calibration of the calorimeter cells
• calibration of response by injection of a known charge over the full dynamic range of the system.

A block diagram of the system is shown in Figure 1.

Bi-gain Analog Circuitry

A bi-gain readout system has been developed. Shaped PMT signals are produced with a gain ratio of 64 and are sent to high-gain and low-gain digitizing ADCs. The maximum signal from the high-gain channel corresponds to 1/64 of 800pC, and the signal clamps for higher inputs. This output is encoded with a 10-bit ADC. Thus one count corresponds to 12.2fC. The low-gain channel has a relative gain of one and covers the entire 800pC range with a second 10-bit ADC. The two channels together provide a 16-bit dynamic range measurement over the 800pC scale. The resolution of a single channel is most limited at the cross over point between scales and corresponds to 3%, for a noise on the low gain scale of 0.5 counts.

Fig. 1: Block diagram of front-end electronics.
Since the calorimeter energy to be measured is the sum of many channels this resolution does not impact the quality of the final measurement.

The advantage of this bi-gain approach is that the signal is processed by an easily calibrated linear system with a good resolution. The analog signals are AC coupled to the continuously operating 40MSPS digitizers and any baseline shift can be directly measured and subtracted with negligible impact on the resolution. The schematic of the bi-gain readout channel is shown in Figure 2.

The current-source nature of the PMT and its fast pulse makes it attractive to use a purely passive shaper. Filters have been designed to satisfy a range of restrictions on their transfer functions. A Bessel filter has a transfer function optimized to obtain a linear phase response[3]. It is attractive in this application since its impulse response has only a tiny oscillatory behavior. A fast 7-pole passive shaper based on Bessel filter characteristics has been developed. The 7 poles provide a fast settling time and a reduced noise bandwidth[3]. A single pole device has an effective noise bandwidth of 136% of the break frequency while 7 poles have a noise bandwidth of 115% [4,5,6,7]. The impedance of this shaper is 124 ohms and the bandwidth at -3db is 12Mhz. It provides outputs for the two gain ranges with sensitivities of 1V/800pC and 2V/800pC. This reduces the amplifier gain needed for the high-gain channel and hence improves the signal-to-noise ratio. The amplifier contribution dominates the output noise of high-gain channel.

The high-gain channel uses a gain-of-16 clamping amplifier followed by a unity gain differential driver to a 100Ω 10-cm-long shielded twisted-pair cable. The maximum output is 1V (±500 mV differential) corresponding to a full scale input signal of 12.5pC. The low-gain channel consists of a unity-gain clamping amplifier and a gain of 1/2 differential driver. This channel receives a signal from the shaper low sensitivity output (1V/800pC), and produces a full scale output into the 100Ω cable of 1V (±500 mV differential) for a full scale input signal of 800pC input.

Comlinear CLC501 and CLC502 are used as clamping amplifiers for the high-gain and the low-gain channels respectively. The CLC502 is a unity-gain stable amplifier. Both amplifiers are high speed current-feedback op amps with output voltage clamping. This protects the system against overdrive. It prevents damage to downstream circuitry and reduces the dead time due to amplifier saturation. The high-gain channel has a recovery time of 3ns for an input overdrive of a factor of 32.

The output drivers employ the Burr-Brown OPA4650. It is a quad, low power, wide band voltage feedback op amp and is used in a cross-coupled differential configuration[8]. This gives a high common mode rejection and comple-
mentary outputs. The differential gain is set by a single resistor ratio (R48/R47 for the low-gain channel, R63/R62 for the high-gain channel and R72/R71 for the trigger signal). There is no need for side-to-side resistor matching with gain changes as is the case for conventional differential amplifiers.

**Trigger summation driver**

The 3-in-1 card provides a differential signal to a Trigger Summation Card, mounted in the electronics drawer on the motherboard. This card performs an analog sum of signals belonging to an individual calorimeter trigger tower. The sum must have a 10-bit dynamic range[9]. This signal is derived from the low-gain output of the card. Its cross-coupled differential output driver is based on the Comlinear CLC405 which has a TTL-compatible disable control. The disable function is provided to prevent faulty behavior of an individual PMT or electronics card from spoiling the output of an entire calorimeter tower. While disabled, the CLC405 exhibits a high input/output impedance. The typical off isolation is 59db. Its quiescent power is 8mW compared to its enabled power of 35mW.

**Charge Integrator**

This circuit is designed to measure photomultiplier current induced by a radioactive source used to calibrate the calorimeter, as well as the current from minimum bias proton-proton interactions at the LHC. The integrator is a low pass DC amplifier with 6 gain settings, one calibration input and a switchable output. It uses a JFET input op amp (LF411) with a resistive and capacitive feedback to define the integration time constant and the DC transimpedance of the circuit. A schematic of the circuit is shown in Figure 3. Because the dynamic range of the minimum bias current varies with position of the cell in the calorimeter and with the luminosity of the LHC, a programmable transimpedance is required to maintain an adequate resolution. The gain is chosen so that the smallest expected minimum bias current will produce 40 counts from the 12-bit ADC, thus allowing current measurements with a minimum resolution of 2.5%. During cesium source calibrations, a resolution better than 1% is achieved. The integrator requires a transimpedance as high as 100MΩ. This infers a very high impedance feedback resistance. Since the largest SMD resistance commonly available is 20 MΩ and we cannot rely on the printed circuit board to exhibit such low leakage, the feedback network was configured as a programmable dual T-network. The value is programmable through the communication interface of the 3-in-1 card. The gains are 7.5M, 20M, 27.5M, 54.3M, 72.9M and 100M. The smallest transimpedance value is set by the largest calorimeter cell minimum bias current at LHC design luminosity, with a margin of 1.5 for higher currents.

The PMT is DC coupled to the integrator through a 100KΩ resistor to measure the average DC current. The equivalent source impedance seen from the integrator input must be as large as possible to minimize the offset voltage at the integrator output. The bi-gain shaper is AC coupled PMT and presents a relatively low impedance (124Ω) at high frequencies. A cutoff is thereby introduced in the frequency response of the integrator, higher than the one needed for calibration purposes. The capacitive feedback of the integrator fixes the time constant at 10ms for the highest gain, giving a ripple of less than one LSB of 12-bit ADC for cesium calibration. The non-linearity is less than 0.3%.

The output of the integrator is connected to a bus on the 3-in-1 mother board with an analog switch operated by a remote controller. The signal on the bus is digitized by one ADC in each super drawer. Thus, there are a maximum of 48 integrators per ADC.

**Electronics Calibration**

Each electronics channel must have a relative calibration better than 1% to avoid degrading the overall resolution. A charge injection system is used for this purpose. The schematic is shown in Figure 4. Two calibration inputs are used to cover the wide dynamic range of the system. A 10-bit DAC receives a low noise, high precision, reference voltage
(4.096V) with extremely low temperature coefficient (0.5ppm per °C) from the mother board. A precise output driver with a gain of 2 boosts this voltage to 8.192V to charge the injection capacitors. A controllable timing pulse (TP) closes the discharge switch for either normal or fine calibration. The normal calibration capacitor is 100pF with a precision of 0.5%. This allows the injection of a signal of 800pC for an 8V DAC setting. The fine calibration capacitor is 5.1pF and provides a maximum charge of 40pC. This small capacitor is calibrated using the larger one. The charging time constants are 1ms and 5us for the normal and fine capacitors.

Calibration is also provided for the integrator. The 10-bit DAC applies a known negative voltage (to -4.096V) to a 2MΩ precision resistor. This serves as a reference current source for the integrator.

3-in-1 Bus and Control Logic
Digital control of the 3-in-1 cards is needed for the charge injection calibration, to control the gain of the charge integrator, to control the switching of the charge integrator output onto the analog bus, and to enable/disble the trigger summation output. The control signals are supplied by a mother board which runs the length of the electronics drawer. A dedicated serial RS-422 differential digital bus is used for communication with the 3-in-1 cards. The RS-422 protocol provides a good noise immunity, together with an excellent speed and long distance transmission capability. The digital control logic is implemented with an Altera EPM7064 EPLD. The connection between the 3-in-1 card and mother board is through a high density 40-position connector and a 1mm-pitch ribbon cable.

Simulation and Test Results
Both frequency and time domain simulations have been performed.

The frequency domain simulations include the shaper impulse and step response, the bandwidth of each output and the noise. The simulation result of the shaper impulse response is shown in Figure 5. It has small oscillatory behavior with a 7% overshoot and FWHM of 35ns. The bandwidth of both high-gain and low-gain channels and their output noise distributions are shown in Figure 6. Both channels have a bandwidth of 12Mhz at -3db. The total output noise is 1.2mV (rms) and 0.3mV (rms) for high-gain and low-gain outputs respectively.

Time domain studies include simulations with the expected PMT input signal and simulations of the charge injection
calibration system. Figure 7 shows the outputs for a 9.6pC PMT signal. Figure 8 shows the response for an 800pC signal injected by the normal calibration capacitor. The high-gain output is clamped and the low-gain channel has a full scale response.

Specialized simulations have been performed to study the sensitivity of the output pulse shape to component tolerances and to variations in the shape of the input current pulse.

(1) Dependence of output shape on component tolerance
The shaper is an LC network of 10 capacitors with a tolerance of ±1%, 3 inductors with a tolerance of ±5% and 2 resistors with a tolerance ±1%. The result of 99 Monte-Carlo simulation runs in which component values are varied within their tolerances are shown in Figure 9. The peak output amplitude varies by less than 0.3%.

(2) Dependence of output shape on input pulse width
Event-to-event fluctuations occur in the energy deposition processes in the calorimeter. Because of this there is the potential for variations in the width of the PMT signal. The typical PMT pulse is 18ns FWHM with a 5ns rise time. A sweep simulation has been run by setting 200pC input current pulses, with a rise time of 4ns and fall times of 16ns, 20ns and 24ns respectively. The result is shown in Figure 10. Changes in the peak amplitude are at the level of ±1%
for ±20% changes in signal fall time. Changes in the integral output signal are considerably less and, if necessary, corrections can be applied based on the digitized samples at ±25 ns from the peak.

To measure the overall performance of the system the charge injection calibration system was used. The 3-in-1 output signals were delivered to a 40MSPS 10-bit VME ADC module. To set the timing of the injected signal relative to the digitizing clock a large signal was injected and the timing was varied in steps of ~185 ps in order to center a digitization on the peak of the 3-in-1 output pulse.

To measure the system linearity, the magnitude of the peak sample was recorded and the charge injection signal was varied over a wide range of amplitudes. For each input charge setting, 25 injections recorded and averaged.

Figure 11 shows the linearity and the deviation from a straight line fit. Both the high and the low-gain channels show deviations from linearity well below the level of one count.

For each charge injection event, 10 digitizations outside the signal region were used to measure the pedestal and its RMS. The pedestal stability can be characterized on the 250 ns time scale of individual events as well as on the millisecond time scale between events. For individual events the RMS values are 0.75 counts and 1.3 counts for the low-gain and high-gain signals respectively. The SPICE simulation described above predicts 0.3 counts and 1.2 counts if the only noise source is the 3-in-1 card itself. The measurements are consistent with an additional noise contribution of ~0.7 counts and is largely attributable to the digitizer. This result is entirely satisfactory for the planned application.

Over millisecond time scales the pedestal RMS values are 0.4 and 0.35 counts for high and low gain respectively.

This bi-gain electronics system was used for test beam studies in 1997 and 1998. Figure 12 shows the measured response to muons from the three sampling depths of the calorimeter. The electronic noise of the readout system can be seen from the shaded pedestal distributions near zero. For all three depths the width of the muon signal is substantially larger than the electronic noise indicating that the electronics contribution is negligible.

The calorimeter resolution and linearity have also been studied using charged pions and protons. The system performance using the electronics described here is excellent and exceeds the design specifications.
4. Conclusions

A novel pulse shaping circuit using only passive components has been designed to exploit the current source capability of the TileCal photomultipliers. This shaper has been combined with a slow integrator, a charge injection calibration system, and a digital control system on a small printed circuit board to be located at each of the PMTs. The performance of the system has been studied with SPICE simulations and with prototype tests using both charge injection signals and test beam measurements. Excellent results were achieved.

For 1998 test beam work a set of 120 prototype bi-gain cards were built with the characteristics described above. The system was tested with the first version of the digitizer system located in the TileCal electronics drawers, as well as with 10-bit digitizers located in VME crates.

References

THE ATLAS TILE CALORIMETER DIGITIZER

S. Berglund, C. Bohm, S-O. Holmgren, K. Jon-And, J. Klereborn, B. Selldén, S. Silverstein and J. Sjölin
Stockholm University
K. Anderson, J. Pilcher, H. Sanders and F. Tang
University of Chicago

Abstract

A prototype digitizing system for the Atlas Tile Calorimeter was developed for evaluation in the ATLAS test beam with the barrel preproduction module during the summer of 1998. The experiences provided important input for the final design, which must be ready for production during 1999.

The digitizer demonstrator consists of 8 boards for read-out of up to 48 channels, which are located in a TileCal "super drawer". The boards are connected in a chain ending in a Fibre-channel S-link interface which transports data at a rate of up to 132 MB/s to a Read Out Driver outside the detector. Each board handles the signals from the front-end electronics of 6 PMT channels. To achieve an overall dynamic range of 16 bits, a high and low gain output from each channel is digitized with 10 bit resolution. A XILINX FPGA controller extracts data from pipeline memories and formats the data for read-out. Commands for control and setup of the digitizer system are provided via a TTC system. An ACTEL PGA with fault tolerant design is used as a Read Out Controller.

1. INTRODUCTION

The Atlas hadron Tile Calorimeter [1] consists of 4 segments, each containing 64 wedge-shaped modules (fig.1). The two center segments form the barrel part and the others the extended barrel. The modules, in turn, consist of interleaved iron and scintillator tiles. Impinging particles produce showers in the iron tiles that cause light flashes in the scintillators.

Light from the scintillators is transferred via wavelength shifting fibers to photomultipliers (PMT) in the base of the module. The PMTs and all other electronics are mounted on a sliding "drawer", which can be removed from the module in one operation.

When excited by light the PMT produces a pulse which is shaped and amplified in a so-called 3-in-1 board [2] (fig.2). The pulses are amplified by both high and low gain channels, with a gain ratio of 64. Differential outputs from both amplifiers are then transferred to the digitizer.

Fig 2 Cross section of the drawer and its case

2. THE DIGITIZER ARCHITECTURE

The size of the barrel drawers is 2.8 meters, along which 45 PMTs are mounted. The extended barrel drawers have the same size but contain only 32 PMTs. For practical purposes the digitizer is split up in boards of the size, 35x10 cm². The barrel digitizer consists of 8 such boards, while 6 boards are sufficient to serve the extended barrel.

The incoming pulses, high gain and low gain, are digitized every 25 ns by 10-bit ADCs. The data are stored temporarily in pipeline memories (fig.3) to await a level-1 trigger decision. The trigger latency is now slightly more than 2 μs. A sequence of samples is transferred to derandomizer buffers when a level 1 accept is issued by the first level trigger. In this way all pulses corresponding to the triggered event will be multiply sampled, allowing a subsequent detailed analysis to extract the correct amplitude value eliminating, as far as possible, contributions from
later pulses (pile-up). However, the buffer contents must be examined to make sure that an overflow did not occur in the high gain channel. In the normal read-out mode an overflow would cause read out of the low gain, rather than the high gain channel.

An event may contain up to 15 samples. Digital data from 3 inputs are packed together as 32 bit words to be transferred to a FIFO. There is also a controller part which is responsible for the insertion of control words into the data stream.

ROC in the first board is responsible for inserting these extra control words.

The TTC system is used for clock generation, to deliver level one accepts, and for control and setup of the digitizer operation. Its phase-adjustable clock is used for the ADCs so that the incoming pulses can be sampled in corresponding positions. The TTC optical signal is converted to an electrical signal on the S-link interface board and then transferred with PECL logic levels to the individual boards where a TTC-rx ASIC interprets the protocol.

In the digitizer demonstrator the pipeline memory and the derandomizers are merged in TEC_DMU pipeline chips [5], which were originally developed for the PHENIX detector at RHIC. These chips contain a pipeline of programmable length and 5 derandomizer stages to store events selected by the first level trigger until they can be read out. The length of the pipeline and the derandomizer depth (192 and 80, respectively) are somewhat large for the TileCal application, but this does not have any serious consequences for performance.

A XILINX FPGA (XC4013XL) controller contains the high-gain/low-gain selection mechanism, as well as most control functions. Data from this controller is, as previously mentioned, stored in a synchronous FIFO before being sent out via a ROC controller to the next board and eventually to the S-link board. The FIFO was inserted since the number of derandomizers did not allow the necessary safety margin against data overrun. To enhance the reliability of the system the vital ROC was implemented in a 41225XL fusable link PGA from ACTEL. Such components have a certain degree of radiation tolerance which may be sufficient for the digitizer design. This must be validated by realistic radiation tests.

Both controller and read-out controller were designed from synthesized VHDL code.

3 BOARD DESIGN

One of the crucial issues when designing the digitizer board was to reduce the noise contribution before digitization to a minimum. This was achieved by using differential inputs, and careful design and layout of the circuit board. Analog and digital power and ground are well separated (fig.4) and connected only at one point. The layout of the channel related circuits was done interactively in two trace layers and then copied five times (see also fig.3). The remaining digital part, on the other hand, was autorouted into four trace layers. An 8 layer board was used for the fabrication. To avoid timing problems all signals that pass through several boards are resynchronized in each board.
data is read out event-by-event and board-by-board, reset the digitizer or the S-link or they can be used to force the S-link itself into trigger when the system is in test mode. They can also set the operation mode:

- **Normal mode:** readout of either low gain or high gain data
- **Calibration mode:** readout of both gains
- **Test mode:** exercise the TEC_DMU test mode

It is possible to adjust the pipeline length (1 to 192), the number of samples in the derandomizers (5 to 15) and the timing of the ADC clocks. One may also set a 24-bit word that will be stored in the TEC_DMU during test mode and read back via the controller.

The two broadcast user defined bits produce a trigger when the system is in test mode. They can also reset the digitizer or the S-link or they can be used to force the S-link itself into test mode.

![Board layout overview](image)

**Fig 4 Board layout overview**

**4 COMMANDS AND DATA FORMATS**

The digitizer is controlled by broadcast or addressed commands via the TTC B channel. The commands are interpreted in the controller. One can set the operation mode:

- **Normal mode:** readout of either low gain or high gain data
- **Calibration mode:** readout of both gains
- **Test mode:** exercise the TEC_DMU test mode

It is possible to adjust the pipeline length (1 to 192), the number of samples in the derandomizers (5 to 15) and the timing of the ADC clocks. One may also set a 24-bit word that will be stored in the TEC_DMU during test mode and read back via the controller.

The two broadcast user defined bits produce a trigger when the system is in test mode. They can also reset the digitizer or the S-link or they can be used to force the S-link itself into test mode.

![Data format during normal mode read-out](image)

**Fig 5 Data format during normal mode read-out.**

In both normal (fig.5) and calibration modes, the data is read out event-by-event and board-by-board, with channels grouped three-by-three. All words are protected by parity, and an extra tail word provides vertical parity as well.

The header contains flags to identify the data, such as a bunch crossing identifier and board id. It also contains information about the gain setting for each ADC value and about the operation mode. Error flags monitor the digitizer operation and the TTC transmission. Single and double bit TTC errors are recorded.

**5 TEST BEAM EVALUATION**

After extensive tests in Stockholm with a chain of up to 8 boards and using internal stimuli and static external stimuli, the system was moved to a test bench at CERN where a small number of 3-in-1 boards provided dynamic stimuli. Five boards were installed in the barrel module 0 at the test beam (fig.6), towards the end of the test beam period. Data were then taken over 24 hours with pion, electron and muon beams.

![Test beam setup](image)

**Fig 6 Test beam setup.**

Almost full functionality was achieved. Preliminary analysis of test beam data (fig.7) shows a noise level of 1.1 LSB (~17 MeV) for the high gain channel, which agrees well with SPICE simulations of the 3-in-1 boards. The low gain channels give a noise level of 0.5 LSB (~0.5 GeV).

![A sample pulse](image)

**Fig 7 A sample pulse.**
6 NEXT VERSION

The final design must be radiation tolerant [6] up to 100 Gy over 10 years of operation, which influences the design and choice of components. For instance, the XILINX FPGA must be replaced. It is also necessary to find a radiation tolerant version of the S-link. A modified Tile_DMU is being planned which will help simplify the design, as well as reduce the cost and increase radiation tolerance.

The new Tile_DMU should contain additional registers and comparators for gain comparisons. By allowing the gain selection decision to be made by the Tile_DMU, a smaller and less complicated controller design can be used, since it is no longer in the data path.

Additional design improvements for the Tile_DMU include:

- Improved test facilities, e.g. JTAG.
- A 12-bit data path instead of 24 bits will allow a smaller package.
- More derandomizers (8 instead of 5) will eliminate the need for an extra FIFO.
- Smaller feature size such as 0.35 μ instead of 1μ process provides reduced chip size increased radiation tolerance and faster logic, allowing safer design (that can be synthesized).
- 3.3 V instead of 5V operation.

The new Tile_DMU will also reduce the board complexity and will lead to an improved reliability. It is also possible to introduce a modularity that allows 6, 9 or 12 channel boards.

7 SUMMARY AND CONCLUSIONS

Based on ideas and experience from the RD-16 (FERMI) project [7], a digitizer has been designed for the Tile calorimeter. A fully functional prototype for the TileCal Digitizer was developed and tested in the test beam summer 1998 with encouraging results. The additional noise contribution of the new digitizer proved to be small.

A final version of the digitizer is currently being designed (and subjected to mandatory design reviews) to be verified in the 1999 test beam, and installed in the first production TileCal modules towards the end of 1999. A new pipeline chip is being developed to bring down system cost and to achieve sufficient radiation tolerance.

8 ACKNOWLEDGMENTS

Many persons were involved in the design and tests of the digitizer. Pontus Stenström and Lars Thollander from Stockholm University gave valuable help in the board layout and the design of the S-link interface. Alfonso Ríos from University of Valencia wrote the DAQ software and the TileCal test beam crew helped to run the test system.

The digitizer design relied on the TTC hardware for timing and transfer of commands, and S-link boards for extraction of data. The help from both support organizations are gratefully acknowledged. We were early users of both systems. Erik van der Bij gave us valuable advice and reviewed the design of the S-link interface board.

9 REFERENCES

1. ATLAS Tile Calorimeter Technical Design Report, CERN/LHCC 96-42
5. Status report on the FERMI project, CERN/LHCC 97-58
A charge integrator and encoder ASIC is being developed at Fermilab for readout of the CMS hadron calorimeter photodetectors. The chip provides eight nonoverlapping ranges and is pipelined for deadtimeless operation. It is intended to be used with an FADC to digitize hybrid photodiode current pulses at 40 MHz. For each clock period, one range is selected depending on the signal magnitude, and the output of that range is fed to the FADC to form the mantissa. The selected range is encoded and output as a 3-bit digital exponent. Previous versions of this device have been designed for use with photomultipliers which can have high gain. Hybrid photodiodes have gains of only a few thousand so that a new version of the chip is needed which includes a current-mode preamplifier. The principle of the device is described and early results from a demonstrator project are presented.

1. INTRODUCTION

Hadron calorimeters (HCAL) in the central and end cap regions of the CMS detector are sampling structures with copper absorber plates and scintillator readout layers. Scintillation light from particle showers is collected and re-emitted by wavelength-shifting plastic fibers embedded in grooves machined into the scintillator tiles. Clear plastic fibers are used to carry the shifted light to the photodetectors located in light-tight enclosures on the outer calorimeter surface. Inside these boxes, the clear fibers that originated from scintillator layers are reorganized to form projective towers of scintillator tiles. Hybrid photodiodes[1] are used as the photodetectors because of the 4 Tesla magnetic field at the readout box position. These devices consist of a photocathode followed by a gap of several millimeters over which a large applied electric field accelerates photoelectrons onto a silicon diode target. The signal is generated by electron bombardment, and the diodes are patterned into pixels to provide many channels in one package.

The HCAL readout system must satisfy demanding requirements for rate, dynamic range, and noise floor. The precision of measurement requirement is less critical in accordance with the intrinsic resolution of a hadron calorimeter. Several techniques have been developed and implemented in other experiments that can meet any two of these three requirements as response bandwidth trades against noise floor and dynamic range. The two approaches finding acceptance today are switched capacitor analog storage arrays and multi-range direct digital techniques. This report describes a direct digital approach which is based on a current-splitter input stage driving a parallel set of identical integrating capacitors, one of which will be selected as within range for digitization. An important characteristic of this approach is that it maintains approximately constant resolution over the full dynamic range.

Originally, the current-splitter technique was proposed for calorimeter readout at the Superconducting Super Collider project[2]. Subsequent events led to development and deployment of these multi-range ASICs in the KTeV experiment at Fermilab[3,4] which features a precision crystal electromagnetic calorimeter with photomultiplier tube readout. The KTeV performance specifications exceed those of prior art. Table 1 indicates the developments needed for the CMS HCAL readout by providing a comparison between the performance numbers of the KTeV system and those for the CMS HCAL requirements. The two areas where performance improvements are needed are apparent, noise floor and sensitivity.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>KTeV</th>
<th>CMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>16 bits</td>
<td>15 bits</td>
</tr>
<tr>
<td>Least Count</td>
<td>8 fC</td>
<td>0.32 fC</td>
</tr>
<tr>
<td>Noise</td>
<td>15,000 e's</td>
<td>3000 e's</td>
</tr>
<tr>
<td>Clock</td>
<td>55 MHz</td>
<td>40 MHz</td>
</tr>
</tbody>
</table>

2. REQUIREMENTS

Front-end electronics for the HCAL calorimeter reside on the outer surface of the absorber inside readout boxes that also house the optical rearrangement structures and photodetectors. At this location, the ionizing radiation dose is very small amounting to tens of kilorads at most. However, the neutron fluence is not negligible amounting to more than $10^{10}$ per cm squared per year for kinetic energies above 100 keV. In today's terms, the electronics is required to be radiation tolerant.

* Work supported by U.S. Department of Energy under contract no.1 DE-AC02-76CH03000.
Performance requirements follow from a combination of physics issues, collider parameters and calorimeter characteristics. The most significant of these include: calorimeter energy resolution and photoelectron response, photodetector gain and signal duration, collider crossing frequency, minimum ionizing signal size and highest energy signal expected. Table 2 provides a summary of the operation and performance requirements.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation</td>
<td>Gated integrator</td>
</tr>
<tr>
<td>Frequency</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Aperture</td>
<td>25 nsec</td>
</tr>
<tr>
<td>Charge loss</td>
<td>Less than 2%</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>35,000 to 1</td>
</tr>
<tr>
<td>Precision</td>
<td>1% rms</td>
</tr>
<tr>
<td>Least count</td>
<td>2,000 electrons</td>
</tr>
<tr>
<td>Noise</td>
<td>3,000 electrons rms</td>
</tr>
<tr>
<td>Cross talk</td>
<td>Less than 2%</td>
</tr>
<tr>
<td>Gain stability</td>
<td>Less than 1%/week</td>
</tr>
<tr>
<td>Temperature coefficient</td>
<td>Less than 0.03%</td>
</tr>
</tbody>
</table>

3. THE QIE ASIC

The abbreviation QIE was chosen to indicate charge (Q) integration (I) and encoding (E). Functioning as a gated integrator, the QIE produces two outputs per clock period: a three-bit integer indicating the range and a voltage proportional to the integrated input charge for that range. Coupled with a fast ADC, the QIE front end produces a floating-point result each clock period: m bits of range (exponent) plus n bits of ADC (mantissa). Figure 1. shows an example of a QIE front-end system from the HCAL project where three hybrid photodiode pixels are processed on one small circuit board. Each channel produces an 8-bit result, 3-bits of range plus the result from a 5-bit FADC, to a 24-bit wide serializer operated at 40 MHz clock rate. Figure 2 and Table 3 are provided for visualization of the design parameter choices.

Figure 2. Resolution performance.

Multi-range integration of the signal is done using a current splitter input stage coupled to a set of identical capacitors. An input bias current is applied to set the operating point of the splitter transistors and provide a unique pedestal for each range so that a companion set of comparators can unambiguously select the voltage on one range for routing to the FADC.

<table>
<thead>
<tr>
<th>Range</th>
<th>Current</th>
<th>Min E GeV</th>
<th>Max E GeV</th>
<th>Bin size GeV</th>
<th>Bin size fC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2.8</td>
<td>0.1</td>
<td>0.32</td>
</tr>
<tr>
<td>2</td>
<td>1/3</td>
<td>2.8</td>
<td>11.2</td>
<td>0.3</td>
<td>0.96</td>
</tr>
<tr>
<td>3</td>
<td>1/9</td>
<td>11.2</td>
<td>36.4</td>
<td>0.9</td>
<td>2.88</td>
</tr>
<tr>
<td>4</td>
<td>1/27</td>
<td>36.4</td>
<td>112.0</td>
<td>2.7</td>
<td>8.64</td>
</tr>
<tr>
<td>5</td>
<td>1/81</td>
<td>112.0</td>
<td>338.8</td>
<td>8.1</td>
<td>25.92</td>
</tr>
<tr>
<td>6</td>
<td>1/162</td>
<td>338.8</td>
<td>792.4</td>
<td>16.2</td>
<td>51.84</td>
</tr>
<tr>
<td>7</td>
<td>1/324</td>
<td>792.4</td>
<td>1699.6</td>
<td>32.4</td>
<td>103.68</td>
</tr>
<tr>
<td>8</td>
<td>1/648</td>
<td>1699.6</td>
<td>3514.0</td>
<td>64.8</td>
<td>207.36</td>
</tr>
</tbody>
</table>

Current splitting is accomplished through a parallel array of common-base NPN transistors and grouping the collectors in the desired weights. An example of a current splitter input stage with binary weights is shown in Figure 3. An external DC bias current is provided to satisfy the comparator requirements and to optimize transistor operating parameters. To maintain performance at small input signals, a feedback amplifier is used at the input with the paralleled transistors of the splitter as the series pass element.

In order to maintain constant split ratios over the full dynamic range, the transistor collectors should be held at
the same voltage. MOS cascode circuits are used to equalize the collector voltages and pass the current through to the next stage. For large signals, the most sensitive ranges experience very high currents. Series current limiters are installed on each range to prevent overloads to the subsequent circuitry.

Deadtimeless operation is another requirement for calorimeter readout at future collider experiments. The QIE incorporates pipelined operations to meet this requirement. A latency of four clock cycles is needed to perform all signal processing operations, and four identical sets of integrating capacitors and comparators are utilized. At any one moment in time, one set is connected to the current splitter, the second set is settling into the comparators, the third set is connected to the outputs, and the fourth set is being reset. The QIE ASICs produced for KTeV have shown that high precision, in terms of settling error, reset residual and charge loss at time slice boundaries, can be obtained with a pipeline only four clocks deep at clock speeds up to ~80 MHz.

Present versions of the QIE have been fabricated in a 2 micron Orbit CMOS process. The CMS HCAL devices are planned for an 0.8 micron BiCMOS process to provide higher performance transistors. The development program, which is beginning now, is planned for a two and a half year period with the production run targeted for January 2001.

4. CMS DEMONSTRATOR PROJECT

Sensitivity and noise requirements for the CMS application are significantly tighter than those for the KTeV experiment as shown in Table 1. The principal reason for such challenging performance numbers is the difference in calorimeter light yield. The crystals used in KTeV have a very high light yield compared to the scintillator and waveshifter sampling calorimeter of CMS. A demonstrator project was organized to explore these issues both on the bench top and in the test beam with prototype calorimeter modules. Convinced that a QIE itself could not achieve the needed performance, the project team focused on developing a current-mode inverting preamp for the KTeV QIE system that provided the desired overall sensitivity. Figure 4a shows a block diagram of the amplifier and Figure 4b shows the diagram for the fast pulse amplifier block. The low pass DC-coupled path is required for measurement of the signal produced by a radioactive calibration source illuminating the scintillator tiles. The cross over point between the AC and DC paths is set at 1 kHz.

![Current splitter example](image)

**Figure 3.** Current splitter example.

![Preamplifier block diagram](image)

**Figure 4a.** Preamplifier block diagram.

The demonstrator preamp uses discrete components and was designed with SPICE. Even then, three iterations of printed circuit layout were needed to conquer the problem of parasitics. The QIE and
readout artwork was taken straight from KTeV files. The final circuit board footprint was chosen to allow use in the calorimeter readout box and limited the density to six channels per board.

On the test bench, noise levels were quite low with an rms of about 2200 electrons. The sensitivity is slightly lower than targeted having a 2400 electron least count instead of 2000. For 10 degree temperature excursions about room temperature, the gain temperature coefficient is 0.07%. Since a rather high value of preamp gain, ~ 20, is needed to use the existing QIE chips, the linear dynamic range was slightly more than 50% of full scale, or about 2 TeV in terms of calorimeter energy. This is quite adequate for the test beam, which is limited to 400 GeV. An ASIC optimization of preamp and QIE stages is expected to only require a current gain of about eight making it possible to cover the full dynamic range.

In the test beam in August, most of the allotted time was spent trying to solve environmental noise and pedestal stability problems. A compromise was taken to allow data taking in which the noise was beaten down to 7500 electrons rms but the slow pedestal instability remained. Muon, pion and radioactive source data were taken with the demonstrator electronics at the end of August. The clock was run at 40 MHz but was not synchronized to the accelerator and hence the triggers were randomly phased. Uncorrected histograms of raw data show that the minimum ionizing signal from a single layer of scintillator is clearly seen. The pion signal is seen in several channels as the shower size exceeds the calorimeter cell size. At this time, information on line shape and resolution waits on establishing relative channel gains for summing and on untangling the pedestal instability effects.

REFERENCES


ELECTRONICS FOR MUON DETECTORS
EL ECTRONICS FOR MUON DETEC TORS
A PROTOTYPE FRONTEND ASIC FOR THE READOUT OF THE DRIFT TUBES OF CMS BARREL MUON CHAMBERS

F. Gonella and M. Pegoraro
INFN Sezione di Padova, Via Marzolo 8, 35131 Padova ITALIA
e-mail: franco.gonella@pd.infn.it; matteo.pegoraro@pd.infn.it

Abstract

A full custom ASIC prototype, integrating the basic frontend electronics for the muon drift tubes of CMS barrel, has been produced and tested.

The task of this IC is to amplify signals picked up by chamber wires, compare them against an external threshold and transmit the results to the acquisition electronics. The working conditions of the detector set requirements for high sensitivity and speed combined with low noise and little power consumption.

We used 0.8 μm BiCMOS technology by Austria Mikro Systeme for this application as it provides most of the basic components and simulation parameters needed for analog designs; also the possibility of mixing high speed NPN bipolar transistors with CMOS devices and standard cells allows one to increase functionality.

As the basic requirement for the frontend is the ability to work at very low threshold to improve efficiency and time resolution, a good uniformity for sensitivity and threshold setting is needed; cost and space reasons force us to attain this goal without any equalization at wafer or board level so special care was taken at design phase to minimize offsets and mismatches.

The prototypes were produced in 100 samples partly used to read out 224 drift tubes (one third of a typical CMS chamber) that were tested with a muon beam in mid August 98. Data are now being analyzed and preliminary results confirm that most of the goals have been reached.

1. CIRCUIT DESCRIPTION

1.1 General

The block diagram and pinout of the ASIC are shown in Figure 1.

One integrated circuit contains 4 complete analog chains, each made of a charge preamplifier and a simple shaper with baseline restorer, whose output is compared with an external threshold by a latched discriminator; the output pulses are then stretched by a programmable one shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels.

Also included are a bias voltage source common to all channels and a temperature sensor for slow control purposes.

Figure 1: block diagram of prototype ASIC

1.2 Analog section

The preamplifier uses a single gain stage with a simulated GBW product in excess of 1 GHz and a feedback time constant of 32 ns. Input is protected against ESD by an integrated resistor and diodes connected to the ground and to a voltage of about 2 Vbe generated internally. Power dissipation for the whole stage is 2.5 mW.

The shaper is a low gain integrator with a small time constant; the noninverting input is connected to the preamplifier while the inverting one makes it possible to put this stage inside the feedback loop of a low offset OTA; this combination implements a time invariant baseline restorer acting as a high pass filter for the signal path. Tests performed on this circuit show that the quiescent level of shaper output can be set anywhere between 1.0 and 3.5 V even in the presence of worst case parameters for fabrication process and operating conditions of the IC. A pin common to the four OTAs is used to control this level from outside.

The output of the shaper is directly connected to the noninverting input of a fully differential discriminator with 2 gain stages. The other input of the comparator is connected to an external threshold pin common to all channels. The input section uses no special technique, except a careful layout, to obtain low offset with high speed; an hysteresis of about ±1 mV helps in avoiding...
autoscroll and in speeding up commutation with slow input signals. Common mode input voltage ranges from 1.2 to 3.8 V. Finally, a buffer prevents switching noise from the following sections to propagate backwards to sensitive paths.

All previously described blocks share a single +5 V supply for about 12 mW power drain.

1.3 Digital section

The buffered output of the discriminator is capacitively coupled to a one shot that is very similar to a classical astable multivibrator; its differential output, when active, stores the status of comparator in the latch so producing a non retriggerable pulse whose width is controlled by a current charging a capacitor. Critical parameters of this section are propagation delay, which sets the ability to catch narrow pulses produced by signals just over threshold, and the time it takes to fully recover after the falling edge of a pulse.

The same lines that activate the latch are used to feed the output driver, again a differential one capable of driving a 100 Ω load at voltage levels compatible with LVDS standard. Voltage driving has been chosen because NPN bipolar transistors are faster than PNP and CMOS devices and also because it is power convenient when the load is a cable terminated at both ends. Working conditions of the driver are a compromise between speed and power drain, rise and fall time are below 2.5 ns and, to reduce external components, terminating resistors are integrated in the pads. To reduce consumption, the supply voltage is the lowest possible, 2.5 V, for a power dissipation, including the one shot, of about 12 mW.

1.4 Temperature Sensor and biasing

Temperature sensor is based on voltage difference between base emitter junctions operated at different current densities. Voltage output is 7.5 mV/K and power drain about 1 mW from 5 V.

Bias circuit controls current generators of the whole chip and supplies voltage for one shot sections.

2. TESTS AND PERFORMANCES

2.1 Acceptance and Yield

This circuit was submitted to a MPW run in mid April 98 and 100 untested samples were delivered in mid July. A first screening test, based just on the measurement of pin voltages and supply currents and on detecting response to a charge pulse, was passed by 88 chips; a more refined procedure revealed that 1 further chip was out of specifications (one channel offset ≈ 2 fc).

Using 72 prototypes 18 readout boards were built to equip a portion of a full scale prototype chamber tested in the Gamma Irradiation Facility at CERN SPS; during the run another channel underwent failure so reducing the number of working ASICs to 86 out of 100.

2.2 Analog performances

Power dissipation was easily measured directly on the chamber portion with readout boards: 224 channels required 5.2 W total power almost equally split between +5 V & +2.5 V thus giving an average power drain of less than 25 mW/ch. Tests performed on a single chip showed that this figure changes at few percent level when pulsing the inputs at rates of 1 MHz and also that there is little dependence on temperature.

Since no test pads have been included in the chip, tests on analog section are based on the statistics of output response to charge pulses, so reproducing normal detector operation except for input stimuli that are now δ-like.

Figure 2 shows typical noise performance as a function of detector capacitance: starting point is ENC = 1600 e− @ 0 pF and the slope is about 80 e−/pF, rather high values not in complete agreement with simulations. This effect is mainly caused by the resistor (50-100 Ω), integrated in input pads for protection, that affects both noise and sensitivity specially in the presence of large capacitance at preamplifier input. Input impedance is also increased by this component; its value is about 120 Ω from DC to 1 MHz and increases up to 200 Ω for frequencies ranging between 5 and 200 MHz; beyond this value it is dominated by parasitic capacitance at input.

Gain has been measured at zero detector capacitance and the typical performance is shown in Figure 3 for input charge pulses from 2 to 50 fc; the linearity is fairly good even if in the first part of the range (2±10 fc) there is a slight decrease (≈ 6%) of sensitivity which is most probably caused by the finite gain of the discriminator. The mean value in the range is 3.4 mV/fC and is constant up to 500 fc input with less than 1% integral nonlinearity. For higher values there is a loss of gain due to slew rate limitations while saturation occurs at about 800 fc.
Gain and noise have been measured on 72 prototype chips equipping 18 readout boards: in this case some 4 pF of additional capacitance (protection diodes, input connector and test pulse capacitors) are connected to the input node and slightly increase noise. Figure 4 herebelow shows ENC evaluated on 288 channels.

In order to investigate the gain, two different values of charge, 3 and 9 fC, have been injected: the resulting threshold distributions have mean values of 9 and 29 mV, respectively, with r.m.s. of 0.45 and 0.64 mV. This small spread is due to gain variations among chips, caused by tolerance (max ±10% from process parameters) of feedback capacitor in charge preamplifier, and by discriminator and BLR offset. The former is unpredictable for chips produced in different sectors of a wafer or in different batches and expected to be dominant for high threshold values.

For low input charges the latter contribution can be the most important cause of threshold inaccuracy and in our case it can be calculated extrapolating, for each channel, the threshold characteristic to 0 mV: the 0 intersection, expressed in fC, shows a distribution, given in Figure 5, whose r.m.s. represents the effect of offsets on threshold inaccuracy. This interpolation, calculated again for 288 channels, is characterised by an r.m.s. of 0.13 fC corresponding to 0.44 mV.

This results ensure that, for example, for a threshold set to 3 fC, the error due to offsets is more or less equal to that caused by tolerance in gain.

Rate of input signals may also affect accuracy as the width of the shaper signal is given by preamplifier decay time and baseline restorer requires a certain time to recover from a large input pulse thus producing some shift of DC level. A test for this characteristic has been made by pulsing one channel via a capacitor with 3 fC charges and setting the threshold to detect 50% of charges rate. Then additional pulses of 800 fC have been injected, using a pin photodiode, in such a way that the capacitor injection occurred with 500 ns delay respect to light flash. No appreciable difference, as predicted by simulation, in the percentage of detection of capacitor pulses was measured with light flashing up to a frequency of about 2 Mhz. This represents a good safety margin taking into account that the maximum rate foreseen for a drift tube is around 10 KHz.

Crosstalk has also been measured on some samples on test boards and on a complete readout board. In the first case the maximum signal induced by neighbours on the channel under test was found to be 0.2% of the total input charge, and half of this figure is due to PCB traces. Signal feedthrough from output drivers is also very low, not distinguishable from noise, even in the worst condition, when an unterminated cable is connected to the chip. These results slightly change in the readout board where the average crosstalk is somewhat lower than 0.3% with a maximum of 0.5% for the channel physically located close to output flat cable.

From above measurements it turns out that a very good precision and accuracy in threshold has been achieved, not spoiled by working conditions even for very small input signals.

Timing performances have been measured on a small test board carrying a single ASIC using an oscilloscope HP54720A and a pulse generator HP8131A. Time walk has been first evaluated: charge pulses of amplitude

---

**Figure 3:** low threshold linearity

**Figure 4:** noise performance

**Figure 5:** interpolation of threshold to 0 mV

2.3 Timing
ranging between 2 fC and 1 pC have been injected with threshold set at about 1.5 fC: response times are shown in Figure 6.

![Graph showing delay versus input charge](image)

**Figure 6**: Time walk

Input to output propagation delay of the whole chip for the strongest signal is 3.4 ns and rises to 6.8 ns for an input charge of 3 fC; the actual time walk is obtained from this difference in delay by subtracting half of the pulse generator rise time, in this case 0.7 ns, and is about 3 ns. The r.m.s. of all measuring points, that for the same range increases from 30 ps to 0.4 ns due to input noise, is also plotted in Figure 6. The 2 fC point is strongly affected by noise and presumably also the delay value (8.5 ns) is worsened by this factor.

![Oscilloscope photograph](image)

**Figure 7**: Narrow pulse capture

The oscilloscope photograph in Figure 7 summarises many critical performances of the digital section of the chip: for this test a negative pulse was applied to the threshold input of the discriminators while using the output of the shaper as reference level. The aim was to measure the minimum width and height for a pulse to be captured by the chain made by the comparator, latch and one shot, and to generate a stretched output from the cable driver. The result is that for an overdrive of 5 mV (including hysteresis) the pulse is detected with 99.9% efficiency when its width is greater than 2 ns. This is a rather conservative assessment as the reference voltage for the discriminator (the shaper output) has about 1 mV r.m.s. of noise superimposed. This performance gives also a rough estimate of the bandwidth used for noise tests based on the distribution of response to stimuli. Also shown in this photograph are the rise and fall times of the LVDS output: less than 2.5 ns with such a low amplitude input. The driver has been tested with cables up to 40 meter long connected to a standard LVDS receiver: the signal is recovered with a rise time of about 1 ns in all cases.

The one shot duration in this setup has been programmed to about 50 ns and, from other tests, is found to be dependent at the percent level on input signals ranging from 3 fC to 1 pC; width uniformity, measured on 56 chips, has an r.m.s. of about 5% while dead time is about 10 ns almost independent on programmed pulse duration.

All timing performances, except for the one shot width, exhibit little variations against temperature and the output levels comply with LVDS standard in the 0±100 °C range and for supply voltage tolerances of ±10%.

### 2.2 Other Tests

Temperature sensors integrated in the ASICs were tested in the chamber used during August run; no cooling system was foreseen as the power consumption was little and the detector was in free air. Temperature readout was made with a multiplexer addressed via the I²C interface of the frontend board. Figure 8 shows the distribution of readings for an ambient temperature of about 24 °C.

![Bar chart showing temperature distribution](image)

**Figure 8**: Temperatures inside superlayer

The rise in temperature respect to ambient is about 5 °C and measuring error is a maximum of ±3 °C; the conversion factor of 7.5 mV/K has been checked with a different setup in which a few ASICs have been put inside a climatic chamber and temperature output sampled in the range of 0±100 °C in 25 °C steps.
3. CONCLUSIONS

Bench tests on the analog and timing sections of this prototype chip have revealed very good performances summarised in Table 1.

A statistically significant sample of devices was used to equip a portion of a full scale chamber for a run with muon beam; data analysis is in progress and preliminary results show good efficiency and time resolution as expected.

The production yield, evaluated on a MPW run, has been more than acceptable.

The final chip will include some features and improvements that will be first tested in a prototype whose submission is foreseen before end of this year; main changes will concern:

- input protection resistor will be moved outside chip in order to reduce noise in excess; for the same reason input stage current will be increased at the expense of 1.5 mW additional power drain;
- a mask circuit with minimal feedthrough on signal path will be implemented.

Further work will also be carried out on radiation tolerance and definition of test at wafer level before mass production.

<table>
<thead>
<tr>
<th>Table 1: ASIC performances</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>$25 \text{ mW/channel @ +5 V &amp; +2.5 V}$</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>$200 \Omega (5 \pm 200 \text{ MHz})$</td>
</tr>
<tr>
<td>Noise</td>
<td>$1600 \text{ e'} @ C_{o} = 0; \text{ slope } 80 \text{ e'}/\text{pF}$</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>$3.35 \text{ mV/FC } \pm 10%$</td>
</tr>
<tr>
<td>BLR + Discriminator offset</td>
<td>$&lt; 0.13 \text{ fC (0.44 mV) r.m.s. }$</td>
</tr>
<tr>
<td>Max input signal before saturation</td>
<td>$800 \text{ fC}$</td>
</tr>
<tr>
<td>Input rate without loss of accuracy</td>
<td>$&gt; 2 \text{ MHz @ 800 fC}$</td>
</tr>
<tr>
<td>Threshold range</td>
<td>$0-500 \text{ fC with } &lt; 1% \text{ nonlinearity}$</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>$&lt; 0.2%$</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>$3.5 \text{ ns (3 fC + 1 pC) }$</td>
</tr>
<tr>
<td>Time walk</td>
<td>$&lt; 3.5 \text{ ns }$</td>
</tr>
<tr>
<td>Output pulse width</td>
<td>$20-200 \text{ ns (5% r.m.s. @ 50 ns)}$</td>
</tr>
<tr>
<td>One shot dead time</td>
<td>$9 \text{ ns}$</td>
</tr>
<tr>
<td>Output $t_i$ &amp; $t_f$</td>
<td>$&lt; 2.5 \text{ ns}$</td>
</tr>
</tbody>
</table>

Figure 9: die photo (2.5 x 2.3 mm$^2$)
FRONT-END ELECTRONICS
OF THE CMS ENDCAP MUON SYSTEM

T.Y. Ling
The Ohio State University, Columbus, Ohio 43210, U.S.A.

Abstract

The design and prototype of the front-end readout and trigger electronics for cathode strip chambers in the CMS endcap muon system is described. Preliminary results obtained from beam test of CSC using the prototype electronics at CERN are reported.

1. INTRODUCTION

The CMS Endcap Muon system [1] uses Cathode Strip Chambers (CSC's). Each of the vertical chamber stations are made of 6-layer CSC's which are trapezoidal in shape. In a CSC layer, the anode wires are in the azimuthal direction and the cathode strips are in the radial direction. The bending of charged tracks by the magnetic field in the endcap region is in the azimuthal direction, and the precise measurement of the azimuthal coordinate of a hit is achieved by interpolation of charges induced on neighboring cathode strips. The anode wires provide precise timing measurement of a hit as well as a coarse measurement of its radial position.

The front-end electronics for the CMS Endcap Muon System has two main purposes: 1) to acquire precise muon position and timing information for offline analysis; 2) to generate muon trigger primitives for the Lev-1 trigger system.

2. GENERAL REQUIREMENTS

Since the environment in the CMS endcap muon region is demanding at the LHC with full designed luminosity of $10^36 \text{ cm}^{-2}\text{s}^{-1}$ - singles hit rate could be as high as 1 kHz/cm$^2$ for the inner CSC’s - the electronics must be capable of: 1) handling the expected high rates, 2) dead-time free operation, 3) discriminating against random hits due to neutrons and gammas and 4) withstanding the expected radiation level. Furthermore, due to the large channel counts (about 200k channels of cathode electronics and similar numbers of anode channels), custom ASIC’s must be used extensively to minimize board sizes, per channel costs and power consumption.

3. PHYSICAL LAYOUT

The CSC front-end electronics consists of four types of boards: cathode front-end boards (FEB’s), anode FEB’s, DAQ Motherboards (MB-DAQ) and Trigger Motherboards (MB-TRIG). Figure 1 shows how the system is organized.

Fig. 1. Schematic layout of the CSC Electronics

Depending on chamber types, there are typically 4 to 5 cathode FEB’s, and 3 to 7 anode FEB’s per chamber. Each cathode or anode FEB serves 96 input channels. There is one MB-DAQ and one MB-TRIG per chamber. All the FEB’s are mounted on the chamber and the motherboards will be housed in crates located around the peripheral of each muon station. The data from cathode and anode FEB’s will be sent on cables to MB-DAQ and MB-TRIG. The 2 MB’s serve as the links between the FEB’s and the rest of the experiment. They send the readout and trigger data to the central DAQ system and the Level-1 trigger system. They receive trigger/timing/control (TTC) and slow control signals and distributes them to the FEB’s.

4. CATHODE FRONT-END BOARD

The cathode FEB consists of 96 input channels per board. Each front-end board is designed to read out a section of the chamber 16 strips wide by 6 layers deep. The functional diagram of the cathode FEB is shown in Fig 2. The input signals from each of the strips are sent into 16-channel amplifier-shaper ASIC’s (There are 6 such ASIC’s per FEB). Each input signal is amplified and shaped into voltage pulses. The output pulse shape is semi-Gaussian and the shaper peaking time is 100 ns. To minimize pile-
up effects in high rate environment, circuits to cancel the long tail of the chamber pulse due to ion drift are integrated into the shaper. Channel-by-channel calibration will be done using a set of precisely matched capacitors that couple a test pulse to each channel's input.

Fig. 2. Functional diagram of the cathode front-end board.

One output of the shaper is connected to the trigger path whose main components are a Comparator Network and a Local Charged Track (LCT) processor. The comparator network locates the centroids of the strip charge clusters in each chamber layer to an accuracy of half the strip width and marks its time. The resulting information is fed into the LCT trigger processor which look for coincidence of cluster centroids from a minimum number of chamber layers which form a "road". The time, location and angle of the LCT are used to determine trigger primitive parameters for the Level-1 muon trigger.

The other output of the shaper is connected to the DAQ readout path. The voltage is sampled every 50 ns (see Fig. 3) and held in a Switch Capacitor Array (SCA) during the Level-1 latency. The readout of the stored samples is data-driven: they are digitized and read out only when an LCT trigger associated with the sampled pulses occurs and that the LCT is time correlated with a Level-1 Accept. This requirement significantly suppresses random background hits induced by neutrons and photons. The digitized data is sent to the MB-DAQ and transmitted to the central DAQ system.

The preamplifier is a charge sensitive amplifier with a gain of 0.9 mV per fC. The input charge corresponding to a minimum ionizing hit is about 110 fC, with nominal high voltage setting for the CSC. The performance requirements for the cathode front-end electronics are

- preamp noise less than 24 e/pF + 1000 e,
- 100 ns shaping with tail cancellation,
- 12 bit dynamic range,
- less than 1% deviation from linearity from 0 - 1.5V,
- ½-strip spatial resolution per layer for LCT trigger.

The output voltage of the preamp-shaper is sampled at 20 MHz rate and stored in an SCA channel. There are 6 SCA ASICs on a cathode FEB. Each SCA ASIC contains 16 channels and each channel has 96 capacitors (cells).

Eight samples for each pulse (see Fig. 3) will be saved. The eight samples include 2 to 3 samples of the baseline voltage for pile-up correction and 5 to 6 samples of the signal pulse for offline reconstruction of the pulse timing and pulse height. The sampling of the preamp-shaper output is a continuous, non-stopping process.

Fig 3. Sampling of the shaper pulse.

The SCA cell addresses for storing the sampled voltage (and addresses for readout of the stored voltages) are generated by the readout control FPGA. The cells to be used in the sampling are kept in a pool of free cells. At any time, 2 blocks (or 16 cells) are taken out of this pool. (since pulses arrive randomly in time, 16 cells are used to ensure the capture of at least 8 samples on a pulse). These cells are put back into the pool a) 800 ns later when no LCT is found (800 ns is LCT decision time); or b) an LCT is found but there is no Level-1 Accept after the Lev-1 latency of 3 μs.

The ½-strip per layer resolution required for the LCT trigger is achieved with the comparator ASIC. Four comparators are used for each input channel of this ASIC. The pulse from the shaper for each strip is compared with a pre-set threshold level. If the pulse exceeds threshold, the peak voltage for a given strip is compared with those from neighboring strips. A strip has the largest charge if its peak voltage is larger than either that of the neighbor strips. The track hit position is then localized to either right or left half of the strip by comparing with pulses between the neighboring strips. The output signals from the comparator ASIC are time-multiplexed into three consecutive bunch crossings. In the first bunch crossing, an output bit represents a hit on either of the strips, while during the following two crossings the output contains encoded information as to the half-strip location of the hit.

The digital signals generated by the comparator ASIC's are brought into the cathode LCT processor which finds track "roads" (see Fig. 4) through the 6 cathode layers within in a time interval of 75 ns.
5. ANODE FRONT-END BOARD

The anode readout is similar to that of the cathode except that the emphasis is on the accuracy of timing instead of pulse height. Each input channel of the anode FEB is a ganged group of wires (10 to 20) within a layer. Each front-end board is designed to read out a section of the chamber 16 wire groups wide by 6 layers deep. The functionality of the anode FEB is shown in Fig 6.

Fig. 6. Functional diagram of the anode front-end board.

The input signals go into 16-channel preamplifier-shaper-discriminator ASIC's (6 per FEB). The amplifiers are similar to the ones on the cathode FEB, but optimized for the summed anode input capacitance. The input charge corresponding to a minimum-ionizing hit is about 140 fC, for the nominal high voltage setting of the CSC. The signals are shaped with shaper peaking time of 30ns and sent into discriminators. The logic pulses from the discriminators are used to form the anode LCT and to determine the bunch crossing time of the track segment. The discriminator output pulses are also latched and pipelined for DAQ readout, providing hit/no-hit information for each of the wire groups.

The performance requirements for the anode front-end electronics are

- preamp noise less than 10,000 e at 200 pF,
- 30 ns shaping with tail cancellation,
- less than 2 ns time slewing of discriminator output,
- bunch crossing tagging efficiency > 92%.

Shorter shaping time results in higher intrinsic electronics noise. For shaping time of 30 ns and for nominal chamber gas gain, the CSC signal arise from the avalanche produced by a single electron is comparable to the equivalent input noise of the amplifier. To stay safely above this noise level, discriminator threshold needs to be set at 7 to 10 initial electrons, which can result in large time jitter. To achieve the 2 ns time slewing requirement the scheme of a two-threshold discriminator has been adopted. In this scheme, a high-threshold discriminator is driven by the initial signal from the amplifier. The threshold level is adjustable from 10% to 70% of a nominal MIP signal. The resulting pulse serves as the enable for the precision-time discriminator. The precision-time discriminator consists of a constant-fraction shaper.
and a low-level discriminator. The constant-fraction shaping is done by adding the differentiated amplifier signal and the corresponding delayed and inverted signal. The resulting pulse is further amplified and delivered to the input of a low level zero-crossing discriminator. The zero crossing point corresponds to approximately half the rise time of the input signal.

The anode LCT trigger processor finds track "roads" through the 6 anode layers just as the cathode LCT trigger circuitry does. There are, however, several differences. The anode segmentation is much coarser and the roads are straight lines to the interaction region, independent of $P_t$. The roads also may differ in different chips and boards due to the changing polar angle. More importantly, the anode LCT timing will be used for bunch crossing identification of the track hit, since the analog preamplifier-shaper is optimized for timing rather than pulse height measurement.

Three 96-channel prototype anode FEB's were built and tested on full-size CSC at CERN in the H2 beam area and at X5 with the GIF facility. The results obtained from this test show that the anode timing requirement have been met. Using the prototype electronics, it has been demonstrated that better than 99% bunch crossing tagging efficiency can be achieved by using information from all six CSC layers.

Fig. 7 shows the measured arrival time distribution of muon hits in a single CSC layer. It has an RMS width of 9.8 ns and full width of about 70 ns - too long for efficient bunch crossing tagging. However, the time distribution for the first (or second, or third etc.) arrival pulses from 6 CSC layers is much narrower. As shown in Fig 8., 99% bunch crossing tagging efficiency can be achieved if either the third or fourth arrival pulse is used.

![Fig 7. Anode arrival time distribution for muon hits in a single CSC layer.](image)

6. MOTHERBOARDS

The Motherboards serve as links to the level-1 muon trigger and to the central DAQ of CMS. There is one DAQ and one trigger motherboard for each CSC module. The functionality of the trigger and DAQ Motherboards is shown in Fig.9.

Trigger Motherboard - The information associated with LCT's generated on cathode FEB's and anode FEB's are sent to the Trigger Motherboard. This information includes the bunch crossing time and the location and angle of each LCT. When the timing between a cathode LCT and an anode LCT's is found to agree within ±1 bunch crossing, the LCT is a valid one. When more than one valid LCT is found for the chamber, only the best two, as determined by quality factors, are retained and passed on to the port cards along with the (anode) LCT bunch crossing number. (Each port card spans a 30 degree sector of an endcap station.) The tasks performed by the trigger motherboard are fully pipelined and synchronous with the beam-crossing clock. Another function vital to the operation of the front-end electronics, receiving and fanout of TTC signals to the FEB's, is also located on the trigger motherboard.
DAQ Motherboard - The readout of the data from each FEB is coordinated by the DAQ Motherboard. The digitization of the stored voltage samples on the cathode FEB's and latching of the hits on the anode FEB's are initiated by the arrival on the MB of a Level-1 accept which has a bunch crossing number matching that of an LCT. When this occurs, the readout controllers on the FEB's are notified. Digitization will begin on the cathode FEB's. Those pulse samples stored in the corresponding time window for all 96 channels on the FEB are digitized. The digitized data is sent to the output buffer on the motherboard and transferred by optical link to the central DAQ. The DAQ motherboard also acts as an interface to the Run Control and to Slow Control. The Slow Control functions include down-loading of the FPGA and DSP programs, resetting of the readout controller on the FEB, down-loading calibration information, down-loading commands for turning off bad channels, monitoring of low voltage levels and temperature. JTAG will be used for the slow control.

Prototype trigger and DAQ motherboards were produced and tested together with the cathode and anode front-end boards in the test beam.

7. DAQ ELECTRONICS IN THE COUNTING ROOM

The DAQ electronics that receives the front-end data will be situated in the underground counting room adjacent to the CMS detector cavern. Each readout crate (6U or 9U VME) will contain standardized front-end driver (FED) boards. The optical data links from the motherboard will be received on PCI-interfaced Mezzanine Cards (PMC) mounted on the FED. These PMC's are detector dependent and they handle data readout/buffering, front-end control and front-end monitoring. Readout from the Mezzanine Cards to the event builder will be performed by a commercial single board PC computer mounted on the FED.

8. SUMMARY

The development of cathode and anode front-end ASIC's for the CMS endcap muon electronics are well advanced. Prototype readout and trigger front-end boards have been produced and tested on full-size CSC in test beams. The preliminary test results demonstrated that key performance requirements of the electronics have been achieved. Next set of prototype electronics will aim to improve rate capability and data throughput rate. The schedule calls for testing of a full-fledged pilot electronics system in the year 2000 before production starts.

Acknowledgements

The work reported here is the joint effort of physicists, engineers and graduate students who are members of the CMS collaboration from the following institutes: Carnegie Mellon University, PNNP, Ohio State University, University of California at Davis, University of California at Los Angeles, CERN and Rice University. The success of the project owes to the ingenuity and hard work of everyone involved. This work is supported in part by grants from the U.S. Department of Energy.

References

TRIGGER ELECTRONICS
Abstract: The level-1 muon trigger of ATLAS, in the barrel region, makes use of a dedicated detector RPC, Resistive Plate Chamber. The processing procedure is accomplished through a Low Pt and a High Pt trigger. To reduce the rate of accidental triggers, due to the background noise in the cavern, for both Low Pt and High Pt, the algorithm is performed in the η and φ projections. The Low Pt trigger uses the information generated in the two Barrel Middle RPC stations, each made of two RPC doublets, one in the η (bending) and one in the φ (non-bending) projection. The High Pt trigger uses the result of the Low Pt trigger and the information of the RPC Barrel Outer station. This station is made of two doublets, one per projection. The η and φ information is combined together to generate the Region-Of-Interest (ROI), that is the region in which a valid trigger was produced.

1 Introduction

The ATLAS level-1 muon trigger is based on dedicated, fast and finely segmented muon detectors, the so-called trigger chambers, Resistive Plate Chamber (RPC) in the barrel and Thin Gap Chamber (TGC) in the end-caps [1],[2]. The RPCs are wireless strip detectors with time resolution $\sigma_t = 1.5\text{ns}$. The TGCs are multi-wire detectors with both wire and induced strip read-out having a finer segmentation albeit a larger timing-resolution. The timing resolution of both kinds of detectors is sufficient to provide unambiguous identification of the bunch crossing containing a high-$p_T$ muon candidate [3].

![Fig. 1 Longitudinal view of the muon trigger systems.](image-url)
As illustrated in Fig. 1, the LVL1 trigger in the barrel region is based on three trigger stations. Two stations are used for low-\(p_T\) muon trigger (threshold range approximately 6–10 GeV), while the third station is used in addition for high-\(p_T\) trigger (threshold range approximately 8–35 GeV). Each station is composed of two detector planes. Each detector plane is read out in two orthogonal projections, \(\eta\) and \(\phi\), that will be referred to as the bending and non-bending projections.

The sharpness of the \(p_T\) cut applied by the trigger is mainly given by the information read out from the detectors in the bending projection. However, the information in the non-bending view helps to reduce the background trigger rate from noise hits in the chambers produced by low-energy photons, neutrons and charged particles, as well as localizing the track candidates in space as required for the LVL2 trigger. In addition, the trigger chamber information in the non-bending view provides the second coordinate for the track candidates in space as required for the LVL2 trigger. 111

The high-\(p_T\) algorithm makes use of the result of the low-\(p_T\) trigger and of the information generated in the RPC3 Barrel Outer station. This station is made of two RPC doublets, one in the \(\eta\) projection and one in the \(\phi\) projection. The algorithm operates in a similar way to the low-\(p_T\) one.

In the low-\(p_T\) trigger, for each of the \(\eta\) and the \(\phi\) projections, the RPC signals of the two detector doublets, RPC1 and RPC2, are sent to a Coincidence-matrix (CM) board, that contains a CM chip. This chip performs almost all of the functions needed for the trigger algorithm and also for the read-out of the strips.

The CM board produces an output pattern containing the low-\(p_T\) trigger results for each pair of RPC doublets in the \(\eta\) or \(\phi\) projection. The information of two adjacent CM boards in the \(\eta\) projection, and the corresponding information of the two CM boards in the \(\phi\) projection, are combined together in the low-\(p_T\) Pad Logic (Pad) board. The four low-\(p_T\) CM boards and the corresponding Pad board are mounted on top of the RPC2 detector, as shown schematically in Fig. 2.

The low-\(p_T\) Pad board generates the low-\(p_T\) trigger result and the associated ROI information. This information is transferred, synchronously at 40 MHz, to the corresponding high-\(p_T\) Pad board, that collects the overall result for low- and high-\(p_T\) (Fig. 3).

In the high-\(p_T\) trigger, for each of the \(\eta\) and \(\phi\) projections, the RPC signals from the RPC3 doublet, and the corresponding pattern result of the low-\(p_T\) trigger, are sent to a CM board, very similar to the one used in the low-\(p_T\) trigger. This board contains the same coincidence-matrix chip as in the low-\(p_T\) board, programmed for the high-\(p_T\) algorithm. The high-\(p_T\) CM board produces an output pattern containing the high-\(p_T\) trigger results for a given RPC doublet in the \(\eta\) or \(\phi\) projection. The information of two adjacent CM boards in the \(\eta\) projection and the corresponding information of the two CM boards in the \(\phi\) projection are combined in the high-\(p_T\) Pad Logic board. The four high-\(p_T\) CM boards and the corresponding Pad board are mounted on top of the RPC3 detector.
The high-$p_T$ Pad board combines the low- and high-$p_T$ trigger results. The combined information is sent, synchronously at 40MHz, via optical links, to a Sector Logic (SL) board, located in the USA15 counting room. Each SL board receives inputs from seven (six) low-$p_T$ (high-$p_T$) Pad boards, combining and encoding the trigger results of one of the 64 sectors into which the barrel trigger system is subdivided. The trigger data elaborated by the Sector Logic is sent, again synchronously at 40MHz, to the Muon Interface to the Central Trigger Processor (MUCTPI), located in the same counting room (Fig.3).

![Diagram of the barrel RPC trigger system](image)

**Fig. 2 - On-detector electronics for low- and high-$p_T$ triggers.**

Data are read out from both the low- and high-$p_T$ Pad boards. These data include the RPC strip pattern and some additional information used in the LVL2 trigger.

The read-out data for events accepted by the LVL1 trigger are sent asynchronously to Read-Out Drivers (RODs) located in the USA15 underground counting room.

![Context diagram of the barrel RPC trigger system](image)

**Fig. 3 Context diagram of the barrel RPC trigger system. Each system component functionality is also indicated (white for trigger, grey for read-out and white/grey for trigger and read-out functionality.**
room and from here to the Read-Out Buffers (ROBs). The data links for the read-out data are independent of the ones used to transfer partial trigger results to the SL boards.

Pad, SL and MUCTPI modules generate themselves read-out data on partial trigger results, in order to monitor the system.

3 System segmentation

![Diagram of barrel trigger segmentation](image)

Fig. 4 - Barrel trigger segmentation. Also indicated in the figure are the areas covered by $\eta$ and $\phi$ CM boards, by an ROI, by a Pad Logic (PL) board and by a Sector Logic (SL) board.

From the trigger point of view, the barrel system is segmented into 64 logically (but not physically) identical sectors (Fig. 4).

The barrel is divided in two parts, $\eta<0$ and $\eta>0$. Within each half barrel, 32 sectors are defined. The Barrel Large (BL) chambers and the Barrel Small (BS) chambers of both middle and outer RPC stations are logically divided in two to produce two large sectors and two small sectors per half-barrel octant.

The region covered by a Pad is $0.2 \times 0.2$ in $D\eta \times D\phi$. Inside the Pad the trigger is segmented into ROIs. An ROI is a region given by the overlap of an $\eta$ coincidence-matrix and a $\phi$ coincidence-matrix. The dimension of the ROI is $0.1 \times 0.1$ in $D\eta \times D\phi$.

The total number of Pads is $7 \times 2 \times 32$ for the small sectors and $6 \times 2 \times 32$ for the large ones, giving 416 Pads altogether. Since one Pad covers four ROIs, the total number of ROIs is 1664.

4 Coincidence-matrix board

The CM receives the signals from the RPC doublets and performs the trigger algorithm and read-out functions using a dedicated coincidence-matrix chip [6]. These functions are:

- timing and digital shaping of the signals coming from the RPC doublets.
- execution of the trigger algorithm.
- data storage during LVL1 latency.
- trigger and read-out data generation.
- storage of read-out data in derandomizing memory.

Fig. 5 shows a block diagram of the coincidence-matrix chip. The chip receives the 40MHz machine clock and through a Delay Locked Loop (DLL) system, it generates a 320MHz internal clock that synchronizes all the pipeline operations inside the chip.

The coincidence-matrix has three times $32 \times 48$ cells, since the trigger must be performed on three different $p_T$ thresholds simultaneously. The cells have the possibility to be programmed at will, through a dedicated serial line, to perform $2/4$, $3/4$, or $4/4$ majority logic, and to be set according to the required cut on the $p_T$ threshold.

The output of the coincidence-matrix is sent to the read-out part, and to the trigger output part of the chip. Before producing the trigger output, the trigger pattern is synchronized back to the 40MHz machine clock.

The coincidence-matrix chip will be designed in 0.25$\mu$m CMOS technology that has some desirable features for the design of the chip. The technology is radiation tolerant for the levels of neutron and gamma radiation (~10krad over 10 years) expected in the muon spectrometer [7]. In addition, the deep sub-micron technology allows the 320MHz working
frequency, necessary to maintain the design performances of the trigger.

5 Pad logic board

The information from two adjacent CM boards in the η projection and the information from the two corresponding CM boards in the φ projection are combined in the Pad Logic (PL) board. The Pad chip combines the low- and high-p_T trigger information in the η and φ projections, assigning track candidates to Rols. It also deals with the overlap inside the Pad region and tags possible ambiguities in case of more than one track in the region.

The Pad trigger logic is shown in Fig. 6. The logic works in pipeline mode at the machine clock frequency. The operations are performed in three pipeline steps.

The trigger logic produces a ten-bit output pattern. Eight bits are sent to the trigger Sector Logic, while the full ten bits are sent to the read-out. In case of more than one muon candidate in the Pad region, the logic transfers only the highest-p_T candidate and informs the level-2 trigger of the possibility of a second candidate using the ambiguity bits.

6 Sector logic

The Sector Logic (SL) combines the trigger results for one of the 64 sectors in which the barrel trigger system is subdivided. It is located in the USA15 underground counting room at a maximum distance of 80m (cable length) from the apparatus. Each SL board receives information from six optical links in the large sectors, and seven optical links in the small sectors.

The logic operates in pipeline mode at 40MHz in four clock periods. In the first clock period, the logic deals with the η overlap within the sector (overlaps between different sectors are solved by the MUCTPI). In the second and third clock periods, the logic sorts the two highest-p_T muon candidates. In case of more than two candidates, the SL retains the two highest-p_T tracks and flags that more than two candidates were found in the sector.
As output, the SL produces a 32-bit pattern that is sent synchronously, at 40MHz to the MUCTPI.

REFERENCES


1 INTRODUCTION

At LHC interesting physics in many cases will be indicated by the presence of muons in an event[1]. Examples are searches for new heavy particles with muons among the decay products. A muon with high $p_T$ could indicate such a decay. Another interesting topic to be investigated at LHC is the search for rare B-meson decays. The branching ratio for the decay $B^0 \rightarrow \mu \pi$ is predicted to be of the order of $10^{-9}$. Measuring a significant larger branching ratio would indicate new physics beyond the standard model. Searching for these events requires a trigger which is able to find muon pairs at relatively low $p_T$ thresholds.

These two examples motivate the strategy chosen by ATLAS for the first level (LVL1) muon trigger[2]: muon multiplicities at six different $p_T$ thresholds are used by the Central Trigger Processor (CTP) to form the trigger decision.

In order to quickly find muon candidates at different $p_T$ thresholds a set of trigger chambers [2][3](RPCs in the barrel region and TGCs in the Endcap region) will be installed in ATLAS in the region of the toroidal magnetic field. By correlating hits in the various planes of trigger chambers a measurement of $p_T$ with respect to the beam axis can be performed by the front end electronics[4][5][6].

The overall layout of the muon trigger system is shown in Figure 1. The detectors are logically divided into 208 sectors[7] for each of which the Sector-Logic (SL) finds the number of muon candidates at different $p_T$ thresholds for each bunch crossing (BC). The MUCTPI[2] collects muon candidates from all SL blocks containing information on their $p_T$ and their position. It forms the total muon multiplicities at the six different $p_T$ thresholds which are then sent to the CTP of the LVL1. Additional functions of the MUCTPI are to provide data to the LVL2 trigger and to the DAQ system for events selected at LVL1. The LVL2 trigger is sent a formatted copy of the information on candidate muon tracks. This information is used to define regions of interest (ROIs) that drive the LVL2 muon-trigger processing. An ROI is a region in the detector where activity merits further investigation by the LVL2 trigger. The information sent to the LVL2 trigger is ordered, according to decreasing in $p_T$. The DAQ system receives a more complete set of information, including in addition the computed multiplicity values.

2 SUMMARY OF REQUIREMENTS

A detailed list of the technical requirements for the MUCTPI can be found in [8] and [9]. In the following, a short summary of some of the main requirements is given, as needed for the understanding of the systems implementation.

- Some muons cross overlapping trigger chambers in such a way that hits are produced in both chambers. If the chambers belong to different sectors, the SL may send two muon candidates caused by the same particle to the MUCTPI. The MUCTPI must make sure that such candidates are counted only once in order to keep the fake rate of a low $p_T$ dimuon trigger at a tolerable rate. To do this it uses information indicating if a muon candidate has been found in a region where trigger chambers overlap.

- The SL can send up to two muon candidates per sector to the MUCTPI. In order to allow for some flexibility in forming the LVL1 trigger decision, two methods of forming the multiplicities have to be provided: for each
sector either all muon candidates are taken into account, or only the candidate with the highest $p_T$ contributes to the multiplicity calculation. The two options have to be independently programmable for each of the six $p_T$-thresholds.

- The maximum overall multiplicity that needs to be handled by the system is seven candidates. Larger multiplicity values are rounded down to seven.

- It must be possible to read out data from a programmable window of up to ±2 BCs width around the LVL1 trigger, in order to facilitate monitoring of activity in the trigger chambers shortly before and after the event which caused the trigger.

- Since the data received by the MUCTPI come from different parts of the detector the MUCTPI must align the incoming data in time, compensating for different times of flight and signal propagation delays, so that only data corresponding to the same bunch crossing are used to form multiplicities and for defining ROIs.

- The latency of the MUCTPI must not exceed eight BCs.

- The interface has to cope with an input data flux of 265 Gbits/sec (207 sectors send 32 bits at a rate of 40 MHz)

- The interface to the LVL2 trigger and the DAQ must operate without data loss up to a LVL1 trigger rate of 100 kHz.

- Sufficient online monitoring information must be provided in order to check the correct functioning of the MUCTPI during beam running and to facilitate fast localization and diagnosis of possible problems.

3 FUNCTIONAL PARTITIONING

The different functionalities of the MUCTPI are implemented in three types of 9U-VME modules which are connected via an active backplane. The functionality of the MUCTPI is shared by these system components as follows (see Figure 2):

- 16 so-called octant boards (MIOCTs) receive data corresponding to an octant in the azimuthal direction and half the detector in the $\eta$ direction. They form muon-candidate multiplicities for this region, correctly taking into account the overlap zones between barrel and end-cap sectors. There is no overlap between muon trigger chambers associated to different octant boards.

- The Muon Interface to the CTP (MICTP) contains the driver unit to the CTP.

- The Muon Interface to Read Out Driver (MIROD) drives, after some data formatting, data to the ROI builder of the LVL2 trigger and serves as the interface to the DAQ.

- All modules are connected via the Muon Interface Backplane (MIBAK). It contains two components: The active part (MIBAK 1) forms the total candidate multiplicities by adding the multiplicities of the MIOCT boards. The passive part (MIBAK 2) contains a bus system to transfer data from the MIOCTs and the MICTP to the MIROD.

3.1 The Octant boards

Sixteen Muon Interface Octant boards (MIOCTs) receive data from the SL. Figure 3 shows the block diagram of one octant board. After signals are received from the SL they are synchronized to the phase of the internal BC clock at the input of the MIOCT boards. A TDC is used to monitor continuously this synchronization. The alignment stage in the MIOCT boards is performed using configurable-length shift registers (range 0–15 BCs).

All the data received from the SL are stored in pipeline memories for the duration of the latency of the LVL1 trigger. In case of a LVL1 trigger (L1A), data is being read out of the pipelines by the derandomizers and written into the local readout buffer. A programmable window around the triggered BC can be defined. Up to ±2 bunch crossings around L1A can be read out.

Before data of the 16 octant boards can be sent via the internal backplane to the MIROD, a zero-suppression stage is needed in order to reduce the data rate to a tolerable level. Subsequently, data belonging to one L1A are formatted into a data package (with header and trailer) and buffered until they are read out via the backplane.
Figure 3: Blockdiagram of the MIOCT module

The multiplicity logic counts the number of muon candidates for each BC clock in the six different transverse-momentum classes taking account of possible overlaps between adjacent barrel sectors and barrel and end-cap sectors. This logic is implemented in FPGAs using lookup-tables and truth-tables. In order to test the system without relying on data from the SL, the input stage can be switched to a test RAM (256 x 32 bits) that can be loaded with an arbitrary test pattern via VME. Monitoring information is acquired from the system via its VME interface. In addition, VME is used to configure the FPGAs of the whole system. This allows for high flexibility even in the case when minor modifications are desired.

3.2 The backplane

The backplane of the system consists of two parts. The upper part (J1, J2, J0) is a standard VME backplane. The lower part (J3), called MIBAK, is a custom backplane designed to form multiplicity sums over the MIOCTs (MIBAK 1), to move data from the MIOCTs and the MICTP to the MIROD (MIBAK 2), and to distribute time-critical signals in the system. The backplane is implemented in ECL technology.

Each octant board drives six 3-bit sums corresponding to the six different transverse-momentum thresholds onto the backplane. With four stages of digital summing circuits the multiplicities of all octant boards can be formed and driven to the MICTP module (see below).

In order to transfer data from the MIOCTs and the MICTP to the MIROD, a simple one-directional 36-bit wide bus with high data throughput based on a token architecture has been developed. A simple handshake facilitates fast readout of all MIOCT buffers. The bus operates synchronously at 40 MHz.

Additionally the MIBAK is used to distribute time-critical control signals to the MICTP system. The backplane layout must make sure that these signals arrive at all relevant modules of the MICTP crate with a fixed phase with respect to the BC signal. This ensures that in all modules these signals are synchronized to the same bunch-crossing.

3.3 The interface board to the CTP (MICTP)

The MICTP collects the multiplicity sums for the six $p_T$ thresholds over the custom backplane, MIBAK, described in Section 3.2 below, and transmits them to the CTP. The MICTP is responsible also for distributing time-critical control signals to the rest of the MICTP system. Figure 4 shows a block diagram of the MICTP.

The multiplicity sums that are sent to the CTP are also stored in a pipeline memory. In case of a LVL1 trigger, data from the pipeline are stored in a derandomizer. These data are sent to the MIROD module over the MIBAK 2 backplane (see below).

In order to be able to test the CTP without relying on data from the MIOCT boards, the MICTP contains a programmable test-pattern RAM which can be multiplexed to the output drivers. Additionally a synchronization pattern can be driven to the CTP. This is used by the CTP to synchronize the input signals to the internal system clock.

For monitoring purposes, eight counters for each $p_T$ threshold count the occurrences of 0, 1, 2,...,7 muon candidates per bunch crossing. At the end of each LHC turn the contents of these counters are copied into a set of registers.
which can then be read via VME. At the same time the counters are reset.

The MICTP distributes the system clock to the rest of the MUCTP. Under normal operation this clock is the LHC BC clock. For test purposes, an internally-generated 40 MHz clock can be used instead. Five other time-critical control signals are sent to all modules of the system via the backplane: The signals ECR (event counter reset) and BCR (bunch counter reset) reset all local event and bunch counters. The L1A signal is distributed to all modules to indicate a valid LVL1 trigger; this signal initiates the transfer of data from the pipelines to the derandomizers. The signal labelled ‘sync_moni’ is used to synchronize the writing of monitoring information into dedicated buffers among all modules of the system, making it possible to investigate data belonging to the same L1A in all modules of the MUCTP by reading out via VME the dedicated buffers. The signal ‘sync_test’ is used to synchronously initiate the test cycle in which the octant boards are fed by the local test-pattern RAM.

In addition the MICTP monitors a BUSY line on the MIBAK backplane. Modules of the MUCTP can activate this line in case they cannot accept more L1A triggers because their internal buffers are nearly full. In case of an activated BUSY in the system, the MICTP drives a BUSY signal to the BUSY_ROD module, which handles all BUSY signals generated in ATLAS.

3.4 The interface board to the LVL2 trigger and to the DAQ (MIROD)

Figure 5 shows a block diagram of the interface board to the LVL2 trigger and to the DAQ. The MIROD module has to collect data from the octant boards and the MICTP before sending them to the region of interest builder of the LVL2 trigger and the ROB of the DAQ system. The data used by the LVL2 trigger for the RoI generation belong to a single BCID. Within the window of data which is sent to the DAQ, the time slice for the data sent to LVL2 can be programmed in the MIROD.

In the MIROD, a $p_T$ threshold can be programmed so that only muons exceeding this threshold will be sent to LVL2. In addition, it is possible to optionally take into account only the highest-$p_T$ muon candidate of each sector. The total number of muon candidates transferred is limited to ten. A flag indicates if, due to this limit, not all candidates are transferred. Candidates are ordered according to $p_T$ before they are sent, the highest-$p_T$ ones being sent first.

The MIROD module performs extensive checks regarding the consistency of the data packages received from the backplane. In order to facilitate the monitoring of data arriving in the module, a buffer is filled with part of the incoming data. To be able to test the LVL2 trigger system and the DAQ system from the MIROD onwards, it is possible to feed the MIROD with test-data from a programmable RAM.
4 LATENCY CALCULATION

The MUCTPI is designed such that it will not contribute more than eight BCs to the overall latency of the LVL1 trigger system. Figure 6 shows how the MUCTPI system components contribute to that latency. The latency estimates have been done on the basis of electronics components which are on the market today.

5 REFERENCES

2 ATLAS First Level Trigger TDR, CERN/LHCC/96-14, June 1998
6 Contribution of E. Petrolo to these proceedings.
7 P. Farthouat, Current Understanding of the Muon LVL1 System, version 2, ATLAS note DAQ-No–89, May 1998
Design study on the read out scheme of ATLAS Muon TGC is in progress. By analyzing requirements for the system, a star switch architecture is chosen. In this architecture, data links from slave modules are concentrated in a star switch, and then the switch and its master module are connected by a faster link. As for the slave to switch connection, a simple point to point communication protocol can be introduced which will reduce the size of the protocol logic circuit. Also, a broken slave can easily be disconnected at the switch, which brings system more reliable. A preliminary result of the system simulation using VHDL hardware description language is reported.

1. INTRODUCTION

The ATLAS endcap muon trigger chamber is ready to start construction. Also, a design work of the readout system is in progress. In preparation work of ATLAS Level 1 Trigger TDR[1], the architecture of the readout system is determined. In this report, first the outline of the architecture will be described, and then the present status of the detailed specification process will be given, in which VHDL hardware description language is introduced for simulation and realistic evaluation of the performance of the readout circuit.

The ATLAS endcap muon trigger chamber consists of 4,000 thin gap chambers (TGC) and forms a part of a big muon endcap wheel of 24 meters in diameter. Figure 1 shows the side view of the TGC system. Several TGC lay-
ers cover the forward region of eta from 1.05 to 2.40. A pair of chamber doublet stations (M2 and M3) are located behind of the MDT, and they produces trigger primitives for low Pt muons, and with a chamber triplet station (M1) in front of MDT, high Pt muon candidates are detected. All the wire and strip (r-phi) information must be read out together with the result of the trigger logic outputs.

2. READOUT SYSTEM ARCHITECTURE

In this section, the procedure is described how we determined the architecture of the readout system.

<table>
<thead>
<tr>
<th>LDB type</th>
<th>LDB octant</th>
<th>Slave boards</th>
<th>No. Channel</th>
<th>Hits/event</th>
<th>encoded (kBa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Doublet F</td>
<td>1</td>
<td>21</td>
<td>2652</td>
<td>0.11</td>
<td>65.0</td>
</tr>
<tr>
<td>E</td>
<td>6</td>
<td>19</td>
<td>2274</td>
<td>0.37</td>
<td>223.6</td>
</tr>
<tr>
<td>Triplet F</td>
<td>1</td>
<td>18</td>
<td>1461</td>
<td>0.07</td>
<td>41.0</td>
</tr>
<tr>
<td>E</td>
<td>3</td>
<td>24</td>
<td>2204</td>
<td>0.19</td>
<td>114.8</td>
</tr>
<tr>
<td>Inner F</td>
<td>1</td>
<td>6</td>
<td>288</td>
<td>0.20</td>
<td>120.2</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>3</td>
<td>252</td>
<td>0.13</td>
<td>75.8</td>
</tr>
<tr>
<td>Hi-PT F</td>
<td>1</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.1. Requirements

In order to clarify the requirement to the readout system, following features should be taken into account.

**Relatively small data rate**

Estimated hit rate is listed in Table 1. Less than 0.2 hits are expected per event for a local DAQ block which covers a certain area of readout channels as shown in Table 1. From this information, it is reasonable to introduce a serial communication mechanism with reduced number of signals.

**Distributed in wide area**

Slave modules which contain front end electronics and trigger logic circuit, are distributed on the chamber, and the distance among them becomes around 10m, where the cable delay is not negligible. It takes 100 ns to make a handshake between two devices. On the other hand, this means we have enough space to place connectors, cables or other staff.

**Access is allowed for maintenance**

The TGC forms a part of the endcap muon wheel. At the edge of the wheel, there will be provided powered crates for trigger and readout purpose. Access to these crates is relatively easy. Important components which needs maintenance should be placed here.

Under these conditions, the system must achieve the readout event rate of 100 kHz and latency of order 100μs for L2 trigger readout. According to discussion above, three kinds of scheme were considered for our basic architecture.

**Bus architecture**

It is necessary to control the traffic, because of the bidirectional nature. This means to have a handshake, like strobe and acknowledge, between modules. From the discussion above, it is not adequate.

**Ring architecture**

Connection can be formed in a unidirectional chain. The least number of connections is required in this architecture. Problem is once even only one module breaks, all the connection goes down. It is critical issue in the case where some components are not accessible.

**Star architecture**

As though this architecture requires a star switch or a some kind of multiplexor for traffic control as an additional component, slave modules are well isolated each other. A broken slave can be cut off without any disturbance to other slaves or the switch. As connection between a slave and the star switch is point-to-point one, protocol logic in slave becomes much simple.
From these considerations, we finally reached the conclusion to introduce the star switch architecture.

2.2. System Specification

According to the discussion in the previous section, outline of our system is fixed. We have four components for the readout system, namely, a slave module, a star switch, a local DAQ master and a readout driver. These components are connected each other by using two kinds of serial links and a bus. Figure 2 shows the schematic diagram of the system.

Slave Module
A slave module contains a level 1 buffer, a derandomizer and a slave link interface. In the present design, 128 signals are managed by one slave chip.

Star Switch
A star switch is a multiplexor module with a readout sequencer logic. It has up to 32 slave link interface connections and one link to a local DAQ master.

Local DAQ Master
A local DAQ master has an interface to the star switch and a buffer memory which will be read by a readout driver. This module will be located in USA15.

Read Out Driver (ROD)
ROD stays in the same crate with local DAQ masters and the data transfer between them will be done via the backplane bus.

There are two kinds of serial links to be introduced.

Local Slave Link
LVDS links connecting between slaves and switches. Three signals are allocated for one direction data transfer, 'Clock', 'Data' and 'Synch'. By adding 'Synch' signal, message decoder becomes very simple, which improves the reliability and reduces the size of the decoder logic substantially. Distance between the source and the destination is about 10 meters. In the present design, 40Mbps band width is supposed.

Optical Fiber Link
An optical fiber link connects a star switch with a master. This connection is one-to-one. The distance becomes around 80 meters. A faster bandwidth than the local slave link (~100Mbps) is expected for this link.

3. Design Procedure

As the architecture and the main staff are given, the next step is to provide a detailed specification of these staff. First, we start from a model analysis using VHDL hardware description language and then implement them on FPGA to verify the design at the hardware level.
3.1. VHDL Model Analysis

We started from the analysis of the slave module. Figure 3 shows how the function of a slave module is broken down into design units. Each ‘entity’, which is a term used in VHDL, is described in VHDL. In VHDL, one entity can have various implementation (‘architecture’). We started from implementation of a behavior model which is used for function simulation. Timing information used here is in a sense ideal because the propagation delay is not included. Even so, as we introduced a synchronous system architecture throughout the design, behavior of the model must be realistic as far as the system clock frequency stays in the acceptable range. This work is done using Workview Office VHDL tools[2]. In the figure 3, following design units are introduced; SIFU (Local Slave Link interface unit), MHDR (module header), BCCU (bunch crossing counter unit), L1CU (level 1 trigger counter unit), SLVU (slave unit), and MTRM (module terminator unit). The SIFU consists from CDEC (command decoder unit), DCTL (de-randomizer control unit), STWU (status word unit), and SOTU (output selector unit). The SLVU consists of LIBU (level1 pipeline), DRDU (de-randomizer with sparse data scan function), PSCU (parallel to serial converter). In this design, LIBU is a simple pipeline of 128 bit wide and 100 step deep. As it is required to record three contiguous bunch crossing data to check the timing at the test run stage, DRDU is a ring buffer of 384 bit (128 bit x 3) wide, 20 step deep(519,705),(908,963), with a write pointer and a read pointer, which are both controlled by DCTL.

Figure 4 is a very preliminary result of simulation which shows a hand shake sequence between a star switch and a slave module. First, the switch asks whether the module has data, and then if it has, triggers the data transfer. It takes 10 clocks, 250ns to receive a command and to reply to it including overhead of logic process in the current design. Another 100ns should be added due to the cable delay between the slave and the switch of order 10m. Thus, 350ns is necessary for data polling. For the hit data transfer, as expected hit rate is so small, minimum size of packets are transferred usually, which consists of (1)module address, (2)bunch crossing ID, (3)level 1 ID, (4)hit address, (5)hit pattern and (6)terminator, in total 48bits. As data transfer is accompanied with 4 clock long start command and 2 clock long overhead, so, 54 clocks, 1350ns is necessary for one transfer. In the case of the endcap triplet listed in table 1., the number of slaves to be scanned is 19 and the number of expected hit is 0.37. From these numbers, 350ns * 19 + 1350ns * 0.37 makes 7.05 μs. This satisfies the required trigger rate of 100kHz. The depth of the derandomizer is also calculated from the worst case consideration. If all the slaves have hits everywhere, the data packet has the maximum length of 304 bit equivalent, this gives 14.4 μs maximum latency in total. This means more than 15 steps are necessary for the derandomizer.

By using these designs, amount of required resources for logic implementation on devices can be estimated. In figure 4, though it is a very rough estimation, number of nets (connection between gates) and number of gates estimated are shown. This estimation is based one the synthesis using a specific FPGA library and not optimized for an ASIC design. Much reduced number will be expected in the actual ASIC design.

3.2. Prototyping Using FPGA

In the next step, we introduced a prototyping VME module which mounts several FPGA chips, as shown in figure 6. In this module, four XC3190A FPGA[3] chips are mounted and they can be configured, read and written
Slave Unit Gate Consumption

Total 115,988 Gates

44.6%

Slave Unit Net Consumption

Total 84,536 Nets

91.5%

Figure 5. Estimated amount of required gate resources for the slave module design. Net means the total number of connections among gates. Preliminary. LIBU128 means resources allocate for level 1 buffer, and so on.

from VME bus. The designs written in VHDL discussed above can be directly synthesized and converted into FPGA configuration data by tools supplied by the vendor. Synthesized data can be also used for gate level simulation in which realistic delay information is included, of course which depends on the technology selected. The configured data can be downloaded into actual devices and the design can be verified at the hardware level. This process is important, especially, for the test of interconnection in which LVDS or fiber-optic links are involved. Those performance must be confirmed in the realistic hardware situation.

4. SUMMARY

The star switch architecture is employed and the major components building up the architecture are defined. A detailed design using VHDL language has been started and the feasibility of the architecture is confirmed. Required gate resources for ASIC is roughly estimated and the result is acceptable one. As the next step, an FPGA module is introduced to perform design verification at the hardware level.

Design of the star switch and the local DAQ master in VHDL will be done next. Using FPGA prototyping modules and LVDS and optical-fiber links modules, a demonstrator set up will be provided to confirm the scheme. Furthermore, various features for diagnostics or parameter downloading should be included and tested according to

Figure 6. VME module introduced for prototyping. This module has four XC3190A, two CPLD for VME interface and clock control.

the user requirement document which will be prepared in a few month. These designs will be ported into the ASIC design in 1999.

REFERENCES

[3] XC3000 Series Field Programmable Gate Array, V3.0 11/97, XILINX Inc.
Local Track Reconstruction for the First Level Trigger in the CMS Muon Barrel Chambers

INFN, Padova, Italy (email: Pierluigi.Zotto@padova.infn.it)

1) Now at Universidade do Algarve, UCEH, Gambelas, Faro, Portugal
2) Also at Dipartimento di Fisica, Politecnico di Milano, Milano, Italy

Abstract

The CMS muon chambers were designed to be a self-triggering device, using an algorithm which provides a rough track reconstruction like in the traditional Level-2 triggers. The track fitting dedicated ASIC devices were designed and have already been produced. A detailed description of their architecture and performance is given.

1. INTRODUCTION

The proposed CMS first level muon trigger primitive generator is a multistage scheme. The front-end trigger device is called Bunch and Track Identifier (BTI): it performs a rough track reconstruction and uniquely identifies the parent bunch crossing of the candidate track by means of a generalized mean-timer technique [1]. The device was realized and prototypes were recently tested.

The BTI is followed by a Track Correlator (TRACO) that is required to associate portions of tracks in the same chamber combining groups of BTIs among them. The TRACO enhances the angular resolution and produces a quality hierarchy of the triggers.

Its introduction is necessary since the BTI is intrinsically noisy and therefore a local preselection and a quality certification of the BTI triggers is required. The TRACO design is completed and submitted for prototype production.

TRACO triggers are transmitted to the chamber Trigger Server (TS) [2]: the TS of the transverse view selects two tracks (looking for the lowest bending angle) among all tracks transmitted by the TRACOs; the TS of the longitudinal view sends the wired-or of the BTI trigger outputs to TRACOs for trigger qualification purposes and codes the triggers in a 32 bits string giving all the tracks pointing to the vertex with a position resolution of 8 cm.

The trigger information is transmitted to the Muon Regional Trigger using optical links.

2. DESCRIPTION OF BTI

The Bunch and Track Identifier was studied to work on groups of four layers of staggered drift tubes called Super Layers (SL). A muon barrel chamber is composed of two SL in the CMS transverse plane and one SL in the longitudinal one. Each SL is equipped with BTIs: thus we position and direction of tracks crossing any SL is measured. Each BTI is connected to nine wires allocated as shown in Figure 1.

The parameters actually computed by the BTI are the angular k-parameter \( k = h \tan \psi \) and the crossing position in the SL center. The geometrical quantities involved are shown in Figure 1: \( \psi \) is the angle of the track with respect to the normal to the chamber plane and \( h = 1.3 \text{mm} \) is the distance between the wire planes.

The BTI track finding algorithm computes in parallel several track patterns hypotheses: a pattern is identified from a sequence of wire numbers and labels stating if the track crosses the tube on the right or on the left of the given wire (e.g. in Figure 1 the track corresponds to the pattern \( 5L3R6L4R \)). Any given pattern includes six pairs of planes (AB, BC, CD, AC, BD, AD), each one providing a measurement of the position (through an \( x\)-equation) and of the k-parameter (through a \( k\)-equation) of the track. The definition and the full list of the preloaded patterns is available in [3].

The value of a \( k\)-equation is proportional to the sum or the difference of the hits arrival time of each pair of planes and corresponds to a rough measurement of the track direction. This value is generally time dependent. Each pair included in a pattern gives its own measurement of the track direction: the hits are aligned when, after applying a pair dependent proportional factor, the values of the k-parameter of each pair are equal.

Hence at every clock cycle all \( k\)-equations are computed and a BTI trigger is generated if at least three of the six k-parameters associated to any of the patterns are in coincidence. The tolerance on the coincidence of the \( k\)-equations is defined according to the resolution of each pair, that in turn depends on the distance between the wires and was chosen to allow a maximum cell linearity error equivalent to 25ns. This coincidence allows the bunch crossing identification owing to the time-dependence of the \( k\)-equations value.

![Figure 1 - Allocation of BTI input channels.](image-url)
If there is a coincidence of all the six k-parameters, the trigger corresponds to the alignment of four hits and it is marked as High Quality Trigger (HTRG), while in any other case, with a minimum of three coincident k-parameters, it is due to the alignment of only three hits and it is marked Low Quality Trigger (LTRG).

If several track patterns give a response, the HTRG is chosen as the triggering track pattern. If there is more than one HTRG or the triggers are all LTRGs, the first one, in an arbitrarily defined order, is selected.

The computed parameters, coded in 6 bits and accompanied by a TRG signal and a quality signal marking H or L, are transmitted with fixed delay with respect to the parent bunch crossing time, thus permitting its identification. The total latency of the BTI is determined by the maximum drift-time to the wires, $T_{\text{MAX}}$, plus 4 clock cycles needed for input signal synchronization and BTI calculations. For a nominal drift velocity of 50 $\mu$m/ns the delay of the TRG signal with respect to parent crossing is 20 bunch crossings.

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 $\mu$m/ns and a sampling frequency of 80 MHz, the angle is measured with a resolution better than 60$\mu$rad, while the position is measured with a resolution of 1.25mm. The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

With the present geometric parameters of the chamber, the angular acceptance is nominally $\psi_{\text{MAX}} = \pm 45^\circ$, although the device works with reduced efficiency till $55^\circ$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

3. TRACO DESCRIPTION

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTIs connected to it and tries, linking the inner layer triggers to the outer layer triggers, to find the pair of BTI track candidates that fits the best track.

The number of BTIs connected to a TRACO is pad-limited and it is determined by the acceptance requirement. The present design connects four BTIs of the inner SL to twelve BTIs of the outer SL allocated as shown in Figure 2, ensuring a full coverage until $\psi_{\text{MAX}}$.

The algorithm starts selecting, among all the candidates in the inner SL and the outer SL independently, the best track segment, according to preferences given to the trigger quality (H/L) and to the proximity to the radial direction to the vertex (i.e. its $\phi$).

Then it computes the k-parameter and the position of a correlated track candidate. The compatibility between the k-parameters of the portions of track selected in the inner and outer SLs and the correlated track is checked against a programmable tolerance.

The internal parameters computed for the correlated tracks are:

$$k_{\text{COR}} = \frac{D}{2} \tan \psi = x_{\text{inner}} - x_{\text{outer}}$$

$$x_{\text{COR}} = \frac{(x_{\text{inner}} + x_{\text{outer}})}{2}$$

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 $\mu$m/ns and a sampling frequency of 80 MHz, the angle is measured with a resolution better than 60$\mu$rad, while the position is measured with a resolution of 1.25mm. The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

With the present geometric parameters of the chamber, the angular acceptance is nominally $\psi_{\text{MAX}} = \pm 45^\circ$, although the device works with reduced efficiency till $55^\circ$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

3. TRACO DESCRIPTION

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTIs connected to it and tries, linking the inner layer triggers to the outer layer triggers, to find the pair of BTI track candidates that fits the best track.

The number of BTIs connected to a TRACO is pad-limited and it is determined by the acceptance requirement. The present design connects four BTIs of the inner SL to twelve BTIs of the outer SL allocated as shown in Figure 2, ensuring a full coverage until $\psi_{\text{MAX}}$.

The algorithm starts selecting, among all the candidates in the inner SL and the outer SL independently, the best track segment, according to preferences given to the trigger quality (H/L) and to the proximity to the radial direction to the vertex (i.e. its $\phi$).

Then it computes the k-parameter and the position of a correlated track candidate. The compatibility between the k-parameters of the portions of track selected in the inner and outer SLs and the correlated track is checked against a programmable tolerance.

The internal parameters computed for the correlated tracks are:

$$k_{\text{COR}} = \frac{D}{2} \tan \psi = x_{\text{inner}} - x_{\text{outer}}$$

$$x_{\text{COR}} = \frac{(x_{\text{inner}} + x_{\text{outer}})}{2}$$

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 $\mu$m/ns and a sampling frequency of 80 MHz, the angle is measured with a resolution better than 60$\mu$rad, while the position is measured with a resolution of 1.25mm. The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

With the present geometric parameters of the chamber, the angular acceptance is nominally $\psi_{\text{MAX}} = \pm 45^\circ$, although the device works with reduced efficiency till $55^\circ$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

3. TRACO DESCRIPTION

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTIs connected to it and tries, linking the inner layer triggers to the outer layer triggers, to find the pair of BTI track candidates that fits the best track.

The number of BTIs connected to a TRACO is pad-limited and it is determined by the acceptance requirement. The present design connects four BTIs of the inner SL to twelve BTIs of the outer SL allocated as shown in Figure 2, ensuring a full coverage until $\psi_{\text{MAX}}$.

The algorithm starts selecting, among all the candidates in the inner SL and the outer SL independently, the best track segment, according to preferences given to the trigger quality (H/L) and to the proximity to the radial direction to the vertex (i.e. its $\phi$).

Then it computes the k-parameter and the position of a correlated track candidate. The compatibility between the k-parameters of the portions of track selected in the inner and outer SLs and the correlated track is checked against a programmable tolerance.

The internal parameters computed for the correlated tracks are:

$$k_{\text{COR}} = \frac{D}{2} \tan \psi = x_{\text{inner}} - x_{\text{outer}}$$

$$x_{\text{COR}} = \frac{(x_{\text{inner}} + x_{\text{outer}})}{2}$$

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 $\mu$m/ns and a sampling frequency of 80 MHz, the angle is measured with a resolution better than 60$\mu$rad, while the position is measured with a resolution of 1.25mm. The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

With the present geometric parameters of the chamber, the angular acceptance is nominally $\psi_{\text{MAX}} = \pm 45^\circ$, although the device works with reduced efficiency till $55^\circ$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

3. TRACO DESCRIPTION

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTIs connected to it and tries, linking the inner layer triggers to the outer layer triggers, to find the pair of BTI track candidates that fits the best track.

The number of BTIs connected to a TRACO is pad-limited and it is determined by the acceptance requirement. The present design connects four BTIs of the inner SL to twelve BTIs of the outer SL allocated as shown in Figure 2, ensuring a full coverage until $\psi_{\text{MAX}}$.

The algorithm starts selecting, among all the candidates in the inner SL and the outer SL independently, the best track segment, according to preferences given to the trigger quality (H/L) and to the proximity to the radial direction to the vertex (i.e. its $\phi$).

Then it computes the k-parameter and the position of a correlated track candidate. The compatibility between the k-parameters of the portions of track selected in the inner and outer SLs and the correlated track is checked against a programmable tolerance.

The internal parameters computed for the correlated tracks are:

$$k_{\text{COR}} = \frac{D}{2} \tan \psi = x_{\text{inner}} - x_{\text{outer}}$$

$$x_{\text{COR}} = \frac{(x_{\text{inner}} + x_{\text{outer}})}{2}$$

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 $\mu$m/ns and a sampling frequency of 80 MHz, the angle is measured with a resolution better than 60$\mu$rad, while the position is measured with a resolution of 1.25mm. The angular resolution of LTRGs is track pattern dependent and is generally worse than the one of HTRGs.

With the present geometric parameters of the chamber, the angular acceptance is nominally $\psi_{\text{MAX}} = \pm 45^\circ$, although the device works with reduced efficiency till $55^\circ$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

Only one track per bunch crossing per BTI is forwarded to the TRACO.
The angular resolution of a correlated track candidate is 10 mrad for the nominal drift velocity, thus improving the BTI value, while the resolution of the position remains unchanged.

These parameters are converted, using a programmable look-up table, to the chamber reference system: position is transformed to radial angle $\phi$ and k-parameter to bending angle $\phi_0$ as defined in Figure 3. The chosen track is forwarded to the chamber TS, for further selection.

If the correlation fails the correlator forwards an uncorrelated track following a preference list that includes the parent SL (IN/OUT) and the quality bit (H/L) of the two tracks selected for correlations.

If no correlation is possible since there is no candidate in one SL, the uncorrelated track is still forwarded.

The track is output on a bus, using 10 bits for the bending angle and 12 bits for the radial angle and it is accompanied by three quality bits identifying HH, HL, LL, H0, H0, L1, L0 track candidates with obvious symbols meaning.

A further preference selection can be activated to connect the trigger generated in the transverse view to the triggers generated from the BTIs in the longitudinal view. In particular, since the noise generated from the BTI algorithm is of LTRG quality, a programmable coincidence between the two views is foreseen to certify the uncorrelated LTRGs.

In order to allow the identification of two muons inside the same correlator, the same algorithm is applied twice to the data received from the BTI. Therefore sometimes a second track is forwarded to the chamber TS. The programmability of the preferences for the choice of the First Track and the Second Track are completely independent, although we believe that the same criteria should apply.

A further selection is needed in the case that more than one TRACO inside a chamber give a trigger. The communication between the TRACOs and the chamber TS to allow this decision is done using a PREVIEW information, in order to minimize the time needed for calculations of the whole trigger chain. A copy (called PREVIEW) of one of the candidates chosen for correlation is sent to the TS according to the programmed H/L and IN/OUT selection flags, before starting any correlation calculation. The TS selection is based on the quality of the PREVIEW (given by the BTI resolution) of the various candidates.

The block scheme of the TRACO implementation, as previously described, is given in Figure 4. The TRACO calculations use 6 bunch crossings.

4. TRIGGER PERFORMANCE

The correlator algorithm was implemented in the standard CMS software including all the possible programmation choices. Several studies using the full GEANT simulation of the detector were done to see the effect on noise reduction and trigger efficiencies according with the programmation parameters in order to decide their default values.

4.1 Noise generation mechanisms

The design of the devices included in the trigger chain was done with the purpose of providing a robust and efficient system. Unfortunately the way to meet these requirements introduces a certain number of redundancies in the system causing a non negligible fraction of false or duplicated triggers.
Figure 5 - Sketch of the generation mechanism of temporal noise inside the BTI.

The BTI trigger algorithm can actually work requiring only three layers of staggered tubes. The drawback of this kind of choice is the fact that an inefficiency or a bad measurement on any of the cells becomes an inefficiency or a wrong trigger. The introduction of the fourth layer enhances the efficiency and reduces the wrong measurements. But some spurious alignments of three hits can occur at any bunch crossing, depending on the track position and direction.

Most of the bad alignments are generated from the unavoidable left-right ambiguity even at several bunch crossing distance from the alignment of the four hits.

An example of the mechanism is shown in Figure 5, where a real track orthogonal to the chamber is displayed and the hit positions are marked with small circles on the track line. The BTI, looking for alignments of at least three hits, is able to find the alignment corresponding to the real track, but other two tracks are detected. These tracks, called ghost tracks, correspond to alignments of a mixture of real hits and their mirror images. Infact the BTI supposing that wire 2 is inefficient and that the signal of wire 4 comes from the right side of the tube, finds a false alignment at time $\Delta t_1$ after the right bunch crossing. In the same way, supposing that wire 5 is inefficient, the BTI finds another ghost track, formed from the signals of wires 2 and 4 and the mirror image of signal from wire 3, at time $\Delta t_2$ after the right bunch crossing.

Let’s call noise of type I the ghosts generated by this mechanism.

In order to be fully efficient the trigger system provides some overlap between adjacent devices: one BTI is overlapped by five cells to its neighbours and BTIs in the outer SL are always assigned to three consecutive TRACOs.

The overlap between BTIs is compulsory to obtain the needed angular acceptance. Furthermore it reduces the impact of the loss of one device on the trigger efficiency, since the remaining one can be programmed to at least partially cover the dead area switching on some redundant patterns.

Unlike it is not possible to define a set of completely non-redundant patterns and therefore some of them are available in two consecutive BTIs: in fact there are five redundant patterns generating LTRGs on the devices close to the one generating the HTRG at the same bunch crossing.

In figure 6 we see a case where a valid HTRG pattern in one BTI is also seen as a valid LTRG pattern in the adjacent one.

Therefore the TRACO will have the chance to make a choice between candidate tracks in adjacent BTI’s that are images of the same track, carrying exactly the same information. The First Track sorting will perform correctly, but it may result that the TRACO is forwarding the same track twice, with a chance of losing other available candidates. This is called noise of type II.

The BTIs in the outer sorter are assigned to three consecutive TRACOs, being in the left, the central or the right group. This is another cause of noise generation (noise of type III). Since the TRACO is designed for a wide acceptance and must have some reasonable tolerance to be enough efficient, the candidate tracks can point to more than one TRACO as shown in Figure 7. Therefore, as in the case of adjacent BTIs, adjacent TRACOs can forward to the TS twice the same track. Again this fact may introduce a bias in the Second Track selection at the TS level where all TRACOs are put together.

Figure 6 - Sketch of the spatial noise due to BTI overlap.

Figure 7 - Sketch of spatial noise due to TRACO overlap. The figure on the right reports at the same origin the angular acceptance of each TRACO on the left.
4.2 Noise reduction methods

We have seen that there is a temporal noise, due to left-right ambiguity (noise of type I), that generates ghost tracks at wrong bunch crossings and spatial noise caused either by redundancy of the BTI equations (noise of type II) or by the overlap of the BTI acceptance ports (noise of type III), generating copies of the same track.

Some filters have been provided to reduce the overall importance of these effects in case the generated background will prove to be not tolerable once on site.

In order to reduce the type I noise we introduced a temporal Low Trigger Suppression: the low quality tracks (LL,LO,L1) are canceled if a HTRG occurred within the neighbouring bunch crossings. This suppression is applied at bunch crossings -1 to +8 with respect to any HTRG within the BTI, while it is also possible to suppress triggers at bunch crossings from -1 to -4 with respect to any HTRG inside the TRACO, without any latency addition.

Spatial noise can affect only the Second Track selection. It is possible to avoid sending twice the same track using a geometrical suppression filter. If a HTRG was selected in the First Track sorting operation, all the LTRG in the neighbouring BTIs are removed from the Second Track sorting list. This filter, always active, acts on type II noise. A similar procedure inhibiting Second Track LTRG selection can be applied to neighbouring TRACOs inside chamber TS to remove type III noise.

There is another possible cut to be applied to clean the TRACO output: a programmable tolerance window is implemented for the bending angle. This filter makes use of the fact that after traversing the coil any track will bend back, since it will find an opposite sign magnetic field. The bending angle as a function of momentum at all the muon stations is shown in Figure 8. Indeed there is a large spread for the average bending values at stations one and two, while it is close to zero at station three. Energy loss causes an overbending of low momentum muons at station four.

We cannot safely apply any cut in the first and second

![Figure 8 - Average value of the bending angle at the CMS four barrel muon stations for different muon pT.](image)

4.3 Efficiency studies

A large number of simulations was performed to check the trigger performance. The most interesting results are the ones concerning the temporal noise distribution and the trigger efficiency in various configurations.

Figure 9 shows the temporal distribution of HTRGs and LTRGs at the BTI output. While the HTRGs are a

![Figure 9 - Time distribution of BTI output triggers for different quality categories. The correct bunch crossing is shaded.](image)

station, while an acceptance window on the bending angle can be used for station 3 and/or 4.

![Figure 10 - Time distribution of TRACO output triggers for the different quality categories. The correct bunch crossing is shaded.](image)

4.3 Efficiency studies

A large number of simulations was performed to check the trigger performance. The most interesting results are the ones concerning the temporal noise distribution and the trigger efficiency in various configurations.

Figure 9 shows the temporal distribution of HTRGs and LTRGs at the BTI output. While the HTRGs are a

![Figure 11 - Efficiency and noise for station 1 as a function of muon pT for different trigger configurations.](image)
Figure 12 - TRACO efficiency versus the angle of incidence for all trigger (solid line), correlated tracks (dashed line) and uncorrelated tracks (dotted line).

clean signal we see that the LTRGs are distributed around the correct bunch crossing and therefore needs to be adequately certified.

Figure 10 shows the time distribution of the different categories of triggers output from the TRACO. Categories including at least one HTRG are again quite clean, while the other categories are badly identifying bunch crossing.

The single station efficiency, corrected for acceptance, of the trigger for few different choices of the noise reduction algorithms is reported in Figure 11. We conclude that we have means of reducing the noise with negligible efficiency loss.

Figure 12 shows the efficiency as a function of the angle of incidence for the relative fractions of correlated and uncorrelated tracks: the correlated triggers dominate till 45° as expected from TRACO acceptance design.

Table 1: Effect of bending angle cut on efficiency and noise at station 4

<table>
<thead>
<tr>
<th>$\Phi_b$ cut</th>
<th>Efficiency</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>51.6</td>
<td>98.0%</td>
<td>102%</td>
</tr>
<tr>
<td>43.5</td>
<td>97.0%</td>
<td>83%</td>
</tr>
<tr>
<td>32.3</td>
<td>96.8%</td>
<td>72%</td>
</tr>
<tr>
<td>17.5</td>
<td>95.1%</td>
<td>56%</td>
</tr>
<tr>
<td>9.0</td>
<td>76.2%</td>
<td>34%</td>
</tr>
</tbody>
</table>

Table 1 shows the effect of the bending angle cut on efficiency and noise for $p_T = 8\text{GeV}/c$ tracks.

5. PRESENT STATUS

While the TRACO has been completely designed and submitted for a test production, a sample of BTIs was already produced, mounted on board, tested on bench and on a muon beam.

The benchmark was composed by a 40K sample of hits generated using the full GEANT simulation of single muons in front of a BTI in order to have a realistic spectrum of the input data.

The efficiency as a function of the angle of incidence is reported in Figure 13, showing that we have a flat response till 45°, while efficiency is rapidly falling till 55°, matching our design expectations.

Figure 14 - Test beam result on angular and position resolution for different trigger quality categories of 80 GeV/c muons at normal incident angle.

The beam test was quite recent (end of August 1998), but apparently it was successful. As an example of the BTI performance in Figure 14 we show the angular and position resolution obtained for 80 GeV/c muons at normal incidence.

REFERENCES

Abstract

A high speed and high throughput (1.3 Gbyte/s) programmable Pattern Unit has been implemented in a single 6U VME board. Such a device represents a basic tool for testing the high throughput devices that are adopted in trigger and readout systems of LHC experiments.

1. MOTIVATIONS

The current phase of research and development of trigger electronics for the CMS experiment at LHC includes the design of complex electronics systems, based on custom-made digital ASIC devices. This implies the production and subsequent tests of ASIC prototypes. The main requirement, in order to perform standalone test of such prototypes, is to dispose of a Pattern Unit, i.e. an input-output device, fulfilling the following constraints:
- large number of I/O channels (>100);
- clock rate multiple of LHC rate (40/80...MHz);
- clock – I/O synchronisation;
- pre-storage/readout of I/O patterns.

At the INFN section of Bologna, when we started working on this project, we immediately realised that with a small additional design effort a more general purpose tools, allowing to test trigger electronics and readout systems in a real-time set-up (typically a test beam), would be achieved. For such a device some of the additional constraints are:
- external clock in the range 0-80 MHz;
- external control signals: Start/Abort/Clear...
- mixed standard ext. signals: NIM/ECL/TTL...
- event counting;
- interrupt generation.

With this target in mind we developed a programmable 6U VME board (one slot) which is able to generate and readout up to 16 Kwords on 128 I/O channels at 80 MHz.

2. FUNCTIONALITY

2.1 Main features

I/O channels are based on 8 independent FIFOs (CY7C42x5), each chip handling 16-bit words. All FIFOs work in parallel, i.e. with the same clock, and can be configured as input or output-FIFOs individually. Read and write operations are allowed in fully asynchronous and simultaneous access through front-panel connectors and VME bus. Therefore the Pattern Unit can work either as a Pattern Generator or a Readout Buffer of “events”, or perform both functions simultaneously in a single board. The latter configuration gives advantages and is typically suitable when testing prototypes of synchronous devices. A pattern unit event represents a word containing up to 128-bits, as multiple of 16-bits. The total number of events to handle is controlled through a pre-settable event counter ranging from 0 to 16 Kevents. The event counting begins when a Start signal is issued and stops when the countdown reaches zero or when an abort signal is generated. This working mode is called “data sequence”. Another feature, useful for testing purposes, is to make the event counter working in “continuous loop” mode: the FIFO address pointer is automatically reset to zero after reaching the end of transmission condition (full/empty FIFO), i.e. input-FIFOs are virtually never full and output-FIco$s are never empty. As a general feature, input-FIFOs ignore events when they are full, while output-FIFOs don’t forward events when they are empty. A Clear signal is necessary to empty input or output-FIFOs. The event flow has a maximum I/O clock rate of 80 MHz.

The board clock can be provided either internally or by an external signal. Some high-resolution delay lines are adopted in order to distribute the clock signal, differently for input and output-FIFOs. This allows keeping synchronization among I/O patterns and intermediate device, for example a chip under test, is placed between input and output-FIFOs.

Since the Pattern Unit has been conceived not only as a laboratory-testing tool but also as a real-time device, it can be adopted in experimental environments like a test beam set-up. For this reason all asynchronous control signals necessary for a “run” (Start, Abort, Clear) can be issued via front-panel LEMO-00 type connectors. In addition, a Gate signal, representing a temporal window of valid clocks, is also available.

Most configuration options for the pattern unit working-mode, as well as the board status, can be fully controlled through VME. A dedicated JTAG bus (4 lines) is also available for external chip programming.

2.2 Usage examples

As already said the Pattern Unit can work either as a Pattern Generator of events or a Readout Buffer, or perform both functions simultaneously. Let’s consider the first application. In this case some or all FIFOs are configured as Output, and a given number of patterns

G.M. Dallavalle, I. D’Antone, I. Lax, A. Montanari and F. Odorici (email: odorici@cern.ch)
I.N.F.N. Bologna
can be loaded into the FIFOs via VME. After pre-setting the event counter (VME register), the Start command (either VME or external) allows a given pattern sequence to be sent to the output connector, at a given clock rate. Only an Abort or a Clear (either VME or external) can interrupt the sequence. The Abort stops the event counter (if it is running) and (normally) re-initializes it to zero. If a Clear is issued also the internal FIFO pointers are reset to zero, unless the "Continue" mode is set. In this case, at the next Start, the readout of the FIFO continues from where it previously ended. The Continue mode allows therefore to readout the FIFO content as "data packets". When Continue mode is not set, Clear resets the FIFO pointers but the data content is still valid and readable. If the event counter runs for a number of events greater than the number of words loaded into the FIFO, then the output word will always be the last pattern loaded.

When the board is used as a Readout Buffer some or all FIFOs are configured as Input. After pre-setting the event counter, the Start command allows a given pattern sequence to be written into the FIFOs through the front-panel input connectors. An Abort or a Clear command can interrupt the writing sequence before the event counter reaches the preset number of events. While the Abort simply stops the event counter and reset it to zero, the Clear command acts as the Abort but also re-initializes the FIFO pointers to zero and cancel the FIFO data content. The Continue mode doesn't affect the input-FIFOs behavior. The FIFO readout is done via VME: the same number of words written on the FIFO can also be read, until the FIFO is empty. If the VME readout exceeds the number of words written into the FIFO, always the last written word will be received.

As a general feature, if a Start is issued during a run (i.e. before the event counter is arrived at zero), it is ignored. Input-FIFOs that are full ignore next events. Output-FIFOs that are empty always give the last loaded event. After a Clear all output-FIFOs give zero on the output bus. For the Start and Clear commands an enable-mask allows to decide which FIFO will be affected by the above signals. The event counting can work in "Loop" mode: the FIFO address pointer is automatically reset to zero after reaching the end of transmission condition (full/empty FIFO), i.e. input-FIFOs are never full and output-FIFOs are never empty.

2.3 Synchronisation

Several synchronization aspects have been taken into account in the design of the board:
- clock-vs-data;
- clock-vs-control signals;
- data-vs-data;
- board-vs-board.

In practice all these aspects have been overcome by including on board programmable delay lines, which allow adjusting the phase among different signals. Two delay lines are inserted on the clock paths associated to the input- and output-FIFOs respectively. In this way clock-vs-data synchronization can be tuned within a 5-bit range, i.e. with a granularity of about 7% per step.

A third delay line is inserted on one of the front-panel control signals, typically the Start, to adjust the phase with respect to the clock.

The necessity to obtain a given data-vs-data synchronization could occur for example when some FIFOs are used as control lines of a given (external) device, while other FIFOs are used as data receiver or transmitter. In this case, control lines will probably change at a lower rate than I/O data. That can be easily achieved via software, by writing the same control patterns into consecutive FIFO locations.

When two or more pattern unit boards are chained together, a board-vs-board synchronization can be obtained on each board by taking as input the output clock provided by the previous board of the chain, and also by adjusting the on board delay lines associated to input- or output-FIFOs.

For an application that needs more than 128 I/O channels, two or more boards can be configured to work in parallel. This requires a board-vs-board synchronization that can be easily achieved by feeding the same clock to all boards. Moreover, all boards' delay lines are programmed to add some extra delay, so that a fine phase tuning can be obtained on each board.

3. CONTROL AND CONFIGURATION

3.2 VME control registers

Most of the board controls and setting, as well as the VME interface, are implemented or handled through an FPGA device (XC3195) so that further functional features can be added in future. The 4 JTAG lines correspond to individual VME registers. The VME access is a standard 32-bit addressing with 16-bit data. The list of VME control registers is reported in Table 1.

<table>
<thead>
<tr>
<th>Registers</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (w-only)</td>
<td>FIFO Configuration: Input/Output</td>
</tr>
<tr>
<td>1 (r-only)</td>
<td>FIFO Status: I/O: empty/full</td>
</tr>
<tr>
<td>8 (r/w)</td>
<td>FIFO data access</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Run Mode: Sequence/Loop/Data-blocks</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Run Status: running/paused</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Event counter</td>
</tr>
<tr>
<td>4 (r/w)</td>
<td>VME signals: Start,Abort,Clear,HWReset</td>
</tr>
<tr>
<td>3 (r/w)</td>
<td>VME signal enable-mask (1-bit/FIFO)</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Front-panel I/O enable: 3-state/active</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Front-panel signal enable</td>
</tr>
<tr>
<td>1 (r/w)</td>
<td>Delay lines programming</td>
</tr>
<tr>
<td>4 (r, w)</td>
<td>JTAG lines</td>
</tr>
</tbody>
</table>
3.3 Front-panel signals

The 128 I/O signals are TTL levels (or TTL differential by inserting adapters), arranged on 4 x 40-pin connectors. All control signals are fed through LEMO-00 type connectors, as TTL, NIM and ECL logic levels. The input clock can be accepted also as a PECL level. The input signals are Clock, Start, Abort, Clear and Gate. The only output signal is the Clock, which can be used to synchronize further boards. An 8-pin connector is provided for handling JTAG signals. Some LEDs are placed on the front panel for a visual check of the FIFOs I/O configuration.

3.4 Jumpers' setting

The board has several jumpers on it which, during an application, are normally configured as a “definitive” setup. Some of them are worth to be mentioned:
- the internal or external clock selection;
- the “routing” of the clock lines, which has to be defined according to the needed delay lines;
- control signals level selection (TTL, NIM ...);
- each input line can be terminated with on-board resistors (pull-down and/or pull-up) in order to properly match the cable impedance;

3.5 Software programming

The aid of a control program is necessary for several reasons. Firstly in order to read/write the VME registers dedicated to the board configuration and in order to get access to the FIFO data locations; secondly to test the board functioning and also to determine the proper delay lines configuration, for example through automatic algorithms based on reference sequences.

4. CURRENT APPLICATIONS

4.1 Standalone test of ASIC prototypes

The first application of the Pattern Unit was for a standalone test of the “Track Sorter Slave” (TSS) ASIC prototype (Bologna, May 1998, see A. Montanari’s talk in these proceedings). For this custom-made digital CMOS device the nominal clock rate is 40 MHz. The chip needs to get 4 input words of 10-bits each and 10 control signals. It gives a 10-bit output word. We therefore used 4 FIFOs to provide the ASIC input data, one FIFO to handle the control lines and one FIFO to get the ASIC output data. We mounted the ASIC device on a very simple “connection board” which has been located as close as possible to the Pattern Unit. The link between the two boards was done via standard 0.5 pitch flat cables (100 Ohm) 30 cm long, properly terminated at their ends. We used an external 40 MHz TTL clock, connected to both the Pattern Unit and the ASIC device. Transmitting and receiving FIFOs were phased with the clock through two on board delay lines (2nsec/step, 5-bit range).

The chip behavior was verified with input test patterns and the output compared to the wanted data. Once the right behavior of the ASIC was proved, the chip processing speed was determined by increasing the clock rate until wrong data started to appear (about 70 MHz in this case). By using the JTAG registers available on the Pattern Unit, also the JTAG logic that is part of this ASIC prototype has been verified.

4.2 Real time test of ASIC prototypes

The next application of the Pattern Unit was a real time test of the “Bunch and Track Identifier” (BTI) ASIC prototypes (CERN, August 1998, see P. Zotto’s talk in these proceedings). Also these CMOS digital devices are custom-made and the nominal clock rate is 80 MHz. In this case the chip test was combined with the test of other objects involved in a quite complex trigger system of a test-beam data taking. Inputs to the ASICs were real data and only the ASIC output words were recorded. All 128 channels of a Pattern Unit were used to get data in phase with an external PECL clock at 80 MHz. The clock was left free running and a start to the data acquisition was given by an external NIM signal, provided by the trigger logic. The start was properly synchronized to the clock through an on board delay line, while clock-vs-data synchronization used a second delay line (both lines with 1 nsec/step, 5-bit range). Between two starts signals a bunch of about 4000 words were read out and a FIFO clear issued. Also in this case the BTIs were mounted on a dedicated connection board, linked to the Pattern Unit through standard flat cables.

At high clock rates, short connection lines between the Pattern Unit and the chip under test, for example through a piggy-board, would improve signal propagation. A pin grid array, present on the Pattern Unit board and conceived for connecting arrays of resistors (to adapt the I/O impedance), can be used for connecting a piggy-board.

5. SUMMARY

A programmable 6U VME board, with the functionality of a high speed and high throughput Pattern Unit has been developed. Already the first version of the Pattern Unit board permitted to fulfill the project goal, that was to design a general tool for testing digital ASIC prototypes, in standalone and real time applications, up to 80 MHz.
Track Segment sorting in the Trigger Server of a Barrel Muon Station in CMS

I.N.F.N. Sezione di Bologna, Italy (email: Alessandro.Montanari@bo.infn.it)

Abstract

The Trigger Server of a Muon Station is part of the muon trigger chain of the drift tube chambers in the CMS barrel. The Trigger Server has to select the best track segments in the station and transmit them to the following stage of the first level trigger chain. The functional requirements and selection mechanism are discussed, as well the performance of an ASIC prototype built using CMOS 0.7 μm technology.

1. INTRODUCTION

The CMS Muon Barrel is formed by 250 stations of drift chambers. Each station is composed of 12 planes of drift tubes divided in 3 groups of 4 planes each, called SuperLayers (SL). Two SLs measure the coordinate in the bending plane (rφ), one SL along the beam direction (z). The four layers in a SL are staggered by half cell: correlation of drift times can be used to compute coordinate and angle of crossing tracks. The trigger front-end device is called Bunch and Track Identifier (BTI) [1]: it finds track segments and correlates them to the corresponding bunch crossings (BX). In the rφ view the track segments found by the BTIs of the two SLs are eventually correlated by the Track Correlator (TRACO) [1]. Each TRACO selects up to two trigger candidates, looking for the segments with higher quality and smaller bending angle (corresponding to higher transverse momentum). In the longitudinal view (only one SL) the BTIs select only tracks pointing to the interaction region.

The Trigger Server (TS) is the final stage of the trigger electronics of one muon station: there are in total 250 TS devices. It has to select the two best segments of the station and forward them to the following device in the trigger chain: the Regional Trigger. The Regional Trigger will match the segments found in the different stations and assign the transverse momentum of the reconstructed track.

The TS is composed by two subsytems: one for the transverse view (TSφ) and the other for the longitudinal view (TSθ).

The TSφ has to detect triggers produced by the 64 BTIs which equip the SL in the longitudinal view. This information is sent to the TRACOs of the transverse view and can be used there as a validation of a trigger in order to reduce background. Besides, a pattern of the track segments found in φ has to be sent to the Regional Trigger. The TSθ consists of groups of OR of BTI hits.

The TSφ is a real processing system. In the following discussion, the TSφ will be addressed.

2. REQUIRED FUNCTIONALITIES

The TS has to select the two best tracks among all the ones selected by all TRACOs of a muon station. These two tracks are then transmitted to the Regional Trigger. The number of TRACOs in a station can be quite large: currently 24 TRACOs are foreseen for the outermost and largest station. The main functional requirements of the TS are:

- Since much of interesting physics has two close muons that can hit the same muon station, much emphasis should be put on the efficiency and purity of both segments selected by TS.
- The latency of the TRACO-TS should be minimal.
- The processing time must be independent of the number of TRACOs in the station.
- The selection should be based on both the bending angle and the quality of the track segment. Selection priorities should be configurable.
- TS has to reject fakes eventually generated by TRACOs [1]. The fake rejection algorithm should be configurable.
- Pile-up events should be treated correctly.
- A JTAG line should be provided in order to control and monitor the system BTI-TRACO-TS.
- Since it is foreseen to mount the BTIs, TRACOs and TS on chamber, redundancy should be put in the TS, which represents the bottleneck of the front-end trigger devices.

3. THE SORTING ALGORITHM

Each TRACO transmits to the TS its two best tracks serially in two consecutive BXs, ordered in quality. In order to minimize the latency of TRACO-TS system, the TRACOs send previews of track segments. While the TS makes its selection (in pipeline), the TRACOs compute the full track parameters (absolute coordinates with higher precision). The TS then serially reads the full track parameters of the two best tracks from the corresponding TRACOs, and sends them to the Regional Trigger in parallel. With this mechanism 2 BXs are gained and the total latency of the TRACO-TS system is limited to 8 BXs.
The preview consist of a 10-bit word: 4 bits are reserved for the quality of the track (First/Second TRACO choice, High/Low trigger, Correlation, Inner/Outer SL [1]), the other 6 bits are used for the bending angle. The best track is the one with best quality (which means higher transverse momentum). If the quality bits are correctly coded, the search for the best translates in search for the minimum.

Let's now define bunch1 and bunch2 respectively the first and the second bunch of tracks arriving from the TRACOs connected to the TS (see figure 1). The sorting algorithm could be simple if it just looked for the best track of bunch1 and the best of bunch2, independently for the two bunches. However, it is not assured that the best track of bunch2 represents the second-best track among all bunch1 and bunch2 tracks. The TS must sort the true second-best track among all bunch1 and bunch2 tracks. In order to achieve this, the TS selects, among the tracks of bunch1, the first-best-track (FBT) and the second-best-track (SBT). On the following BX, the search for the best is done among bunch2 tracks and the SBT of previous BX (carry). Therefore the sorting algorithm is applied in pipeline at each bunch. In this way the true two best tracks are found among all the possible 58 tracks. For normal triggers, the TS is able to sort the two best tracks within two BXs. In case of pile-up triggers, the TS is able to provide to the Regional Trigger at least the FBT data resulting from the sorting of bunch1. In case of two close muons, they likely produce two track segments in bunch1 from different TRACOs in the same stations, which are correctly picked up by the TS algorithm through the carry.

4. HARDWARE ARCHITECTURE

The TS logic diagram is shown in figure 2. The selection algorithm uses a two layer cascade of processing units. This architecture has been chosen in order to minimize the number of logic cells within a unit and the amount of I/O between blocks[2]. In each unit, a parallel minimum and next-to-minimum search is performed over a small group of input words, using 2 by 2 fast 10-bits comparators. The full parallel approach guarantees a fixed time response, independent of the amount of TRACOs in a station. Each unit of the first layer (TSS: Track Sorter Slave) processes up to four data words, while the second layer unit (TSM: Track Sorter Master) processes up to six data words.

The functionality of each unit is performed in two consecutive cycles (one cycle per BX), called sort1 and sort2. The sort1 processing status is recognized when at least one TRACO gives a non-null track of bunch1 type, while the sort2 status simply corresponds to the cycle following sort1. The sort2 status can be aborted in case of pile up triggers. In the sort1 cycle, each TSS unit analyses four preview data words and transmits the minimum to the TSM unit in the second layer, while the next-to-minimum is stored locally and carried over to the sort2 cycle. At the same time a local select is given in output to enable transmission of the full data from the selected TRACO to the TSM. In the sort2 cycle, each TSS unit analyses the four input words of bunch2 together with the carry word of the sort1 cycle.

The TSM unit in the second layer analyses the six preview words from the TSSs. It behaves similarly to a TSS unit of the first processing layer, but its processing begins two BXs later. The information handshake between the TS logic system and the TRACO devices allows data from up to twelve tracks to be stored in the TSM unit. The selected output signal from the TSM, corresponding to the FBT in the first processing cycle and to the SBT in the second cycle, are used to enable the transmission of full track data to the Regional Trigger for two out of the twelve possible candidates stored in the TSM unit.

The TS0 unit (TS0), forms the OR of groups of BTIs: the information about the presence of a trigger in the longitudinal view is sent to the TSSs and from there to the TRACOs and can be used as trigger validation in the transverse view. Besides a pattern of trigger hits is sent to the TSM and forwarded to the Regional Trigger.
As shown in figure 2, the hardware partitioning of the system matches with the logical blocks. Each TSS device is housed on a board which contains 4 TRACOs (and 32 BTIs). The TSM device is on a separate board which receives the output of at most 6 TSSs (for the larger chamber). It is foreseen to mount this trigger electronics directly on the muon chambers.

The control and monitoring of the system is possible through a JTAG serial line which links the TSM, the TSSs, the TRACOs and BTIs. In case of failure of this link a backup solution is provided: a Parallel Interface which uses the lines normally dedicated for data transmission.

5. THE TSS PROTOTYPE

The TSS was designed using the VHDL language: in this way an easy portability of the project on different platforms was guaranteed. The main blocks which form the TSS device are shown in figure 3.

The central block is the sorting core, which is designed to perform the sorting of the two smallest among 4 words of 10 bits in one BX. The type of sorting algorithm is programmable (for example it is possible to disable the carry). Also the priority order of quality bits is programmable: in this way it is possible to optimise the selection locally, according to the local BTI-TRACO efficiency and the background conditions. The sorting core takes care also of the fakes rejection (see Section 6): different programmable algorithms are provided.

The functionality of the sorting core is controlled through the configuration registers which can be accessed by the JTAG controller or the Parallel Interface. It is possible to monitor or test the sorting core through Snap and Test registers.

As a first test the design was fitted on different types of programmable devices. The Altera and Xilinx FPGA and the QuickLogic pASIC were used. These tests revealed that it was impossible to fulfil the speed requirement of sorting in one cycle. At the beginning of 1998 it was then built an ASIC prototype using CMOS 0.7μm technology. The chip has 104 I/O pads and a Silicon area of 23 mm². All the required functionalities are provided: full programmability of sorting and fake suppression, JTAG and backup Parallel Interface.

The 10 chips delivered by ES2 foundry were tested in standalone mode, using a VME Pattern Unit [3]. Test patterns were injected at 40 MHz and the outputs cross-checked with the results of software emulation for the same patterns. No error was detected. In the next future a combined test with BTIs and TRACOs is foreseen.

6. SIMULATION

The TS algorithm was tested in the frame of the simulation of CMS detector. Events were generated with one or two muons, with energy in the range of 200 to 400 GeV, going in the same muon station. The ideal algorithm should find only one track segment in single
7. CONCLUSIONS

A fast track sorting device was developed, which selects the two best tracks found by the front-end trigger devices of a muon station and sends them to the following stage of first level trigger. It is a two stage system based on two basic units: a Track-Sorter-Slave (TSS) and a Track-Sorter-Master (TSM).

The TSS sorts out the two best tracks among groups of four. A full performance ASIC prototype was built and successfully tested.

The TSM design is currently under study and the first prototype is expected for next year. Its functionality is similar to that of the TSM, but it is a more complex device. Since it represents the bottleneck of the front-end muon chamber trigger, particular effort will be put on hardware redundancy.

8. REFERENCES

[1] P. Zotto, Local Track Reconstruction for the First Level Trigger in the CMS Muon Barrel Chambers, these Proceedings.
[3] F. Odorici, Pattern Unit for high throughput device testing, these Proceedings.
SYNCHRONIZATION OF THE CMS MUON DETECTOR
Grzegorz Wrochna
CERN
wrochna@cern.ch

ABSTRACT
Precise synchronization is crucial for the functioning of the CMS Muon Detector. In this paper we first discuss the possible sources of data misalignment, like variations in particle time of flight, signal formation and propagation within a detector (e.g. drift time), connections between various elements, set-up times and jitters of digital electronics. Then we review several methods which can be used to synchronize the system for the first time and to maintain the synchronization over a long period of time. Finally we discuss in detail a possible application of those methods to the Resistive Plate Chambers. We also briefly discuss the cases of Drift Tubes and Cathode Strip Chambers.

1. TRIGGER SYNCHRONIZATION

Fig. 1. Generic trigger structure.

The CMS Trigger System has a tree-like structure which is schematically shown in Fig. 1. The data flow through the entire chain should be synchronous, driven by the 40.08 MHz clock. Let us consider simplified signal flow diagram of the CMS Trigger shown in Fig. 2 with only one trigger device (e.g. Local Trigger) indicated.

Fig. 2. Synchronization with real data and test data.

The LHC Control system determines the interaction moment by driving RF and magnet currents (dashed line). Its clock is distributed by the TTC system [1] to Front End and Trigger electronics (dotted line). Particles created at the Interaction Point are flying towards detectors (thick solid line). Generated detector signals are sent from the Front End boards to the Trigger Processors (thin solid line). The following requirements have to be fulfilled:

- incoming data should be in phase with the local clock
- clock phase adjustment
- data from different sources should correspond to the same bunch crossing (b.x.)
- relative b.x. synchronization
- the data should correspond to the b.x. given by the local TTCrx — absolute b.x. synchronization

Phase adjustment at digitisation
Analog signals from the detectors have to be in a right phase with respect to the clock in order to be correctly digitized and processed. The signals often have a jitter due to time of flight, detector response and the signal propagation.

Phase adjustment of digitized signals
Once the signals are digitized they have no jitter, except for the electronics jitter which is usually below 1 ns. However, when the signals are sent to another board they might have a constant shift in phase in respect to the local clock at the destination. The rule to be followed is synchronize the phase of the signal at the destination to the local clock.

In order to synchronize the system one can use real data or test data. The first iteration, however, should be done without data, by measuring and calculating all the delays in the system. Test data provide an efficient way for partial synchronization of the system. However, final synchronization can only be done with real data, because there is no other way to measure precisely the path LHC Control → Interaction Point → particle flight → detector → Front End.

1.1. Synchronization without data
All particle and signal paths should be measured or calculated. Corresponding time differences should be compensated either by cutting the cables or by adjusting programmable electronics delays. It should not be too difficult to achieve precision better than 5 ns, which corresponds to ~1 m of cable. Special care should be taken with TTC fibres. Good knowledge of their length will facilitate synchronization with test data.

1.2. Synchronization with test data
Relative synchronization
Test patterns should be generated at the source (e.g. Front End board) and transmitted on request broadcasted by the TTC. At the destination (e.g. Trigger Processor board) they should be compared to the generated ones. Let us consider a simple example — a sequence (00100) sent through all channels. The same sequence should be observed at the destination, namely the "1" should come
at the same time, defined by the bunch crossing number provided by TTC. If in one of the channels, the “1” was observed e.g. one bunch crossing later, it means that this channel is delayed by one b.x. in respect to others.

**Absolute synchronization**

Test data can be used for absolute synchronization of data to the LHC clock at the destination if the absolute synchronization was already done at the source. Before using real data this can be done only approximately, taking the LHC clock and bunch crossing number provided by TTC at Front End as a reference. Precision of this method is limited by the knowledge of all delays in the TTC network. The main purpose of this procedure is to setup the system, so it can fully operate with test data. In this way trigger hardware and algorithms can be tested before the LHC beam is available.

Generated test pattern should unambiguously mark one b.x. Let us denote by \( N \) its number given by the TTC at the source. Again one can use the sequence (00100) as an example. The “1” should be sent in bunch crossing \( N \). The delay of the signal or the TTC clock at the destination should be adjusted in such a way, that the “1” is received in b.x. \( N \), according to the local TTC.

1.3. **Synchronization with real data**

The LHC frequency of 40.08 MHz corresponds to a 25ns period. One LHC orbit consists of 3564 periods. They are often call “bunches” although some of them do not contain protons. The proton bunches are grouped in 35 trains, 81 bunches each. The structure of gaps between them can be used for the absolute synchronization [2],[3]. Events containing data in a given detector region (e.g. a muon hit in a given RPC) are histogrammed according to the b.x. number (mod 3564). Accumulated histogram can be compared to the expected bunch structure. The same method can be used for relative synchronization of two channels by comparing their histograms.

**Special synchronization run**

A special run dedicated to the synchronization might be very useful. It may differ from a normal physics run:

- **Special LHC bunch structure** (e.g single, separated bunches) can be set up
- **Different trigger and DAS partitions** can be run independently in order to facilitate internal synchronization of each one
- **Trigger algorithms** may run in a “loose” mode to collect needed statistics in a shorter time
- **DAS partitions** may run in special modes, e.g. without zero suppression, reading out several consecutive b.x.

**Normal physics run**

During a normal physics run one can perform synchronization with both test data and real data. The gaps in the LHC bunch structure, especially the Abort Gap of 3.17 \( \mu \)s at the end of the orbit, can be used for sending test data. Real data can be used to accumulate timing histograms, as described above. They can also be used to monitor the synchronization by observing efficiency maps of the trigger, because desynchronization of a certain part of a system will very probably result in efficiency loss in corresponding region.

2. **DAQ SYNCHRONIZATION**

Two places are crucial for synchronization in the DAQ chain:

- **Phase adjustment at Front End**
- **Trigger - data matching at the end of DAQ pipelines**

The first item was discussed in the previous section, so we concentrate here on the second one. Data in a given DAQ channel are waiting for the LV1 decision in the pipeline. They are read out from the end of the pipeline if there was a positive LV1 response. The “LV1 Accept” corresponding to a given b.x. has to match the data from the same b.x. This can be achieved by delaying the “LV1 Accept” or adjusting the length of the pipeline. The value of the delay can be established using one of the following methods.

**Multi-crossing readout of real data**

This method is especially suitable for low occupancy detectors participating in the trigger, e.g. RPC, CSC and Drift Tubes. A given detector region is read out if there was a “LV1 Accept” caused by the data from this region. Several consecutive b.x. are read out in order to discover a possible misalignment of data with respect to “LV1 Accept”, High occupancy may disturb this method if probability of having data in consecutive b.x. is high.

**Multi-crossing readout of test data**

This method is suitable for any detectors participating in the trigger, i.e. muon detectors and calorimeters. A test pattern causing a trigger is generated in a certain detector region. The data from this region, covering several consecutive b.x. are read out in order to discover a possible misalignment of data with respect to “LV1 Accept”.

**Histogramming real data**

This method is similar to the trigger b.x. synchronization with real data (Sec. 1.3). Whenever there was a trigger, the data are stored in a histogram according to the b.x. number given by the trigger. Possible misalignment can be detected comparing obtained histograms to the LHC bunch structure. This method can be used by any detector, not necessarily participating in the trigger, e.g. by the tracker. High occupancy is of advantage in this method, because needed statistics can be collected faster.

3. **OPTICAL LINKS**

Special attention should be given to 1 GHz optical links connecting the detector with the counting room. In addition to the problems discussed above an internal synchronization of each link should be maintained. The first symptom of any synchronization problem will probably be higher bit error rate. Therefore, the data must be accompanied by an error detection code. Every time an error is detected the resynchronization procedure should be invoked. More detailed discussion of this problem can be found in [2] and [3].
4. MUON RATES

Proton-proton interactions provide the only way to make the absolute synchronization. Unfortunately the rate of muons, especially in the barrel, is very low. On average less than 1 muon per 1000 pp interactions enters the first barrel station MB1 and a few times less enter the last one MB4. At luminosity $10^{33}\text{cm}^{-2}\text{s}^{-1}$ the muon rate at MB4 of about 6 Hz/m$^2$ is expected. The area of MB4 RPC is $1.28\times3.75\text{m}^2 = 5\text{m}^2$. Similarly, the area of the smallest Drift Tube chamber at MB4 (the one in the CMS leg) is $2.52\times2.0\text{m}^2=5\text{m}^2$. This gives ~30 Hz per chamber, i.e. ~1800 muons / minute / chamber.

In the endcap the rate expressed in Hz/m$^2$ varies rather fast with rapidity. Therefore, it is more useful to quote the rate per $\eta$-unit. The lowest rate will be seen by the CSC ME1/3, which is $10^6$ wide and covers $\eta=0.88$-1.14. In this region the muon rate is about $4-10^3\text{Hz}/\eta$-unit, which results in 300 Hz/chamber. This is 10 times higher than in the case of RPC and Drift Tubes, therefore later in this paper we consider only the RPC/D T rate, as the worst case.

4.1. Relative synchronization

In order to make the relative station-to-station synchronization one can use all muons traversing a given detector region. It can be assumed that all channels of one chamber are aligned in time by construction with a precision better than 1 ns. In such a case one needs to collect ~1000 μ per chamber. This can be done in 1 minute.

4.2. Absolute synchronization

Absolute synchronization can be done only with muons from isolated (at least from one side) bunches. Running with only one bunch in the machine would reduce the luminosity by factor ~5000 to the level of $2\times10^{32}\text{cm}^{-2}\text{s}^{-1}$. In such a case only 20 μ / hour / chamber are expected, i.e. 50 hours are needed to collect 1000 μ / chamber.

Much better solution is to run with the full available luminosity, e.g. $10^{33}\text{cm}^{-2}\text{s}^{-1}$ and make use of the LHC bunch structure. For the absolute synchronization only the first or last bunch in each train can be used. Hence ~1% of muons is useful. This gives an effective rate of 0.3 Hz / chamber, i.e. 1000 μ / hour / chamber. It does not sound unreasonable.

The most effective configuration should have single bunches of protons separated by several “empty bunches”. For example 1 bunch of protons followed by 4 “empty bunches” would give the muon rate of ~6 Hz per chamber, i.e. ~360 μ / min / chamber. In such a case 3-5 minutes would be enough to collect reasonable statistics.

4.3. Background

Synchronization with muons can be disturbed by the presence of background. There are two major kinds of background to be considered:

- electrons — mainly from thermal neutron capture followed by γ emission and conversion,
- charged hadrons — mainly due to punchthrough from hadronic showers and backshales from the forward calorimeter (HF).

The single hit rate due to neutrons ($n\rightarrow\gamma\rightarrow e$) is 1-3 orders of magnitude higher than that of muons. CSC and Drift Tubes are able to eliminate this background by local coincidence of several layers in one chamber. The relative timing of those layers is ensured by construction, so the synchronization is not affected. The case of RPC is more difficult, because there is no local coincidence within one muon station. The only place when the neutron background can be suppressed is the Patter Comparator processor, looking for coincidence of at least 3 RPC planes. This implies that the RPC synchronization with real data (Sec. 1.3) must involve the trigger. That, in turn, means that the first iteration, done without the beam (Sec. 1.1 and Sec. 1.2), should be precise enough to enable trigger to work with at least 10% efficiency and thus to make the relative synchronization (Sec. 4.1) in <10 min.

The rate of charged hadrons is of the same order as the rate of muons. Charged hadrons can traverse several CSC or DT layers and satisfy the local trigger coincidence. However they often come in time, so their presence helps, rather than disturbs the synchronization process. Those created in HF can come 1 bunch crossing later. Their number, however, is too small to cause any synchronization problems.

5. RPC PACT SYNCHRONIZATION

5.1. PACT block diagram

Block diagram of the RPC PACT is shown in Fig. 3. Each chamber is equipped with Front End Boards (FEB) containing Front End Chips (FEC) with preamplifiers and discriminators. The signals are shaped and aligned with the clock by the Synchronization Unit (SU). Signals from several Front End Boards are collected by a Link Board (LB) through twisted pair cables, up to 3 m long. Then, the data are compressed (LMUX) and transmitted (TX) through optical fibers to the Counting Room. The data are split into two streams. The trigger stream data are decompressed (DEMUX) and processed by Pattern Comparator (PAC) processors. Recognized muon candidates are sorted according to their transverse momentum $p_t$ and sent to the Global Muon Trigger. The DAQ stream data are stored, event by event, in pipeline memories (PIPE). Events selected by Level 1 Trigger (LV1) are derandomized (DRND) and sent by Front End Driver (FED) to the DAQ system.

Main elements important for synchronization are also marked on the diagram. Synchronization Unit (SU) consists of WINDOW electronics for phase adjustment and Synchronization Buffer (SBUF) for b.x. synchronization. Synchronization with test data is done by test data generator (TEST DATA) and error detection circuit (CHECK). The TTC network is also shown. There is one TTCrx per Link Board and one per each crate in the Counting Room.
5.2. PACT timing

From the timing point of view the RPC PACT system consists of two distinct parts:
- upstream — before Synchronization Unit — signals are randomly spread in time with a jitter of ~20 ns;
- downstream — after Synchronization Unit — signals are aligned with the clock.

Since the downstream part is very similar for all detectors we discuss in this section only the upstream one.

The total signal propagation time in the upstream part $t_{up}$ has four components:

$$ t_{up} = t_{flight} + t_{RPC} + t_{propag} + t_{preamp} $$

The time of flight $t_{flight}$ is different for different chambers. It varies from $4m/c = 13ns$ for station MB1, to $12.6m/c = 42ns$. More important is variation within one chamber. The worst case is MB/2/1. The strip length of 1.26m causes the flight path variation of 1m and the time of flight variation $\Delta t_{flight} = 3.5ns$. The differences between various chambers can be corrected by adjusting the length of cables or electronics delay. The variation within one chamber cannot be corrected and it should be considered as a random jitter.

Second contribution is the time of intrinsic RPC phenomena: ionization, avalanche formation, drift to electrodes and pulse formation — denoted all together by $t_{RPC}$. It has quasi-gaussian distribution with $\sigma = 1.5ns$. An example is shown in Fig. 4.

The third contribution is signal propagation along the strip $t_{propag}$. The signal induced on the strip at the particle impact point propagates towards the preamplifier with velocity of about $\frac{2}{3}$ of $c$, i.e. $-0.2m/ns$. The propagation time varies from 0 to $max t_{propag}$, which for the longest strips of 1.26m is ~6.3ns. One cannot correct for it on-line and from the trigger point of view it should be considered as having approximately flat random distribution. However, one can achieve partial compensation of $\Delta t_{flight}$ and $\Delta t_{propag}$ by a proper placing of the amplifier (see Fig. 5), such that

$$ \Delta(t_{flight} + t_{propag}) = (min t_{flight} + max t_{propag}) - max t_{flight} < \Delta t_{flight} + \Delta t_{propag} $$

In the worst case of MB/0/1 the combined variation $\Delta(t_{flight} + t_{propag}) = 5.7ns$.

![Fig. 5. Partial compensation of time of flight $\Delta t_{flight}$ and signal propagation along the strip $\Delta t_{propag}$](image)

The contribution from preamplifier and discriminator jitter $\Delta t_{preamp}$ is usually much smaller than 1ns. Moreover, it is difficult to distinguish it experimentally from the intrinsic RPC jitter $\Delta t_{RPC}$. Therefore, the measured value of $\Delta t_{RPC}$ often contains $\Delta t_{preamp}$ and we will follow that convention in this paper.

The total jitter of the upstream part $\Delta t_{up}$ must be lower than 25ns in order to recognize the bunch crossing.

We have seen that is has two major contributions:
\(\Delta (t_{\text{flight}} + t_{\text{propag}})\) and \(\Delta \text{RPC}\). Assuming 1-3 ns for the setup time of the synchronization electronics and taking the worst case of \(\Delta (t_{\text{flight}} + t_{\text{propag}}) = 5.7\) ns, one gets 15-18 ns remaining for \(\Delta \text{RPC}\). In the case of a Gaussian distribution this would correspond to \(\sigma \text{RPC} < 3.0-3.5\) ns with 99% efficiency. This requirement is fulfilled by recently tested RPC prototypes (Sec. 5.9 of [4]).

5.3. Synchronization Unit

The Synchronization Unit (SU) is an integrated circuit which shapes the detector signals and aligns them with the LHC clock. It is done in the following way (see Fig. 6). From the LHC clock (denoted as CLOCK) provided by the TTCRx, a WINDOW signal is derived. Its width and phase can be adjusted from 0 to 25 ns with 1 ns step. They should be adjusted in such a way that the rising edge of INPUT from the detector is always within the high level of WINDOW. The WINDOW should be wide enough to contain the jitter \(\Delta t\). The coincidence of the WINDOW signal and the rising edge of the INPUT generates the OUTPUT signal which is 25 ns wide and is in phase with the CLOCK. The OUTPUT might be delayed by 0-3 clocks using Synchronization Buffer (SBUF).

![Fig. 6. Timing in Synchronization Unit.](image)

5.4. PACT synchronization procedures

All the methods described in Sec. 1 will be used for setting and maintaining the synchronization of PACT. The full sequence of actions may look as follows.

Procedure without the beam — first iteration

- Calculate the time of flight and measure the cables as precisely as possible — expected precision: < 5 ns
- Adjust the WINDOW phase and the Synchronization Buffer shift accordingly
- Set the WINDOW width close to 25 ns to maximize the efficiency

Procedure with the beam — special run

- For each trigger collect data from several (e.g. \(\pm 2\)) consecutive b.x.'s
- Observe how the data are distributed among b.x.'s
- Correct the WINDOW position and the synchronization Pipeline shift accordingly
- Narrow the WINDOW width to the calculated jitter

Procedure with the beam — "physics" run

- Monitor efficiency map of the detector — inefficiency in certain regions may be caused by wrong timing

6. SYNCHRONIZATION OF CATHODE STRIP CHAMBERS

The timing structure of the CSC system has several components similar to those of RPC. The difference is that the chamber response time \(t_{\text{CSC}}\) includes drift time, which makes the \(t_{\text{CSC}}\) distribution as wide as 50-70 ns at the base (Fig. 4.4.13 of [4]). Because of that the bunch crossing identification is more difficult, but on the other hand, the synchronization requirement for the phase adjustment at the Front End can be slightly relaxed. Apart from that the synchronization procedures are similar to those of the RPC PACT.

The local trigger is based on a coincidence of at least 4 out of 6 layers within 75 ns gate. The bunch crossing is identified by the second (in time) hit of those contributing to the coincidence. Prototype tests indicate that the distribution of the second hit arrival time is fully contained within 20 ns (Fig. 4.8.20 of [4]). Assuming 1-3 ns for the setup time of the electronics, about 2-4 ns remains for the phase adjustment precision.

In the DAQ path the anode (wire) signals are discriminated, whereas the cathode (strip) signals are sampled 8 times with 50 ns step. Because the signal can arrive at any clock phase due to the long drift time, there is no requirement on the phase adjustment precision.

7. SYNCHRONIZATION OF DRIFT TUBES

Requirements for Drift Tubes are similar to those of CSC. Here the drift time is even longer — about 400 ns. The bunch crossing recognition is performed by Bunch and Track Identifier (BTI) circuit, using generalized time marker technique (Sec. 3.4.2 of [4]). This method relies on the clock phase adjustment relative to the incoming data. The required precision is about 5 ns. In order to determine the delay one has to find the maximum of the BTI efficiency for real muons.

There is no requirement on phase adjustment at the Front End in the DAQ path. The signals are digitized by TDC, so the exact time can be reconstructed off-line.

CONCLUSIONS

Synchronization of an LHC detector is a complex issue which requires advanced studies involving both engineers and physicists. Procedures for setting and maintaining the synchronizations must be developed and necessary hardware has to be built. This paper represents one of the first attempts to this problem with respect to the CMS Muon System. The author is very grateful to Maciek Kudla, Paul Padley, Wesley Smith, and Joao Varela for many useful discussions.

REFERENCES

A RADIATION-HARD 80 MHZ CLOCK AND DATA RECOVERY CIRCUIT FOR LHC

Thomas Toifl, Paulo Moreira and Alessandro Marchioro
CERN, EP-Division, CH-1211 Geneva 23, Switzerland (Thomas.Toifl@cern.ch)

Abstract

An ASIC was developed to recover clock and data from an 80 MHz Biphase Mark encoded signal coming in from an optical link. The chip consists of a Limiting Amplifier to restore the signal, and a Phase Locked Loop (PLL) which uses a special phase detector to lock directly on the Biphase Mark signal. The circuit was implemented in a radiation hard BiCMOS Process (DMILL), and will be used in the radiation hard version of the Timing Trigger and Control Receiver circuit (TTCrx). To accommodate eventual changes of MOS transistor parameters due to process variations, temperature and irradiation, the PLL uses a transistor-parameter independent biasing scheme.

Figure 1. Basic function of the circuit. The clock and data signals are derived from the incoming biphase mark encoded input signal.

Figure 2. Block diagram of data and clock recovery circuit.

1. INTRODUCTION

In the Timing, Trigger and Control (TTC) system [1], the LHC clock is transmitted together with the first level trigger and control information over optical fibers using a biphase mark encoding scheme. At the receiver side the signal is detected by a pin-photodiode with integrated pre-amplifier, and is fed into the TTC receiver (TTCrx) ASIC. The circuit presented here describes the analog front-end of the radiation hard TTCrx, providing its clock and data recovery functionality (Figure 1). As shown in Figure 2, it consists of a Limiting Amplifier (LA), where the incoming signal is restored in 4 bipolar gain stages, and an 80 MHz Phase Locked Loop (PLL). Hence, the circuit delivers, on one hand, a low jitter 80 MHz clock, and on other hand, the decoded data signal. The clock signal can then later be used to derive the 40MHz LHC clock.

Figure 3. Limiting Amplifier Gain stage.

2. LIMITING AMPLIFIER

In the limiting amplifier the signal from the pin-diode undergoes amplification and hard limiting in four bipolar stages (Figure 3). Each stage consists of a bipolar transistor differential cell and an emitter-follower stage to achieve a high gain-bandwidth product. In order to avoid that the NPN-transistors of the differential pair go into saturation, the bias current is derived from a $V_{BE}$ reference via a resistor matched to the resistors in the gain stages.

Figure 4. Phase-Locked-Loop architecture.
3. PHASE LOCKED LOOP

3.1 Basic Architecture

A PLL is used to recover the clock and filter out phase noise from the incoming signal. As seen in Fig. 4, it consists of a voltage-controlled oscillator (VCO), a frequency- and phase-detector, a charge-pump and a loop-filter. The VCO uses differential delay cells with symmetrical loads [2] in order to achieve low sensitivity with respect to power supply voltage. A replica biasing scheme is used to regulate the voltage swing of the oscillator \( \Delta V \) to equal the control voltage \( V_c \). The loop control voltage \( V_c \) is directly connected to the oscillator delay cells, thus avoiding any additional buffer circuitry used in similar VCO implementations [2]. With this structure, the VCO frequency changes by only 0.6 \%/V supply-voltage deviation.

3.2 Parameter Independent Biasing

Although the used process (DMILL) is inherently radiation hard, changes in MOS transistor parameters \( \beta \) and \( V_t \) are not negligible, especially when regarded in conjunction with variations of process and temperature. The crucial value of the PMOS transistor threshold voltage \( V_{th} \), for example, can deviate by +420mV/-150mV from its nominal value of 800 mV. Hence a parameter independent biasing scheme [3] was developed to achieve a constant and predictable loop behaviour.

Disregarding the logic added to guarantee correct locking to the incoming biphase Mark sequence, the phase detector is essentially a flip-flop. At every cycle, the incoming signal is sampled and a binary decision (either early or late) is derived and maintained over the whole cycle. Thus a fixed current, either \(+I_{cp}\) or \(-I_{cp}\), flows through the loop filter. The filter resistor causes a stepwise change of the control voltage \( V_c \) (and the loop delay time \( T \)), providing the proportional part of the loop response, while the capacitor provides the integral part of the loop response. In order to achieve stability the proportional part must dominate over the integral part. For the given oscillator structure, the loop delay \( T \) is related to the control voltage \( V_c \) and the process parameters \( \beta \) and \( V_t \) through [3]

\[
T = \frac{C \cdot V_c}{\beta_p (V_c - V_t)^2}, \tag{1}
\]

leading to a relative delay sensitivity with respect to \( V_c \) of

\[
\frac{1}{T} \frac{dT}{dV} = \frac{1}{V_c} \frac{V_c + V_t}{V_c - V_t}, \tag{2}
\]

which can be fairly accurately approximated by

\[
\frac{1}{T} \frac{dT}{dV} \approx -\gamma \frac{1}{V_c - V_t}, \tag{3}
\]

where \( \gamma \) is a constant in the interval [1.4..1.8], depending on the expected ranges of \( V_c \), \( V_t \), and \( V_{th} \) of a given VCO. The change of the loop delay in one cycle is given by

\[
\Delta T_p = I_{cp} \cdot R \frac{dT}{dV_c} \tag{4a}
\]

\[
\Delta T_i = -I_{cp} \cdot T \frac{dT}{dV_c}. \tag{4b}
\]

To achieve parameter independence, the charge pump current is derived as proportional to \( (V_c - V_t) \) with the circuit of Figure 5,

\[
I_{cp} = \frac{(V_c - V_t)}{R_{ref}}, \tag{5}
\]

which leads to the resulting loop behavior

\[
\frac{\Delta T_p}{T} = \gamma \frac{R_{ref}}{R_{ref}}, \tag{6a}
\]

\[
\frac{\Delta T_i}{T} = \gamma \frac{T}{C \cdot R_{ref}}. \tag{6b}
\]

Hence, loop dynamics are independent of \( V_t \) and \( \beta_p \).

3.3 Frequency detector

Since the VCO central frequency must be expected to vary - due to radiation effects, process and temperature conditions - in a one to four range, a frequency detector circuit is necessary for locking to the input signal. The task is complicated by the properties of the biphase input signal, since unlike an ordinary square wave, the time between two edge transitions depends on the transmitted symbol. The frequency detection problem is similar to the case found in NRZ clock recovery [4]. The typical solution for that kind of circuits is the rotational frequency detector [5], which has the drawback that it can only detect frequencies within a 50\% range of the frequency of the input signal. To overcome this limitation a novel frequency detector [6] was developed. After a reset, the VCO starts with the lowest frequency. The frequency detector circuit then detects the condition that between two rising edges of the biphase input signal BPM there is no rising edge of the VCO signal (Fig. 6). If the condition is found the VCO frequency is increased.

![Fig. 5. Simple V_c-V_t extraction circuit.](image-url)
thus approaching the target frequency. As can be seen in Figure 7, the frequency detector circuit is essentially built of a “Last-Positive-Edge” (LPE)-detection circuit and a sampling flip-flop. The LPE circuit signals whether the last positive edge transition occurred at the VCO or the BPM input signal. Hence, LpeVCO gets high when there was a rising edge on VCO, and gets zero again after a rising edge on BPM. The implementation of the LPE circuit is shown in Figure 8.

Figure 6. The principle of operation of the frequency detector circuit. When high, the signal LpeVCO indicates that positive edge of the VCO signal was last. Sampling the signal with the rising edge of BPM results in the correct frequ_low signal (after inversion).

Figure 7. Frequency detector circuit.

Figure 8. LPE circuit. A rising edge on the VCO or BPM line creates a negative impulse on VCO’ or BPM’, thus changing the state of the RS-flip-flop.

3.4 Phase detector

In the Phase Detector, the biphase mark input signal is sampled at three different positions at time t₀, t₁ and t₂, resulting in sample values s₀, s₁ and s₂. The times t₀, t₂ are derived by using 3 phases of the VCO separated by 1/8 of the loop period (=1/8*12.5ns in lock).

If s₀ equals s₁, the incoming data edge comes after t₁, hence the VCO signal is early. Otherwise, if s₀≠s₁, the input edge comes before t₁ and VCO is late. Thus the phase detector decision (early or late) can be simply derived by xoring s₀ and s₁. In the locked state the data transition must happen in the gate between t₀ and t₂, hence s₀ must differ from s₂.

In order to exclude the possibility of a false lock to a middle transition of the biphase mark code (when a long string of Ones is transmitted), and to provide some frequency detection capability, a state machine was added to the phase detector. When the PLL is not locked, the charge-pump is switched off completely, thus maintaining the current frequency. The state-machine only switches on the charge-pump, when (a) the input transition occurs within the gate defined by t₀ and t₂, and (b) the previous decision (early or late) is different to the current decision. Hence, the condition is detected that the input edge migrates from the time interval [t₀,t₁] to the time interval [t₁,t₂], which would mean that the VCO frequency is slightly too high, or, in the second case, that the input edge travels from [t₁,t₂] to [t₀,t₁] and the VCO
frequency is slightly too low, the latter case shown in figure 9.

In order to avoid any timing differences between rising and falling edges of the input signal, the entire signal path has to be fully differential. Therefore differential flip-flops, based on CVSL-type latches [7], as shown in Figure 10, are used in the phase detector.

Because matching of the transistors used in the charge-pump deteriorated.

Figure 12 shows the rms clock jitter as a function of radiation dose for two levels of the optical input signal, -20dBm (nominal case) and -30 dBm (worst case). To avoid imbalance in the charge-pump, the reference current was set to 2x $I_{cp}$, leading to higher than minimum, but fairly constant jitter values at different levels of irradiation.

5. CONCLUSIONS

In this paper a radiation hard clock and data recovery circuit was presented. The circuit consists of a limiting amplifier and of an 80 MHz phase-locked loop. The paper describes a newly developed frequency-detector for biphase mark signals and the concept of self-biasing PLL's – especially useful in environments where the effects of radiation can drastically affect transistor parameters and thus decrease performance. Measurements on the circuit proved that it does not show significant degradation after a 10 Mrad irradiation, therefore fulfilling the LHC requirements.

6. REFERENCES

A 4-CHANNELS RAD-HARD DELAY GENERATOR ASIC WITH 1 NS MINIMUM TIME STEP FOR LHC EXPERIMENTS

Thomas Toifl, CERN, Geneva, Switzerland (email: Thomas.Toifl@cern.ch)
Riccardo Vari, INFN-Roma, Italy (email: Riccardo.Vari@roma1.infn.it)

Abstract

The ASIC can delay 4 digital signals in the range 0-24 ns with 1 ns single step. The delay values of the four channels can be independently programmed by an I²C field bus interface. A delay locked loop (DLL) generates the control voltage used for controlling the four delay channels. The common control voltage guarantees independence from process, supply voltage and temperature variations. The DLL is synchronised to an external 40 MHz clock signal. A first version of the chip was developed in 0.8 µm CMOS technology. The design of the prototype has then been transferred with few modifications to DMILL radiation hard process. Design functionality and measurement results will be presented.

1. INTRODUCTION

This chip is intended to be used in next High Energy Physics experiments realised at CERN for the Large Hadron Collider (LHC). Since timing distribution is essential in this kind of experiments, any time misalignment has to be avoided, in order to obtain high resolution measurements. LHC is a synchronous system, thus precise phase adjustment will be essential [1, 2].

The ASIC substitutes traditional delay elements, and can be used for timing adjustment. It provides four delay lines, capable of delaying digital signals, each line having 25 steps. The four channels can be independently programmed via an I²C interface. Since each delay tap is equal to 1 ns, the signals can be delayed in the range 1-24 ns. The chip needs an external 40 MHz timing reference signal. No external reset line is needed, since an auto-reset logic is implemented, for initialising all internal registers at power up. Power supply is 3.3 V.

The chip main objectives are: short delay adjustment (max 25 ns), moderate precision (~100 ps), low power and radiation hardness [3].

The ASIC has been realised in DMILL (Durci Mixte Isolant Logico Linéaire), a radiation-hard technology (up to 10 Mrad, 10¹⁴ neutrons/cm²), based on a BiCMOS 0.8 µm SOI hardened technique. Only CMOS were used for designing this ASIC.

The chip is composed by an analogue, full custom part, containing the four delay channels, and a digital, standard cell part, containing the I²C interface, the auto-

reset logic and the chip internal registers. DMILL standard cells were developed for CERN by IMEC, Belgium.

2. CHIP ARCHITECTURE

Figure 1 shows the basic structure of the chip. A central delay locked loop (DLL) is used for chip timing control. The DLL receives as input the external 40 MHz reference clock. It locks on this signal, and assures the right timing to the four delay lines.

![Chip architecture](image)

The four delay channels have the same layout as the central DLL, in order to achieve good matching properties between the DLL itself and the four delay lines. All the delay channels have the loop opened. This assures a unique control from the central DLL on the chip timing. The four channels receive the reference control voltage from the DLL, and adjust their delay in respect to this voltage. For this reason the chip layout has to guarantee a minimum voltage drop on the line feeding...
the control voltage, in order to avoid any time mismatching between channels.

Figure 2 shows the architecture of one DLL. The incoming digital signal passes through 25 identical delay elements. Each delay element, a double current starved inverter, can delay the passing signal according to the common control voltage on the filter capacitor. The last delay element output is compared, into a phase detector, with the incoming signal. The phase detector, implemented as a balanced flip-flop, controls a charge pump which can charge or discharge the filter capacitor, thus speeding up or slowing down the whole delay line. If the rising edge at the last delay element output comes after the rising edge at the first delay element input, the phase detector will take the decision of speeding up the delay line. So it will give to the charge pump the command for adding charge to the capacitor. Instead, for a signal coming before the delay line input, the charge pump will have to decrease the control voltage, subtracting charge to the capacitor.

When the DLL is locked to the 40 MHz clock (25 ns period), each delay element generates exactly a delay of 1 ns. A multiplexer can tap the delay line at the desired position, in order to select one of the possible 25 outputs. For each delay element, an inverter is used as buffer between the multiplexer and the delay element itself, for isolating the delay line from the multiplexer.

The four delay lines have both the phase detector and the charge pump disconnected. All the filter capacitors (five in total) are connected together so that their voltage is the same.

The I²C interface is used for programming separately the delay lines multiplexers. Each delay line has one five-bit register, programmable via the I²C interface, containing the desired value which selects the multiplexer output.

The chip contains an automatic reset logic, implemented for avoiding the use of an external reset signal, which is not provided at system level. At power up, a digital initialisation procedure guarantees the DLL locking.

The main considerations used for designing the chip layout were: using large area devices, for a good short-distance matching, and keeping the delay line structure as compact as possible, in order to have small distances between matched structures [4]. The final chip layout is shown in Figure 3.

![Figure 2 DLL architecture](image1)

![Figure 3 Chip layout](image2)

3. MEASUREMENT RESULTS

The ASIC has been tested obtaining the following results. Figure 4 shows the channels and clock measured output delay, for all the 25 programmable taps, demonstrating the correct functionality of the circuit.
DNL and INL are lower than the values required in the specifications as shown in Figure 5 and Figure 6. Both DNL and INL are lower than the values required in the specs. DNL shows good transistor matching properties within every delay line. INL increases with the tap number because transistor matching properties get worse with the distance between the DLL and the channels.

![Graph showing Delay vs. tap number](image)

**Figure 4** Delay vs. tap number

Differential and integral non-linearity are characterised as shown in Figure 5 and Figure 6. Both DNL and INL are lower than the values required in the specs. DNL shows good transistor matching properties within every delay line. INL increases with the tap number because transistor matching properties get worse with the distance between the DLL and the channels.

![Graph showing Differential non-linearity vs. tap number](image)

**Figure 5** Differential non-linearity vs. tap number

![Graph showing Integral non-linearity vs. tap number](image)

**Figure 6** Integral non-linearity vs. tap number

Jitter at the channels output, at the last tap, is less than 26 ps RMS and less than 180 ps P-P, as can be seen in Figure 7 and Figure 8, which show jitter vs. tap number. Jitter increases with the increasing tap number, because tapping more delay elements means adding in the multiplexer the noise coming from the delay line. In this type of DLL a relevant contribution to the jitter may come from the phase detector scheme (bang-bang jitter). Measurements showed that the loop capacitor is big enough to minimise this kind of contribution.

Power consumption has been measured with different output loads, and in both cases of output enabled and disabled. Measurements have been done with the DLL only (Figure 9), and feeding one channel input (Figure 10). The DLL was able to work properly in the range 25-65 MHz.

The chip power consumption, with a 40 MHz input clock and 500 Ohm channel output load, has been estimated as: 29.6 mW + 9.7 mW/channel + 0.29 mW/MHz/channel. 29.6 mW is the DLL contribution; 9.7 mW is the channel contribution at 500 Ohm output load at 0 MHz frequency; 0.29 mW is the contribution of one channel per MHz.

![Graph showing RMS jitter vs. tap number](image)

**Figure 7** RMS jitter vs. tap number

![Graph showing P-P jitter vs. tap number](image)

**Figure 8** P-P jitter vs. tap number
irradiated with

have both remained unchanged after irradiation. Due to

module, and this causes the peaks showed in the figures.

current in

a modularity of eight taps. After ilTadiation, the

shown in Figure 11 and Figure 12. The peaks present in

the plots, both in the DNL and the INL, are due

the loss in symmetry between the nmos and pros

channels output duty cycle is the same as the input one.

Power consumption increases after irradiation by a

factor is static, and it comes from the increased leakage

current under 3.3 V

under 3.3 V

have been

been

been

have both remained unchanged after irradiation. Due to

the loss in symmetry between the nmos and pmnos

different threshold voltage shift) inside the circuit, the

chip has worse linear properties after irradiation, as

shown in Figure 11 and Figure 12. The peaks present in

the plots, both in the DNL and the INL, are due to the

multiplexer scheme adopted in the delay lines, which has

a modularity of eight taps. After irradiation, the

multiplexer loses matching between every eight tap

module, and this causes the peaks showed in the figures.

Power consumption increases after irradiation by a

factor of 10% (Figure 13). The only contribution to this

factor is static, and it comes from the increased leakage

current in the chip.

Delay lines have been designed symmetrically, so that

channels output duty cycle is the same as the input one.

After irradiation, the loss of symmetry between pmnos and

nmos causes a symmetry degradation. After 10 Mrad the

output duty cycle decreases by a factor of ~10%.

4. REFERENCES


ATLAS Level-1 Calorimeter Trigger
System Architecture

P. Bright-Thomas, A. Connors, J. Garvey, S. Hillier, R. Staley, A. Watson (1)
C. Geweniger, P. Hanke, E. Kluge, K. Meier, U. Pfeiffer, (2)
A. Putzer, K. Schmitt, C. Schumacher, K. Tittel, M. Wunsch (2)
K. Jakobs, G. Quast, U. Schäfer (3)
E. Eisenhandler, M. Landon, J.M. Pentney (4)
C. Bohm, M. Engström, S. Hellman, S. Silverstein (6)

Correspondence
Ulrich Pfeiffer
Institut für Hochenergiephysik, Universität Heidelberg
Schrödingerstrasse 90
D-69120 Heidelberg
Tel. ++49 6221 54 4971
e-mail: pfeiffer@ihep.uni-heidelberg.de

Abstract
The Level-1 Calorimeter Trigger is a fast pipelined system for the selection of rare physics processes in the ATLAS experiment at LHC. Its selectivity contributes to a rate reduction from the 40 MHz LHC bunch crossing rate down to the first level accept rate of 75 kHz maximum. This is done by searching for isolated electrons and photons, hadrons, jets of particles and by calculating global energy sums in the calorimeter within the 2.0 μs total latency of the level-1 trigger. Hence, fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) are required.

1 Introduction
At the ATLAS experiment, which is one of the general-purpose experiments at the CERN Large Hadron Collider (LHC), bunches of 7 TeV protons cross each other every 25 ns with a design luminosity of 10^{34} m^{-2}s^{-1}. At this luminosity each bunch-crossing induces 25 inelastic proton-proton interactions on average which corresponds to a total proton-proton interaction rate of about 10^9 Hz. Due to the very small production rate for “interesting” decay channels, only a small fraction of these inelastic proton-proton interactions is used for the physics processes of interest. Therefore the ATLAS experiment requires a high selectivity paired with optimal efficiency to retain interesting particle decays.

The overall ATLAS trigger system is divided into three levels of processing (level-1,2 and 3). Each level reduces the detector readout data volume by a given factor. Data from the tracking system, the muon detectors and the calorimeters are stored in pipeline-memories at a rate of 40 MHz until the level-1 trigger has made a decision indicated by a level-1 accept signal. Remaining data are then stored in readout-buffers until the level-2 trigger reduces the readout.
rate to about 1 kHz for the event-builder. Finally the level-3 trigger decides on the basis of full event data and causes the data to be permanently stored for offline analyses. In addition to the detector readout, data from the level-1 trigger are captured in order to keep the raw information on which the event was selected.

To reduce the size, and hence cost of pipeline-memories, the level-1 trigger has to derive a decision as fast as possible. Therefore the total latency for the level-1 trigger is limited to 2 µs (80 bunch-crossings). Figure 1 summarises the level-1 trigger latency share between processors, enclosed by the time-of-flight and the time needed to redistribute the level-1 accept signal to the front end electronics.

Coordinates of detector regions (Regions of Interest, ROI) inside which the level-1 trigger has identified local energy distributions (e.g. hadronic clusters and/or electromagnetic clusters) are given to the level-2 trigger. Based on this information the level-2 trigger reads detector data from the event-buffers for that region, with full detector granularity.

The level-1 trigger itself is divided into three sub-systems, the calorimeter trigger, the muon trigger and the Central Trigger Processor (CTP). The role of the CTP is to combine information from the calorimeter and the muon trigger to make the final level-1 trigger decision. This decision is distributed by the Timing, Trigger and Control system (TTC) to the front-end electronics of the detector systems, where it initiates the readout.

2 Overall architecture of the level-1 calorimeter trigger

The ATLAS level-1 trigger requires analogue signals with a coarse granularity in pseudorapidity and azimuth ($\eta$, $\phi$) as input from the calorimetry. For a total $\eta - \phi$ coverage of $|\eta| < 4.9$ and $0 < \phi < 2\pi$ calorimeter signals are summed together to form trigger-towers with a granularity of 0.1 x 0.1 in $\eta$ and $\phi$. This summation is done separately for signals from the electromagnetic and hadronic calorimeter. All in all about 7200 trigger-tower signals are transmitted to the trigger electronics, which is located near the detector at a distance of about 60 m. The chosen granularity is a balance between rejection of background and cost and complexity of the trigger processor.

The Level-1 Calorimeter Trigger is divided into three processors, the Preprocessor (PPr), the Cluster Processor (CP) and the Jet/Energy-Sum Processor (JP). The Preprocessor performs several functions on each of the analogue input signals. It provides digital data for the CP and JP processors, which work in parallel to each other. The digital data from the PPr contains the deposited transverse energy identified to a corresponding bunch crossing in time (BCID). For the CP this is done for all trigger-tower signals up to $|\eta| < 2.5$ and for the JP up to $|\eta| < 4.9$. In case of the JP the trigger-towers are summed further to form jet-elements with a coarser size of 0.2 x 0.2, still treated separately for electromagnetic and hadronic signals. The CP performs the electron/photon and hadron/tau algorithm, whereas the JP performs the Jet algorithm and calculates the global sums for the $E_T$-miss/sum-$E_T$ triggers. Physically, these processors are composed of printed-circuit modules mounted in crates. In order to optimise the signal fan-out between crates and modules the trigger matrix is divided into quadrants in $\eta$. Each quadrant is then mapped into two PPr crates, one CP crate and one JP crate. Signals at the boundary between each quadrant are duplicated at the PPr in such a way that shared signals, needed by the sliding-window algorithms from neighbouring quadrants, are received via the PPr rather then by inter-crate links. Signals shared between modules in the $\eta$-direction are transmitted via point-to-point backplane connections only.
3 Calorimeter trigger algorithms

The Level-1 Calorimeter Trigger performs four basic algorithms. An electron/photon, a hadron/tau, a jet and a $E_T$-miss/sum-$E_T$ trigger. Figure 3 shows basic elements to construct the algorithms. Each algorithm identifies objects classified to their transverse energy. The number of objects passing a programmable $E_T$-threshold is counted as multiplicity. The multiplicity of objects which have passed is sent for eight different thresholds to the Central Trigger Processor (CTP). The region-of-interest, and the coordinates of the identified objects, is sent to the level-2 trigger.

The first three algorithms are looking for different objects, but the basic computing steps are the same for all of them. Each algorithm is performed within a trigger window of a given size, which in case of the jet algorithm is programmable (see table 1). To cover the whole trigger region in parallel, the algorithms are applied to trigger windows stepped by one trigger element (trigger tower or jet element) at the same time. For each of these windows the algorithms decide whether an object passing the condition was found. Because of the stepping through the $\eta - \phi$ coverage (sliding-windows) the algorithms must be resistant against double counting of objects which is referred to as declustering.

Except for relevant distinctions given in table 1 the processing of the first three algorithms can be summarised as follows:

- Each algorithm identifies a RoI-cluster which has a local $E_T$ maximum inside the trigger window (declustering). To pass this condition, the RoI-cluster must be more energetic than the neighbouring RoI-clusters to the right and one above, and at least as energetic as the nearest neighbours to the left and one underneath.

- Inside the RoI-cluster the energy of all possible $E_T$-measure clusters are compared against eight thresholds.

- Trigger elements inside an isolation region are summed together and compared against an isolation threshold. (Not used for the jet algorithm.)

- An object is identified if it has passed all conditions. Then the multiplicity for the corresponding threshold is increased by one. The position of the RoI-cluster is sent as region-of-interest to the level-2 trigger.

The sum-$E_T$ trigger adds up all trigger elements up to $|\eta| < 4.9$ (table 1) and the $E_T$-miss trigger does the same for the components $E_x$ and $E_y$ separately.
Table 1: Comparison of Trigger algorithms. The × means Δη × Δϕ size of the η - ϕ coverage or the number of elements in each direction. A · stands for summation of electromagnetic and hadronic layers and o for separate processing.

<table>
<thead>
<tr>
<th>size of</th>
<th>El./photon</th>
<th>Had./tau</th>
<th>Jet</th>
<th>E_7-miss/sum</th>
</tr>
</thead>
<tbody>
<tr>
<td>trigger element</td>
<td>0.1 x 0.1 o 2</td>
<td>0.1 x 0.1 o 2</td>
<td>0.2 x 0.2 o 2</td>
<td>0.2 x 0.2 o 2</td>
</tr>
<tr>
<td>trigger window</td>
<td>4 x 4 o 2</td>
<td>4 x 4 o 2</td>
<td>(4 x 4, 3, 2 x 2) o 2</td>
<td>-</td>
</tr>
<tr>
<td>window step</td>
<td>0.1</td>
<td>0.1</td>
<td>0.2</td>
<td>-</td>
</tr>
<tr>
<td>RoI cluster</td>
<td>2 x 2</td>
<td>2 x 2</td>
<td>2 x 2</td>
<td>-</td>
</tr>
<tr>
<td>Isolation (em./had.)</td>
<td>(ring/square)</td>
<td>(ring/ring)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>¦-coverage cluster</td>
<td></td>
<td></td>
<td>2 x 1 or 1 x 2</td>
<td>trigger window</td>
</tr>
<tr>
<td>Jet trigger</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E_7-measure cluster</td>
<td>[η] &lt; 2.5</td>
<td>[η] &lt; 2.5</td>
<td>[η] &lt; 3.2</td>
<td>[η] &lt; 4.9</td>
</tr>
</tbody>
</table>

Table 2: Mapping of calorimeter regions into processor modules.

<table>
<thead>
<tr>
<th>size of</th>
<th>PPM</th>
<th>CPM</th>
<th>JEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>element</td>
<td>0.1 x 0.1</td>
<td>0.1 x 0.1 o 2</td>
<td>0.2 x 0.2 o 2</td>
</tr>
<tr>
<td>local area</td>
<td>4 x 16</td>
<td>4 x 16 o 2</td>
<td>2 x 8 o 2</td>
</tr>
<tr>
<td>total area</td>
<td>4 x 16</td>
<td>7 x 19 o 2</td>
<td>5 x 11 o 2</td>
</tr>
<tr>
<td>from neig.</td>
<td>-</td>
<td>3 x 19 o 2</td>
<td>3 x 11 o 2</td>
</tr>
<tr>
<td>to neig.</td>
<td>-</td>
<td>3 x 19 o 2</td>
<td>3 x 11 o 2</td>
</tr>
</tbody>
</table>

Figure 3: Calorimeter trigger algorithms.

4 Processor modules

As described in section 2 one quadrant in ϕ is mapped into crates of processors. Each processor crate contains electronics modules and components, providing pre-processed data or calculating the actual sliding algorithms in parallel for the local area given in table 2. The following section focuses on the components and technologies which are used inside these processor modules.

4.1 Preprocessor module

The Preprocessor module (PPM) has 64 analogue receivers to accept the trigger-tower signals from the calorimeter. The signals are processed by commercial integrated circuits (ICs) and application-specific ICs (ASICs), most of which are hosted inside 16 Multi-Chip Modules (MCMs). A MCM combines different IC technologies, e.g., analogue or digital components together to increase the die/package size ratio. Inside each MCM 4 ADCs digitise the analogue signals to 10 bits. Two PreProcessor ASICs (PPrAsics) perform the BCID algorithm, the transverse energy calibration to 8 bits in a look-up-table and the presumming of jet-elements. It also contains pipeline memories to store trigger data up to 2 μs until a level-1 signal arrives from the CTP initiating the readout. Codes for the detection of transmission errors are generated before trigger tower data is serialised to 800 Mbit/s using gigabit links manufactured by Hewlett-Packard (G-links). A bunch-crossing multiplexing scheme, which doubles the effective bandwidth of the high-speed serial link by a factor of two is used for the transmission of pre-processed trigger-towers to the CP. Pre-summed jet-
elements are serialised off the MCM and linked to
the JP with 9 bit resolution. The $\phi$-duplication of
links at quadrant boundaries is fanned out to ca-
ble drivers. The readout data from all PPRAis are
collected by one Readout Merger ASIC (RemAsic).
This ASIC interfaces to a custom token-ring-like bus
on the backplane (PipelineBus) which shifts read-
out data via a readout-driver board to the readout-
buffers. Slow control is used to set up the configura-
tion and to load test data.

4.2 Cluster Processor module

A local area of 4x16 trigger towers, plus the $\phi$-
duplicated towers, is received by the Cluster Pro-
cessor Module (CPM) on 40 gigabit links (electro-
magnetic and hadronic towers are transmitted sep-
rately, see table 2). Two of these gigabit chips and
two Serialising ASICs (SAsic) are placed inside a
Multi-Chip Module for the CP (20 CPMCMs in total).
The SAsic reduces the number of lines by multiplexing the data from 40 MHz up to 160 MHz.
It also checks the data for transmission errors, in or-
der to avoid a trigger on faulty data, and the clock for the Cluster Processor Asic (CPAsic) is synchro-
nised. Eight CPAsics on a module perform the actual
CP algorithms on signals coming from two sources:
SAsics on the same CPM provide PPPr data and $\phi$-duplicated towers; $\eta$-duplicated towers come via
point-to-point backplane connections (at 160 MHz)
from the SAsics of neighbouring CPMs. The multi-
plicity of objects at each threshold from all CPMs is
merged by Cluster Merger Modules (CMM) and
then sent to the CTP. RoI data are sent in parallel
to the level-2 trigger and to the readout-buffers, after
they are collected via gigabit serial links and merged
into Slinks (CERN standard links, preferred for AT-
LAS data acquisition). Slow control is used to set up
the configuration (e.g. threshold- and timing-values)
and to load test data.

4.3 Jet/Energy-sum module

On a Jet/Energy-sum module (JEM), 22 gigabit re-
ceivers convert the serial data from the PPPr into
40 MHz. Compared to the CPM the data volume is
smaller, because of the larger jet-element size used
for the Jet and $E_T$-miss/sum-$E_T$ algorithm (see ta-
ble 2). Therefore the multiplexing of data to twice
the link speed (80 MHz) is sufficient. The multiplex-
ing is performed by field programmable gate arrays
(Sum-FPGAs). At 80 MHz a FPGA device is pre-
f erred to ASICs because of its flexibility, an easier
and faster design process, and the prices are compe-
titive with ASICs at low quantities. The Sum-FPGA
sums electromagnetic and hadronic layers together
to form the final jet-element. The total energy and
the components in Ex and Ey are computed for the
local area (see table 2). These sub-sums are merged
inside Sum Merger Modules (SMM) to their global
values and readout data from the Sum-FPGA is col-
lected for the readout-driver and then send via Slinks
to the readout-buffers. The Jet algorithm is also
implemented inside a FPGA (Jet-FPGA). This of-
fers the flexibility to change the algorithm depend-
ing on the size of the actual chosen trigger-window
(see section 3). A total of 22 jet-elements from the
Sum-FPGA and 33 jet-elements from the neighbours
(via a 80 MHz backplane) are used to perform the
jet algorithm. Finally a Jet Merger Module (JMM)
merges the multiplicity and RoI-data from all mod-
ules.

5 Summary

The algorithms of the ATLAS Level-1 Calorimeter
Trigger are based on sliding-windows in the $\eta$-$\phi$ trig-
ger space. Parallel processing of these overlapping
windows is implemented in a $\phi$-quadrant architec-
ture. This architecture minimises the data sharing
between electronic modules and processors. It sim-
plifies the design of transmission line backplanes and
the layout of modules in terms of system size and
costs. However, it requires the usage of advanced
technologies to limit the total level-1 trigger latency
to 2.0 $\mu$s.

References

[1] ATLAS First-Level Trigger Technical Design
Report. ATLAS Level-1 Trigger Group, ATLAS
TDR-12, CERN/LHCC/98-14, 24 June 1998
The $e/\gamma$ and $\tau$/hadron Processor System for the ATLAS First-Level Trigger

Rutherford Appleton Laboratory, Chilton, Oxon, UK

P. Bright-Thomas, A. Connors, J. Garvey, S. Hillier, R. Staley, P. Watkins, A. Watson
School of Physics and Astronomy, University of Birmingham, Birmingham, UK

E. Eisenhandler, M. Landon, J. M. Pentney
Queen Mary & Westfield College, University of London, London, UK

P. Hanke, E-E. Kluge, U. Pfeiffer, C. Schumacher, M. Wunsch
Institut für Hochenergiephysik der Universität Heidelberg, Heidelberg, Germany

K. Jakobs, G. Quast, U. Schafer
Institut für Physik, Universität Mainz, Mainz, Germany

C. Bohm, M. Engström, S. Hellman, S. Silverstein
Department of Physics, University of Stockholm, Stockholm, Sweden

Abstract

The $e/\gamma$ and $\tau$/hadron first-level trigger system for ATLAS will provide electron/photon and tau/hadron trigger multiplicity information to the Central Trigger Processor (CTP), and region of interest (RoI) information for the second-level trigger processor. The system will also provide intermediate results to the DAQ system. This paper will outline some of the more interesting and challenging technologies we have studied, ranging from ASIC design, through high-density packaging, to exploitation of commercial high-speed links for the final system.

1. INTRODUCTION

The $e/\gamma$ and $\tau$/hadron cluster processor (CP) will process $0.1 \times 0.1$ (eta x phi) electromagnetic and hadronic trigger towers covering a pseudo-rapidity region of $\pm 2.5$. It will receive 6400 eight-bit trigger tower signals from the preprocessor system, serialised and BC-multiplexed [1] to transfer four trigger towers per link at 800 Mbit/s on 2080 coaxial cables. The CP system will provide electron/photon and tau/hadron trigger multiplicity information to the CTP, and region of interest information to the level-2 processor. Also the system will provide intermediate results as well as the final results to the DAQ system for monitoring and diagnostic purposes.

The trigger algorithms (see Algorithms below) use sliding and overlapping windows, and each trigger tower participates in sixteen different windows, implying a massive fan-out of signals. To keep the fan-out and the pin counts of modules and ASICs to a manageable minimum, careful system partitioning is necessary.

The CP system consists of four crates of cluster processing electronic modules, each processing a quadrant of the calorimeter in phi and a complete space in eta ($\pm 2.5$). This is carried out by using 13 cluster processor modules (CPMs) in each crate, each CPM processing a $16 \times 4 \times 2$ area of the calorimeter.

The partial trigger multiplicity results from all the CPMs are then merged in a separate crate using cluster merger modules (CMMs) and the results transferred to the CTP. The RoI information and the DAQ data from all the CPMs are transferred to read-out driver modules (RODs) in a separate crate. Figure 1 shows the block diagram of the system.

1 Single-Board Computer
1 VME interface
13 RODs
1 CM crate
16 CMMs
3 bit multiplicity threshold 1
To CTP
threshold 16
To DAQ and Level-2
CM Crate
3bitmultiplicity
threshold1
13CMFs crate
CP Crate 1 CP Crate 2 CP Crate 3 CP Crate 4
Fibres from TTC system CAN Bus VME
Signals from the Preprocessor System
(-2000 links @ Gigahits/s)

Figure 1: CP System
2. ALGORITHMS

Using a $4 \times 4$ sliding window and trigger towers of $0.1 \times 0.1$ in $\eta \times \phi$ space (figure 2), the algorithm will search for isolated electromagnetic (e.m.) energy clusters and tau candidates and provide triggers and RolIs.

For the electron/photon trigger, one of the two horizontal or two vertical sums in the electromagnetic calorimeter must be greater than a cluster threshold (eight thresholds), and separate electromagnetic and hadronic isolation threshold criteria are imposed (eight thresholds). Also, the central $0.2 \times 0.2$ region must be a local $E_T$ maximum compared to its eight overlapping neighbours. This also performs the de-clustering and defines the RolIs.

The $\tau$/hadron trigger algorithm is very similar to the electron/photon trigger algorithm but uses both the electromagnetic and hadronic calorimeters for the core energy calculations. More details on the algorithms can be found in reference [1].

Figure 2: e/\gamma algorithm

3. TECHNOLOGY

The performance requirements of the ATLAS level-1 calorimeter trigger processor are extremely demanding in terms of advanced technologies. A great deal of work over the last few years has been involved in design studies of novel techniques and components, many of which are essential to the operation of the trigger and others of which could add significant improvements. In general, these studies have culminated in the design and fabrication of various items of hardware, most of which have been evaluated in a lengthy demonstrator programme. Whenever possible, the demonstrator system has been operated in the demanding environment of the ATLAS test-beam at CERN, and fed with signals from prototype calorimeters, although more detailed electronic studies and measurements have taken place in the laboratory.

Figure 3 shows the key technologies; such as Gigabit/s links, MCMs, 160 Mbit/s backplane, 40 MHz pipeline processing, etc., required within a 'data chain' from the preprocessor to the cluster processing electronics.

3.1 Serial Links.

The CP system has to process 6400 trigger towers. Given the algorithmic requirement to process overlapping windows, minimizing fan-out implies maximising processing per module. If each CPM were to receive 8-bit parallel data from 160 trigger towers it would require 1280 connections. This would clearly be impractical, so it is proposed to transport the data serially. Serialisation at 520 Mbit/s would require one link per trigger tower, but by using Gigabit chip-sets (e.g. HP G-Link) and BC-multiplexing four trigger towers could share one link.

3.1.1 Hewlett Packard (HP) G-Links

HP G-Links (HDMX 1012/1014) [2] have been used in the trigger demonstrator system since 1995, driving optical fibres via Finisar [3] devices and driving coaxial cables. As the link lengths for the chosen architecture will be less than 10 m, the simple electrical solution is adequate and has been more extensively studied. Although designed to operate as ECL devices the G-Links may be operated in PECL mode, allowing direct interfacing to subsequent circuitry without additional conversion chips. Provision of clean power supplies, adequately filtered from the TTL supplies, is essential for reliable operation in this mode.

The demonstrator system has 18 links operating with two channels per link at 800 Mbaud. Nine of the links may alternatively be run with four channels per link at 1600 Mbaud.

The links have been successfully operated at 800 Mbaud both in the lab and in the CERN test-beam environment. Using a purpose-built real-time hardware bit-error rate (BER) tester, BERs better than $5 \times 10^{-13}$ have been measured with coaxial links up to 11 m in length. To avoid increasing the ATLAS trigger rate by $> 1\%$ a BER $< 10^{-9}$ per channel will be required. Link-lock was very robust, with no losses experienced.

In the 1600 Mbaud dual frame mode two 16-bit words are time-multiplexed within the 25 ns clock period, thereby achieving a density of four trigger towers per link and requiring only half the number of links and chip-sets. Corresponding module real-estate and power density requirements are also halved. Lab tests showed the links to be robust and error-free until VME accesses occurred in the crate housing the G-link transmitters, when lock was frequently
lost. At 1600 Mbaud these chips appeared very sensitive to +5V power supply noise, especially as the links were operated in PECL mode. HP now offers a version of the chip-set to operate with standard TTL logic. Also, the chip-sets are only specified to operate up to 1500 Mbaud (0°C to +85°C), although this may be extended to 1800 Mbaud over a reduced temperature range (0°C to +65°C).

The requirement to operate at 1600 Mbaud has now diminished since the BC-multiplexing scheme, which also packs four trigger towers into each link has been adopted.

### 3.1.2 GaAs Custom Tx ASIC

We have collaborated with the Middlesex University Microelectronics Centre to design a low-power high-speed chip-set. In the first instance, a transmitter ASIC has been designed to operate at 1600 Mbaud with a maximum power dissipation of 650 mW. This chip was designed to interface with the HP G-link 1014 Rx chip so that it can be tested within the existing test infrastructure. The Tx ASIC is under test at RAL at the time of writing this paper.

### 3.1.3 ECL “Simple Link”

This is a customised serial data link designed to run at 320 Mbit/s using differential ECL. At the transmitter end the eight bits (no error detection bits or clock encoding) are simply serialised at a 320 MHz rate. At the receiving end the bit-stream is latched on to two latches with anti-phase 160 MHz clocks to generate two 160 Mbit/s data streams. This scheme requires a clock and data alignment strategy as described in section 3.1.6. For testing, daughter cards have been designed to replace the G-link daughter cards in the demonstrator system. This scheme will not require any additional ASIC such as the serialisation ASIC used with the G-Links, but additional circuitry would be needed for 'spying' on the data.

### 3.1.4 LVDS Chip-sets

An alternative to the above scheme would be the use of commercial low-voltage differential signalling (LVDS) chip-sets, such as 'channel link' from National Semiconductors. As they are designed for the portable PC market to interface colour LCD displays, the modularity is three bytes (three colours) with four control bits, somewhat inconvenient for the trigger system. However at the time of writing this paper National Semiconductors have announced a new chip-set, which is a low power 10-bit serialiser/deserialiser which can operate at 40 MHz [4]. We will be investigating the possibilities of using this chip-set to reduce system power.

### 3.2 160 Mbit/s Serialiser ASIC

As shown in figure 3, in the demonstrator system the serial data are transmitted from the preprocessor system at 800 Mbaud using G-Link transmitter chips, and are received by the corresponding receiver chips and converted to parallel data. To reduce pin counts on backplanes and cluster processor ASICs, a dual function ASIC (RAL 163) was designed to demonstrate the interfacing between a G-link receiver chip and a cluster processor ASIC receiving data at 160 Mbit/s, as well as module-to-module data transfers via the backplane at 160 Mbit/s.

The first function of this ASIC is to convert a 16-bit parallel word every 25 ns into four serial links operating at 160 Mbit/s. Hence two 160 Mbit/s links are required to transfer 8-bit data to a cluster processing ASIC within the 25 ns bunch crossing interval.

The 16-bit parallel word, together with the G-link error signal, can be captured in a 80-deep (2 μs) dual-port memory, to be read out following a level-1 YES decision. This memory can also be used in a playback scheme for test purposes, and for diagnostics.

The second function of this ASIC is to convert the 160 Mbit/s data back into parallel data to be compatible with the demonstrator cluster finding ASIC (see section 3.3). This functionality demonstrates the operation needed for the front-end of the final cluster-finding ASIC by receiving the 160 Mbit/s serial data, de-serialising them, and synchronising the resultant parallel data to the 40 MHz system clock before they enter the algorithm processor, using 6.25 ns delay elements.

The dual-function ASIC was designed using the 0.7 μm CMOS technology from ATMEL-ES2, and has been tested successfully on the bench up to 176 MHz, as well as being used during the 1996 and 1997 beam tests in CERN.

### 3.3 Cluster Processor ASIC

The demonstrator cluster processor ASIC (RAL 114) was a cut-down version of the final CPASIC, processing only one trigger tower in the e.m. layer. It was a 0.8 μm, 20,000 gates CMOS gate-array design to demonstrate the implementation of the cluster-finding algorithm using pipeline processing elements of adders and comparators.

When it was designed in 1993, the LHC bunch-crossing period was foreseen to be 15 ns, hence the ASIC was designed to work at 67 MHz.

This ASIC has been used since 1993 at various stages of the demonstrator program, and has been interfaced with the 160 Mbit/s data streams using the dual function ASIC (RAL 163) as described above, to convert the serial data to parallel data. In the final CPASIC, the data will be received on 160 Mbit/s serial links to minimise pin counts and maximise processing, with the 160 Mbit/s to 40 Mbyte/s conversion performed internally.

### 3.4 Timing and Synchronisation

In the final CP system, the G-link transmitters will use the 40 MHz LHC clock and the internal phase-locked loop circuits to multiply the clock to the required bit-rate clock. The 40 MHz clock will then be extracted at the receiving end by the G-link receiver chips, and phase-locked to the on-board 160 MHz clock to generate the 160 Mbit/s data streams. Unlike the high-speed serial links, the 160 Mbit/s data links do not have a clock recovery scheme. Therefore when the 160 Mbit/s data are received on the CPASICs they must be aligned to the 160 MHz clock. After conversion, the 40 Mbyte/s data then have to be synchronised to the 40 MHz LHC clock before entering the cluster finding logic.
In the 36 channel demonstrator system, clock alignment and synchronisation were performed manually using programmable delay lines, which was very time consuming, so to align 6400 trigger towers in the final system, an automated process will be required.

An ASIC (RAL 215) was designed to evaluate such a process. Using delay-locked loop (DLL) techniques the delay lines were built into the ASIC. The calibration logic on the ASIC scans through the 160 MHz clock phases (five 1.25 ns taps) and through a statistical process selects the appropriate clock phase to capture the calibration data. Then data are synchronised to the 40 MHz clock by using 6.25 ns delay elements. This process takes approximately 1.5 μs. Figure 4 shows the block diagram.

![Figure 4. Clock Synchronisation Logic](image)

### 3.5 Backplane

A 3U section of the 9U backplane on the demonstrator cluster processing crate is a high-speed transmission-line backplane operating at 160 Mbit/s single-ended. The high-speed backplane is required to fan-out trigger data within a crate to the neighbouring cluster processor modules. The signal transmission is point-to-point using ECL drivers, with path lengths ranging from two to eight slots. Figure 5 shows the multi-length fan-out from module to module. Nine double-width modules were used to fully process a 0.3 (η) x 0.3 (φ) calorimeter window.

Standard 2 mm, four-row Futurebus+ connectors are used, having 192 connections for signals and power.

The backplane was manufactured with 33 Ω transmission-line tracks, using strip-line design in a 12-layer construction with four signal layers and eight power and ground layers. Ground guard tracks between signal tracks are used to minimise cross-talk.

Lab tests indicate that the backplane can be operated with a bit-error rate better than 10⁻¹³.

Since the Technical Proposal [5] was written in 1994, the architecture has changed, and with the proposed φ-quadrant architecture as described in the Technical Design Report [1], each CPM will cover a quadrant in φ and 0.4 in η. The modules processing neighbouring regions in η will be in adjacent slots in the same crate, hence all backplane paths will be only one slot in length. The final backplane is therefore much less complex than the demonstrator version, which can already provide a performance considerably better than required.

![Figure 5. Backplane Multi-Length Fan-out](image)

### 3.6 Multi-Chip Module (MCM)

The use of multi-chip module packaging technology brings many benefits such as:

- package efficiency (die size to package size), giving the capability of implementing many channels per module
- high-speed signals and interconnect routing confined to a small area (minimising the requirement of transmission lines on the PCBs)
- good EMC performance, etc.

The cluster-finding algorithms operating in the CPMs require a high degree of trigger tower fan-out to neighbouring modules, which should be minimised by maximising the processing in each module. Architectural studies indicate that data from 160 calorimeter trigger towers should be fed directly to each CPM from the preprocessor modules, thus demanding compact MCM packaging solutions.

Studies have been carried out at RAL into the use of MCM-L (laminate) technology with ball grid array packaging, and lead-less chip carrier packaging built-in to the substrate, as well as MCM-C (ceramic) technology. For reasons of thermal management (~5 W per MCM) and cost, MCM-C technology was chosen for the demonstrator design.

The demonstrator MCM incorporates two HP G-link dies (HDMP-1014D) to receive the trigger tower data at 800 Mbaud and convert them to 16-bit parallel words, and two serialiser ASIC dies (RAL163) which convert each 16-bit parallel word into four 160 Mbit/s bit-streams for the cluster-finding ASICs.

A summary of the MCM specification is given below

- Ceramic substrate (96% Alumina)
- Three metal (gold) layers
- Standard thick film technology
- Four dies (2 HP G-Links and 2 RAL163 ASICs) and printed resistors on substrate
- Capable of handling 200 ps rise-time signals on the substrate
- All components contained within a 30 mm × 30 mm area
- All dies bonded to the MCM using 33 µm gold wire
- 120-pin hermetically-sealed package
- 6 watts power dissipation

The complete specification, design and thermal modelling were carried out at RAL. The track layout of the MCM was carried out by industry.

The MCMs were manufactured and delivered to RAL in September 1997. After various manufacturing problems had been resolved the devices were tested. As the RAL163 ASICs were designed with built-in test facilities they could be rapidly checked, but G-link operation could be verified only by observing the lock condition and the resultant data via the RAL163 ASICs. Communication with the RAL163 ASICs worked correctly, but the G-links did not lock reliably. After a thorough investigation the cause of the problem was revealed to be excessive noise on the 5 V supply lines, which the G-links use as the reference. In this design they operate with positive ECL (PECL) logic levels. Noise, due to poor power supply track layout on the MCM, was studied. Further tests need to be carried out to eliminate minor problems such as loss of lock when DAQ system intervenes. These problems are still related to power supply noise, due to poor power supply track layout on the MCM substrate.

Figure 4: MCM

4. Demonstrator Programme

The ATLAS test beam has been used every year since 1993 to test various components and technologies required for the final ATLAS trigger system, and in 1997 a complete system 'slice test' was carried out [1]. The strategy for the demonstrator programme was to build a small scale version of the trigger system to evaluate critical components required for the final system. Except for the MCM all other technologies required for the final trigger system have been tested in the CERN test beam environment. Figure 5 shows various milestones achieved during 1993 to 1997.

Further to the test beam work extensive lab tests have been carried out, including bit-error rate measurements on the complete 'data chain'. The measured BER is better than 5 × 10⁻¹², which should be compared to the <10⁻⁹ BER limit imposed by restricting the trigger rate increase to <1%.

Figure 5: Technology Milestones

5. SUMMARY AND CONCLUSIONS

The cluster processor system relies on several key technologies which the demonstrator programme was designed to evaluate.

The first phase of the project studied the implementation of the cluster-finding algorithms on semi-custom ASICs at full LHC speeds. In the latter part of this phase the implementation of digital bunch-crossing identification logic was studied.

The second phase of the demonstrator programme concentrated on the 'data chain' from the detector through the FADCs and into the processing crates, and then the fan-out on a transmission-line backplane.

Most of the key technologies have now been successfully tested, and proven solutions exist in all areas to support the final system design as described in the Technical Design Report [1].

The final CP system architecture includes two ASIC designs, a MCM design and four module designs.

6. REFERENCES

CMS CALORIMETER TRIGGER RECEIVER SYSTEM

W. H. Smith, W. Badgett, S. Dasu, M. Jaworski, J. Lackey
Physics Department, University of Wisconsin, Madison, WI 53706 USA

Abstract

The CMS level-1 calorimeter trigger electronics is designed to identify signatures for high-energy electrons, photons, neutrinos and jets. The calorimeter regional trigger system receives and processes 1.2 Gbaud digital serial data transmitted from the calorimeter readout electronics on copper cables and transmits the results for further processing at 160 MHz. The heart of this system is the Receiver Card, which uses the new generation of Gigabit Ethernet receiver chips on dedicated mezzanine cards that convert serial data to parallel data. This data is then deskewed, linearized, summed and further processed on the main Receiver Card before transmission on a high speed point-to-point backplane for subsequent processing by cards that sum energies and identify electrons and jets.

1. CMS TRIGGER OVERVIEW

The CMS detector for the Large Hadron Collider (LHC) [1] presents an extraordinary challenge for its trigger and data acquisition system. Its trigger system must carefully sift the 40 MHz data to retain only interesting physics signals at 100 Hz level while discarding the well-known QCD background. The CMS trigger is implemented in two physical levels, one based on custom electronics and the other relying upon commercial processors. The level-1 system uses only coarsely segmented data from calorimeter and muon detectors, while holding all the high-resolution data in pipeline memories in the front-end electronics, to produce a trigger decision in 3 μs. Level-1 triggered events at a 75 kHz rate are sifted further in higher levels of triggers implemented as software filters.

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of physics objects such as photons, electrons, and jets, as well as global sums of E_t and missing E_t (to find neutrinos) [2].

For most of the CMS ECAL, a 5 x 5 array of PbWO4 crystals is mapped into trigger towers. In the rest of the ECAL there is somewhat lower granularity of crystals within a trigger tower. There is a 1:1 correspondence between the HCAL and ECAL trigger towers. The trigger tower size is equivalent to the HCAL physical towers, .087 x .087 in η x φ. The φ size remains constant in Δφ and the η size remains constant in Δη out to an η of 2.1, beyond which the η size increases.

As shown in Figure 1, the CMS level-1 calorimeter trigger starts with a basic 3 x 3 sliding-window electron algorithm [3] that involves two separate cuts on the longitudinal and transverse isolation of the ECAL energy deposit. The first electron cut involves the hit tower HCAL to ECAL energy ratio, H/E. A second cut is placed on the HCAL transverse energies in the nearest eight towers surrounding the hit tower.
Additional trigger cuts are imposed to permit lower \( E_t \) thresholds. An ECAL transverse isolation cut considers all four 5-tower corners of the 3x3 window and requires that at least one of them be below a programmable cutoff. The act of checking all four 5-tower corners ensures that the candidates depositing energy in any corner of the central tower do not self-veto due to leakage energy. Another cut is based on a summary of the energy found in the ECAL crystals before summation in trigger towers. A “fine-grain” electromagnetic isolation bit is set and transmitted with the trigger tower energy if the maximum energy found in a pair of strips of five crystals represents a large fraction of the total energy found in the 25 crystals summed in a single ECAL trigger tower. An electron found in a region where this bit is set can be triggered with a lower threshold.

As shown in Figure 1, jet triggers are based on sums of ECAL and HCAL transverse energy in non-overlapping 4x4 trigger tower (0.35 \( \eta \) x 0.35 \( \phi \) ) regions. Results of detailed simulation of both electron and jet algorithms have shown good performance on the CMS physics signals [4].

The calorimeter level 1 trigger system, shown in Figure 2, receives digital trigger sums from the front end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers for the same crossing will be sent on a single link in eight bits apiece, accompanied by five bits of error detection code and a “fine-grain” bit characterizing the energies summed into the trigger towers. For ECAL, this is the “fine-grain” electromagnetic isolation bit. In HCAL, this bit is set based on the ratio of energy in the first and second longitudinal HCAL sections.

The calorimeter regional crate system uses 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. The remaining crate covers both Very Forward Calorimeters.

Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum \( E_t \), \( E_x \) and \( E_y \). It also sends its 4 highest-ranked isolated and non-isolated electrons and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide electrons and jets, as well as the total calorimeter missing and sum \( E_t \) to the CMS global trigger.

Figure 3. Schematic view of a typical Calorimeter Level 1 Regional crate.

The regional calorimeter trigger crate, shown schematically in Figure 3, has a height of 9U and a depth approximately of 700 mm [5]. The front section of the crate is designed to accommodate 280-mm deep cards, leaving the major portion of the volume for 400 mm deep rear mounted cards.

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are eight rear-mounted Receiver cards, eight front-mounted Electron Identification cards, and one front-mounted Jet Summary card for a total of 17 trigger-processing cards per crate.

2. CALORIMETER TRIGGER HARDWARE

The calorimeter level 1 trigger system, shown in Figure 2, receives digital trigger sums from the front end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL...
The Receiver Card synchronizes the input data and passes it through look-up tables to separately linearize the energies into the number of bits needed for electron identification and energy triggers. Data in parallel form is shared with the neighboring crates at 80 MHz. The entire system operates in lock step after this stage at 160 MHz. The energies are then summed in 4 x 4 trigger tower regions. The crate is built on a central "backplane" which provides data sharing at 160 MHz. Data for electron identification logic, which includes both the data, received on the serial cables and that received on inter-crate cables, are transferred to the Electron Identification cards plugged into the front-side of the "backplane". The 4 x 4 sums are transferred to Jet/Summary card plugged into the center of backplane on the front-side of the crate.

The Electron Isolation card implements its algorithm in a custom integrated circuit. The candidate electrons are ranked and top candidates are passed to the Jet/Summary card. The Jet/Summary card sorts the electron and jet candidates in the crate to output the top four candidates of each kind on a cable to the global trigger. It also calculates sums of E_x, E_y and E_z for transmission to the global calorimeter trigger cards, which sort objects and sum energies from their inputs to obtain the final output of the calorimeter trigger which is used together with the muon trigger data to provide the final trigger decision.

3. RECEIVER CARD SYSTEM

The Receiver Card is the largest board in the crate. It is 9U by 400mm. The design is optimized to forward data for further processing only at appropriate resolution and only on a need-to-know basis. Figure 4 shows the rear side of the Receiver Cards. It receives the calorimeter readout data from copper cables, and converts from serial to parallel format.

The Receiver Card receives the 8-bit non-linear E_x and 1-bit fine-grain ECAL or HCAL ID data from 32 ECAL and corresponding HCAL trigger towers for a total of 64 input channels per card. The same technology is employed for both HCAL and ECAL. Each input copper link carries 2 channels of either HCAL or ECAL data in one 24-bit frame per 25-nsec crossing. The frame contains 2.9-bit data words for the two towers, with each data word containing the 8 bits of energy and the single bit of identification information. Each frame also contains 5 bits of error detection code, which are used for error logging and to zero problem channels that can cause high spurious trigger rates. The 24-bit word is then 8/10 bit encoded, resulting in a 1.2 Gbaud serial link.

The data is brought in on 20-m non-halogenated cables of the type presently being developed for 1000Base T Ethernet. Four links are incorporated into a single cable that is connected into one of eight mezzanine cards, each of which contains a single Vitesse VSC7214 4-channel Interconnect Chip. The mezzanine cards contain circuitry for on-board cable and connector equalization. The data is already synchronized across the HCAL and ECAL and transmitted on equal length cables, so only a limited phase adjust is required. The tower geometry in the ECAL and HCAL is designed to match and the ECAL and HCAL tower mappings on the cables also match so that correlating the two calorimeters is straightforward.

Figure 4. Rear side of the Regional Calorimeter Trigger Receiver Card.

Figure 5 shows the front side of the Receiver Card that contains the circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. The data emerges from the Vitesse 7214 as 120 MHz TTL and is brought to the front side for processing by the Phase ASIC. It deskews the data, checks the error detection code, and multiplexes the data out at 160 MHz ECL. The Receiver Card then outputs an error bit for each 4 x 4 region of input towers. The Phase ASIC also provides test vectors for board and system checkout.

The Phase ASIC is designed to receive four channels of parallel data from the Vitesse Receivers. Each channel of data arrives at 120 MHz eight bits wide in 3 cycles for each 25 ns bunch crossing. This provides a 24-bit frame at 40 MHz that contains the 18 bits of data described above and 5 bits of error detection code, with one bit in reserve. A block level diagram of the ASIC is shown in Figure 6. The single clock for four channels is derived from the Vitesse Receiver. Data is transmitted from each Receiver channel along with two status bits and an error bit. The status can be used to determine whether the link is in
setup mode or data transmission mode. The input stage of the Phase ASIC is a 44 bit wide FIFO that is six frames deep. The FIFO accommodates minor phase shifts between the transmitter and local clocks. The FIFO is followed by a circuit, which sets the proper phase between the incoming data and the local bunch-crossing clock. Once properly phased, the data and error bits can be separated into 18 bits of data (two channels) and 5 bits of Hamming code. The Hamming code is recomputed from the data and compared with the received Hamming code bits. The data leave the Phase ASIC at 160 MHz in two data channels with 9 bits apiece, and one error channel, also 9 bits. The technology for the Phase ASIC is the same Vitesse 0.6 µm GaAs process as used for the Adder ASIC described below.

The Adder ASIC is designed to add 8 11-bit numbers (including the sign) in 25 nsec, while providing bits for arithmetic and input overflows. It has been produced by Vitesse in 0.6 µm GaAs, consists of approximately 11,000 cells, uses 4 W and has been tested to 200 MHz, considerably above the 160 MHz requirement.

The Receiver Card also ORs the ECAL fine-grain EM ID and HCAL Muon ID bits separately for each 4x4 region. It then stages the 4x4 region data to the Jet/Summary cards. There are a number of lookup tables and adder blocks on the front of the Receiver Card. The lookup tables translate the incoming information to transverse energy on several scales. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for inter-crate sharing. The Receiver card also has separate lookup tables to provide linearized 8-bit ECAL transverse energy, and H versus E comparison bits, for the electron/photon algorithm. These data are staged to both the cards within the crate at 160 MHz on the backplane, and to the neighboring crates on cables at 80 MHz.
MHz. The prototype Receiver Card has recently been manufactured and is under test. Figure 7 shows a photograph of the front side of the completed card.

**Figure 7. Photograph of the front side of the prototype Receiver Card**

The backplane[6] is a single 9U-high printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128-pin) DIN connectors, capable of full 32 bit VME. The first two slots of the backplane use three row (96-pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME module can be inserted in the first two stations. The form factor conversion to the remaining slots is performed on the custom backplane.

The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high-speed controlled-impedance connector for both front and rear insertion. The design is based around a 340-pin connector, by AMP Inc. to handle the high volume of data transmitted from the Receiver cards to the Electron Identification and Jet Summary Cards. There are 1419 differential 160 MHz point-to-point links on the backplane between the various cards. The backplane is constructed with six ground and power planes and seven signal layers.

In order to test the feasibility of operation at high frequency we built a complete prototype backplane, which can house up to eight Receiver and Electron Isolation card pairs, a Clock card and a Jet/Summary card. The layout of this prototype backplane is shown in Figure 8. The figure shows the read side of the backplane projected onto the front, revealing both front side and rear side connectors. Results from testing clock signals on the backplane show rise and fall times of 0.8 ns from 20% to 80% height with full ECL signal levels even when measured at the farthest card slot. This performance meets the requirements of 160 MHz operation of the backplane.

**CONCLUSIONS**

The construction and test of the CMS regional calorimeter trigger Receiver Card, Backplane and associated ASICs that implement the Level-1 trigger algorithms represent an important step towards demonstrating the feasibility of the trigger design.

This work is supported by the United States Department of Energy and the University of Wisconsin.

**Figure 8. Layout of the backplane**

5. REFERENCES

The Global Calorimeter Trigger for CMS
H.H. Wills Physics Laboratory, University of Bristol, Bristol BS8 1TL, UK
A.J. Maddox, V. Perera
CLRC Rutherford Appleton Laboratory, Chilton OX11 0QX, UK

Abstract: The CMS calorimeter trigger logic is designed to search for objects, such as electron/photon or jet candidates, in local regions of the calorimetry. Objects found in different regions must then be compared with each other and the best candidates selected for onward transmission to the CMS trigger decision logic. This paper describes the design of the Global Calorimeter Trigger for CMS, which performs the selection. In particular we describe a low latency pipelined sort algorithm which has been developed, and preparations for the test of an ASIC implementation of the algorithm.

1. Introduction

The Level 1 trigger logic for CMS is designed to search for specific signatures, which distinguish physics events of interest from the large background of hadronic events. In the calorimeter processing, the most important of these is the search for energetic electromagnetic showers from either electrons or photons. This part of the logic is known as the $e/\gamma$ trigger. Other signatures of interest include high transverse energy jets and large missing transverse momentum.

The pattern recognition logic for the various types of object is housed close to the readout electronics for the calorimetry, in the Regional trigger processor crates[1-3]. Up to four different types of object will be searched for, including two separate processing chains for the identification of $e/\gamma$ candidates. One of these will impose strict isolation requirements, with cuts optimised for the identification of electrons or photons from the decay of high mass objects such as the Higgs. The other is intended to search for electrons from the semileptonic decay of heavy quarks, which may be found relatively close to some hadronic activity in the calorimeters. The Regional trigger will also search for jet-type objects, and for isolated single hadrons e.g. from $\tau$ decay. In addition, each Regional trigger crate will produce transverse energy sums. The Global Calorimeter Trigger (GCT) collects together all the data output from the Regional Trigger Crates. Its function is to extract the 4 highest ranked objects for each type and to complete the calculation of total and missing transverse energy, to be transferred to the Level 1 Trigger Processor.

This paper is organised as follows. In the following section we will introduce the components of the Global Calorimeter Trigger. Section 3 describes the link used to transfer data from the Regional crates to the GCT, as well as for inter module communication within the GCT crate. In Sections 4 and 5 we concentrate on the object sort processor and introduce a fast sort algorithm. Finally we report on the design of an ASIC implementation of the sort algorithm and a test system, which will be used to check the ASIC function at clock frequencies up to 200 MHz.

Figure 1. Mapping of the regional trigger crates onto the central calorimeter
2. Global Calorimeter Trigger

The input to the GCT is determined by the topology of the Regional Calorimeter Trigger electronics. The Regional trigger processor is distributed over 18 crates, with a mapping as depicted in figure 1. Data from the two very forward calorimeters, which contribute to the transverse energy sums only, are processed in a 19’th crate.

Each regional crate receives data from the ECAL and HCAL front end electronics for (30 x 8) trigger towers (in the \( \eta \times \phi \)-space). The pattern recognition logic identifies objects and assigns them to fixed, non-overlapping (4 x 4) trigger tower windows. This results in an initial map of (2 x 8) objects. The objects found in each Regional crate are collected on the Jet/Summary Card (JSC), the interface to the Global trigger. The object energy, plus additional information like isolation status or the fine grain bit, which identifies objects with electron type showers, are translated into a 6 bit rank using a lookup table. In order to reduce the number of interconnections 4 data words are time multiplexed on each link within the Regional crates. All object data processing in the Regional as well as in the Global trigger takes place at 160 MHz.

Within the JSC, the ranks are input to the first stage of a sort tree. The four highest ranks for each object type are identified and transferred, including a 4 bit location identifier to the GCT (see fig.2). This processor identifies the 4 highest ranked objects and sends them including a location identifier to the global trigger. In addition, the number of jets above a threshold will be sent to an interface module in the GCT, to allow a fast online measurement of the luminosity for every bunch crossing separately.

Partial transverse energy sums in \( E_{t} \), \( E_{x} \) and \( E_{y} \) are also calculated on the JSC. These data are transferred to a global sum module in the GCT, for \( E_{t} \) as a 12 bit unsigned and for \( E_{x} \) and \( E_{y} \) as a 12 bit signed number. Additional partial sums from the two very forward calorimeters (covering the range \( 3 < |\eta| < 5 \)) are received from a 19th crate. The total transverse energy values are calculated and forwarded to an interface module. The missing transverse energy is calculated using LUTs and data is scaled for the transfer to the global Level-1 Trigger.

All GCT modules store their input data for the level-1 latency time, and provide data for readout in the case of a level-1 accept. The Luminosity values are read out after an appropriate integration time.

3. Links between Calorimeter Trigger Modules

The GCT has to receive data for the sort processor from a large number of data sources running internally at 160 MHz. No commercial link technology is available to serialise data at this data rate. Hence parallel data transfer is unavoidable. The link length of up to 15 m, and the the expected spread of data arrival times, of \( \pm 6 \) nsec, have led us to the decision to transfer data as differential ECL at the 40 MHz bunch crossing frequency. A compact con-
nector (CHAMP 0.8) has been chosen, which can transfer up to 68 differential pairs on a 4 cm high connector.

On the Sort Processor modules discrete ECL logic will be used to time multiplex data back to 160 MHz. Data transfer between modules within the GCT crate will use the same links to avoid the design of a custom backplane. Data for the transverse energy sum modules is only updated with the bunch crossing frequency. Since we need to utilise the full width of the chosen link, we have to reorder the partial sum data using a patch panel. Transverse energy data from up to 5 Jet Summary Cards will be combined into one link, resulting in 4 input connectors for the Global Sum Modules.

4. Sort Processor

The four highest ranked objects are extracted in two stages. Figure 3 depicts the general structure of the sort processor with three input sort modules and one final sort module. Each input sort module receives 24 ranks from six JSCs. The four highest ranked objects are determined and forwarded to the final sort module. This module identifies the absolute four highest amongst the remaining (3 × 4) objects and transfers them to the global trigger. The data link width is increased during the sort process by the numbers of bits needed to locate the sorted objects. This location identifier is 4 bits wide for data from the JSCs and 7 bits for data exchanged between input and final sort module.

All input data are recorded in a latency buffer for readout. In the case of a level-1 accept, data for three bunch clock cycles are stored in a de-randomizer buffer. ECL FIFOs are used for both buffer stages. Another mezzanine card is used for the interface to a Front-End Driver Module.

5. Object Sort Algorithm

The object sort is accomplished in the calorimeter trigger in a 3 stage sort tree. A location identifier is created on every sort stage. A pipelined sort algorithm with 2 bunch crossing cycle latency has been developed. Its implementation on an ASIC will be employed on all three sort tree levels.

The number of input data links is six, corresponding to the number needed at the input sort module stage of the tree. Each input link receives four data words per bunch crossing cycle. The algorithm shown in figure 5 assumes that these four words arrive already sorted in descending order. The sort of the up to 24 data words is performed in two pipelined steps. First the highest ranked data words from the six input busses have to be compared with each other. The order is determined by counting how often a rank is higher than the others. The second step investigates the ranks of those objects which may be buried in the lower ranks of the input data. A multiplexer is used to select those data words which could contribute. The link with the highest rank may also contain data of the second, third and forth highest ranked object. The link with the second highest object may contain data for third and fourth highest and so forth. The first sort stage already determines
the object with the highest rank. The other 9 objects remain to be sorted in the second step. This second sort stage can be implemented with 15 comparators, since the input data is already pre sorted and also only the four highest ranks have to be identified. A second multiplexer is used to select the four highest ranked objects and multiplex them in descending order on a 160 MHz output link. This algorithm requires a pre sort unit for the initial sort, where data is received unsorted.

Figure 5. Object sort algorithm of Sort ASIC

The definition of the location identifier is closely related with the data origin. The JSC provides unsorted data for 16 ranked objects on 4 input links. The pre sort unit reorders the input data. The first 2 bits of the identifier specify the 160 MHz clock cycle of the initially received rank. The object sort algorithm appends always the number of the input link to the identifier. This means 2 plus 2 bits additional on the JSC. The input sort module provides data on 6 input links so another 3 bits are added and on the final sort module another 2. This adds up in total to a 9 bit identifier to be passed out to the Global trigger.

The ASIC implementation of the object sort algorithm will be configurable to work on all sort tree levels. The sort ASIC will include pre sort units for four input data links. All data I/O will be true single ended ECL. All I/O pads will be equipped with boundary scan registers.

6. Demonstrator Project

The goal of a demonstrator project is to show the ability to design the technically demanding components of the proposed system. In this case we need to show that we are able to implement the sort algorithm as an ASIC and that it works at the required speed. We also have to demonstrate that we are able to handle a PCB design with 160 MHz clock and data lines for the Sort Module.

Figure 6. Prototype Sort ASIC

A prototype ASIC with the proposed object sort algorithm has been developed. The input data links are 11 bits wide. The data is composed of 8 bit ranks plus 3 bits of location identifier. The object sort circuitry was designed to receive 8 data links, instead of 6 as currently foreseen. However to avoid a pad limited design for the prototype, only the first four are connected to I/O pads. The unconnected data links are wired internally to a small, fixed rank value. The sort processor of the ASIC adds 3 bits to the location information for each output word to identify one of the eight input data links. No pre sort unit or configuration control is included in this version. Single ended PECL pads have been used for the I/O. The input data is translated into TTL, which is used for all internal logic functions. All I/O pads are latched in boundary scan registers. The circuit (figure 6) was developed as schematic design based on the AMS 0.8 μm BiCMOS process library and was successfully built in 1997. A Verilog simulation of the Sort ASIC design works above 200 MHz, with the unimportant boundary scan registers failing first.

We were initially only able to test the function of the ASIC up to 50 MHz on a commercial chip tester. The ASIC performed well and sorted the input data in the expected 2 bunch crossing cycles latency.

The next step was the development of a test system for the sort ASIC, which will be able to test the Sort ASIC up to 200 MHz. The system consists mainly of two modules. The Sort ASIC test mod-
ule, which is shown in figure 7, hosts four pseudo-random test pattern generators, a Sort-ASIC and time demultiplexer. The board receives a variable input clock frequency, which is quadrupled and which is used for all fast components on the board. All fast data links have been implemented as impedance matched lines. The demultiplexed output is connected to a compact connector, of the type which we intend to use in the final system. Data is received on a multi purpose memory module, see figure 8. The module is equipped with four dual-ported RAMs, which can be used to record data at variable frequency up to 50 MHz. The data are then read out over a custom field bus system. The memory board can also be used to provide test patterns, a feature which will be used in a later stage of the project.

Figure 7. Test Module of the prototype Sort ASIC test system

Figure 8. Memory Module of the prototype Sort ASIC test system

The PCBs for the test modules have been manufactured. The components on the boards are currently being assembled. The FPGA-firmware, driver software and a graphical user interface for the custom field bus system have been developed. We expect to start the high speed tests in October.

7. Summary

The CMS calorimeters provide object information and transverse energy sums for use in the Level 1 trigger decision. The Global Calorimeter Trigger crate is required to collect and sort the objects found during Regional processing, and to complete the summing of energy components from the whole calorimetry. The design of this crate is constrained by the need to collect a large number of input data words. We have devised a fast, low-latency sort algorithm which has been implemented in an ASIC. We have also developed a modular test system to exercise trigger components at LHC clock speeds. This system is currently being used to test prototype ASICS, and first results are expected shortly.

REFERENCES

THE NA57 TRIGGER PROCESSOR

F. Antinori\(^1\), H. Beker\(^3\), I.J. Bloodworth\(^2\), D. Evans\(^3\), G.A. Feofilov\(^7\), G.T. Jones\(^2\), P. Jovanovic\(^2\), A. Jusko\(^1\), J.B. Kinson\(^2\), A. Kirk\(^2\), B. Kocper\(^3\), A. Kolovjari\(^7\), I. Králík\(^4\), V. Lupták\(^4\), V. Manzari\(^1\), P.I. Norman\(^2\), F. Piu\(^2\), P. Staroba\(^6\), W.N. Stokes\(^2\), I. Suchodolinská\(^4\), G. Tomasicchio\(^1\), M. Thompson\(^3\), G.D. Torrieri\(^2\), P. Vande Vyvre\(^3\), A. Vascotto\(^3\), O. Villalobos Baillie\(^3\), M.F. Votruba\(^2\), S. Wu\(^2\) and P. Závada\(^6\)

\(^1\)Bari, Italy, Dipartimento di Fisica dell’Università and Sezione INFN
\(^2\)Birmingham, United Kingdom, School of Physics and Space Research, University of Birmingham
\(^3\)CERN, Geneva, Switzerland, European Organization for Nuclear Research
\(^4\)Kosice, Slovakia, Institute of Experimental Physics, Slovak Academy of Sciences
\(^5\)Padova, Italy, Dipartimento di Fisica dell’Università and Sezione INFN
\(^6\)Prague, Czech Republic, Inst. of Physics, Academy of Science
\(^7\)St.Petersburg, Russia, Institute for Physics of St.Petersburg State University

Abstract

The NA57 trigger system provides a testing ground for the concepts of the ALICE trigger. In this report the operation of the trigger system is described, and some results from the first operation of the trigger are given.

1. INTRODUCTION

The ALICE experiment \([1, 2, 3]\) has requirements for the central trigger system quite different from those of ATLAS and CMS. In particular, the ALICE trigger must handle:

(i) **Trigger Priority** - Parallel triggers in which one trigger type is much rarer than another, and therefore receives a high priority. (This is the case with high \(p_T\) dimuon triggers, which have a frequency \(10^4\) times lower than central triggers in Pb-Pb interactions.) Additionally, the signals which the trigger attempts to enhance, \(\Upsilon\) and \(\Upsilon'\) resonances, have a very large background, so the ratio of the \(\Upsilon\) triggers to good central triggers is about \(10^6\) before priorities are applied. In order to maximize the number of \(\Upsilon\)'s available for offline analysis, ALICE aims to record as many as possible of the dimuon high \(p_T\) triggers. It does this by reading out the dimuon system more frequently than the main detector, as discussed in ref. [1]. To do this, the central trigger must determine the trigger type for a given interaction, e.g. dimuon or central, and then check whether the appropriate detector set is not busy. This means that, in general, different detector sets can be read out in consecutive events.

(ii) **Past-Future Protection** - Some of the ALICE detectors have very long sensitive times. For example, the drift time of the ALICE TPC is \(100\mu s\). Events in which the detectors also register tracks from earlier or later interactions are deemed unrecognizable owing to the very high track densities (\(dN/d\eta \approx 8000\) for central Pb-Pb interactions). For this reason it is necessary to apply a past-future protection time, different for each sub-detector system in ALICE, in order to veto events which would be spoilt by pile-up.

The NA57 experiment \([4]\) provides an opportunity to test the above concepts. The principal aim of this experiment is to measure strange particle yields, (a) in Pb-Pb interactions and (b) in pA interactions. These may be selected using a trigger based on patterns of scintillator pulses. In addition, NA57 will take data at the same time as ALICE test detectors. These may be read out separately from or together with the "principal" detectors. This requirement is similar to the requirement for "central" and "dimuon" events in ALICE.

In addition is possible to set past-future protection intervals for each detector. In NA57 the detectors are all based on silicon, and have sensitivity times which are around \(1\mu s\), much shorter than for ALICE. Nevertheless, the past-future protection feature of the ALICE experiment can be tested by imposing appropriate past-future protection times in NA57. However, in order to optimize the timing of events, the trigger starting signal is an incoming beam particle with random arrival time, while in ALICE it is the LHC clock.

2. THE NA57 TRIGGER

The NA57 layout \([5]\) for pA collisions is shown in fig. 1. An incident beam is defined as one in which the beam particle passes through the S2 and S3 beam counters, and does not hit the V3 veto counter. A final trigger is defined by demanding a beam particle in coincidence with signals in four scintillators (SPH1, SPH2, ST2 and SP) placed along the length of the NA57 silicon telescope, as shown in fig. 2. This ensures that at least one track passes through the silicon telescope. This request can be modified by demanding pulse heights consistent with two or more particles in the counters SPH1 and SPH2, which then produces a two track trigger.
The trigger conditions in Pb-Pb are different. The beam is defined by a single quartz Cerenkov counter S2, instead of a system of scintillators. It is set up to select Pb ions. It is not necessary to demand a track (or two tracks) in the telescope, as most events have about 10 tracks. Instead, a global multiplicity requirement is made using a detector array consisting of six radial scintillators ('petals') placed close to the target so as to cover the pseudorapidity interval $1 < \eta < 2$. In each petal, the discriminator fires if at least 10 minimum ionizing particles go through the detector; a central event is one in which at least 5 out of 6 petals fire.

3. **TRIGGER PROCESSOR LAYOUT**

The principle of the NA57 trigger is shown in Fig. 3. It consists of three VME boards. In the first board (BPL) an incoming beam is defined by a coincidence of up to three signals, using a set of predetermined options. In parallel with this, signals from different channels in a detector used to define (i) a central Pb-Pb interaction or (ii) an interaction having a certain minimum number of tracks in pA interactions (i.e. 1 or 2) are processed.

Digital signals from these detectors define an input pattern; a look-up table, the "PETAL matrix" (PTL matrix), contains precomputed decisions for any arbitrary input combination.

In the second board (TMX), these decisions are transferred to a second larger matrix known as the "TRIGGER matrix" (TMX matrix). The trigger inputs and BUSY inputs are strobed, in order to fix, at a unique time, the status of the detectors for a given event. The values are kept in an input register. Six independent
trigger decisions are defined. Notice that at this point the BUSY status of the detectors is not taken into account, i.e. the decisions indicate the trigger class which would be allocated without any constraints on the availability of detectors.

The second step is to check the trigger decision against the BUSY status of the detectors. This is done in a second matrix, called the “BUSY matrix” (BMX matrix). For each trigger type, a list of required sub-detectors is defined through the BUSY matrix. If none of the required sub-detectors is busy, the trigger proceeds and a final trigger class is allocated. The final trigger pattern is written to the output register.

The final trigger is converted to a NIM signal on the third trigger board, the “trigger output” (TOP) board. An event clock signal, which is the OR of the trigger outputs is also generated. An additional feature of the TOP board is to generate a BURST signal, i.e. to specify a period, synchronized with the beam extraction from the accelerator, when valid triggers may occur. The trigger is only enabled when the BURST signal is present.

**Fig. 3** Schematic layout of the trigger logic for the NA57 trigger. The functions performed on each of the three boards BPL, TMX and TOP are shown by the dotted lines.

**Fig. 4** Flow diagram for the definition of the S2 signal.
A menu driven program has been written to set the trigger configuration. For each flow diagram, a sub-menu is defined allowing each of the parameters to be changed and written to a file. In addition, a provision exists to select signals at any one of a number of intermediate points (S2, S2or, S2ck, S2ff, etc.) and send a copy of the signal to oscilloscope outputs where it can be used to check the timing. Table 1 shows, as an example, the sub-menu corresponding to fig. 4. Once a set of configuration values has been defined it can be copied to a reference file so that it can be loaded from a trigger type menu when the control program is initiated.

### Table 1 S2 menu from computer control program, showing adjustable quantities and their current values.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[a]:</td>
<td>DS2_ENABLE=00000000</td>
</tr>
<tr>
<td>[b]:</td>
<td>DS2M_DELAY= 00000000</td>
</tr>
<tr>
<td>[c]:</td>
<td>S2M_DELAY= 00000010</td>
</tr>
<tr>
<td>[d]:</td>
<td>S2D1_DELAY= 00000003</td>
</tr>
<tr>
<td>[e]:</td>
<td>S2D2_DELAY=00000000</td>
</tr>
<tr>
<td>[f]:</td>
<td>CLEAR_COUNTER</td>
</tr>
<tr>
<td>[m]:</td>
<td>DS2</td>
</tr>
<tr>
<td>[n]:</td>
<td>DS2m</td>
</tr>
<tr>
<td>[o]:</td>
<td>S2</td>
</tr>
<tr>
<td>[p]:</td>
<td>S2or</td>
</tr>
<tr>
<td>[q]:</td>
<td>S2ck</td>
</tr>
<tr>
<td>[r]:</td>
<td>S2ff</td>
</tr>
<tr>
<td>[s]:</td>
<td>S2p</td>
</tr>
</tbody>
</table>

[P]: save values to disk; go to previous menu  
[Q]: restore original values; go to previous menu

ENTER MENU ITEM ID:

The trigger boards may also be controlled via a graphical interface, written using Tcl/Tk [6], which has the same functionality. Fig. 5 shows the panel corresponding to the sub-menu of fig. 4. Here, each of the boxes can be selected from the screen, allowing the user to interrogate the system to determine the current value of a given variable and set a new one.

The graphical approach allows easy access to all the steps in the setting up of the trigger. In its current state it allows full access to the trigger functions. In the future, extensive help facilities are planned to aid the user to choose sensible parameter values, and to indicate where parameters are correlated. (For example, in the case of the delays S2M_DELAY and S2D1_DELAY, as discussed above.)

---

Fig. 5 Trigger graphics display for the sub-menu shown in fig. 4. Selecting a box allows its parameter value to be checked and modified.
4.1 Trigger Matrices

Most of the trigger conditions (except the beam definition) are handled through the three trigger matrices TPL, TMX and BMX. A trigger language has been developed in which the logical conditions can be specified. Table 2 gives an example of a matrix script.

Table 2 Example of a trigger matrix for the TMX matrix (see text).

<table>
<thead>
<tr>
<th>TMX_TRIGGER_SPECIFICATION</th>
<th>: LOGICAL OPERATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>; INPUT DEFINITION</td>
<td>TRG_a = S4.PTA.V0*</td>
</tr>
<tr>
<td>BEAM_sc = Input_0</td>
<td>TRG_b = (TRG1sc TRG2sc TRG3sc)2</td>
</tr>
<tr>
<td>PTA = Input_1</td>
<td>TEST1 = TRG4.S4</td>
</tr>
<tr>
<td>S4 = Input_2</td>
<td>TEST2 = BEAM_sc . PTA.TRG1sc</td>
</tr>
<tr>
<td>V0 = Input_3</td>
<td></td>
</tr>
<tr>
<td>TRG1sc = Input_4</td>
<td></td>
</tr>
<tr>
<td>TRG2sc = Input_5</td>
<td></td>
</tr>
<tr>
<td>TRG3sc = Input_6</td>
<td></td>
</tr>
<tr>
<td>TRG4sc = Input_7</td>
<td></td>
</tr>
<tr>
<td>TRG5sc = Input_8</td>
<td></td>
</tr>
<tr>
<td>TRM1 = Input_9</td>
<td></td>
</tr>
<tr>
<td>TRM2 = Input_10</td>
<td></td>
</tr>
<tr>
<td>TRM3 = Input_11</td>
<td></td>
</tr>
<tr>
<td>TRM4 = Input_12</td>
<td></td>
</tr>
<tr>
<td>TRM5 = Input_13</td>
<td></td>
</tr>
</tbody>
</table>

It is in three parts. In the first part, the hardware inputs are associated with logical names. In the second part logical relations are defined; TRGa demands S4 AND PTA AND NOT V0, TRGb demands at least two out of the three inputs TRG1sc, TRG2sc and TRG3sc. Finally, in the third part, the results of part 2 are associated with hardware outputs. A program mload, written in C, parses the script, computes the contents of the trigger matrices as 8-bit words and loads them into look-up tables in the VME boards.

In addition to the six trigger outputs described above, the TMX matrix allows two further test outputs to be defined. These do not give rise to further trigger classes, but are nonetheless monitored via scalers. They pose no additional overheads in computation time. Their purpose is to allow additional coincidences to be studied, e.g. for trigger development purposes, without disturbing any trigger classes already defined.

4.2 Monitoring

A number of different options for monitoring have been provided. The propagation of signals through the trigger electronics may be monitored using the two oscilloscope outputs, as described above.

Table 3 Scaler output for a single burst, from the trigger control program.

```
S2_COUNTER=01343590  DS2_COUNTER=00000000  S3_COUNTER=01519437
DS3_COUNTER=00000000  V3_COUNTER=00287083  BEAM_COUNTER=01341332
PT1_COUNTER=00000000  PT2_COUNTER=00000000  PT3_COUNTER=00102783
PT4_COUNTER=00000000  PT5_COUNTER=00000000  PT6_COUNTER=00000000
PT7_COUNTER=00000000  PT8_COUNTER=00000000

S4_COUNTER=01205962  V0_COUNTER=00000000  TEST1_COUNTER=00085842
TEST2_COUNTER=00085785  TRG1_COUNTER=00000000  TRG2_COUNTER=00000000
TRG3_COUNTER=00000000  TRG4_COUNTER=00000000  TRG5_COUNTER=00000000
BEAM_COUNTER=00000000

CTR1_COUNTER=0001182  CTR2_COUNTER=0001182  CTR3_COUNTER=0001182
CTR4_COUNTER=00000000  CTR5_COUNTER=00000000  CTR6_COUNTER=00000000
EVENT_COUNTER=0001182
```
In addition, the number of events for each of the inputs and outputs is recorded. For each valid trigger, the values of the input and output registers are copied to a buffer. The integrated time during which the BUSY signals from each detector are present is recorded. All these values are read out between bursts and are written to the end-of-burst record. Table 3 shows the output from monitoring the scalers for a single burst, taken from the trigger control program. In addition, a copy of the trigger output pattern is written to a FIFO, where it may be read out at any time. This is done so as to allow the trigger output to be read out for each event and written to the event record. If different trigger classes with different sub-detector requirements are running concurrently, the FIFO output is needed in order to specify, for a given event, which detectors should be read out.

5. RESULTS

The new trigger system was tested during NA57 data taking in September 1998. Figure 6 shows the trigger latency. In this example, it takes 91 ns to generate the BEAMd signal from the beam counter inputs; it takes a further 54.8 ns to propagate signals through the TMX and BMX matrices and obtain a final trigger. Only the second delay contribution is directly relevant for ALICE, where the LHC clock takes the place of the BEAMd signal. The trigger decisions were compared with those from a trigger system based on NIM electronics which already existed in NA57. It was found that the two agreed in 98% of cases, the residual disagreement being attributed to a difference in the past-future protection intervals for the two triggers.

6. CONCLUSIONS

A new trigger system has been built and operated in the NA57 experiment. It has been shown to provide decisions compatible with those from the original NA57 trigger in a mode of operation in which all detectors contribute to every event. In the new system, it is also possible to read out different detector sets in consecutive events, according to the trigger type. The full trigger latency was found to be 146 ns, of which only 55 ns were used to propagate through the trigger matrices. This is already close to the requirement for ALICE.

Preparations are in progress to test the trigger system further in 1999, allowing trigger classes to require different sub-detector sets. In addition, further development of the control software, in particular to provide an interactive help facility, is being studied.

REFERENCES

1 ALICE Proposal CERN/LHCC 95-71 LHCC/P3 (1995); CERN/LHCC 96-32 LHCC/P3 Add. 1 (1996)
6 J.K. Ousterhout Tcl and the Tk Toolkit, Addison Wesley 1996
OPTOELECTRONICS
AND DATA TRANSFER SYSTEMS
Optically activated GaAs devices for MSGC cathode strip high-voltage control in the CMS tracker

M.G. Bisogni (bisogni@pisa.infn.it), M.E. Fantacci (fantacci@pisa.infn.it), Universita' and INFN, Pisa, Italy
A.Cola (cola@axpmat.unile.it) Istituto per lo Studio di Nuovi Materiali per l’Elettronica (IME), CNR, Lecce, Italy
M.Conti (conti@napoli.infn.it) Universita' and INFN, Napoli, Italy
G.Stefanini (stefanini@cern.ch), CERN, Geneva, Switzerland

Abstract
Optically activated devices are being developed for the switching and control of the cathode-strip high voltage (≈520V) of Micro Strip Gas Chamber (MSGC) in the CMS tracker. The devices consist both of GaAs bulk reverse-biased Schottky diodes and planar photoresistors, which conduct when illuminated by Vertical Cavity Surface Emitting Lasers (VCSELs). We believe that certain features of the devices described here, and their specific application, are novel in the domain of the detectors for High Energy Physics. We discuss the principle of operation for HV switching and possibly fine tuning. We overview the design of bulk and planar GaAs test devices, and present the results of radiation measurements with neutrons and pions.

The optimisation of the device geometry is discussed. The design concept of a hybrid package, under development in collaboration with two industrial companies, is presented.

1. INTRODUCTION
The outer volume of the CMS tracker consists of 6 barrel layers and 11 disks (per end-cap) of MSGCs, for a total of 6.6x10^6 strips. On a MSGC module substrate, the cathode strips are connected to the bias voltage (≈520V) in groups of 32 strips each one [1]. The strips cluster draws a current of less than 100 nA in normal operating conditions. It is requested that any one group can be individually deactivated by a suitable HV switching device if an overcurrent is detected in that group. The overall number of switching devices is therefore about 200,000.

Moreover, the MSGC tracker elements must survive a total dose of around 1 Mrad and 1x10^9 neutrons/cm² (1 MeV equivalent) integrated over the nominal period of 10 years at the maximum luminosity [2].

The requirements on the HV switches in terms of post-rad hold-off HV and leakage current (not higher than the strips current) are particularly challenging and we could not find any commercial device that would match them.

We have recently started to develop a custom device in which the switching element is a GaAs Schottky diode reverse biased at the cathode strip HV or a planar GaAs photoresistor.

The device leakage current does not increase above a few tens of nA even after irradiation. The switch is optically activated by illuminating it with an IR light source at 850 nm wavelength [3]; this causes a considerable decrease of the device internal resistance and the corresponding group of strips is short-circuited to ground.

In this paper we first describe the cathode strip switching configuration chosen on the basis of general feasibility considerations. The design and fabrication of proof-of-principle test devices, in bulk and planar geometry, are reviewed. Preliminary results of irradiation measurements at neutron and hadron fluence exceeding far by those expected in the MSGC tracker are reported.

The optimisation of the device geometry and the design concept of a complete low-mass hybrid package, under development with two industrial companies, are presented.

2. FEASIBILITY STUDY
2.1 GaAs devices description
ALENIA S.p.A. developed bulk devices on SI-LEC GaAs 200 μm thick substrate. Eight square Schottky pads (dimensions from 70 x 70 μm² up to 170 x 170 μm²) are deposited on one side at 520 μm pitch (fig. 1a). On the other side an original ohmic contact allows to bias the GaAs diodes up to 1kV before breakdown [4].

Planar photoresistors were developed by the IME-CNR starting from SI-VGF wafers 200 μm thick [5]. In fig. 1b the shape and dimensions of the contacts are shown. The common contact is a standard Schottky contact comb shaped. Four individual Schottky
contacts constitute the cathodes of the device: they are spaced by 500 μm and they are 600 μm away from the anode.

2.2 Experiment

As proof-of-principle, we started to test our switches on a small prototype of MSGC. The detector consisted of 128 cathode strips for a total active area of 2.54 x 2.54 cm². A 64 strips group was put in parallel with a GaAs device and biased via a 10 MΩ current limiting resistor at Vc = -520 V (see fig. 2). To compare the performance of the MSGC-switch assembly, the other 64 strips were connected directly to Vc.

Figure 2 Electrical connection of the GaAs diode to a 64 cathode strips cluster of the MSGC prototype.

In normal operating conditions the GaAs diode resistance is of the order of 10¹⁰ Ω and the voltage drop across the resistor is negligible. Therefore, the bias voltage applied to the strips V_{APPL} is almost equal to Vc. When the diode is illuminated with an AlGaAs LED (nominal wavelength of 880 nm), its resistance decreases to 10⁷ Ω; hence, V_{APPL} drops far below the MSGC multiplication regime and the strips result short-circuited.

2.3 Results

The detector was exposed to a Fe⁵⁷ source, which emits 6 keV photons, and the signal coming from two strips was monitored on a digital scope (figure 3a). The upper curve represents the signal from a strip in the cluster connected to the switch. The lower curve is the signal of a not connected strip. When the LED is “off”, the two signals are quite similar in width and amplitude. By switching on the LED, the signal from the connected strip disappears while the other one does not change appreciably (fig. 3b).

Figure 3 (a) Upper curve: signal from a strip connected to the switch. Lower curve: signal from a not connected strip in case of “LED off”. (b) The same curves when the LED is turned-on.

In figure 4 the behavior of V_{APPL} as a function of the LED forward current is plotted. As can be seen, the V_{APPL} was reduced at almost one half of V_{BIAS} at the maximum forward current I_{LED}=100 mA.

Figure 4 the voltage applied to the strips as a function of the forward current of the LED.

At this current value, the P_{OC} incident onto the diodes was only 10 μW due to the low conversion efficiency and large beam divergence (θ = 90°) of the LED.
amplitude of the signal carried out by the connected strip, \( V_{\text{Signal}} \), is linear with \( I_{\text{LED}} \). This behavior suggests the possibility to perform a fine-tuning of the MSGC gain.

3. RADIATION DAMAGE TESTS

3.1 Neutron irradiation

Neutron tests were performed at the SARA facility of the ISN in Grenoble [6]. Various GaAs samples were exposed to the 6 MeV neutron flux in two 60 hours irradiation cycles. The total fluence on the GaAs diodes was of about \( 2 \times 10^{14} \) cm\(^{-2} \) [7]. In figure 6 we report the leakage current of a device as a function of the bias voltage. The curves refer to measurements done before (filled squares) and after (filled dots) the irradiation tests. The same figure also shows the current drawn by the GaAs diode when illuminated with the AlGaAs LED before (empty squares) and after (empty dots) the neutron exposure.

![Figure 5: Amplitude of the signal as a function of the forward current of the LED.](image)

3.2 Pion irradiation

The pion tests were undertaken at the Paul Scherrer Institute (PSI/Villigen) [8] on GaAs samples similar to those used for the neutron tests. The high intensity \( \pi E1 \) beamline produces a \( \pi^+ \) beam at 300 MeV/c from a primary proton beam. The pion fluence on the GaAs diodes over 230 hours was of about \( 6 \times 10^{14} \) cm\(^{-2} \) [7]. In figure 7 we report the leakage current of a device as a function of the bias voltage. The curves refer to measurements done before (filled squares) and after (filled dots) the irradiation tests. In the same figure is also shown the current drawn by the GaAs diode when illuminated with the same LED before (empty squares) and after (empty dots) the pion exposure.

3.3 Discussion

The diodes have been irradiated at dose levels higher at least by a factor of 10 than those anticipated in the MSGC section of the CMS tracker. The leakage current increases slightly but remains within acceptable limits, comparable to the intrinsic MSGC strip leakage, even in these extreme conditions as observed also by previous measurements on GaAs particle detectors [9, 10].

The photocurrent, produced by illuminating the diode by an IR light source, is a factor of 10 smaller than before the high fluence irradiation. Previous works on GaAs particle detectors shown that the Charge Collection Efficiency decreases with the radiation dose [11, 12]. Even if the optical responsivity (light current vs incident optical power) of the GaAs is specific to our application, these results could be taken to explain the large decrease of the photocurrent with the radiation dose.

![Figure 6: Leakage current before (filled squares) and after (filled dots) the irradiation tests.](image)

![Figure 7: Leakage current before (filled squares) and after (filled dots) the irradiation tests.](image)

Anyway, by increasing the optical power incident on the diode, the photocurrent loss due to the radiation damage could be partially retrieved. This can be done by illuminating the GaAs diode with a Vertical Cavity Surface Emitting Laser (VCSEL) which shows a much higher conversion efficiency with respect to a LED.
Therefore, we illuminated our GaAs prototypes with the Honeywell VCSEL interfaced to a multimode fiber. The plot represented in figure 9 was obtained by scanning the beam spot at 100 µm steps. The distance of the diode from the fiber output was 6.2 mm. From this plot the beam divergence results of about 9° (FWHM).

The beam from the VCSEL was then focused by means of a lens and the spot was about 100 µm. Figure 10 shows the photocurrent as a function of the incident optical power. The current is linear with the P_{OC} and high enough to short-circuit the chamber even for low P_{OC} values.

4. VCSELS TESTS

A VCSEL is made up on an n-type-doped GaAs substrate. The basic structure consists of two mirrors made up of alternating quarter-wavelength-thick layers of AlAs and AlGaAs. The bottom mirror is doped n-type and the top one is doped p-type. An active layer between the mirrors contains p-n junction, which generates the light. The junction is made from several GaAs quantum layers between AlGaAs barrier layers (quantum well) [13].

The active region is one wavelength (850 nm) and the whole chip is a 0,5 mm cube. The optically active region is smaller in a VCSEL than in a laser diode, thus reducing the radiation damage.

Figure 8 presents a plot of the output power of a Honeywell VCSEL (HFE4380). As can be seen the low threshold current (≈ 4 mA) and the high P_{OC} values above the threshold make the VCSEL the ideal driver for the GaAs diodes [14].

5. HYBRID PACKAGE DESCRIPTION

The HV system must be integrated in the overall Front-End control system by taking in account the high number of channels foreseen to cover the whole tracker, the power dissipation and the material budget.

The best match in terms of package issues would be obtained by directly coupling arrays of GaAs diodes to arrays of VCSELS.

As shown in figure 11, the general structure of the package proposed consists of an array of four VCSELS and four GaAs diodes.

A linear array of four Schottky pads at 250 µm pitch is realized onto a 200 µm thick substrate of SI-LEC GaAs. Each Schottky pad will be connected to a 32 strips cluster and biased a -520 V via a limiting resistor. On the other side of the crystal, four drilled ohmic pads are realized.

An array of four VCSELS is realized under the GaAs switches array. Each VCSEL is aligned with a hole on the GaAs ohmic contacts in order to optimise the light collection.

A high resistivity silicon or alumina spacer with etched holes is interleaved between the two arrays.

The volume of the hybrid package will be about 2 mm³.

To control 16 groups of strips in a MSGC four packages are foreseen.

An ASIC called HVSD (High Voltage Switch Driver) has been designed to drive 16 VCSELS using the information coming from the APV (overcurrent alarms) on dedicated pins (4 for each APV) [2]. If the HVSD is enabled, it switches off a cluster of strips.

Figure 8 Optical power from the VCSEL coupled to a fiber as a function of the bias current

Figure 9 Surface plot of the VCSEL beam spot obtained by scanning the beam with a GaAs diode. The scan step is 100 µm.

Figure 10 Photocurrent drawn by the GaAs diode as a function of the incident optical power.
The handshake between HVSD and CCU follows the Philips I2C standard.

![Figure 11 Hybrid package sketch.](image)

6. CONCLUSIONS

A system of GaAs diodes optically activated by an IR light source has been proposed as MSGC cathode strips HV control for the CMS tracker. Preliminary structures with tentative geometry have been developed as switching devices.

Measurements done on a small test chamber provided the proof-of-principle for the use of these devices for the application proposed.

Moreover, the irradiation tests at very high dose levels shown that these diodes can hold off the operating voltage (-520 V) with a slight increase of the leakage current. The loss in responsivity could be attributed to the Charge Collection Efficiency decrease due to the radiation damage. This loss could be partially recovered by increasing the optical power incident on the diodes.

Using VCSELs to drive the GaAs diodes could easily do this. Measurements of the GaAs diodes optical response to VCSEL illumination shows that low optical power values are enough to short circuit an MSGC.

A compact package where a VCSELs array is coupled to a GaAs diodes array was proposed and it is actually under development.

7. REFERENCES


A 4-channel parallel analogue optical link for the CMS-Tracker

CERN, Geneva, Switzerland (email: francois.vasey@cern.ch)

Abstract
A radiation-hard, 4-channel wide parallel optical link has been developed for the analogue readout of the CMS-tracker detector. It is based on edge-emitting laser transmitters and pin photodiodes aligned to single-mode fibres on Si-submounts and housed in custom developed 4-way ceramic packages. The operating wavelength is 1310nm. Experimental results obtained with prototypes closely resembling the final system are presented. Measurements of dynamic range, linearity and bandwidth are shown, together with first results of inter-channel crosstalk. The resistance of the laser transmitter module to neutron irradiation is also reviewed.

1. INTRODUCTION
A radiation-hard, 4-channel wide parallel optical link has been developed for the analogue readout of the CMS-tracker detector (Fig. 1). It consists of a monolithic quad-laser driver ASIC followed by a hybrid assembly of 4 InGaAsP/InP edge emitting lasers housed in one single custom-developed low-mass, non-magnetic package. Single-mode optical fibre ribbons transmit the light at a wavelength of \( \lambda \approx 1310\text{nm} \) over a distance of approximately 110m, through 3 patch panels based on angle-polished MT-connectors. On the receiver side, four InGaAs/InP pin photodiodes housed in a package identical to the laser module are followed by 2-stage transimpedance amplifiers based on commercially available, single-channel discrete ICs. Altogether, about 50000 optical links will be required to read-out the CMS tracker.

Results of performance and radiation hardness tests of individual components and single-channel optical links have been previously published [1]. This paper reports for the first time on the performance of a full length 4-channel parallel link, which closely resembles the final CMS-tracker optical readout system. Static and dynamic performance of the complete link are presented in section 2, together with first results of inter-channel crosstalk. The resistance of the laser module to neutron irradiation is briefly reviewed in section 3, while the evolution path towards the final system is sketched in section 4.

2. LINK PERFORMANCE
2.1 Link under test
Most of the components used to build the parallel optical link have been described previously [2,3,4] and single channel link demonstrators have been characterised and distributed to the CMS community [5, 6]. However, it is the availability of a 4-way package, custom developed by Italtel Milano [7] which has made this more realistic evaluation possible.

![Fig. 1. 4-channel parallel analogue optical link prototype](image-url)
The Italtel 14-pin ceramic DIL package houses up to four (known good) laser or photodiode assemblies in a volume of approximately 15mm x 10mm x 4mm. With the exception of the leadframe (still to be optimised), it contains no metallic parts and is thus low-mass and non-magnetic. A bundle of 4 standard telecom-grade single-mode fibres exit the package through a ceramic ferrule, and are terminated by an angle polished MPO connector. Three pairs of 4-way transmitters and 4-way receivers have been tested. The lasers have an average threshold current of 10.3mA and a slope efficiency of 0.059W/A at 25°C, while the photodiodes have an average responsivity of 0.93A/W. A diagram and photograph of an open 4-channel receiver are shown in Fig. 2.

The working point and operating range of the tested links have been set to closely match the system specifications [8]: a laser driver transconductance of approximately 6.3mS converts the full range input swing of ±400mV into a laser optical output signal of approximately 300µW amplitude. This signal corresponds on the receiver side to an output swing of almost 4.2V into a high impedance load. If one includes 2dB of optical loss for the three in-line patch panels, the output swing becomes 2.65V, or 1.33V into a 50Ω load.

### 2.2 Experimental set-up

The experimental setup used to characterise the parallel optical link is shown in Fig. 3. It consists of pairs of generating and measuring instruments linked via GPIB to a computer running labview software. For the static characterisation, an arbitrary waveform generator and an oscilloscope are used; the dynamic characterisation is performed with a tracking generator coupled to a spectrum analyser; a pulse generator, together with an oscilloscope, are used to evaluate crosstalk. For high resolution measurements such as linearity, a 12bit A to D converter on a VME board is used. Also hooked on the VME bus is an I2C interface board which controls the laser driver and allows individual setting and adjustment of the lasers working points. The I2C bus remains idle during link measurements.

The laser driver ASIC features differential inputs. However, to ease the interface with laboratory instruments, only one input is active in this test, while the other one remains grounded.

On the receiving side, all outputs are terminated with 50Ω to ground, resulting in a 50% reduction of link net gain. It has been experimentally demonstrated that when integrating the receiving amplifiers close to the A to D converters on the Front End Drivers, this termination can be removed, thus eventually allowing to recover the full gain of the readout chain.

### 2.3 Static characterisation

The measurement procedure of the optical link static transfer characteristic consists in scanning the laser driver input voltage and, for about 100 input points, measuring the DC value and standard deviation of the receiver output voltage.

The static transfer characteristics of the 12 tested optical channels are shown in Fig. 4 for an input voltage range slightly exceeding the nominal value of ±400mV. The kink at very low input voltages is due to the laser being operated below threshold. Even though this could be easily avoided by adjusting the laser bias point, it is useful in the characterisation phase to have an absolute reference point indicating the operating conditions of the system. The measured link gains (outputs terminated with 50Ω resistors) range from 0.98 to 1.7 V/V, with an average value of 1.2 V/V. This spread is essentially caused by the inhomogeneity in the insertion losses of the three in-line connectors.

---

**Fig. 2.** 4-way Rx module internal configuration

**Fig. 3.** Experimental setup for link performance evaluation
To evaluate the system linearity, a regression line is drawn between the working point and a calibration point selected on the static transfer characteristic, within the operating range of the link. The relative deviation from linearity is defined as the normalised error between the output signals extracted from the transfer characteristic and those predicted by the regression line. In the present evaluation, the calibration point has been chosen to be 250mV above the working point (input voltage = -0.15V) for all channels. The calculated relative deviation from linearity is plotted in Fig. 6 as a function of input voltage. It is zero at the calibration point, and practically does not exceed 2.5% in the link full operating range. This figure is however dependent on the specific choice of the calibration point, and has not been finely optimised in this example. Around the working point (\(X_{\text{w}}=-0.4V\)), the relative deviation from linearity diverges as the signal reaches zero. Below the working point, the linearity is degraded by the laser approaching threshold; above the working point, it is essentially determined by the laser driver static transfer characteristic.

The system signal to noise ratio is obtained by dividing the output signal (extracted from the static transfer characteristic) by the output noise (from the output noise characteristic). As can be seen in Fig. 7, peak signal to noise ratios in excess of 350:1 are achieved for all measured channels (at \(X_{\text{w}}=+400mV\)), with the best link reaching a value close to 600:1. As was the case for the deviation from linearity analysis, the signal to noise ratios shown here are dependent on choice of working point, and could be further optimised on a channel by channel basis.

In order to assess the impact of the optical link on the total noise of the CMS-tracker readout chain, one must map the output range of the front-end chip into the input range of the optical link. Assuming an 8MIP dynamic range would correspond to the 800mV input range of the
system described here, then the equivalent input noise generated by the optical link would for instance be less than 0.023MIPs for all channels.

Due to the pulsed nature of the signal transfer scheme used for the CMS tracker, the crosstalk (or relative feedthrough from one channel to its neighbour) is defined at sampling time $t \geq 20ns$ for a step input injected at $t=0s$. Even though some feedthrough is apparent during the few nanoseconds after the step edge, very little effect remains visible after 20ns. We measure typical crosstalk values of about -63dB, in no cases exceeding -55dB.

2.6 Summary of test measurements

We compare in Table 1 the results presented in this section with the system specifications [8]. The 12 tested prototype channels all meet the objectives of the CMS tracker readout system.

3. RADIATION HARDNESS

With the exception of the laser-driver ASIC, which is still integrated in a radiation-soft technology, all opto-electronic front-end components have been validated for radiation hardness. Single-channel laser-transmitters [10], standard telecom-grade optical fibres [11] and multi-way MT connectors [12] have shown good resistance to levels in excess of the CMS-tracker requirements. Figure 9 shows the normalised degradation of laser threshold current and efficiency as a function of neutron fluence for a 4-channel module. As expected, the results are similar to the ones obtained with single channel devices. Fluences (integrated over the lifetime of the CMS experiment) to be expected at the innermost Si-tracker layers are $\sim 10^{14}$neutrons/cm² (1MeV) and $1.6 \times 10^{14}$ charged hadrons/cm² [13] (mainly charged pions, $10^7$ - $10^9$ MeV, found to be almost 4 times more damaging than neutrons (6MeV) [10]).
4. CONCLUSION

With the demonstration of a functional and radiation-hard 4-channel parallel analogue optical link, the baseline for the CMS-tracker optical readout system is set:

- Assemblies of edge-emitting lasers, pin photodiodes and optical fibres on silicon submounts are the basic building blocks of the optical link transmitters and receivers. They can be individually tested for performance and radiation hardness, packaged into one-way or multi-way housings, or possibly even assembled directly onto hybrids or printed circuit boards. This flexibility in the packaging scheme allows testing and validation of opto-electronic components in submount form before the full details of the system architecture and implementation are known, and before a final package or hybrid has been selected and designed.

- Standard telecom-grade single mode fibre ribbons link front-end to back-end. They are connected in three points with MT-compatible connectors to ease installation, test and maintenance of the detector.

Three 4-way parallel analogue optical links closely resembling the final CMS system have demonstrated a performance complying with the specifications. The custom developed 4-way package used both for the transmitter and receiver modules has been successfully tested for mechanical robustness [7], and will be subjected to magnetic field tests in the coming months. Irradiated and non-irradiated lasers and pins are currently undergoing accelerated ageing tests. Up to this day, no significant degradation effects have been observed in more than 1200 hours of operation at 80°C.

Work is in progress to better adapt the link modularity and density to the needs of the CMS tracker. In particular, projects with industrial partners have been launched to increase the density of the optical patch-panel, multi-ribbon cable and receiver modules.

5. REFERENCES


[7] M. Magliocco, P. Nugent, "Four channel fibre optic transmitter and receiver modules for CMS detector tracker readout links", these proceedings.


Development of Radiation-hard VCSEL/PIN-diode Optical Links for the ATLAS SCT

D.G. Charlton, J.D. Dowell, R.J. Homer, I.R. Kenyon, G. Mahout, H.R. Shaylor, J.A. Wilson
Birmingham University, U.K.
A. Rudge
CERN, Switzerland
D.J. White
DRAL, U.K.
R.B. Nickerson, J. Fopma, I. Mandic, P.D. Shield, R.L. Wastie, A.R. Weidberg
Oxford University, U.K.

Abstract

A summary of the architecture of the ATLAS SCT optical links is given. The radiation-hard, low mass packaging techniques are described. The performance of VCSELs in these type of packages is discussed. Detailed tests of these links are presented in this and the following paper.

1. LINKS ARCHITECTURE

Optical links will be used for the readout of the 4088 modules of the ATLAS SemiConductor Tracker (SCT)[1]. The components in the system are illustrated schematically in Figure 1 below.

Data will be readout by two data fibres each transferring data at 40 Mbits/s. The Timing, Trigger and Control (TTC) Data for each SCT module will be distributed to the modules by optical fibre. Bi-phase Mark encoding will be used to encode the control data on top of the 40 MHz bunch crossing clock. In this scheme a 20 MHz clock is sent and extra transitions are used to encode "1"s in the data as illustrated schematically in Figure 2 below.

![Figure 2 Bi-phase mark encoding of TTC data.](image)

The links are based on radiation-hard VCSELs and PIN diodes. The radiation-hardness of the components are described in the following paper. The VCSELs will be driven by a simple VCSEL driver chip (VDC), which is a slightly modified version of the LED Driver Chip (LDC)[X]. The PIN diode signal is received by the DORIC chip[2]. The DORIC chip has a low noise pre-amplifier followed by circuitry for decoding the Bi-phase mark TTC data to provide the 40 MHz bunch crossing clock and the commands for the SCT module.

The DORIC chip and the VCSEL driver chip (VDC) have been designed in the AMS 0.8 μm BiCMOS process.

This is not usually used as a radiation hard process but a radiation hard design has been made by

- using bipolar npn transistors only
- operating the transistors with relatively large currents such that the DC current gain $\beta$ is large and less sensitive to radiation damage.
- Using a design in which the circuit is very insensitive to changes in $\beta$.

Immunity to single point failure is provided in the system: if a data link fails then the data can be routed through the other fibre of that module. If a TTC link fails, the TTC data can be taken from a neighbour module.

## 2. OPTO-PACKAGES

### 2.1 Existing LED/PIN Package

A radiation-hard, low mass, non-magnetic package containing two LEDs and one PIN diode has been produced by GEC. The scheme is illustrated in Figure 3 below.

![Figure 3 GEC Silicon package for LED/PIN.](image)

The opto-package is mounted on a ceramic hybrid circuit which also contains the LED driver chip (LDC) and the DORIC chip. The LEDs are wire bonded to the LDC and the epitaxial Silicon PIN-diode is wire bonded to the DORIC chip. The ceramic hybrid is wire bonded down to a flexible kapton cable which allows for electrical connection to the SCT module and to connect to the low mass Aluminium tape carrying the DC voltages[1].

### 2.2 Proposed VCSEL package.

As the VCSELs are surface emitting devices like LEDs, similar types of packaging can be used. Since the light output of VCSELs is more focussed than for LEDs there is no need for the micro-lenses. Since the light output is much larger for VCSELs than LEDs it is possible to trade-off coupling efficiency for ease of assembly. The proposed package for VCSELs which will be prototyped is illustrated in Figure 2 below.

![Figure 4 Proposed VCSEL/PIN Silicon package.](image)

The light from the VCSELs is coupled into the fibre via the silicon lid which is cut at a 45° angle. The VCSELs are aligned relative to the marks on the Silicon base plate and the fibre is aligned by the v-groove in the Silicon. Hence no active alignment is required.

### 3 VCSELs

#### 3.1 Use of VCSELs

There are many advantages of VCSELs for this application. The most important are:

1. VCSELs are an extremely radiation hard technology[3] and therefore they can be used for both the SCT and the Pixel detector. The VCSELs used by ATLAS operate at a wavelength of 850 nm which allows for the use of Si PIN diodes for the link receiver. For the TTC links the VCSELs will be in the counting room whereas the PINs will be on the detector and hence receive large radiation doses. Epitaxial Silicon PIN diodes are extremely radiation hard [4],[5].
2. VCSELs are much brighter than LEDs, which greatly simplifies the other end of the optical link.
3. As VCSELs are surface emitters they can be packaged in a similar way to LEDs as discussed in section 2.2 above.
4. Manufacturer's data on lifetime of VCSELS indicate lifetimes greater than $10^7$ hours at 40°C. Tests of VCSEL lifetime after radiation have also shown very good results[6].

3.2 Tests of packaged VCSELS

Bare chip VCSELS from MITEL\(^1\) have been packaged by GEC in the same Silicon package as used for LEDs (see Figure 3) and the same driver chip (LDC) was used. The VCSELS were easy to couple into the 50 micron core multi-mode fibre and were very easy to operate at the required 20 MHz speed. The laser threshold was about 4 mA and the best operation was achieved with a small bleed current of about 1 mA. It was not necessary to bias the laser on which simplifies the driving electronics. The LI curves for the two VCSELS in the package are shown in Figure 4 below.

4 SYSTEM TESTS OF OPTICAL LINKS

In order to test the two way optical links Bit Error Rate (BER) tests were performed of the TTC and data links.

\(^{1}\) MITEL VCSEL 1A440.

4.1 TTC Links

The DORIC chip decodes the BiPhase Mark data by generating the 40 MHz clock from the incoming data stream and using this back edge of this recovered clock to gate in pulses generated from the extra transitions in the input signal which correspond to a "1" bit. The width of these pulses is only 2 ns wide so the timing of the delay, $\Delta T$ between the back edge of the clock and the data is critical. This is illustrated in Figure 6 below which shows the BER versus delay time $\Delta T$.

![Clock to data edge (ns)](image1)

![Clock to data edge (ns)](image2)

Figure 5 Optical power coupled into 50 $\mu$m core fibre with MITEL VCSELS in GEC package.

One of the VCSELS has the fibre 50 $\mu$m back from the VCSEL and the other has the fibre 1000 $\mu$m back. Both channels worked well and there is a trade off possible between coupled power and alignment precision. Rise and fall times of the order of 1 ns were achieved and were only limited by the speed of the driver chip.

There is an approximately 2ns wide window in which a very low BER can be achieved. With the timing optimised a long run was performed and demonstrated that the BER was less than $2 \times 10^{-6}$. This requirement for the very precise timing required the construction of a special VME timing module and would not be practical in a large system. A new version of DORIC has been designed which removes this problem and allows the window for the capture of data to be 12.5ns wide.

The dynamic range of DORIC is illustrated in Figure 7 which shows the BER vs input optical power.
At low values of the input optical power, errors are caused by the increased jitter of the recovered clock due to the low signal to noise ratio. At the highest values of input optical power, errors are caused because the preamplifier starts to saturate and hence the timing of the recovered clock is degraded. It is interesting to note that the performance of a DORIC irradiated to $2 \times 10^{14}$ n/cm$^2$ (at ISIS) and $3 \times 10^{15}$ p/cm$^2$ (at the CERN PS) show the same noise performance as the unirradiated devices. The existing DORIC chip was optimised for the low light levels expected from LEDs whereas the new DORIC has been optimised for the much larger signals expected from VCSELs. Therefore the new DORIC requires a lower gain and will therefore have a higher dynamic range.

4.2 Data Links

The results of a BER versus optical power scan for the data links are summarised in Figure 8 below. The optical power was adjusted by controlling the LED forward current with the LDC chip. The receiver amplifier was AC coupled and BER measurements were done for two values of the receiver bandwidth. The BER versus optical power gives a good fit to a Gaussian distribution. Although there were no significant sources of non-Gaussian noise the value of the noise is considerably grater than that derived from measurements of the receiver alone and this discrepancy is under investigation. These results show that the required BER of below $10^{-10}$ can be achieved with the optical power as low as $4 \mu$W. This power can be achieved with LEDs and trivially with VCSELs. In the ATLAS application, the occupancy of the link will vary from near zero to close to 100%, so the use of the NRZ scheme implies the need for DC coupled links. A test was made of a DC coupled link by removing the AC coupling capacitor: with an input optical power of 20 $\mu$W and the 100 MHz bandwidth, the operation was stable over a 64 hour period and the measured BER was $4 \times 10^{-12}$.

Figure 7 BER versus optical power received by the PIN. Low BER values ($1.9 \times 10^{-10}$) are 90% C.L. upper limits corresponding to observing 0 errors in a 30 seconds measurement.

Figure 8 Results of BER versus optical power measurements.

4.3 Cross-Talk Measurements

In the SCT architecture there are two emitters (VCSELs) and one receiver (PIN-diode) on the same silicon package. It is therefore essential to check that cross-talk between the emitters and the receivers is not a problem. The cross-talk was measured by setting the LED current amplitude to 20 mA and pulsing the LDC with 20 MHz pulses from a pulse generator. At the same time the BER of the TTC links was measured as a function of the input optical power received by the PIN diode. The results of these measurements are given in Figure 9 below. Although there is measurable cross-talk a safe operating regime can be found for the two way links. The dominant source of bit errors occur when "1"s are wrongly decoded as "0"s due to time jitter on the back edge of the recovered clock. This effect is illustrated in Figure 10 below where the BER is plotted as a function of jitter on the back edge of the clock. Roughly the same value of the BER is observed at the same value of the jitter independently as to whether the LEDs are pulsed.

The effects of cross-talk will be greatly reduced with the new DORIC because

\[ \text{NRZ (Non-Return to Zero) was chosen to minimise emitter on- time and hence maximise lifetime.} \]
the large time window (12.5 ns) will make it very insensitive to jitter

- the gain of the pre-amplifier will be lowered to make it suitable for operation with the larger light signals obtained from VCSELs.

5 CONCLUSIONS

The ATLAS SCT optical links architecture has been described. A suitable low mass, radiation-hard package has been developed. Tests of VCSELs show them to be ideally suited for application in the LHC environment and they will be used for optical links in ATLAS. BER tests of the TTC links gave very good results and currently being used in system tests of the ATLAS SCT modules.

6 ACKNOWLEDGEMENTS

Financial assistance from the UK Particle Physics and Astronomy Research Council is acknowledged. We thank Dr. Jon Hall of GEC-Marconi for many useful discussions.

7 REFERENCES

4. J.D. Dowell et. al., “Irradiation Tests of Photodiodes for the ATLAS SCT Readout”, ATLAS internal note INDET-No-200. Accepted for publication in Nucl. Instr. And Meth. A.
Tests of Prototype ATLAS SCT Data Links

D.G.Charlton, J.D. Dowell, R.J.Homer, I.R. Kenyon, G.Mahout, H.R. Shaylor, J.A.Wilson
Birmingham University, U.K.

A. Rudge  CERN, Geneva, Switzerland.

J. Fopma, I. Mandic, R.B. Nickerson, P.D. Shield, R.L. Wastie, A.R. Weidberg
Physics Department, Oxford University,
D.J. White Rutherford Appleton Laboratory, U.K.

Abstract
An Octal receiver block has been developed for the readout of the ATLAS SCT. Measurements of noise and frequency response are presented. The overall performance is described using both Light Emitting Diodes (LEDs) and Vertical Cavity Surface Emitting Laser diodes (VCSELs) as optical sources with particular emphasis on Bit Error Rate (BER) and phase jitter versus input power. Measurements of the transmission of linear signals using VCSELs are presented and discussed.

Introduction
Digital data from the silicon strip detector will be transmitted from the ATLAS SCT via ~10000 optical links running at 40 Mbits / channel, using a Non Return to Zero (NRZ) code. Initial work focussed on a LED / PIN diode system [1], however the commercial availability of VCSELs has enabled ATLAS to adopt them as the baseline.

Description
The receiver is designed to work with either LEDs or VCSELs as the optical source. Owing to the very different levels of transmitted power, two daughter boards consisting of an eight channel PIN diode array with an MT type connector and pre-amplifier were developed, one optimised for LEDs and the other for VCSELs. These plug into a mother board containing the main amplifier and bandwidth determining time constants, followed by the discriminator and Low Voltage Driver Standard (LVDS) output drivers. The daughter boards are screened to minimise extraneous pickup. A block diagram of the receiver is shown in Fig. 1.

Fig. 1 Optical receiver block diagram.

The daughter board for use with LEDs has the Analog Devices AD8015 as the active element. This has an input current noise of 2.5pA/√Hz and a differential transresistance gain of 20 Kohms. It is linear over an input current range of ± 40 μA corresponding to a nominal 80 μW of optical power. The bandwidth is in excess of 200 MHz. The mother board consists of the Burr-Brown OPA680 as a differential amplifier followed by a buffer to give an independent analog test output signal. The analog bandwidth is defined by RC
networks incorporated in these two stages, and is shown in Fig 2.

The LeCroy discriminator MVL407 is followed by a level conversion stage to drive the DS90C031 LVDS output driver.

The total system RMS noise has been measured over the bandwidth of both the AD8051 and OPA686 systems and found to be 1.15 mV and 270 µV at the output, corresponding to 2.5 and 4.3 pA/√Hz at the two inputs respectively.

BER is an excellent indication of system performance and may be defined as [2]

\[
BER \approx \frac{\varphi(-SNR^2/2)}{SNR \times \sqrt{2\pi}}
\]

where the signal to noise ratio (SNR) is defined as the peak signal to noise power ratio.

System BER is shown in Fig 4 as a function of input power.

Errors are observable. In Fig. 6 the input has been increased to 177 nW. No errors are observed after \(5\times10^7\) sweeps; the measured BER for this input is \(2.3\times10^{-6}\).
Fig. 7 Eye diagram for a VCSEL signal with an average input power of 24μW.

Time jitter is also an important parameter of optical links. Fig. 8 shows the leading edge of the transmitted signal and that of the LVDS received signal together with the histogram of their time difference distribution, as measured on a Le Croy LC334A oscilloscope. One major division is 50 ps.

Fig. 8. Histogram of leading edge jitter between transmitted and received signal.

Fig. 9. Shows the time jitter versus drive current for LEDs and VCSELs respectively, together with the corresponding optical power.

A jitter of $\sigma < 10$ps. was observed for a drive current of 15 mA.

The ATLAS baseline for data transmission is Binary. However the use of VCSELs for the transfer of linear information may be interesting for other applications. Available optical power and bandwidth present no problems. The total system frequency response from VCSEL constant current driver to receiver output is shown in Fig. 10.

Fig. 10. Bandwidth of linear chain.

Fig. 11 shows the corresponding time domain response.

Fig. 11. Total linear chain pulse response.

Fig. 12 shows the DC transfer characteristic of VCSEL current versus received PIN diode current.
357

products, i.e. 2f₁-f₂ and 2f₂-f₁ plus higher order terms, as seen in Fig. 15.

Fig. 12. Linearity of the D.C. VCSEL current to PIN diode transfer characteristic.

The threshold is observed to be at 4.8mA and the transfer characteristic is far from linear due to mode shifts in the excitation of the laser. The linear region is expanded in Fig 13.

Fig. 13. Linearity of selected range.

Fig. 14. Shows the residuals of a least squares fit.

Over this range the RMS linearity is of the order of 0.5%. The dynamic nonlinearity was also measured using the two-tone method. Two frequency sources are merged in a resistive network, this signal is then fed into the network under test and the output displayed on a spectrum analyser. If there is no distortion then only the two input frequencies will be present. Distortion will produce intermodulation products, i.e. 2f₁-f₂ and 2f₂-f₁, plus higher order terms, as seen in Fig. 15.

Fig. 15. Intermodulation products produced by non-linearity of entire chain.

Total harmonic distortion i.e. the ratio of the output signal compared to the sum of all the intermodulation products versus output amplitude is shown in Fig.16.

Fig. 16. Total distortion versus output voltage.

The VCSEL produced additional noise, adding to the total system noise when biased to the centre of its linear characteristic. This was measured to be 515 μV at the output, i.e. 0.1% of the linear range.

This system was used for the transmission of the linear output of the SCT 128A chip [3] as shown in Fig. 17. This chip comprises five basic blocks: front end amplifiers, analog pipeline, control logic with derandomizing FIFO, command decoder and analog output multiplexer. Measured noise performance is 707 ± 43 RMS electrons per pF.[4].

The VCSEL was driven by a high impedance linear driver circuit and biased to provide the maximum linear operating range. The excellent quality of the signal after transmission down the optical fiber may be observed at the output of the receiver.
Conclusions.

An eight channel optical receiver accepting an MT ribbon light fiber input has been constructed and tested using both LEDs and VCSELs as optical sources. Performance is satisfactory with low light power, BERs of \(<1*10^{-9}\) have been achieved using LEDs with an average received power of \(1\mu W\) with a corresponding time jitter of \(~100\) ps The use of VCSELs as the optical source enables a robust and low cost receiver design with drive currents of the order of \(6mA\) on the detector, and a time jitter of \(<10ps\) at \(15mA\) drive current.

A linear link has been demonstrated using VCSELs. The frequency response to the 3dB roll off point is 120 MHz By careful selection of the linear bias point a linearity of 0.5% can be achieved. With presently available VCSELs this linearity is not repeatable from VCSEL to VCSEL. Other modulation techniques, for example frequency modulation may dramatically improve linearity while retaining simplicity and low cost, and are currently under investigation.

References


RADIATION TESTS OF OPTICAL LINK COMPONENTS FOR THE ATLAS
SCT.

D.G. Charlton, J.D. Dowell, R.I. Homer, P. Jovanovic, I.R. Kenyon, G. Mahout, H.R. Shaylor,
J.A. Wilson
University of Birmingham, U.K.

A. Rudge
CERN, Switzerland

J. Fopma, I. Mandic, R.B. Nickerson, P.D. Shield, R.L. Wastie, A.R. Weidberg
University of Oxford, U.K.

D. White
Rutherford Appleton Laboratory, U.K.

Abstract
Optical fibre and silicon epitaxial PIN photodiodes, developed for reading out the ATLAS SemiConductor Tracker, have been irradiated up to levels expected after 10 years' running at LHC. The irradiated fibre showed a negligible increase in attenuation. The DC and AC response of the photodiodes remained at acceptable levels. Progress on aging tests is reviewed.

1. INTRODUCTION

The architecture and the overall performance of the optical links to be used for reading out the ATLAS SemiConductor Tracker have been described in earlier contributions [1,2]. A crucial issue is the radiation hardness of various components of the links. For the SCT, lying between 20cm and 52cm from the beamline, ten years of LHC operation is equivalent to up to $1.3 \times 10^{14}$ (1MeV) neutrons cm$^{-2}$. The bulk radiation damage depends on the Non Ionising Energy Loss (NIEL) experienced by the incident particle in the material [3]. Since the NIEL depends on both the incident particle type and energy as well as the material involved, the effective fluence of particles is expressed in terms of an equivalent number of 1MeV neutrons. This convention is used throughout the paper.

The ionisation deposited in the silicon of the SCT amounts to 100kGy (10MRad). For the pixel detectors, which lie closer to the beamline, the fluence and dose are significantly higher: up to $5 \times 10^{14}$ (1MeV) neutrons cm$^{-2}$ and up to 300kGy (30MRad).

A schematic of the SCT links is shown in figure 1. Data are transmitted from detector modules to the control room while Timing, Trigger and Control signals are sent from the control room to the detectors. All apparatus from the detector modules to the patch panel must be capable of surviving the radiation levels described above. Also the links must function at rates of 40M bits per second.

2. IRRADIATION OF FUJIKURA FIBRE

A sample of Fujikura's 50/60/125/250 optical fibre, 12m long, was irradiated by gamma rays, using the "1 curie" Co-60 source at the University of Birmingham Radiation Centre. The gamma rays had a mean energy of 1.25MeV. The fibre was irradiated overnight and during weekends for two months until the total dose received amounted to 300kGy, the level expected for the innermost layer of the pixels after 10 years of LHC operation. The attenuation of the fibre was measured regularly using an LED light source.

---

1 Fujikura, Optical Fiber Products Div., 1-5-1 Kiba, Koto-ku, TOKYO 135, Japan.
2 A step-index multimode fibre comprising: a pure silica core (radius 25μm); 5μm of fluorine doped depressed refractive index cladding; pure silica cladding out to radius of 62.5μm and finally a protective jacket out to 125μm.
(850nm, 3μW<power<16μW) and is plotted in figure 2. For doses up to 300kGy, the attenuation induced by the irradiation is negligible.

\[
\text{loss} = (-0.96 \pm 0.08) \times 10^{-4} \text{ dB/m/MRød/m}
\]

Figure 2. The power transmitted (in dBm) through the irradiated Fujikura 50/60/125/250 optical fibre versus the received total dose of ionising radiation.

A similar sample of Fujikura fibre was irradiated with an equivalent of \(10^{15}\) (1MeV) neutrons at the Ljubljana reactor centre. This fluence induced an attenuation of only 0.13dB/m.

We conclude therefore that the Fujikura 50/60/125/250 fibre is entirely satisfactory; it shows a radiation hardness almost an order of magnitude larger than that required for the ATLAS SCT optical links.

3. IRRADIATION OF PHOTODIODES

Sets of Centronic\(^3\) silicon photodiodes, operating at 850nm, have been irradiated with neutrons and protons during the last two years. In 1997, the first irradiations showed that Si photodiodes produced by an epitaxial process were encouragingly radiation hard [4]. These photodiodes were mounted in sets of three on the GEC\(^4\) packages [1] (in which the alignment of optical fibres with photodiodes is performed using “V groove” technology). Three GEC packages, containing 9 devices, were irradiated. Their dark currents and DC response were measured while the devices were being irradiated; this allowed the performance of the photodiodes to be monitored online.

In 1998, a different procedure was adopted. Sets of 8 silicon photodiodes were mounted on ceramic tiles and were measured only before and after the irradiation. The photodiodes are measured using the scanning machine, developed by the Berne group [5]. (This apparatus enables an LED light source to be moved in precise steps across sets of photodiodes; the position of maximum signal is found for each photodiode and the dark current and DC response are then measured). The Berne machine was transported to Birmingham early in 1998 in order to continue its use in the characterisation of large numbers of devices.

3.1 Results from the 1997 irradiation.

Nine epitaxial Si photodiodes were irradiated first with neutrons from the Dynamitron at the Birmingham University Radiation Centre (neutron energy centred around 2 MeV). Since the neutrons were emanating from effectively a point source, the irradiated photodiodes experienced significantly different fluences. Then the same devices were irradiated at the ISIS spallation source at the Rutherford Laboratory (which produced neutrons of energy centred around 1MeV). Later in the year, the photodiodes were irradiated along with ATLAS SCT silicon microstrip detectors by 26GeV protons at the CERN PS. For the proton run only, the photodiodes were placed in a box, cooled to \(-10^\circ\text{C}\), which was scanned through the beam in order to irradiate all items uniformly.

During the irradiations at Birmingham and CERN, light from an LED was fed via optical fibres into each photodiode so that the dark current and DC response of each device were monitored online. This was not feasible at ISIS where the characteristics of the photodiodes could be measured only before and after irradiation.

\[\text{Fluence} = 0.0357 \text{ MRød/h}\]

\[\text{loss} = (-0.96 \pm 0.08) \times 10^{-4} \text{ dB/m/MRød/m}\]

\[\text{Figure 2. The power transmitted (in dBm) through the irradiated Fujikura 50/60/125/250 optical fibre versus the received total dose of ionising radiation.}\]

\[\text{Figure 3. Darkcurrent versus fluence. The vertical lines indicate series of measurements when the devices were not being irradiated but were operated at different temperature. (During the irradiation at the Dynamitron, the PINs received different fluences).}\]
The increase in dark current with accumulated fluence is shown in figure 3 above. During the neutron irradiation at room temperature, the dark current increased from a few nA to approximately 25nA. In the proton irradiation, carried out at about -10°C, the dark current falls by a factor 10 approximately as expected due to the lower temperature, before rising in proportion to the total fluence received.

The dark currents observed are completely negligible compared to the magnitude (≥ 0.1mA) of the expected signals.

In figure 4, the photodiode response is plotted versus time. Initially, the response of the devices is about 0.36A/W (cf the response of a photodiode, operating with 100% quantum efficiency at 850nm, would be 0.68A/W).

The performance of the photodiodes is shown in more detail in figure 5. The response drops by about 30% at the first bout of irradiation and then remains constant thereafter, with no further degradation seen even up to the highest fluences expected for the pixel detectors.

The picture is very encouraging. The photodiodes are sufficiently radiation hard to withstand fluences up to $4 \times 10^{14}$ (1MeV) neutrons cm$^{-2}$. Further tests will show whether the devices can survive the fluences expected for the innermost pixel detectors.

Figure 5. The response of the PIN diodes is plotted against the fluence received. The fluences are given in terms of equivalent neutrons of 1MeV energy, as described in the text.

The AC response of the photodiodes is similarly satisfactory. In figure 6, we see that, at bias voltages above 5V, an upper limit of the response time of the device (limited by the measuring apparatus) is about 1ns. This is adequate for the ATLAS SCT links which will operate at 40MHz.

Figure 6. The rise and fall times of irradiated photodiode signals (in response to an instantaneous light pulse) are plotted against the applied bias voltage.
3.2 Results from the 1998 Irradiation.

Twelve tiles of photodiodes, containing 96 PIN devices, were irradiated by neutrons in ISIS at the Rutherford Laboratory. The total fluence was measured (using activated foils) to be $1.45 \pm 0.05 \times 10^{14}$ (1MeV) neutrons cm$^{-2}$.

During the irradiation (at room temperature), the diodes were biased but were not read out. The dark current per photodiode increased from several nA before irradiation to values in the range, 10nA to 20nA, after irradiation. This increase is quite consistent with results obtained in 1997 (figure 3).

On the other hand, a larger drop in response was observed, compared to the 1997 results. In figure 7, the responses of a set of irradiated and non-irradiated photodiodes are plotted. (A direct comparison of response for the same photodiodes, before and after irradiation, was not performed since the LED light source on the Berne machine had been replaced). In figure 7, the two sharp peaks indicate that the devices in each set perform very similarly. The response after irradiation has fallen to a factor, $0.46 \pm 0.05$, of the response before irradiation.

Figure 7. The response of sets of photodiodes, non-irradiated and irradiated with neutrons, as described in the text.

This is a more significant reduction than the 1997 results which suggested a degradation by a factor, $(0.70 \pm 0.05)$, for even larger fluences. This discrepancy is thought to be due to the LED/PIN layout within the Berne scanning machine. At the standard separations between LED source and PIN diode receiver, the emitted light forms an envelope larger than the photodiode diameter (375μm). Therefore, as the LED light produces charged carriers throughout the silicon volume of the photodiode, a significant fraction of the diode response is due to charges outside the region of high electric field in the depletion layer. The collection of these extraneous charges is expected to be more strongly affected by radiation damage in the silicon than the charges produced in the active volume of the device. The data of 1997 will not be sensitive to this effect since, in those tests, the LED light was channelled directly to the active area of the photodiode via optical fibres.

As a check of this hypothesis, a photodiode, which was irradiated in 1998 and which showed a fall in response of a factor 0.46, was illuminated with light from a VCSEL (which illuminated an area smaller than the active area of the device). Results are shown in figure 8. We see that the non-irradiated photodiode operates efficiently at very low bias while the irradiated device commences efficient operation only above a bias of 3.5V. This behaviour is qualitatively similar to that observed with silicon detectors; during irradiation, "type inversion" occurs so that the initial intrinsic silicon becomes increasingly p type. As the charge carrier density rises, the applied bias voltage must be increased in order to deplete fully the material.

Figure 8. For constant incident light, the currents produced by an irradiated and an unirradiated photodiode are plotted against the applied bias.

We see that the plateau value of response has fallen to around 70% after irradiation. As a further crosscheck, several photodiodes from a different manufacturer but made using the same process, were irradiated by $4 \times 10^{14}$ (1MeV) neutrons cm$^{-2}$ in Ljubljana. These too showed a 30% only fall in response. We conclude that the discrepancy between the 1997 and 1998 results is due to the mismatch in light, emitted by the LED and received by the photodiodes, in the Berne machine.
Since the observed 30% degradation in PIN diode response is negligible given the large light levels produced by VCSELs, the PIN diodes seem entirely adequate for the ATLAS SCT links.

3.3 Further irradiation tests (1998)

During September 1998, three tiles (each containing 8 photodiodes which had already been irradiated by neutrons in ISIS) were exposed to 24GeV protons at the CERN PS. The devices were irradiated along with a batch of silicon microstrip detectors and so were maintained at a temperature of about –10°C. The total fluence received was 2.8 \(10^{14}\) protons cm\(^{-2}\) (corresponding to 1.6 \(10^{14}\) (1MeV) neutrons cm\(^{-2}\)). Once the induced radioactivity in the photodiodes is sufficiently low, they will be remeasured in Birmingham.

In late September, three tiles containing 24 photodiodes were returned to ISIS to be irradiated again with neutrons.

After this second round of irradiation, by protons and by neutrons, we shall check that the response of the PIN diodes has not degraded further (as expected from the 1997 results). Results will confirm (or not) on a larger sample than in 1997 whether the photodiodes can survive radiation up to the levels expected for the pixel detectors.

4. AGING TESTS

A prototype test setup is operational whereby each of the 8 photodiodes of an unirradiated tile is coupled via optical fibre to its own VCSEL. The VCSELs supply about 1mW of optical power continuously to each device. After 40 days operation, no major problems have occurred. The apparatus is now being constructed so that 96 irradiated PIN diodes can be subjected to long term aging tests.

5. CONCLUSIONS

The ATLAS SCT irradiation programme has led to the following conclusions:

- The Fujikura optical fibre (50/60/125/250) is radiation hard well beyond the required level.
- The optical receivers (Centronic PIN silicon photodiodes) showed a degradation of response of approximately 30% in the 1997 tests and of 54% in 1998. Further tests will be carried out to confirm that the lower result in 1998 is due to the systematic bias in the setup, described in section 3.2. Given the large levels of light available if VCSELs are used as optical transmitters, this fall in response is acceptable for operation in the SCT and pixel readout. The darkcurrents after irradiation are negligible compared to the expected signal size.
- The electrical drivers and receivers (LDC and DORIC) are adequately radiation hard [1].
- Aging tests have begun; preliminary results are encouraging.

We conclude that the ATLAS SCT/Pixel readout, based on 850nm optical links, can survive the fluences, expected after 10 years of LHC operation; the complete system appears feasible.

6. ACKNOWLEDGEMENTS

We are very grateful for the expert technical assistance of Dennis Grant, Roger Harris and Ian McGill in Birmingham and of Derrick Hill at RAL. We thank the UK Particle Physics and Astronomy Research Council for financial assistance.

7. REFERENCES

2. A. Rudge et al., “Tests of Prototype ATLAS SCT Data Links”; these proceedings.
5. J. Beringer et al., “Radiation Hardness and Lifetime Studies of LEDs and VCSELs for the Optical Readout of the ATLAS SCT”; ATLAS Internal Note INDET-NO-183.
DEVELOPMENT OF RADIATION TOLERANT Gb/s OPTICAL LINKS FOR THE FRONT-END READOUT OF THE ATLAS LIQUID ARGON CALORIMETER


(a) Centre de Physique des Particules de Marseille (CPPM), 163 Avenue de Luminy, Case 907, 13288 Marseille, France.
(b) Institut des Sciences Nucléaires (ISN), 53 Avenue des Martyrs, 30826 Grenoble, France.
(c) Royal Institute of Technology (KTH), Physics Department Frescati, Frescativägen 24, 10405 Stockholm, Sweden.
(d) Southern Methodist University (SMU), Department of Physics, Dallas, Texas 75275-0175, USA.

Abstract

In the baseline readout solution for the ATLAS liquid argon calorimeter, approximately 1500 unidirectional Gigabit/s (Gb/s) fibre-optic links are used to transfer data from the calorimeter to receivers in data acquisition electronics situated up to 200 m away. In an architecture currently under study, ‘G-Link’ serialiser chips manufactured by Hewlett Packard are used to convert calorimeter data words into a 1.6 Gb/s serial data stream which is fed into a VCSEL (vertical cavity surface emitting laser diode) based emitter system operating at 850 nm. Graded index multimode optical fibres are used to couple the on-detector emitters to PIN-photodiodes located in receivers. In this note results from neutron irradiations of a complete G-Link based link demonstrator are presented along with results from neutron and ionising irradiations of potential link components (packaged VCSEL’s and graded-index fibres).

1 INTRODUCTION

1.1 Link Architecture

Approximately 1500 unidirectional optical interconnects are required for the readout of the ATLAS liquid argon (LArg) calorimeter [1]. Each on-detector front-end board (FEB) is fed by 128 ‘raw’ calorimeter channels which are processed and on receipt of a level-1 trigger accept readout over an optical interconnect. The interconnect must allow a throughput of 1.28 Gb/s (32 bits every 25 ns). The bit error rate (BER) of the interconnect must be better then $10^{-9}$ so the performance of the LArg data acquisition as a whole is not compromised. The interconnect architecture currently favoured is a single serial optical link per FEB as this reduces cost due to the fewer number of components required compared to a parallel link implementation. The link is based around commercial ‘off-the-shelf’ components. The emitting end of the link comprises of a Hewlett Packard G-Link serialiser chip connected to a VCSEL laser diode [2]. Graded index multimode (50/125) fibre is used to connect the emitters to off-detector receiver units which contain G-Link deserialising chips. This architecture is shown schematically in figure 1.

1.2 Radiation Issues

Over 10 years of LHC running, the components at the emitting end of the link will be subject to high levels of both neutron ($1.7\times10^{13} n(1 \text{ MeV Si}) \text{ cm}^{-2}$) and ionising (gamma) radiation (800 Gy). The receiving part of the link is not exposed to significant levels of radiation. Access to link components mounted on-detector would require a lengthy access into ATLAS and so it is important that the...
components operate reliably for 10 years in this hostile environment.

Components were irradiated with 6 MeV neutrons at the SARA cyclotron facility in Gronoble [3]. The neutrons are produced by impinging 20 MeV deuterons on a beryllium target. The components under irradiation are located approximately 30 cm from the target, behind a liquid nitrogen cryostat which is used for other tests. The activation of nickel foils was used to determine the absolute neutron fluence to an accuracy of around 15%. The typical neutron flux at SARA is approximately $5 \times 10^{11} \text{ n cm}^{-2} \text{ hr}^{-1}$, about 1500 greater than that expected in ATLAS.

The gamma irradiations were performed with $^{60}$Co facilities at BNL, Brookhaven (only fibre) and Karolinska Hospital, Stockholm (fibre and VCSEL’s). As the $^{60}$Co source decays it emits two gamma rays at energies of 1.17 MeV and 1.33 MeV. Polymer-alanine dosimeters were used to measure the total ionising dose received by the components under test to an accuracy of around 4%. Solid state detectors were used to cross-check the result. The dose rate delivered at BNL (Karolinska) is approximately 200 (80) Gy hr$^{-1}$, about $10^4$ (4000) greater than that expected in ATLAS.

2 **IRRADIATION STUDIES**

2.1 **Demonstrator Link**

**Overview**

A set of demonstrator links based around the G-Link chipset have been constructed and the emitting end of the link irradiated with neutrons. Both emitter and receiver boards do not have the optics mounted directly. Instead, there is a socket following the industry standard for transceiver modules. This allows a variety of different optical solutions to be easily evaluated – such as a driver circuit (if necessary) coupled to the VCSEL’s described in section 2.2. The receiver board also features an Altera PLD to allow some processing of the G-Link outputs. During the tests described in the remainder of this note, industry standard VCSEL-based Gb/s transceiver modules have been used. As the links are unidirectional only half a transceiver is used at either end of the link. Due to this partial use, it is unlikely that such transceivers will be a final solution for ATLAS. However, in a demonstrator link they are very suitable for gaining experience with the irradiation of Gb/s link components.

**G-Link Chipset**

The G-Link chipset enables parallel data loaded into the transmitter to be delivered to the receiver over a serial channel. The chipset is particularly attractive as it hides the complexities of encoding, multiplexing (transmitter) and clock extraction, demultiplexing and decoding (receiver) from the user. Furthermore, frame synchronisation and DC balance are maintained automatically. The G-Link protocol attaches a 4 bit control word to every 16 bit data word sent over the link, making a 20 bit frame, as shown in figure 2. The control word denotes the data type being sent (control, data or fill frame) and contains a ‘master transition’ which the receiver uses for frequency locking. The chipset is run in the ‘double frame mode’ which, with the addition of external (de)multiplexing elements, allows a 32 bit data word (40 bit frame) to be sent as two separate 20 bit frame segments. Data inputs to the chip are TTL and the serial Gb/s output is PECL. The (de)multiplexing elements are standard ATLAS components, used by many subdetectors, and not expected to present any additional radiation tolerance issues. The monolithic silicon bipolar G-Link chipset is based on a masked ‘sea of gates’ architecture using 25 GHz transistors.

**Transceiver Modules**

The transceiver modules contain a 850 nm VCSEL emitter and driver packaged together with a PIN-diode based receiver and amplifier and discriminator. Optical connections are made with push-fit ‘SC’ connectors. The modules accept PECL inputs and so can be directly coupled to the output of the G-Link. Three varieties of transceiver have been tested: Hewlett Packard, Honeywell HFM2450 and Methode MDX-19-4-1. The Hewlett Packard and Honeywell transceivers use silicon bipolar laser drivers whereas the Methode driver is based on discrete components.

**Testing Procedure**

The neutron irradiations have two aspects. Firstly, the components on the emitting end of the link must survive
the total neutron fluence expected after 10 years of LHC running without any effect on the performance of the link - total dose studies. Secondly, the radiation induced bit error rate in the link must be acceptable - single event studies. During irradiation all components were biased and approximately 70 m of fibre joined the emitter to the receiver.

A figure of merit describing the performance of a link is traditionally given by the bit error rate. Performing industry standard bit error rate tests at Gb/s speeds requires the use of expensive equipment which is often not optimised for the transfer of 32 bit data words. Moreover, only a single link can be tested at once, which is not ideal for irradiation studies when larger sample sizes are desirable.

A purpose built bit error rate tester is under construction for testing LArg links but was not available at the time of the irradiations. For the tests described in this note a simpler approach was followed. Before and after (up to a week afterwards due to a ‘cool down’ period) an irradiation, the integrity of a single link could be assessed using a logic analyser comparing received data to a reference table. The single link limitation and large dead-time of this method makes it unsuitable for irradiation tests. A simpler scheme, using the G-Link’s inbuilt error detecting functionality, is therefore used. The G-Link receiver provides an error flag which is generated internally from a check of the control field in the transmitted frame. The control field check is sensitive to illegal control words (not all 2^4 combinations are allowed) and deviations from a strict alternation of the master transition bit. The data word is not checked. There is also a ‘link-down’ indicator which is asserted when the G-link cannot identify a frame to lock on to. It is important to understand the frequency of this type of error during irradiation as the G-link error recovery procedure takes a minimum of 128 frames (1.6 μs) to recover the link.

With no radiation present, both tests indicated no errors during many days of operation.

**Total Dose Studies**

Total dose studies were made in three separate tests, as summarised in table 1. In the first and last tests, the G-Link chips were coupled to transceiver modules. In the second test, the link was run at 160 Mb/s over 15 m copper links. This is discussed further in the next section. In all cases the G-Link chips survived the irradiation with no errors being indicated during the two test procedures described above (using fresh transceivers). Note that G1-4 survived a 30 year LHC equivalent irradiation. The only transceiver modules not to suffer damage during irradiation were those supplied by Methode. A post-irradiation ‘autopsy’ on the Honeywell transceivers revealed that the laser driver had failed but the VCSEL still functioned within specifications when coupled to a fresh driver. The Methode transceiver had a driver comprised of discrete components. For technical reasons, the HP transceiver could not be easily tested after dissection.

<table>
<thead>
<tr>
<th>Test</th>
<th>G-Link</th>
<th>Optics</th>
<th>Gn status</th>
<th>Optics status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (10 years equiv.)</td>
<td>G1</td>
<td>HW1</td>
<td>OK</td>
<td>Dead</td>
</tr>
<tr>
<td>2 (20 years equiv.)</td>
<td>G2</td>
<td>HW2</td>
<td>OK</td>
<td>Dead</td>
</tr>
<tr>
<td>3 (10 years equiv.)</td>
<td>G3</td>
<td>HP1</td>
<td>OK</td>
<td>Erratic</td>
</tr>
<tr>
<td></td>
<td>G4</td>
<td>M1</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>G5</td>
<td>Cu</td>
<td>OK</td>
<td>n/a</td>
</tr>
<tr>
<td></td>
<td>G6</td>
<td>Cu</td>
<td>OK</td>
<td>n/a</td>
</tr>
<tr>
<td></td>
<td>G7</td>
<td>Cu</td>
<td>OK</td>
<td>n/a</td>
</tr>
<tr>
<td></td>
<td>M2</td>
<td>OK</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>M3</td>
<td>OK</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>M4</td>
<td>OK</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>M5</td>
<td>OK</td>
<td>OK</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: Summary of G-Link (Gn) demonstrator link irradiations. G-Links G1-4 and G5-7 come from different batches. Transceivers are denoted by: HWn, Honeywell; HPn, Hewlett Packard; Mn, Methode. Test 2 used copper (Cu) links, with the link running at 160 Mb/s.

**Single Event Studies**

Four complete links equipped with Methode transceivers were used to investigate single event effects during a neutron irradiation. During irradiation, the link-down time was estimated by monitoring the G-link error flag and link-down indicator. The distribution of the link-down times can be seen in figure 3. The sharp peak around zero (12.5 ns)

is composed solely of error flag errors. The rest of the entries (all >1.6 μs) occur when the G-link asserts the link-down indicator after loosing frame lock. Note that a single link-down event lasting 300μs corresponds to the loss of 24000 20 bit frames, which is clearly unacceptable. In order to maintain a bit error rate of O(10^-9), approximately
one such 300µs link-down event can be tolerated every 100 hours.

The majority of this data was taken at a SARA deuteron beam current of 5 µA which corresponds to a neutron dose rate approximately 1500 that expected in ATLAS. At 5 µA there was approximately 1.5 (1) link-down (error-flag) error recorded per minute. To estimate the error rate at ATLAS-like dose rates, some data was also taken at lower beam currents. The error rate was observed to drop rapidly with beam current, but insufficient beam time was available to allow any robust conclusions to be drawn.

Future tests will be dedicated to low dose-rate studies and improved monitoring of the G-Link error flags will allow the link integrity at ATLAS-like dose rates to be determined. As single event type errors were also observed in the low speed test with copper links (see total dose section), it would be instructive to separate the G-Link and transceiver in a high speed test. As it is impossible to do this with copper links, there is a development under way to drive VCSEL's directly from the G-Link.

2.2 Packaged VCSEL’s

Nine Honeywell HFE4080-321 and nine Mitel 1A440 VCSEL’s were irradiated with both neutrons and gammas [5]. The VCSEL chips were housed in TO-46 packages encapsulated into metal ST assemblies to allow simple fibre connections. The Honeywell VCSEL’s were equipped with plastic lenses to facilitate efficient fibre coupling, the Mitel VCSEL’s had a flat window. The active VCSEL chips are approximately cubic with sides of length 500 µm. Similar VCSEL’s are used in the transceiver units discussed in section 2.1. During the irradiations the aim was to investigate radiation induced attenuation of the VCSEL’s light output and possible changes in the VCSEL’s threshold current. As such, the tests purely investigated the DC (time averaged) characteristics of the VCSEL’s. Each VCSEL was equipped with a fibre which was routed away from the radiation beams to a PIN-based receiver unit [4] connected to an ADC mounted inside a PC. During irradiation, the VCSEL’s were biased above threshold. At periodic intervals the bias current was varied between 0 mA and 10 mA and the corresponding light output recorded. After the irradiation period was over the VCSEL’s remained biased to check for any evidence of annealing effects. The total neutron fluence received by the VCSEL’s was measured to be $(2.1±0.4)×10^{15} \, \text{n/(1 MeV Si)} \, \text{cm}^{-2}$, corresponding to 10 years of LHC running, and the total ionising dose was $(5.1±0.2) \, \text{kGy}$, corresponding to 66 years of LHC running.

Figure 4 shows the relative attenuation in the light output from a Honeywell VCSEL as a function of the time during neutron irradiation. The vertical lines denote the start and end of the irradiation period. This plot is typical for all the Honeywell VCSEL’s tested and compatible behaviour is seen for all the Mitel VCSEL’s. Figure 5 shows the corresponding results from a gamma irradiation. The neutron (gamma) irradiation reduces the light output by about 10% (5%) for 10 year LHC equivalent exposures. After the neutron irradiation a few days of annealing restores the light output to pre-irradiation levels. No such annealing behaviour is observed after the gamma irradiation. The threshold current for either type of VCSEL did not move significantly during either type of irradiation.

2.3 Multimode Fibre

Two 10 m long pieces of commercial off-the-shelf fibre have been irradiated with neutrons and gammas. The fi-
bres were not chosen for any particular reason, but rather to be representative of commercially graded index fibre. Due to the speed of the link, graded index fibre with a small core size is needed to ensure dispersion does not compromise the performance of the link. The first fibre is a piece of 50/125 germanium doped silica core 8-way fibre ribbon supplied by Acome. The second piece is a duplex patch cord supplied by Alcoa-Fujikura and designed for use with the transceiver modules described in section 2.1.

The fibres were arranged in coils to maximise the amount of fibre in the radiation beam. A 850 nm VCSEL emitter was used to send light through the fibres and a calibrated optical multimeter used to measure the received amount of light. The emitter was monitored during the irradiation to check that the output power remained constant. Figure 6 (7) shows the induced attenuation during the neutron (gamma) irradiation. The induced attenuation in the two fibres after a 10 year LHC equivalent dose is significantly different after both the neutron and gamma irradiations. The Alcoa-Fujikura fibre exhibits extremely good neutron and gamma radiation tolerance whereas the Acome fibre fails catastrophically during gamma irradiation.

3 SUMMARY
A serial optical link running at 1.6 Gb/s and based around the G-Link chipset and commercial VCSEL/PIN-diode transceiver units has been developed. The link fulfills the specifications of the readout links required for the ATLAS LArg calorimeter and runs error-free in the laboratory for many days. Initial results on the neutron tolerance of the link are presented. The link satisfies total dose requirements if Methode transceivers are used, but further tests are needed to fully understand single event effects. In particular, a better understanding of errors induced by a loss of frame lock which can result in a mean link-down time of 300 $\mu$s is needed. Results from the neutron and gamma irradiation of packaged VCSEL emitters and multimode fibre are also presented. Both brands of VCSEL are sufficiently radiation tolerant for use in LArg links. The radiation tolerance of the two off-the-shelf graded-index fibres tested differed greatly. One of the fibres would be suitable for use with LArg links. The reason for the marked difference in behaviour between the fibres is under investigation.

ACKNOWLEDGEMENTS
The authors would like to thank B-I. Ruden (Karolinska hospital), the SARA cyclotron operation crew, J. Isaksson (Honeywell AB, Malmö) and Mitel Semiconductor (Järfalla) for VCSEL samples, J. Tatum (Honeywell Microdevices, Texas) and A. Benahed and A. Fontaine for dosimetry services. The efforts of the technical staff at all the laboratories are well appreciated.

References
The ALICE Detector Data Link Project

György Rubin, Pierre Vande Vyvre
CERN, CH-1211 Geneva 23, Switzerland
Péter Csató, Ervin Dénes, Tivadar Kiss, Zoltán Meggyesi, János Sulyán, László Szendrei, György Vesztergombi
KFKI-RMKI, H-1525 Budapest, P.O.Box 49, Hungary
Bertalan Eged, Ákos Fauszt, István Gelencsér, István Novák, György Vesztergombi Jr.
Technical University of Budapest (BME), H-1111 Budapest, M• egyetem rakpart 3-9, Hungary

Abstract

In this paper we present the ALICE detector data link (DDL) project, which is running in the collaboration of CERN, RMKI and BME. The DDL is a multi-purpose full-duplex digital optical link, providing high-speed transmission of data blocks in both directions between the front-end electronics and the data acquisition system. It can also be used as a transmission medium for the remote control and test of the front-end electronics during the normal operation and for the remote debugging during the system integration of the ALICE detector. A prototype has been developed according to the requirements of the ALICE experiment and first it will be used in the ALICE-TPC test system.

Introduction

During the preparation of the ALICE Technical Proposal [1] the need emerged for a common interface between the front-end electronics (FEE) of the different detectors and the data acquisition system (DAQ). A dedicated working group was formed to collect in a document [2] the needs of the detectors and the DAQ. The following main requirements have been identified:
- only one standard link for the information transfer between the FEEs and the DAQ;
- standard protocol for all of the detectors;
- point-to-point full-duplex optical connection;
- high-speed transmission of event data;
- remote control and test of the FEEs from the DAQ;
- bi-directional data block transfer between the DAQ and the FEEs.

Figure 1 shows a part of the ALICE DAQ, consisting of a detector read-out chain and a sub-event building system.

Figure 1 A part of the ALICE DAQ

The DDL will be used in the detector read-out chain together with the read-out receiver card (RORC). The RORC is plugged-in the front-end digital crate (FEDC). The DDL consists of the following components:
- source interface unit (SIU), connected to the FEE;
- destination interface unit (DIU), connected RORC;
- physical medium (two fibre optic cables).

The DDL transfers the event fragments from the experimental pit to the computing room and stores them in the input buffer of the RORC.

The FEDC is responsible for the sub-event building. The local data concentrator (LDC) reads-out the event fragments from the RORCs and assembling them into sub-events. Then the sub-events are sent to the central event building switch. If it is reveals to be needed, separate backplanes could be used for the control and the read-out functions in this crate. The modules are controlled by a single board computer (SBC) via VME bus. The event data read-out from the RORCs will be carried out by using a dedicated read-out bus, which is not defined yet. We hope, that these two backplanes can

1 E-mail: Gyorgy.Rubin@cern.ch
be merged in few years, if a really fast backplane will be available (e.g. VME320).

In most of the applications, the SIU will be connected directly to the FEE (see Figure 2).

**Figure 2 Direct connection to the FEE**

In some of the applications (for example, where the level of the radiation is too high for the SIU), the SIU will be placed outside of the detector with a distance of several meters. In this configuration a radiation hard medium-speed transceiver shall be used inside the FEE. The DDL is connected to the FEE through a DDL. This configuration is foreseen for the Si-Pixel detector.

**Figure 3 Indirect connection to the FEE**

Figure 4 shows an other possibility for the indirect connection. In this case the DDL concentrator is implemented as a VME interface, and the information is transmitted between the two VME crates by using two DIUs and two RORCs. This configuration is foreseen for the trigger detector, because the trigger unit will be placed in a VME crate. A dedicated software will emulate the behavior of the SIU and the FEE, so from the DAQ point of view this configuration will be identical to the basic configuration.

**Figure 4 Indirect connection through VME bus**

The DDL is connected to two external systems (e.g. FEE and RORC). The architecture of these interfaces are different (see Figure 5). The RORC-DIU interface consists of two uni-directional busses for the full-duplex information transfer. It is for example possible to send commands to the FEE or the interface units, while event data are transmitted from the FEE to the DAQ.

The DDL also provides a port for the JTAG BST [3] which can be used for the remote testing and control of the FEE.

**Figure 5 The DDL interfaces**

**Main technical parameters**

The main data flow will take place from the FEE to the RORC. The DDLs will be able to read-out the complete ALICE events (40 MB) within less than 2 ms, transmitting event data from the FEE to the RORC with a detected bit error rate of < \(10^{-5}\). Each DDL will be able to transmit data at a rate of 100 MB/s. As the zero suppression algorithm requires downloading blocks of data into the FEE, a throughput of 10 MB/s is needed in the opposite direction. Both the FEE and the SIU will be remotely controlled from the FEDC through the DDL, since their placement inside the detector will not allow using any other cabling apart from the DDL physical medium. Therefore, commands and status information will also be transmitted between the FEE and the RORC. Since the SIU is located inside the detector, the requirements for the lifetime (> 10 years), the power consumption (< 5W) and the footprint (< 50 cm²) of this unit are key issues. More strict requirements have been identified for the ITS [2] sub-detectors where radiation tolerant electronics is needed and the maximum footprint of the SIU shall be less than 15 cm². To achieve the high reliability of the experimental apparatus, efficient test of all the sub-systems will be provided. The DDL will allow to test the FEE remotely by using JTAG BST. The DDL itself will also have a powerful self-test mode.

**DDL protocol**

1. **Protocol layers**

The DDL protocol consists of four layers: the DDL interface layer (most upper), the signaling and framing layer, the coding layer and the physical layer.

The DDL interface layer is described in the Interface Control Document (ICD) [4]. It includes the physical and electrical description of the interface units, the description of the interface signals, the definition of the
information structures (e.g. data blocks, commands and status words), the interface transactions and the timing.

The signaling and framing layer is described in the Physical and Signaling Interface Specification [5]. It is a mixture of the FC(2) layer of the Fibre Channel Standard [6] and DDL specific solutions (e.g. ordered set definition, frame structure, flow control).

The coding layer is compatible with FC(1) layer of the Fibre Channel Standard (FCS), where the well known FCS. For the DDL

parameters: 100 MB/s transmission speed, 50 μm multi-mode optical fibre, 850 nm laser transmitter, data transmission up to 500 m distance. In the next generation of the DDL we intend to use Gigabit Ethernet physical layer [8], for cost and speed reasons.

2. Transactions

The information transfer on the DDL is organised in control-status transactions and block transfer transactions. The control-status transactions are simple, while the block transfer transactions are complex, consisting of several control-status transactions. All the transactions are started by a command and terminated by a command transmission status word. It indicates, if any errors have occurred during the transaction.

The following control-status transactions are defined:
- front-end electronics control;
- front-end electronics status read-out;
- interface unit control;
- interface unit status read-out.

Figure 6 shows the FEE status read-out transaction, as an example of the control-status transactions.

The following block transfer transactions are defined:
- event data transmission;
- data block downloading;
- data block read-back;
- self-test.

Figure 7 shows the event data transmission transaction, as an example of the block transfer transactions.

Prototype project

The main goals of prototype development project are:
1. to build a prototype of the complete read-out chain;
2. to develop hardware and software tools for the test;
3. to try out the system in normal working conditions.

1. Components of the read-out chain

The following task are included in this project:
- experimental media interface (MI) design and test;
- DIU development;
- RORC development;
- SIU development.

Within the MI test sub-project, the design and the test of an 1.06 Gb/s MI circuits and an experimental PCB layout and stack-up have been accomplished. Three main functional components have been selected and tested: a VITESSE V5C7125 and a HP HDMP1526 FCS transceiver chip, and also a METHODE MDX-19 optical transceiver module. An 8-layer PCB has been designed with a particular attention to the signal.
integrity problems, using the buried capacitance technology to improve power supply de-coupling. The tests included bare-board measurements, functional tests with critical data patterns, DC power measurements, and electrical signal integrity measurements. The signal integrity tests were time-domain measurements of the signal wave forms and the power supply noise, and frequency domain measurements of the components and PCB impedance. The results of these test [9] allow us to safely integrate the high-speed serial MI directly on the DDL cards.

Within the DIU development sub-project a first prototype and an improved prototype version have been designed, built and tested. The DIU photos can be seen on the WEB [10]. The DIU consists of two main functional parts: the protocol engine and the media interface (see Figure 8). In the protocol engine the three upper layers of the DDL protocol are implemented by using two ALTERA PLDs$^2$ (EPF10K50VRC240). The MI interfaces the protocol engine to the physical medium. It realtises only the lower protocol layer. It is able simultaneously to send and receive serial data stream with a transmission speed of 1.06 Gb/s, so some signals in this sub-system can have harmonics up to 7 GHz. The PCB layout design is quite critical here, this is the explanation why a MI test project was necessary.

The prototype DIU has the following main features:
- media interface is integrated on the board;
- power consumption < 5 W;
- +3.3 V and +5 V supply voltages;
- footprint < 50 cm$^2$ (12 x 4 cm);
- 4 signal and 2x2 VCC-GND$^3$ PCB layers;
- PLD configuration either from EPROM or a PC;
- two 64-pin CMC interface connector;
- duplex SC fibre optic connector;
- LEDs: power, loss-of-link-synch., and test.

The main task of the RORC is to receive and store the event fragments, coming from the FEEs through the DDL [1]. After the decision of the trigger system, these fragments are transmitted from the RORC to the LCD through the read-out bus for the sub-event building. The RORC shall also be able to transmit data blocks and commands to the FEEs and receive status information from them through the DDL. According to the DDL requirements [2], at least 4 DDLs shall be connected to a RORC.

Within the DIU development sub-project a first prototype and an improved prototype version have been designed, built and tested. The DIU photos can be seen on the WEB [10]. The prototype version RORC does not have full functionality: no trigger interface is implemented and only two DIUs can be connected to it [11]. This RORC consists of two memory buffers for the high-speed transmission of the incoming and the outgoing data blocks and a FIFO for the incoming status information. For the testability a loop-back multiplexer and a DDL test multiplexer are used, supporting the RORC self-test and the DDL self-test working modes. Figure 9 shows the architecture of the prototype RORC.

Figure 8 The architecture of the DIU

The prototype DIU has the following main features:
- media interface is integrated on the board;
- power consumption < 5 W;
- +3.3 V and +5 V supply voltages;
- footprint < 50 cm$^2$ (12 x 4 cm);
- 4 signal and 2x2 VCC-GND$^3$ PCB layers;
- PLD configuration either from EPROM or a PC;

2 PLD - programmable logic device
3 Distributed bypass capacitor is implemented in the PCB by using special buried capacitor structure for the VCC and GND layers.

Figure 9 The architecture of the prototype RORC

The prototype RORC has the following main features:
- normal, RORC self-test and DDL self-test working modes;
- two DDL channels;
- up to 3M x 32 bit input buffer;
- 512K x 32 bit output buffer;
- 64 x 32 bit status FIFO;
- VME64x (VITA 1.1-199x) module and connectors;
- 6U board height;
- A32, D8-32, D32_BLT transfer types;
• 40 MB/s block transfer rate;
• slave and interrupter building blocks;
• programmable base address;
• interrupt event: status FIFO is not empty.

The prototype SIU now is under development. The components have been selected, the mechanical design is ready and the digital design of most of the subsystems is done. In this device only +3.3 V components will be used, so the estimated power consumption is around 4 W. Comparing to the DIU (48 cm²), a 40 % decrease of the footprint has been reached for the SIU (27 cm²). The protocol engine will be implemented in a single IC (FLEX10K100E in FineLine BGA package).

2. Hardware and software tools for the test

For testing and monitoring of the DDL and the RORC, the following hardware tools have been developed:
• DIU extender (DIUEXT);
• SIU extender (SIUEXT);
• SIU simulator (SIMU);
• FEE emulator (FEMU).

The DIUEXT is an extender board, having the same footprint as the DIU. It can be inserted between the DIU and the RORC. There are 5 connectors on this board, providing connection for logic analyzers for the monitoring all the RORC-DIU interface signals. The photo of the DIUEXT can be seen on the WEB [10].

The SIUEXT is an extender board, having the same footprint as the SIU. It can be inserted between the SIU and the FEE. There are 4 connectors on this board, providing connection for logic analyzers for the monitoring all the FEE-SIU interface signals.

The SIMU is a manually controlled simple device, having the same footprint as the SIU. It can be used for the basic hardware tests of the FEE. The SIMU is able to execute all the FEE transactions, according to the DDL protocol.

The FEMU is able to emulate the behavior of all the ALICE detectors. It is based on a HP logic analyzer system (see Figure 10). A special interface card has been developed for the connection of the HP-LA to the DDL.

Figure 10 The DDL test setup

Figure 10 shows the DDL test setup, consisting of:
• a FEMU system;
• a MVME 2604 SBC, running on AIX platform;
• a fibre channel line monitor and analyzer.

The DDL test software is running on a MVME2604 processor under AIX. It has been developed for the functional, the performance and the qualification tests of the DDL [12].

The data traffic on the optical fibres can be studied by using a FCS monitor and analyzer device.

3. System test in normal working conditions

The DDL will be tried-out in the ALICE-TPC test system (see Figure 11) in normal working conditions. In this test setup the DDL is used in indirect configuration (see Figure 4). The analog part of the FEE is placed inside the detector, while the digital part of the FEE in the front-end crate, about 1.5 m far from the detector. The event data transmission has a pull organization. First a command is sent from the readout crate (ROC) to the front-end crate (FEC), requesting the next event transfer. This action is followed by an event transfer in the opposite direction. The system performance has been measured. The task-to-task command delivery time from the FEC to the ROC is about 6 μs. The processor memory-to-memory throughput from the ROC to the FEC is more then 34 MB/s in 64-bit block transfer mode.

Figure 11 Integration in the ALICE-TPC test system
Project status

The prototypes of the DIU and the RORC have been designed, built and tested. The first version of the whole ALICE detector read-out chain will be available at February 1999, when the prototype SIU will be ready.

All the hardware and software tools are ready for the system tests of the complete detector read-out chain.

The DIU, the RORC and the DDL software library have been successfully integrated in the ALICE TPC test system.

References

6. Fibre Channel Physical and Signalling Interface (FC-PH); ANSI X3.230-1994
8. Gigabit Ethernet (1000Base-Sx); IEEE-802.3z/D2
11. G.Rubin and J.Sulyán: "VME Read-out Receiver Card (RORC) for the ALICE-TPC Test System"; ALICE/97-14, Internal Note/DAQ, 05.05.1997
S-LINK: A Prototype of the ATLAS Read-out Link

Erik van der Bij, Robert McLaren, Zoltán Meggyesi
EP-Division CERN, CH-1211 Geneva 23

Abstract

The ATLAS data acquisition system needs over 1500 read-out links between the read-out drivers and the read-out buffers. As it is too early to define the physical layer of those links, the S-LINK specification has been written. It defines a media independent 32-bit synchronous FIFO-like interface for both the sender and receiver side of a link. S-LINKs can send control and data words, can detect link errors and have a self-test mode. Fibre-optic gigabit versions of S-LINK are used by various ATLAS detectors as prototype read-out link and also as trigger information distribution link.

1. INTRODUCTION

The ATLAS data acquisition system [1] (Figure 1) needs many different types of links. The links that move raw digitised data out of the detector are called front-end links. About 50 000 of those links are needed; they will have a length of about 80 m, and move the data to an area without radiation where the read-out drivers (ROD) are located.

The front-end links are not standardised: some detectors use electrical transmission with a rate of 40 Mbps while others use transmission over optical media with rates of 1 Gbps or 1.6 Gbps. The RODs, which are specific to each detector, will format the data so that all detectors send similar structured data streams to the read-out buffers (ROB) where the data will be stored until a level-2 trigger decision has been made.

For cost and support reasons it is desirable to minimise the amount of different elements in the final DAQ system. The read-out link is a logical location to go from detector specific logic to standard logic. The ATLAS Trigger-DAQ Steering Group therefore has specified [2] that a standard read-out link specification will be used. In total about 1500 of these 200 m long links are needed, while the average data rate over each link is in the order of 100 MByte/s.

Although there is a requirement for a standard read-out link specification, link technologies are changing too rapidly to specify the physical layer of the read-out links already now. On the other hand designers of the RODs and ROB have to build systems for testbeams in order to work towards the final system. To cope with this problem the S-LINK specification [3] has been written.

2. S-LINK OVERVIEW

The idea of S-LINK is that, unlike other standards that define the physical layer, it defines a simple FIFO-like interface (Figure 2) on which the use of the signals remains independent of the technology used to implement the physical link. The mapping of the S-LINK signals to the protocol used on the physical link is left open to the designers of the links, allowing them to map it in the most suitable way for the technology used.

To allow interchangeability of different implementations of S-LINK cards, the specification recommends the use of small daughter boards. A single, high-density, 64-pin connector connects the ROD to the Link Source Card (LSC) and the Link Destination Card (LDC) to the ROB. Both the format of the daughter board and the type of connector used correspond to the IEEE Common Mezzanine Card standard, which is the same format as used by PCI Mezzanine Cards (PMC). This daughter card implementation should be used during the prototyping phases, while for the final systems the link logic may be integrated onto the motherboards.

Both LSC and LDC are designed by one group. With this approach the link, including both link cards, can be treated as a component in the system, which offers the advantage of having well defined inputs and outputs.
This means that various implementations of S-LINK (copper, fibre optic, standard or radiation tolerant components) can be developed using new technologies, independently of the design of the RODs or the ROBs.

With the plug-in cards, S-LINK relieves the ROD and ROB designers from making high-speed designs having signals with frequencies of 500 MHz and more. It also means that a designer may change from one link technology to another without needing to modify the motherboards. Apart from that, the S-LINK specification adds important features to the direct use of basic link components:

- detection of bit errors
- start/end of event control words
- generation and checking of a known test pattern
- optional flow control
- controlled reset

Other links that may benefit from this standard link interface approach are the front-end links and the links used in the trigger system.

3. S-LINK DEVICES

Today two types of link cards exist: one based on Fibre Channel technology (Figure 3) [4], capable of moving data serially at 103 MByte/s over 500 m fibre-optic or 30 m electrical media and another based on parallel electrical transmission over a 10 m SCSI cable [5].

These link cards are implemented as plug-in modules. For final applications the link electronics may be integrated into the ROD and ROB designs. We are testing such an integration procedure (Fibre Channel S-LINK integrated with S-LINK to PCI) to see if there are any complications in copying the high-speed design with other CAD tools and PCB layouts.

4. ATLAS APPLICATIONS

4.1 DAQ Prototype-1

The ATLAS DAQ/Event Filter Prototype-1 Project (DAQ-1) [6] is producing a prototype system representing a “full slice” of a DAQ suitable for evaluating candidate technologies and architectures for the final ATLAS DAQ system.
In this project S-LINK is used as the prototype of the read-out link. Currently, in the Read-out Crate, a CES RIO2 with an S-LINK to PMC interface is used to emulate the ROB (Figure 4). A LynxOS library [7] has been written and performance measurements have been made [8]. For simple ROB applications implemented on a RIO2/8062, an event handling frequency between 36 KHz and 67 KHz have been measured for event sizes of 1084 and 64 bytes respectively. Maximum performance measured on this platform is 72 MByte/s for packet sizes of 8 KByte or more, with an overhead of 8μs. Those tests have been made with the SLIDAS test tool which can generate full-speed ROD-like data. Also programs that can emulate ROD data to be fed into the read-out crate have been made to test the functionality of the system without needing a real detector or ROD.

The DAQ-1 project has also defined the format of the data that is sent over the read-out link (Figure 5)[9]. For ease of implementation and cost reasons, the dataformat is designed in such a way that the ROD may be implemented easily in hardware, i.e. without the need for processors or large storage. The dataformat includes both a header and a trailer, and uses the ability of the link to transfer control words to signal the start and end of each event.

![Figure 5: Draft Read-out Link data format](image)

### 4.2 ROB-in

The Royal Holloway / University College of London has designed the input stage of the ROB, called the ROB-in [10]. The PCI board (Figure 6) contains an INTEL i960RP processor with a PCI interface and a 512 KByte memory which stores the event data. Data coming from S-LINK is written directly into the memory without needing any intervention of the processor. The processor is mainly used for memory management and for handling Region of Interest request messages.

Performance measurements with the SLIDAS data generator show that the input to memory can sustain a speed of 130 MByte/s. With an event size of 1 KByte, the processor can handle the event data at a rate of 75 KHz. The new version of the board will use an i960RD processor, which runs internally at 66 MHz. It is expected that this board will be able to run at the rate of 100 KHz that the final ATLAS system requires. One prototype of the ROB-in board is in use in the ATLAS DAQ/Event Filter prototype - 1 project. A PMC version of the board is being manufactured which better fits the VME environment that is used in the project.

![Figure 6: PCI version of ROB-in with S-LINK connector](image)

### 4.3 Transition Radiation Tracker (TRT)

The block diagram of the Transition Radiation Tracker (TRT) read-out driver (Figure 7) [11] shows a typical ROD design. Links from the read-out chips running at 40 Mbps using LVDS levels are connected to the readout part (RD). The outputs from the RDs are connected to Zero suppression (ZS) circuitry and buffer.

The clock and data are received from the Trigger module through the Trigger Module Interface. The header of the event, which follows the ROD data format (Figure 5), is generated at the Header Generator part using headers from the read-out chips and data from Trigger Interface.
4.4 Calorimeter trigger ROD

The ROD of the Level-1 Calorimeter Trigger [12] collects data from level-1 accepted events over a pipeline bus and sends them via an S-LINK interface to a ROB. The pipeline bus was designed to match all important aspects of the S-LINK hardware: e.g. both interfaces employ a FIFO concept with a 32-bit bus and they are clocked with the same clock frequency of 33 MHz. The data is already received on the ROD in a sequential order. The ROD adds an event header and trailer to the data set and stores it in a FIFO memory until it can be transmitted with the S-LINK to the level-2 buffer. In total eight to sixteen S-LINKs will be needed.

4.5 Monitored Drift Tube (MDT)

The first detector to use S-LINK for the readout was the Monitored Drift Tube detector (MDT) [13]. In 1997 it used the test beam at H8 in which the data was read out over a fibre-optic S-LINK and an S-LINK to PMC interface plugged on a RIO2. This card in turn was read out by the RD-13 DAQ software which still is the standard software for test beams.

They could either read the outputs of the discriminators over analog links into Time to Digital Converters (TDC) in a VME crate, or they could use the TDCs which are on the chamber and read the digitised data out over S-LINK. In both the 1997 and 1998 testbeams the two systems have been used in parallel. In this application S-LINK is actually used as a front-end link.

NIKHEF designs the MDT ROD, called NIMROD (Figure 8). The NIMROD version with an S-LINK output is expected to be ready by the middle of 1999.

4.6 TileCal

In August 1998 the ATLAS TileCal became the second detector to use S-LINK as the front-end link [14]. The DAQ system looked similar to the one from the MDT. They read out both over S-LINK and with separate digitiser/ADC cards. The data from the two read-out paths matched very closely except for some gain differences between the two different digitiser cards. In total more than 100,000 events have been read out over S-LINK, which corresponds to a few GB per event. The maximum rate data was taken into RIO2 was 15 KHz with 2 KByte events. This includes processing of the data in the RIO2.

4.7 Trigger supervisor

The ATLAS Trigger Supervisor [15] uses S-LINK as a trigger link. It dispatches level-1 trigger information describing the regions of interest (ROI) to the level-2 processing farm and the ROBs. Currently the way it accomplishes this is through a processor farm coupled with hardware assisted buffered I/O. On the input to the Supervisor there is an S-LINK connection from the level-1 system that provides a transmission per event with the level-1 data needed by the Supervisor. The Input S-LINK Distributor buffers and dispatches this data (which arrives at a maximum rate of 100 KHz) to one of several PMC cards attached to the Supervisor processors (one PMC per processor). The processors send requests to the ROBs via the same PMC connection. The S-LINK Distributor buffers the requests and intelligently fans the requests out to a number of S-LINK channels (one per ROB crate in the current scheme). This application also uses the ability of S-LINK to send control words.

A prototype of the Trigger Supervisor was built and has been used in several level-2 demonstrator systems. In those demonstrator systems, the level-1 input was emulated by a RIO2 with a PMC to S-LINK card. With a single processor, an event handling rate of 27 KHz has been shown. As the system is scalable, with only five processors the final ATLAS requirement of 100 KHz can readily be met.
5. APPLICATIONS OUTSIDE ATLAS

S-LINK is also used outside ATLAS. The COMPASS experiment will use 200 commercial fibre-optic S-LINKs and has built an S-LINK to PCI interface with a large buffer memory that can hold all data from one spill [16]. The COMPASS equivalent of a ROD is the CATCH-X board. It has 16 HOTLINK inputs and one S-LINK output; a prototype in VME format with four HOTLINK inputs will be ready by the end of 1998.

Applications outside HEP such as the ASDEX Upgrade fusion experiment and the MegaPrime astronomy camera have advanced plans to use S-LINK. Since 1997 the Olivetti and Oracle Research laboratories use S-LINK in combination with Linux drivers for moving video and keyboard data to and from remote terminals.

6. FUTURE

As the Muon Trigger and Tile Calorimeter are planning to use S-LINK as the front-end link, there is a requirement of making a radiation tolerant version. We will build such a version if a suitable serialiser chip is selected by the ATLAS front-end link working group. In preparation of this we are investigating radiation tolerant programmable logic chips. When this rad-tol version is available, link users may just replace the link card without modifying their own hardware as all S-LINK link cards are compatible. Another project will try out a method to have S-LINK inputs on the rear-side of VME crates, as this can solve both wiring and cooling problems that may arise in a large scale setup. Other ongoing projects aim to reduce the cost of the physical links by using components of more popular technologies like Gigabit Ethernet. Last but not least, a major part of the S-LINK project will continue to focus on supporting users by performing design reviews and loaning equipment.

7. CONCLUSIONS

The S-LINK specification describes an easy-to-use datalink which relieves read-out designers from the task of designing high frequency transmission circuits with error detection capabilities. Links, interfaces and test tools have been designed and are commercially available. S-LINK has been used already in several applications within ATLAS, other experiments and also outside high energy physics. Considerable knowledge and experience with the links, test tools and software has been built up, while also the robustness of the cards and tools has been proven. Ongoing efforts are being made to reduce the price of the links, to make a radiation tolerant version and to allow easier integration into large scale systems. Furthermore extensive support is given to projects inside and outside ATLAS that want to incorporate S-LINK (http://www.cern.ch/hsi/s-link).

8. REFERENCES


[10] B. Cranfield, “Prototyping hardware for the ATLAS readout buffers”, *


DAQ
ARCHITECTURE OF THE BABAR ELECTRONICS SYSTEM

A.J. Lankford, Department of Physics and Astronomy, University of California, Irvine, CA 92697-4575 (email: lankford@lankford.ps.uci.edu)

and the BABAR Collaboration

Abstract

An overview of the Electronics System for the BABAR Experiment, emphasizing architectural issues and development of new components, is presented. The BABAR architecture is quite similar to the architectures planned for the LHC. It is multilevel, pipelined, and nearly deadtime-free. An unusual level of standardization has been achieved across front-end electronics subsystems. Buffer architecture, links and protocols, readout module, and interfaces to timing, DAQ, and controls are all standardized. Seven custom integrated circuits have been developed to tailor the architecture to the detailed characteristics of, and to realize the full performance of, the BABAR detector systems.

1. INTRODUCTION

The BABAR Experiment will study CP violation at the SLAC B-Factory. Its detector consists of five major systems: a silicon vertex tracker [1], a cylindrical drift chamber with dE/dx capability [2], a particle identification system (DIRC) based on imaging of Čerenkov rings [3], a cesium-iodide crystal calorimeter [4], and a muon identification system (IFR) based on resistive plate chambers [5]. The specialized requirements of each detector system are addressed by front-end electronics customized to the detector technology but integrated into a uniform data acquisition architecture.

2. OVERVIEW OF ARCHITECTURE

BABAR has adopted a two-level trigger and data acquisition architecture. At Level 1, the trigger is optimized for simplicity and speed. It is based on a reduced set of detector data from the drift chamber and calorimeter. It consists of a pipelined, hardware processor and is nearly without deadtime. Its latency is 12μsec, and it is designed to provide an output trigger rate of less than 2kHz. During the level 1 latency, the full detector data sample is held in circular buffers. At the final level, which is referred to as Level 3, the data acquisition system assembles events over a commercial network into the memory of a farm of level 3 processors. The level 3 output rate is expected to be about 100Hz.

The level 3 trigger, or Online Event Processor, performs final event selection in commercial CPUs working with the complete set of detector data. The level 3 trigger is followed by online prompt reconstruction in the same farm. The architecture is designed to accommodate an optional Level 2, operating over the same network, if unexpected background conditions demand higher performance.

Although BABAR's architecture greatly resembles those designed for the LHC, it includes some unusual characteristics. The 12μsec level 1 latency is relatively long, but can be accommodated because all level 1 latency buffers are digital. Long latency simplifies and reduces the cost of the level 1 trigger. A minimum level 1 trigger spacing of 2.2μsec is enforced. This spacing simplifies logic design of the readout ICs, because each datum in the silicon tracker and drift chamber is then associated with only one level 1 accept; whereas, it introduces minimal deadtime, 0.4%. BABAR has no fast counters for triggering purposes, and bunch crossings are nearly continuous at 4ns. Hence, the timing of the trigger must be derived from the chamber, as part of track segment reconstruction, and from the calorimeter, as part of waveform processing. The resolving time of the trigger is approximately 150ns worst case. A window of data centered on the estimated trigger time, and covering several times this value plus the detector resolving time, is read out for each detector. For instance, this window is about 500ns wide for the silicon vertex tracker and 4-16μsec wide for the calorimeter. The precise event time is determined off line.

3. DETECTOR-SPECIFIC ELECTRONICS SUBSYSTEMS

All detector-specific, or front-end, electronics subsystems of BABAR share a common architecture. Each front-end chain consists of an amplifier, digitization (discriminator or flash ADC), a circular buffer (to store data during level 1 latency), and a derandomizing buffer (to store data between the level 1 accept and transfer to a Readout Module). Analog signal processing, digitization, and data readout occur simultaneously. All front-end subsystems except the IFR provide data sparsification. All level 1 latency buffers are digital; hence, it is possible to store data longer than analog buffers would
allow. The buffers of all front-end systems are managed by a common protocol. All level 1 latency buffers function as pipelines of fixed length, and all derandomizing buffers function as FIFOs which are capable of storing a fixed number of events, regardless of the actual implementation of the buffers. Each detector-specific subsystem also shares standard Babar interfaces to the detector-spanning, or common, electronics subsystems. In all cases, the front-end electronics is mounted directly on the detector for performance reasons. This solution also substantially reduces required cable plant. The design of the actual implementation of the buffers. Each custom integrated circuit solutions have been adopted for most subsystems.

3.1 Silicon Vertex Tracker Electronics

The Silicon Vertex Tracker (SVT) Electronics must record hits with coarse (~4-bit) pulse height resolution for 150,000 silicon strips. A readout IC [6,7], in Honeywell radiation-hard 0.8μm CMOS, integrates all functionality between the strip and 60Mbps serial readout links. It provides low-noise amplification and shaping, with programmable time constants to adjust shaping to detector capacitance and hit rates. It records pulse height using a time-over-threshold technique. It also provides level 1 buffering, sparsification, derandomizing buffer, and readout control logic.

3.2 Drift Chamber Electronics

The Drift Chamber Electronics must measure drift time and dE/dx for 7104 small drift cells. Drift time resolution of 2ns and pulse height measurement with dynamic range of 6 bits are required. In addition, prompt hit cell information must be provided for the level 1 trigger. The electronics is mounted on the chamber endplate opposite the center-of-mass boost. A 4-channel amplifier IC [8] in Maxim CPI semi-custom bipolar provides analog and discriminated outputs. An 8-channel digitizer IC [9, 10] in Hewlett Packard triple-metal 0.8μm CMOS provides a TDC with 1ns bins and 4MHz, bilinear, 6-bit flash ADC for each channel. The digitizer IC also provides level 1 buffering, derandomizing buffer, and sparsification.

3.3 Particle ID Electronics

The Particle ID (DIRC) Electronics must measure single photoelectrons from Cerenkov light sensed by 10,752 photomultiplier tubes. Time precision of at least 1ns is required in order to reject background. Amplitude resolution of 6 bits is required for gain calibration. Photomultiplier signals are received by Front-end Boards in crates mounted inside magnetic shielding for the PMTs. Eight channel analog ICs [11] in AMS 1.2μm CMOS provide zero-crossing discriminators for timing and a multiplexed analog output for pulse height measurement on a sampling basis. Digital ICs [12] in Atmel-ES2 double-metal 0.8μm CMOS contain TDCs, programmable level 1 latency and readout window, latency and derandomizing buffers, and sparsification for 16 channels.

3.4 Calorimeter Electronics

The Calorimeter Electronics must measure pulse height with very low noise (~500e) and large dynamic range (18 bits) for 13,320 photodiodes on 6,660 CsI crystals. In addition, it must tag the time of event data and provide prompt energy sums to the level 1 trigger. Redundant low-noise, charge-sensitive amplifiers are mounted on the crystals. The amplifier is based on a single-channel amplifier IC in AMS 1.2μm BiCMOS with split-range output. The two outputs of each amplifier are fed to a 4-crystal calorimeter auto-ranging and encoding (CARE) IC [13] in AMS 1.2μm BiCMOS which provides large dynamic range via four amplitude scales multiplexed to a 10-bit flash ADC.

3.5 Instrumented Flux Return Electronics

The Instrumented Flux Return (IFR) Electronics [14] must record hit strips for 50,000 channels of resistive plate chambers (RPCs) and associate the hits with the level 1 trigger. RPC strips are read out via 16-channel Front-End Cards (FECs) which discriminate and delay the signals during the level 1 latency. FECs are read out in groups of 64 by FIFO Boards, which are located in crates mounted on the flux return iron. TDC Boards provide precise timing information on groups of RPC strips.

4. DATA ACQUISITION

4.1 Front-end Links and Protocols

All elements of Babar front-end electronics are controlled via Babar-standard protocols on Babar-standard serial links. 60Mbps control streams are time-division multiplexed in groups of 16 by Readout Modules onto 1Gbps fiber control links which transport the control stream to transition cards on the detector. The transition cards derive the 60MHz system clock, demultiplex the 60Mbps control data, and distribute these signals to the front-end electronics, along point-to-point crate backplanes to the DIRC and IFR and via direct connections to the SVT, drift chamber, and calorimeter. This path transports both timing and slow control. The standard data path from detector-mounted electronics to Readout Modules is parallel to the control path. Groups of 16 serial data streams, up to 60Mbps, are multiplexed by the transition cards onto 1Gbps fiber data.
links. Data streams are demultiplexed and buffered on the Readout Modules. The standard readout protocol allows for both fixed and variable length records. This path is used for both event data and read back of registers. The calorimeter uses a separate set of Gbps links for its large data volume.

4.2 Readout Module

A single Readout Module (ROM) design, with two Personality Card types, serves all detectors. It provides the standard interfaces, deep event buffers, and a processor (300MHz PowerPC). Its implementation consists of a commercial single-board VME computer (Motorola MVME2306) with PCI mezzanine slots plus two custom boards. Together these two boards provide a DMA interface between the standard BABAR data and control links and PCI, via a PCI/960-bus bridge. The Controller Card provides a fast control and timing interface and manages front-end buffers. The Personality Card multiplexes and demultiplexes the control and data streams, provides the electro-optical interface, and provides intermediate storage of events. Two types of Personality Card were developed. The standard (triggered) Personality Card receives data from detector-mounted electronics in response to a level 1 trigger request. It is used by all subsystems for control and by all but the calorimeter for event data. An untriggered Personality Card interfaces to the untriggered Gbps data streams of the calorimeter and provides a triggering mechanism such that calorimeter data is presented in the same way as other detector data to the CPU. The commercial CPU and two custom boards assemble into a single-slot 9Ux400nm VME card. The ROM runs a real-time operating system, VxWorks, and provides a well-supported coding environment.

4.3 Event Assembly

ROMs assemble event data from front-end elements into “segments” of the event. Preprocessing of event data, or “feature extraction”, is also performed by the ROM. For instance, amplitude samples from the calorimeter are reduced to measurements of energy and time. Segments are read out from ROMs over VME by crate-level processors, the “Slot-1 ROMs”, which are standard ROMs, either without links to front-end electronics or performing this data collection function as well as their other functions. Slot-1 ROMs assemble segments into larger event “fragments”. From the crates, fragments are assembled into events in Level 3 processor memory over a commercial switching network. The initial implementation of this network used switched 100Mbps Ethernet. Studies have established that this solution provides adequate bandwidth for BABAR’s modest (~65Mbps) aggregate bandwidth. The BABAR data acquisition system consists of about 165 ROMs in 18 physical VME crates that are divided into 24 logical crates by segmented backplanes. The DAQ system is partitionable at the crate level such that any combination of subsystems or crates can run independently and autonomously with any combination of triggers.

4.4 Event Data Flow Control

Event synchronization is established by a Fast Control and Timing System (FCTS). This system consists of a DAQ master crate plus a Fast Control Distribution Module in each data acquisition crate. A system-wide clock of approximately 60MHz is derived from the PEP II RF system. A 5-bit event id and a 56-bit time (in units of 1/60MHz) are distributed with each level 1 accept signal and are checked at each stage of data collection and event assembly. Transmission to all crates and within all crates is isochronous. Distribution to Readout Modules in each crate is from distribution modules along a custom P3 backplane. The design of this backplane provides for standalone operation of a single crate in a laboratory without a master crate. Only the 5-bit event id is passed to the front-end electronics. The front-end electronics return the event id and trigger time (typically 5 bits) with the data for each level 1 accept. FIFOs in each module in the fast control distribution chain record the history of all fast control transactions for diagnostic purposes. Fast control modules are read out with each event to corroborate synchronization. Detection of an error in synchronization will result in a request through the FCTS to resynchronize.

Collection of data from the front-end electronics to the Readout Module occurs upon the issuance of a ReadEvent command from each ROM via the Clink to its associated front-end electronics. Each front-end element responds by synchronously transmitting data for the next event in its derandomizing (output) buffer. This mechanism simplifies event synchronization and prevents overflow of front-end buffers. Bandwidth of front-end data links and depth of front-end buffers are sufficient to limit the deadtime introduced by this mechanism to a fraction of a percent.

The data acquisition issues a buffer Full signal to throttle the trigger whenever any buffer in the system cannot accept an additional event. Each Readout Module monitors the occupancy of its associated front-end buffers, and issues a Full signal through the FCTS if either the front-end buffers or its own buffers fill. When a downstream buffer fills, for instance in the level 3 farm, backpressure builds until the ROM buffers fill and Full is issued by a ROM.

5. SUMMARY

In order to address the requirements of its detector and operating environment, BABAR has designed an electronics, trigger, and data acquisition architecture that is quite similar to architectures being designed for the LHC. For instance, the BABAR architecture is multilevel,
pipelined, and nearly deadtime free. It employs detector-specific custom ICs to realize the full performance of detector systems. Front-end electronics is detector-mounted. It simultaneously digitizes analog signals, writes data to buffers, and is read out to the data acquisition system. Although analog front-ends and digital readout circuits are located in close proximity, full analog performance has been realized without digital noise. The trigger system has two levels, with the option for an additional intermediate level. The first level trigger is based on pipelined hardware processors and utilizes tracking and calorimeter data. The higher level trigger is based on an online event processing farm of commercial processors and is integrated with a network-based event builder into the data acquisition system. The online system also includes a prompt reconstruction phase that performs full "offline" processing of the data.

The BABAR design incorporates an unusual level of standardization across detector-specific subsystems. Front-end electronics is customized to detector-specific needs; however, front-end buffer architecture and front-end links and protocols, for both readout and control, are standard. All off-detector electronics is standardized. The BABAR Readout Module provides standard interfaces to timing, data acquisition, and detector controls systems. It also provides a standard platform and code framework for detector-specific preprocessing and calibration code. Data acquisition crates, fast control and timing modules, and much detector controls hardware are also standard across BABAR systems.

All electronics design, fabrication, and testing for BABAR is now almost complete, as is installation of the components on the detector. BABAR will be commissioned with a cosmic ray run during the Autumn of this year, and will be installed in the PEP II accelerator during Spring 1999.

6. ACKNOWLEDGEMENTS

BABAR Electronics is the product of a large group of talented scientists and engineers, from laboratories and universities in Canada (Montreal), France (LAL Orsay, LPNHE Paris 6-7, X-PNHE Palaiseau), Italy (Frascati, Genova, Milano, Napoli, Padova, Pavia, Pisa, Torino), the United Kingdom (Bristol, Edinburgh, Imperial College, Royal Holloway, RAL), and the United States (UC Irvine, UC Santa Cruz, Caltech, Colorado, Colorado State, Iowa, Iowa State, LBNL, Maryland, Pennsylvania, Princeton, SLAC, Stanford), who deserve credit for the outstanding work described here. The author's work is supported in part by U.S. Department of Energy Grant DE FG03 91ER40679.

7. REFERENCES
The COTS Approach to the Read-Out Crate in ATLAS DAQ Prototype -1

G. Ambrosini\textsuperscript{a}, H-P. Beck\textsuperscript{b}, S. Cetin\textsuperscript{c}, T. Conka\textsuperscript{d}, A. Fernandes\textsuperscript{e}, D. Francis\textsuperscript{f}, F. Hogbe Nlend\textsuperscript{g}, M. Joos\textsuperscript{h}, G. Lehmann\textsuperscript{i}, A. Mailov\textsuperscript{j}, L. Mapelli\textsuperscript{k}, G. Mornacchi\textsuperscript{l}, M. Niculescu\textsuperscript{m}, J. Petersen\textsuperscript{n}, D. Prigent\textsuperscript{o}, B. Rensch\textsuperscript{p}, L. Ribeiro Monteiro\textsuperscript{q}, J. Rochez\textsuperscript{r}, R. Spiwoks\textsuperscript{s}, L. Tremblet\textsuperscript{t}, G. Une1\textsuperscript{u}

\textsuperscript{a} Laboratory for High Energy Physics, University of Bern, Switzerland.
\textsuperscript{b} CERN, Geneva, Switzerland.
\textsuperscript{c} Institute of Atomic Physics, Bucharest, Romania.
\textsuperscript{d} Bogazici University, Istanbul, Turkey.
\textsuperscript{e} Niels Bohr Institute, Copenhagen.
\textsuperscript{f} CERN, Geneva, Switzerland and Portugal.

Abstract

A prototyping project has been undertaken by the ATLAS DAQ and Event Filter group. The aim is to design and implement a fully functional vertical slice of the ATLAS DAQ and Event Filter with maximum use of Commercial Off The Shelf components (COTS).

The Read-Out Crate is a modular component within the vertical slice whose principle functionality is to receive, buffer and forward detector data to the Event Filter systems via an event building network and to the Level 2 Trigger. As required by the project, the initial implementation is based on commercial components, namely VMEbus, PowerPC based single board computers and the Lynx-OS real-time operating system. The measured performance is compared to the results of a discrete event simulation of the Read-Out Crate using the PTOLEMY modelling tool. It has allowed us to model and study the Read-Out Crate performance based on a mixture of existing and forthcoming technologies, an example of the latter being VMEbus 2еSST, and different architectures. Results from studies in this area are also presented. The design and initial implementation of the Read-Out Crate is presented.

1. INTRODUCTION

The final design of the Data Acquisition (DAQ) and Event Filter (EF) system \cite{1} for the ATLAS experiment at the LHC is not scheduled to start before 2000. However, due to the complexity of the system and to the severe requirements in terms of data rate and volume, hardware and software technologies must be evaluated and aspects of system integration studied before a final design can be implemented. The ATLAS/DAQ group has chosen to approach these investigations by building a fully functional prototype of the DAQ system \cite{2} consisting of a complete "vertical slice" of the ATLAS DAQ/EF architecture including all the elements of an online system from detector read-out to data recording. Since it is understood that this prototype will not fulfil the final performance requirements it has been given the name DAQ/EF prototype "-1".

The DAQ/EF prototype -1 architecture contains a component which is responsible for receiving and buffering event fragments, event building and mass storage. This logical component, called the DataFlow is shown schematically in Figure 1.

Figure 1: DAQ/EF DataFlow architecture

The Read-Out crates (ROCs) are responsible for moving the data between a subdetector and the Event Builder. Each of the Read-Out Buffers (ROBs) in a ROC receives and buffers detector event fragments of size ~1 Kbyte at a rate of ~100 kHz. This rate is determined by a Level 1 trigger system. To cope with the total amount of data from the detector (~100 Gbyte/s) a large number (~150) of ROCs is required.

A Level 2 Trigger system accesses a subset of the data in the ROBs - the so-called Regions Of Interest (ROIs) - to provide an event rejection factor of ~100. For events accepted by the Level 2 Trigger, the associated event fragments within a crate are collected and sent via the Event Builder \cite{3} to the Event Filter \cite{4} where a final event selection based on the reconstruction of complete...
events is performed before the events are written to mass storage.

2. THE READ-OUT CRATE

A logical view of the ROC is shown in Figure 2. It consists of a Local DAQ (LDAQ), one or more Read-Out Buffers, an Event Builder Interface (EBIF) and a Trigger (TRG). This logical view also foresees the possibility to collapse several logical modules (e.g. TRG and ROB) into one physical module. The ROB, EBIF and TRG are instances of a logical object referred to as an I/O Module (IOM)[6]. The different modules have the following functionality, related to the main data flow:

- The LDAQ provides the run control and monitoring functions within the ROC and communicates for that purpose with the other modules in the ROC.
- The TRG is responsible for the control of the data flow in the ROC. It receives and buffers data control messages from the trigger system and distributes them to other IOMs within the ROC. The types of data control messages are described below.
- The EBIF receives data control messages from the TRG. It collects and buffers event fragments from the ROBs via a process called Data Collection (DC). The crate fragments are output to the event builder.
- The functionality of the ROB includes the reception and buffering of event fragments from the detector Read-Out Drivers (RODs). In addition the ROB receives data control messages from the TRG and the EBIF which define the actions to be performed on the buffered event fragments. The ROB provides data to the EBIF for data collection and to the Level 2 Trigger system.

Figure 2: Logical model of the ROC

Data control messages are exchanged between the IOMs via an intra-crate message passing system. The following data control messages are defined:

- **Level 2 Reject (L2R):** This is sent from the TRG to the ROB. On reception of this message the ROB removes and event fragment from its internal buffers.
- **Level 2 Accept (L2A):** This is sent from the TRG to the EBIF. On reception of this message the EBIF collects all the event fragments associated to a single event from the ROBs.
- **Region-Of-Interest (RoI) Request:** This is sent from the TRG to the ROBs. It is a request from the Level 2 trigger system for data. On reception of the message the ROBs output data to the Level 2 Trigger system.
- **Discard:** This is a message sent by the EBIF to the ROBs. It is essentially the L2A message relayed to the ROBs to inform those that data collection for a specific event has been performed and that the associated event fragments may be removed from the ROB buffers.

3. INITIAL IMPLEMENTATION

The initial implementation of the ROC does not provide all the functionality foreseen by the high-level design. External data producers and consumers (e.g. the ROD, the trigger system) are not yet available. Consequently the performance measurements focus on the data flow within the ROC while external data input and output are emulated in different ways.

![Figure 3: Architecture of the CES RIO2 VMEbus CPU module](http://www.ces.ch/Products/Processors/RIO28060/RIO28060.html)

The hardware used consists of a multiprocessor system based on the CES RIO2 8061/8062 and the Motorola MVME2600/2300 CPU[7,8]. The architecture of these modules, see Figure 3, is common to most VMEbus boards based on PowerPC and PCI. An extensive evaluation of the RIO2 and other second generation VMEbus CPU boards[9] have shown that their CPU and I/O (PCI, VMEbus) performances are similar (for the same type of CPU).

---

The DAQ software runs under LynxOS\(^5\) but the use of operating system specific features was reduced to a minimum in order to obtain a good level of code portability and performance. The OS features still used are:
- Direct access to H/W components from user libraries via shared memory segments
- Reservation of physically contiguous memory
- Time functions
- Exit handling

The TRG, EBIF and ROB applications are single process. For reasons of performance, requests for I/O are served via polling and not by interrupts and I/O drivers.

In this implementation all interprocessor communication is via VMEbus and implemented in software as a message passing library based on shared VMEbus memory. The flow of data control messages and event fragments on VMEbus and the associated VMEbus parameters are listed in Table 1. Write posting and read pre-fetching on VMEbus are enabled whenever possible to achieve the best performance. In addition, a single VMEbus request level and fair arbitration were used.

---

### Table 1: Data flow on VMEbus

<table>
<thead>
<tr>
<th>Msg/transfer type</th>
<th>Size (bytes)</th>
<th>Relative frequency</th>
<th>Direction</th>
<th>Transfer type</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2R</td>
<td>24</td>
<td>N*100</td>
<td>TRG -&gt; ROB</td>
<td>DMA MBLT D64</td>
</tr>
<tr>
<td>RoI</td>
<td>56</td>
<td>N*10</td>
<td>TRG -&gt; ROB</td>
<td>Single cycle D32</td>
</tr>
<tr>
<td>L2A</td>
<td>24</td>
<td>1</td>
<td>TRG -&gt; EBIF</td>
<td>Single cycle D32</td>
</tr>
<tr>
<td>Discard</td>
<td>24</td>
<td>N*1</td>
<td>EBIF -&gt; ROB</td>
<td>Single cycle D32</td>
</tr>
<tr>
<td>DC</td>
<td>N*1024</td>
<td>1</td>
<td>ROBs -&gt; EBIF</td>
<td>DMA MBLT D64</td>
</tr>
<tr>
<td>Monitoring</td>
<td>N*1024</td>
<td>&lt;1</td>
<td>ROBs -&gt; LDAQ</td>
<td>DMA MBLT D64</td>
</tr>
<tr>
<td>LDAQ communication</td>
<td>-100</td>
<td>N*&lt;1</td>
<td>LDAQ -&gt; IOMs</td>
<td>Single cycle D32</td>
</tr>
</tbody>
</table>

a) Number of ROBs, b) Number of IOMs

As mentioned above, the initial implementation has reduced functionality in several areas compared to the logical model described in the previous section:

- In the TRG application, data control messages are generated internally. The loading of the PCI bus by an external trigger system is emulated using a simple PMC. The latter transfers data over PCI bus to system memory in DMA mode with a block size of about 1 KByte and at a rate corresponding to that at which control messages are generated internally.
- The ROBs generate event fragments internally and do not transfer any ROB fragments to the Level 2 Trigger system. The RoI requests received do not trigger any data transfers.

- The EBIF performs data collection over VMEbus but does not transfer any event data to the Event Builder.

Since there are no external data sources, the synchronisation between the TRG and the ROBs has to be emulated: whenever a ROB has produced an event it transmits its current event number over VMEbus to the TRG. The TRG will then only send data control messages corresponding to events where all fragments have been generated by the ROBs. The data control messages generated internally by the TRG are produced with the ratio 1 L2A : 100 L2R : 10 RoI.

### 4. PERFORMANCE MEASUREMENTS

A measure of the global performance of the ROC is indicated by the frequency at which the individual ROBs input event fragments from the detector links. This quantity was measured in a ROC configuration without the LDAQ module, as a function of the number of ROBs in the crate (see Figure 4). The measurements were performed using operating system timing functions and cross-checked using VMEbus analysers from VMetro\(^6\). These allow the measurement of the VMEbus transfer rate and bus utilisation.

![Figure 4: Performance with TRG, EBIF and ROB applications working without the LDAQ control](http://www.lynx.com)

In the following sections the type of ROB (RIO2 or MVME2604) will not be mentioned explicitly since it has been verified that the results of the performance measurements are not significantly different for the CBS and Motorola CPU boards.

For one ROB a performance of 126 kEvents/s has been measured. This value drops to 26 kEvents/s for five ROBs. In the ROC the VMEbus throughput was measured to be 6 Mbyte/s while the VMEbus utilisation was 70% independent of the number of ROBs. A VMEbus utilisation\(^7\) of 70% is not far from the

\(^{5}\)http://www.lynx.com

\(^{6}\)http://www.vmetro.com

\(^{7}\)The number of bus samples with BBSY# active divided by the total number of samples
maximum obtainable in a single cycle dominated multiprocessor environment\footnote{The remaining 30\% are consumed largely by arbitration overheads}.

This clearly indicates that, even in a single ROB configuration, the performance is limited by the bandwidth available in a single cycle dominated VMEbus system. The overlaid 1/N curve in Figure 4 confirms this in showing that the product of the number of ROBs and the number of events processed remains constant. This is because all data control massages are sent sequentially to the receivers. As the messages contain identical information it would be more efficient if they could be broadcast.

Performance measurements have been done for a ROC configuration controlled by an LDAQ module and having only one ROB. In this case the focus was on the effect of event monitoring on overall event rate. One LDAQ sampling transaction with an IOM means in this case an LDAQ monitoring request followed by a DMA transfer of 1KByte event. As Figure 5 shows, an increasing rate of the event sampling by the LDAQ, on different IOM types (ROB, EBIF or TRG) has the effect of degrading the event rate in the ROC by few percent. The comparison between the three curves shows that the impact of event monitoring is stronger for the ROB than for the other two IOMs. Nevertheless for a event monitoring in the range of 100Hz, the event rate in the ROC has decreased by only ~2 percent in case of ROB monitoring and by 0.4 percent in case of TRG or EBIF monitoring.

![Figure 5: LDAQ impact on the event rate in a ROC configuration: LDAQ, TRG, EBIF, 1* ROB](image)

5. MODELLING

The performance of VMEbus transfers between two RJ02s as well as the characteristics of the on-board PCI have been studied\footnote{The Almagest – Volume O: Ptolemy 0.7 User’s Manual. http://ptolemy.eecs.berkeley.edu/papers/almagest/user.html}. Based on these measurements and the knowledge of the data flow on VMEbus in the ROC, see Table 1, a model of the ROC (without LDAQ) has been developed to study rate-limiting factors and variations in technologies and architectures. All IOMs (TRG, EBIF, ROB) of a ROC have been simulated\footnote{The Almagest – Volume O: Ptolemy 0.7 User’s Manual. http://ptolemy.eecs.berkeley.edu/papers/almagest/user.html} within the discrete event domain of the Ptolemy framework\footnote{The Almagest – Volume O: Ptolemy 0.7 User’s Manual. http://ptolemy.eecs.berkeley.edu/papers/almagest/user.html}. The model is shown in Figure 6. The ROD, Level 1, Level 2 and EB are simply modelled as external data producers / consumers. As the measurements done with the ROC have indicated that the overall system performance is limited by the available I/O bandwidth on VMEbus and PCI, software latencies have not been taken into account. Additionally, the transfers on PCI and VMEbus have not been modelled at the protocol level. All external links run at the nominal speed of PCI except for the links to the detector front-end which have infinite bandwidth as the maximum event rate otherwise would be limited by the PCI of the ROBs to less than 70 kHz. The model was parameterised with performance figures measured on the VMEbus processors used and included arbitration mechanisms for both VMEbus and PCI.

![Figure 6: ROC model](image)

The maximum event rate is shown in Figure 7 for five cases:

- Measurements: these are the event rates measured for one to five ROBs and have already been discussed in the previous chapter.
- VME model: this curve was calculated to check the model. It simulates the full intra crate traffic on VMEbus including the synchronisation messages that are sent from each of the ROBs to the TRG (one single cycle per ROB and event). The calculated figures match the measured performance to within a few percent, and therefore confirm that the system is I/O bound and computing times can be neglected.
- VME model w/o synchronisation: this is a simulation of the system performance without the synchronisation messages. These are only required in the prototype to replace the missing external synchronisation.
parameterised with measured performance figures for the total bandwidth is limited by the common PCI bus.

- PVIC. The intra-crate traffic has been organised such that VMEbus is efficiently used for the data collection (ROBs to EBIF) that mainly consists of D64 MBLT transfers. The PVC carries all the data control messages. The reject messages from Level 2 are now broadcast to the ROBs as well as the RO messages and the discard messages. The improvement in performance is mainly due to the broadcast. The additional bandwidth of PVIC and the more efficient use of VMEbus only play a minor role as the total bandwidth is limited by the common PCI bus.

- VME model w/o synchronisation + 2eSTT: the 2 edge Source Synchronous Transfer (2eSTT) protocol\(^{11}\) is a proposed addition to the VMEbus standard. Its main features are improved bandwidth (>300 MByte/s) and broadcast protocol. The system performance has been modelled with all traffic routed across VMEbus. As VMEbus, in the model, still is routed via PCI, the PCI bandwidth was adjusted to the figures for a 64bit / 66 MHz PCI (528 MByte/s) in order to be able to exploit the full potential of the 2eSTT protocol. The comparison to the curve “VME model w/o synchronisation” demonstrates the effects of the 2eSTT protocol. The higher bus bandwidth globally speeds up the system by a factor of three and the additional broadcast capability flattens the curve, which leads to an even better performance for ROCs with many ROBs.

Figure 7: Maximum event rate (measurements and simulations)

\(^{10}\)http://www.ces.ch/Products/Connexions/PVICFamily/PVIC.html

\(^{11}\)VITA 1.5, 2eSTT, draft 1.5, http://www.vita.com/vso/draftstd/2eSTTd1.5.pdf

It is to be noted that the model has been parameterised with (conservative) speculative figures for the timing of a 2eSTT capable VMEbus processor.

6. SUMMARY AND CONCLUSIONS

The Read-Out Crate in ATLAS DAQ/EF prototype -1 has been described. A configuration consisting of a LDAQ, TRG, EBIF and up to five ROBs has been implemented in VMEbus using CES RIO2 8061, RIO2 8062 and Motorola MVME2604 PowerPC/PCI based processor modules. Data control and synchronisation messages between IOMs are exchanged via VMEbus, which is also used for the Data Collection. External input to the TRG is emulated by a simple PMC interface, while the ROBs and the EBIF have no external I/O. The performance was measured in terms of the event rate seen by the ROBs.

The performance results can be summarised as follows:

- With one and five ROBs the performance was measured to be 126 kHz and 26 kHz, respectively. The performance decreases inversely to the number of ROBs.

- The performance was limited by the rate at which data control messages could be transferred over VMEbus. A throughput of only 6 Mbyte/s was measured and is due to the use of VMEbus single cycles in the message passing and the method of synchronisation between the TRG and the ROBs.

A simple discrete event model (PTOLEMY) of the data flow on both the PCI of the IOMs and VMEbus has been developed. It has allowed to quantitatively verify that the global performance of the ROC is dominated by VMEbus I/O. Based on measured and estimated values for two broadcast capable buses, PVIC and VMEbus 2eSTT, the system performance has been computed. The results of the model are:

- There is a good agreement between the measurements and the model for the current implementation.

- The model has shown that the additional synchronisation messages, required due to the absence of an external trigger, do influence the overall system performance at the level of 20-30%.

- Adding a secondary, broadcast capable bus (e.g. PVIC) to the system significantly improves the performance by a factor of ~3 to 240 kHz for one ROB and 110 kHz for 10 ROBs respectively.

- Routing all traffic via an improved VMEbus based on the proposed, broadcast capable 2eSTT protocol leads to a speed-up slightly higher than that calculated for the dual bus scenario with the additional advantage of a less complex system.

The results presented above, obtained in a complex multiprocessor DAQ application, confirm some
7. REFERENCES


observations made previously'. Modern PowerPC/PCI VMEbus CPU boards have shown impressive progress in the area of processing but much less so in the area of I/O, notably VMEbus. This may change with the advent of new VMEbus standards (VME64x and 2eSST).

The results also show that a system based on COTS components is a viable solution. Even though the maximum performance obtainable with today's hardware is still significantly below the final ATLAS requirements, we are confident that this design in combination with forthcoming technologies can provide the required performance on the time scale of ATLAS.
Backend VME module for ATLAS TRT read-out system

Peter Lichard, CERN, Geneva, Switzerland (email: Peter.Lichard@cern.ch) for the TRT collaboration

Abstract

The ATLAS TRT detector is very demanding in terms of data volume to be transferred from the front-end to the back-end electronics. The data from 27000 high speed digital links will be collected in Readout Drivers (ROD) where the first data compression and event building are performed. A reduced ROD prototype (miniROD) has been built and tested in a small scale system. A description of the ROD is given as well as test results of the miniROD and plans for the complete ROD.

1. INTRODUCTION

The ATLAS TRT is a gaseous detector consisting of 420000 straws covering the barrel and endcap regions. It aims at providing tracking information with a good resolution and electron identification. The large occupancy of the detector requires special care on data compression and use of high speed digital links.

The back-end readout module (ROD) collects data from 104 40Mbit/s digital links, thus processing more than 4Gbit/s data flow. Collected data are formatted and made available to both the data acquisition system via a high speed serial interface (S-Link) and the local monitoring system. The output data are compressed to cope with the limited bandwidth of the output link. Different data compression schemes have been studied and implemented in FPGAs in the ROD.

A full version of the ROD has been designed and a prototype of a scaled-down ROD (miniROD) has been produced and tested.

A complete description of the ROD is given as well as the description and test results of the miniROD. A description of the different data compression schemes is presented.

2. POSITION OF THE ROD IN THE ATLAS TRT READOUT

A schematic view of the ATLAS readout system is shown in figure 1. Front-end boards transmit data to the RODs located in USA15 counting room. In the case of the TRT, the ROD is responsible for resynchronisation of all incoming links, data buffering, zero suppression and local event building. RODs are VME 9U modules connected to TRT-TTC modules used for trigger, timing and control (TTC) distribution; a local VME computer is used for control and monitoring purposes. Zero suppressed and formatted data are sent through a fast data link to the readout buffers (ROB) located in the surface counting room [1].

3. COMMUNICATION WITH ROD

There are four basic communication channels. The ROD receives data from the front end ReadOut Chip (ROC), clock and trigger information from the TRT-TTC module. Monitoring and control is done through the VME backplane. Packed and zero-suppressed data are sent to the ROB via a high speed link.

Figure 1. Schematics view of the ATLAS readout system

Figure 2. Read-out and TTC segmentation
3.1 Front End Interface

The front-end electronics applies two thresholds to the detector signal, one for tracking functionality (low threshold to detect minimum ionising particles) and one for transition-radiation functionality (high threshold to detect transition-radiation X rays). The low-threshold signal is sampled every 3ns in order to yield the proper position resolution (and hence momentum resolution). This leads to 9-bit information per channel and bunch crossing.

An event generated by a ROC consists of a header block (trigger number, BC number, status bits, etc.), and of 16 data blocks containing data from 16 straws and three consecutive bunch crossings.

There are 104 ROCs connected to one ROD. Each ROC outputs data on one serial differential copper link running at 40 Mbits/s and using LVDS electrical standard [2]. NRZ encoding is used and a proper phase adjustment of receiver clock is done in the ROD.

In order to facilitate the task of the level-2 trigger system, the detector is read-out according to the trigger level-1 region of interests (Rol). In the case of the end-cap TRT, the read-out is done along the ‘z’ (beam) direction as shown in figure 2. Three RODs cover oneRol.

3.2 Timing, Trigger and Control interface

The TTC signals are sent to geographical zones of the detector within which there is no need for fine timing adjustment. Such zones are 1/32 of a wheel in the end-cap region (figure 2) and 1/32 of a module in the barrel.

The TTC distribution zone (e.g. 1/32 of a wheel in the end-cap) and the read-out zone (e.g. 1/96 of all the wheels of an end-cap) being different, the TTC interface to the front-end cannot be included in the ROD and hence an additional TRT-TTC module is necessary. One such module, associated with 3 RODs cover 1/32 of the end-cap part and 3/32 of the barrel part. So, 3 RODs are connected to one TRT-TTC module through the P3 VME 9U connector from which they receive the 40 MHz BC clock, the 24-bit L1A number (LIID), the 12-bit BC number (BCID) and the 8-bit trigger-type word.

3.3 VME interface

The configuration of the ROD and the monitoring of events are done through VME.

3.4 Interface to the ROB

A high speed data link (S-LINK [3]) is used to transport the data to the ROB. The maximum data transfer rate is 800Mbits/s.

4. BLOCK SCHEME OF ROD

The block diagram of the ROD is shown in figure 3. The links coming from the ROCs are connected to the front end readout part (ROC_RD); outputs from ROC_RDS are connected to the Zero suppression (ZS) circuitry and buffer. Clock and trigger information are received from the TRT-TTC module. The header of the event is generated at the HEADER part using the header blocks coming from the ROCs and data from the TRT-TTC. A buffering capability before and after the ZS block allows to check the proper work of the board. The complete event is fed to the S-LINK. The ROD is built in a modular way and there are four identical blocks for 26 inputs each.

![Figure 3 ROD block diagram](image-url)
synchronise data from one event a mechanism described at the end of this chapter is implemented.

There is a need to adjust the clock phase in the ROD for each input serial line in order to use a proper sampling data window. For this purpose, a phase measurer is implemented and there is the possibility to choose either the rising or the falling edge of the ROD clock to strobe the data in the input synchronisation circuit.

This rather crude (rising or falling edge of clock) delay is sufficient as the input data are guaranteed to be valid for more than 12.5 ns by the serial link design.

**Synchronisation of input data**

To facilitate zero suppression, storage and (local) event building it is necessary to convert data from serial to parallel format and resynchronise them. If the “start of event” preamble is detected, data of one channel (27 bits) are stored in a shift register with parallel output. After all data from one channel have been loaded, the content of the shift register is written into a parallel register and the shift register can handle data from another channel.

If one (or more) ROC does not provide data within a time span of 5 clock cycles after the first ROC transmitted data, an error condition is detected and written into the header of the event.

### 4.2 Zero Suppression (ZS)

Different zero suppression schemes have been proposed and simulated [5]. The ‘classical’ zero suppression scheme where a non-empty channel is coded with an address followed by the data is inefficient because of the high occupancy of the TRT detector. Few viable ZS schemes have been found, based on contents oriented data suppression mechanism. The optimum ZS scheme depends on the LHC luminosity and hence ZS should be programmable. Two possibilities were studied:

- The use of a Digital Signal Processor with different software for different ZS formats. It was found that there was not sufficient computing power in a single device for the expected data rates (4 Gbits/sec peak).
- The use of in-situ programmable FPGAs, assuming that the pin-out of the chip is not affected by the algorithm change. This option was successfully implemented in ALTERA Field Programmable Gate Arrays.

Output data from ZS are stored in a VME accessible buffer for monitoring and testing purposes and/or sent to S-LINK interface.

**Example of a gated zero suppression scheme**

Physical simulations have shown that the following data suppression scheme is very efficient at high luminosity. A gate (of programmable width) is applied in the second read-out bunch crossing.

- if the low threshold signal is active within the gate, the channel is defined as valid and ‘1 H F E1 E2 (DTM1) (DTM2)’ is transmitted. ‘H’ is the value of high threshold signal. ‘F’ flags the presence of a falling edge in the third read-out bunch crossing, ‘E1’ and ‘E2’ flag the presence of up to 2 rising edges in the 2 first read-out bunch crossings, (DTM1) and (DTM2) are optional 3-bit positions of rising edges.
- if the low threshold signal is not active in all 3 read-out bunch crossings, the channel is defined as empty and only ‘0 0’ is transmitted
- if the low threshold signal is not active within the gate but active outside, the straw is defined as not empty, not valid and ‘0 1 H’ is transmitted where ‘H’ is the value of the high threshold signal.

With this zero suppression scheme the output bandwidth of the ROD does not exceed 800 Mbits/s even for twice the nominal luminosity. Results from simulation with different gate widths are shown in Figure 4.

![Figure 4. Data bandwidth from the ROD to the ROB in the end-cap region](image)

**4.3 Event Header generation**

The ROD receives the clock, the L1ID, the BCID and the trigger-type from the TRT-TTC module [7]. All L1ID and BCID are stored in a FIFO. They are then included in the event header. L1ID and BCID are compared with those generated on all ROCs in order to check event synchronisation and results are appended to the event. At the end of the header there are bits indicating status of the ROC chips and of the data transmission (See table 1).

**4.4 VME interface and buffers**

All configuration, set-up and control of the ROD is done through the VME bus using A32/D32 cycles. There are two kind of buffers accessible from VME for monitoring purposes. One before zero suppression and one after zero suppression with a programmable write rate to avoid overflow during data taking. These buffers will also be used during test beam runs when the ROD
will work without S-LINK interface and data will be read out through the VME. The chosen write rate depends on the speed with which it will be possible to extract data through the VME bus and on the processing power of the monitoring workstation.

5. TESTING TOOLS AND ERROR DETECTION

Testing tools have been designed in order to be able to test the ROD main dataflow stream. Inputs can be switched from receivers to an internal static memory output which can be filled up with data corresponding to up to 8 full events and flushed, thus simulating real system operation. Each line can have individual data, thus all possible situations can be simulated. All data buffers are accessible for separate read and write operations from the VME bus.

6. MINIROD

In order to verify the functionality and the feasibility of the most important parts of the ROD and to provide a simple tool for system tests, a simplified version of the ROD has been produced and tested. Only one data block from Figure 3 has been included and the S-LINK interface was not implemented. Three miniROD have been produced. They are now used for system tests with the front-end electronics and the detector prototype.

7. CONCLUSION

A full version of ROD has been designed and fully simulated. Different parts of the ROD have been discussed including a contents based data compression scheme. A prototype of a scaled down ROD (miniROD) has been produced, tested and is now used in the ATLAS/TRT system tests.

8. REFERENCES

PROTOTYPING HARDWARE FOR THE ATLAS READOUT BUFFERS

R. Cranfield (rc@hep.ucl.ac.uk), G. Crone, University College London
G. Boorman, B. Green (B.Green@rhbnc.ac.uk), Royal Holloway University of London
O. Gachelin, M. Huet (huet@hep-saclay.cea.fr), P. LeDu, M. Mur, Saclay
H. Boterenbrood, P. Jansweijer, G. Kieft, J. Vermeulen (i73@nikhef.nl), NIKHEF
A. Kugel (Andreas Kugel@ti.uni-mannheim.de), R. Rissmann, University of Mannheim

Abstract

Current design studies for the ATLAS readout assume that detector data is held in standard buffers until needed for full event building. These buffers are fed with data in parallel via a large number of high bandwidth links from the sub-detector readout electronics for events accepted at the first level, but only a subset of this data is required for level 2 trigger processing, selected from "regions of interest" identified at level 1. It is assumed that such buffers will not be available "off-the-shelf", so ATLAS is pursuing a programme of buffer design building prototypes and exploring architectural options. This paper describes both the current mainline prototypes, which use Intel i960 processors and interface to PCI, as well as an entirely FPGA-based solution, and a SHARC DSP-based board which is being designed to explore an alternative buffering strategy.

1. ASSUMPTIONS

The basic strategy[1] adopted by ATLAS for taming the enormous data rate expected after Level-1 (hardware) triggering is to concentrate Level-2 processing on only that subset of the data issuing from "regions of interest" identified by Level-1. In this way only a fraction of the data needs to be merged from the readout lines into the Level-2 processors, and subsequently only the fraction of events selected at Level-2 needs to be sent on to the Event Filter.

This strategy implies the incorporation of special buffering into the readout lines where data can sit until either rejected by Level-2 or required by the Event Filter. The system components responsible for the whole buffering process are referred to as ROBs (Read Out Buffers) and are assumed to form the first common stage in the readout chain. A ROB has several interfaces: it must be able to accept detector data at a high rate from one or more Read Out Lines; it must communicate with the Level-2 system, servicing requests for data "fragments" from regions of interest; it must communicate with the Event Filter, servicing requests for whole event data for accepted events; and it must communicate with the readout software infrastructure, providing downloading, initialisation, monitoring and debugging facilities as required.

The ultimate structure of a ROB is not yet decided, but for hardware prototyping purposes its functionality has been split into an input component (ROB-in) which includes the data buffer, a supervisory component (ROB-controller), and a network interface component (ROB-out). This enables different groups to concentrate on the development of the different parts, as well as allowing for experimentation with different degrees of input and output multiplexing. This paper describes recent work on the development of the ROB-in component.

The basic references for this work are the ESA-style User Requirements Documents (URDs) which have been drawn up for both the ROB[2] and the ROB-in[3] on the basis of current knowledge. Final versions of these documents are planned for the end of the prototyping phase.

2. PROTOTYPES

The rationale for designing and building ROB-in prototypes is two-fold. Real modules are needed for the construction of "vertical slices" of both the Level-2 trigger and the DAQ front-end, required for proving designs for these sub-systems. At the same time the design process gives us hands-on experience of the problems intrinsic to building an appropriate hardware buffer. This is particularly important since it is by no means clear that such buffers will be available as "Commodity Off-The-Shelf" items and they may well need to be custom-made. This is notwithstanding the fact that there are now commercially-produced boards[4][5] suitable for the implementation of a ROB-in. The scale of the eventual ATLAS buffering (~2,000 Read Out Links) justifies further exploration of the cost, density and modularity of the final buffer system through development of the present prototypes and their use in multi-channel configurations.

One of the commercial boards, the microEnable, is described here. It is a multi-purpose design with SRAM memory, FPGA and S-Link interfacing, that evolved from development work at Mannheim University[6]. The ROB-in "design" consists of programming the FPGA such that the ROB-in requirements are satisfied. The current ROB-in implementation on this board includes a Level-2 pre-processing task, which is potentially useful for sub-detectors such as the TRT, where only a
compacted form of the data is needed for making the Level-2 decision.

Two of the custom prototypes have evolved from earlier designs that used Texas Instruments' DSPs. The UCL/RHUL ROB-in RD board[7] followed on from the C40-based T2B buffer successfully used in early small-scale trigger demonstrators, whilst the Saclay ROBIN[8] was developed from on an earlier C80-based design. Both these boards are intended for use in demonstrators associated with the Level-2 Pilot Project[9], as well as in prototype multi-ROB-in ROB Complex[10] configurations. The RD board is also being used in the DAQ Prototype-I[11] front-end demonstration.

The CRUSH board[12] is a recent design from NIKHEF using the SHARC DSP and a different buffer management technique and is aimed at local tests of ROB Complex configurations.

3. APPROACH

The two current mainline ROB-in prototype variants, the UK ROB-in RD and Saclay ROBIN, follow similar design approaches. Detector data enters (from one of many Read Out Drivers associated with a sub-detector) on a Read Out Line and is written into fast dual-port memory by programmable logic, under the direction of buffer manager software running on a microprocessor.

The microEnable-based design is completely realised in programmable logic (Xilinx FPGAs). It uses a circular buffer like the NIKHEF board, but there is no microprocessor and the buffer management is built directly into the firmware.

4. COMPONENTS

4.1. Data Input

Data is assumed to enter the buffers via a dedicated link from the detector readout components. The

The buffer manager software receives data request messages across a PCI interface and initiates DMAs of

...
canonical speed for this link is 100 MB/s or 100 kHz of 1KB event fragments. The implementation of this link is still under discussion, but most of the prototyping work assumes that it will be interfaced according to the S-Link specification[13], which provides a 32-bit-wide data connection together with control and status lines.

The S-Link interface provides an error bit that can be read by the ROB-in and reported to the controlling infrastructure. It also carries an XON/XOFF protocol, which is used both for holding off data prior to initialisation and signalling when the buffer memory is nearly full. It is assumed that this handshake will be propagated back along the readout chain in some way ultimately blocking the data flow out from the sub-detector.

The detector data is fed into an input fifo which accommodates the lack of synchronisation between the clock controlling the Read Out Link and the clock controlling the buffer memory. In general it can therefore be quite short, though in the Saclay design it is also necessary to buffer data in this fifo before it can be burst into the buffer memory.

It is assumed that the beginning and end of each event fragment is marked in the data. The S-Link specification defines a special bit marking a word as a control word, and the proposed Read Out Link format[14] defines a pair of control word patterns (BOB and EOB) indicating the beginning and end of a data block respectively. Actually only the end marker is strictly necessary, enabling the ROB-in hardware to know when to record the event details and to ready itself for the next fragment.

4.2. Buffer Memory

The buffer memory must take in data at an average rate of 100 MB/s i.e. one 32-bit word every 40 ns. However the memory must be a lot faster than that since it must also be read both by the buffer manager software (to pick up the event ids) and by the DMA engine responsible for outputting event fragments to Level-2 and the Event Filter. The rates for these tasks are about 400 KB/s and 10 MB/s respectively.

In the ROB-in RD normal fast (10ns) asynchronous SRAM is used and advantage is taken of the difference in access rates required on the two ports with the output side being allowed up to one access in every four. Memory size is limited by the size of available SRAM chips with the current prototypes providing 1 MB total buffering.

The Saclay ROBIN meanwhile uses SDRAM. This permits a larger memory (8 MB) to be accommodated in the available board space though at the expense of increased logic complexity and with the constraint that the fastest access requires the use of burst mode. This in turn has resulted in the selection of a longer input fifo, as noted above, and the restriction of fast access from the microprocessor side to read-only. Slow read and write word access is possible, however, from either local or host CPU.

The microEnable uses standard asynchronous SRAM (0.5 - 2 MB), with dual-port capability being emulated in the FPGA by running the RAM-control task at twice the speed (40 MHz) of the I/O task.

The CRUSH design makes use of ZBT (Zero Bus Turnaround) memory, which avoids the wait states necessary with fast synchronous SRAM when alternating between reading and writing. The buffer memory runs on an 80MHz clock, allowing one write from the S-Link interface every 25 ns (resulting in a maximum input bandwidth of 160 MB/s) plus one access from the SHARC. Due to pipeline delays in the FPGA and the properties of the bus protocol of the SHARC the bandwidth to/from the SHARC is limited to 40 MB/s.

4.3. Microprocessor

Both the ROB-in RD and Saclay ROBIN make use of the Intel 1960 family of I/O microprocessors. The Saclay ROBIN uses the more established JX variant, whilst the London-designed board incorporates the newer RD chips. These latter chips have the convenience of built-in PCI bridging, but introduce the complications of increased power dissipation and BGA mounting technology. The i960 family provides an appropriate balance between speed, power dissipation, size and complexity.

As already noted, the NIKHEF design uses instead a SHARC DSP as its microprocessor. This also provides an appropriate balance of operating parameters, as well as the possibility of interconnection of ROB-ins via its proprietary communication links.

The fourth prototype does away with a microprocessor altogether. This potentially increases the speed of buffer manager processing, though making the coding less transparent and hence arguably less versatile. The trade-off between hardware and software implementations of buffer management in the ROB-in is an important open question.

4.4. Buffer Management

The heart of the ROB-in design is the buffer manager. It is this that allows the input data to be written at a continuously high rate whilst also allowing for the variable amount of time that an event fragment might need to remain in the buffer during Level-2 processing or whilst waiting to be requested by the Event Filter.

In the page-managed schemes (ROB-in RD and Saclay ROBIN) all the pages can be used since the buffer manager notifies the hardware of all the free pages, and keeps track of their usage. The only inefficiency arises from the use of a fixed page size. This is no problem for those sub-detectors with fixed event fragment sizes (no zero-suppression), but in the case of
variable fragment sizes a compromise has to be established between minimising the number of pages used per event fragment and minimising the amount of wasted space within pages.

An alternative buffer management scheme has been tested in the ROB-in RD in which the overhead associated with tracking several pages per event has been minimised by linking the pages of an event directly in the buffer memory. This means that small pages can be used without penalty and enables particularly efficient memory utilisation.

Both the CRUSH and the microEnable designs incorporate a circular buffer, which simplifies the input task, since it needs only a cyclically repeating address counter. However it means that an event fragment can block the buffer if it needs to be retained for longer than the buffer cycle time. In the CRUSH design it is assumed that the SHARC microprocessor will transfer such an event fragment into the microprocessor's own heap memory. This then requires a management scheme for the fragments on the heap, but should be feasible if it is a relatively rare occurrence. In the microEnable prototype it is also planned to try a fifo-style buffer as an alternative to the circular buffer.

All the buffer management schemes need to maintain some sort of index table to associate an event ID with the address of its data fragment in buffer memory. In the i960-based designs the microprocessor reads which pages have been used by the hardware via a "used page fifo" and is then able to read the event IDs directly from the buffer. In the SHARC-based design the hardware itself notes the IDs (along with a few other key data words) and passes these to the microprocessor together with the address window of the event fragment in the circular buffer. In the FPGA-based design the Fpga generates a simple lookup table as it reads event fragments into the circular buffer.

4.5. PCI & Format

All four prototypes use PCI for communications other than the front-end data input. The PCI bus provides a convenient common connection standard for prototyping work, as well as constituting a real technology option for the final system, since the total bandwidth required for a operation of a single channel ROB-in is about 15 MB/s, which is well within the PCI spec.

Both the i960 modules come in PMC format, enabling them to be plugged directly onto a motherboard via the PCI bus. The possibility then exists of constructing a complete ROB from e.g. a VME single board processor as a ROB-controller, with a pair of PMC daughter boards, acting as ROB-in and ROB-out respectively.

The microEnable module and an alternative version of the ROB-in RD come in a standard PCI format suitable for plugging directly into a PCI slot in a standard PC, whilst the CRUSH module communicates via its SHARC links with a second PCI module containing a SHARC and a PCI interface.

4.6. Error-Handling

The ROB-ins must be sensitive to several kinds of errors in the data-stream, as well as being able to recognise errors reported by the link system itself. Event fragments might arrive without BOB or EOB markers and/or they may contain too much data. Level-2 or Event Filter requests may be received for data that has not yet arrived at the buffer and/or the data may never arrive. Data may also be corrupted in various ways. Whilst data corruption in general has to be left for further processing downstream, corruption of identifying information must be handled non-fatally at the ROB-in.

In general situations in which data is not released quickly enough from the buffers are handled by the S-Link handshake mechanism. The ROB-in RD, for example, asserts XOFF whenever the number of free buffer pages drops below a certain level, or if the input fifo fills too much. This means that extra-long event fragments, possibly caused by the absence of EOB markers, will not disrupt operation; they can be recognised by the buffer manager and immediately released.

Requests for events not yet received can be handled by flagging the corresponding entry in the index table, so that the request can be satisfied once the data arrives.

It is not yet clear whether fragments can be guaranteed to arrive in strict order of ID, but the buffer manager can easily check that they are not grossly out of sequence, or for duplicates, as part of the indexing process.

The thorniest problems concern event data and requests that never match up. This begins to be a concern once the buffer manager needs to re-use an already occupied slot in its index table. It is easy to avoid the immediate problem by linked-list extensions to the simple lookup table, but it is not yet clear what should be provided in the way of timeouts from the point of view of overall system efficiency.

4.7. Monitoring

It is assumed that event fragments will be requested for monitoring purposes as well as for the mainstream DAQ dataflow. Such requests can simply be handled by the standard fragment-request mechanisms. What is not yet decided is the extent to which individual ROB-ins will need to select and/or store events of different types; this could have a major impact on future ROB-in design.

5. OPERATION

The i960-based prototypes boot from ROM, but there is enough on-chip memory for the main buffer manager code to run from cache, with consequent speed improvements. Code has also been downloaded across PCI, which is useful for testing and might be convenient.
for online program changes. JTAG is used extensively for downloading both programmable logic and microprocessors and also as a route for emulator-based debugging of the microprocessors.

The SHARC prototype is booted across a SHARC link by the SHARC on its associated PCI interface board, itself booted via PCI. The SHARC on-chip memory has room for the buffer manager code, index table and overflow buffer, as well as a library supporting terminal and disk I/O via the host PC.

Testing is carried out both by running special programs in place of the regular buffer manager and by connecting to auxiliary test facilities, such as the SLIDAS S-Link data source. The designs also incorporate mechanisms for injecting data directly into the front-end of the ROB-in under host control.

SOFTWARE

The buffer manager software on the microprocessors is written in C for transparency and possible portability. Earlier experience with the "T2B" buffer shows that C code can achieve about half the speed of assembler in this kind of application.

Since the buffer manager's role is essentially to service its input sources, with no significant background tasks, it has generally been implemented as a large polling loop, rather than employing interrupts. Comparative timing measurements justify this design choice. Efficiency has been gained, however, by servicing a group of inputs from each source at a time.

The Xilinx chip on the microEnable board is coded using CHDL, a C-like high-level language developed for easy programming of FPGAs.

At the moment each prototype uses its own proprietary programs, but the aim is to define a set of common APIs for future prototyping work which could eventually evolve into the production software. Work has begun on this with the first iteration of an API for the operation of a ROB within the Level-2 Reference Software[15] framework.

As well as the buffer manager code itself attention must also be paid to the interaction between the ROB-in and the rest of the world. Currently APIs have been defined[16] in the context of the DAQ Prototype-1 covering communication between a ROB-in and the rest of the DAQ front-end and these have now been implemented for the ROB-in RD.

6. PERFORMANCE & STATUS

The designs described here are intended primarily for prototyping experiments to be conducted over the next eighteen months, essentially the Level-2 Pilot Project and the DAQ Prototype-1. Versions now exist of all four boards, though some hardware debugging and refinement remains to be completed.

Early results from simulation environments and measurements of loop times suggest that all the prototypes are fundamentally capable of coping with the specified 100 kHz event rate, and can comfortably provide the required output bandwidth.

7. FUTURE DEVELOPMENT

The main focus of ROB-related work in the Level-2 Pilot Project will be to analyse the options for a ROB Complex, defined to be a generalised buffering system incorporating one or more front-end links and network connections. This will involve exploration of hardware possibilities and constraints as well as extrapolation of technology and performance relevant to the Level-2 trigger, preparatory to a final design programme starting in 2000. At the same time the DAQ Prototype-1 programme will explore the integration of ROB components into the full DAQ system.

As well as using the current ROB-ins in Level-2 vertical slice demonstrators it is planned to configure several test setups, each containing a number of the current prototype ROB-ins, to measure the performance of different architectural organisations for a ROB Complex. It is also planned to pursue paper designs for possible multi-ROB Complexes, which will explore possibilities for tighter coupling and closer packing of ROB components.

8. REFERENCES

5. http://www.ces.ch/Products/Products
6. http://www-mp.informatik.uni-mannheim.de/groups/mass-par-1/parallelproc
http://attdoc.cern.ch/Atlas/Notes/065/Note065-1
http://attdoc.cern.ch/Atlas/Notes/071/Note071-1
MICROENABLE
A RECONFIGURABLE FPGA COPROCESSOR

O.Brosch, P.Dillinger, K.Kornmesser, A.Kugel, R.Männer, M.Sessler, H.Simmler, H.Singpiel, S.Rühl
University of Mannheim, Mannheim, Germany (email:kugel@ti.uni-mannheim.de)
R.Lay, K.-H.Noffz
Silicon Software Co., Mannheim, Germany (email:noffz@silicon-software.com)
L. Levinson
Weizmann Institute of Science, Rehovot, Israel (email: fhlevins@wicc.weizmann.ac.il)

Abstract

Where commodity hardware has too low performance, inadequate real-time behavior or incompatible interfaces, reconfigurable FPGA' processors can make custom hardware unnecessary. microEnable is a PCI board with a single FPGA, 2 MBytes SRAM, and CMC and S-Link mezzanine connectors. PCI performance reaches 125 MBytes/s which is close to the specified limit. Supported OS are Linux and WindowsNT.

Recent applications in ATLAS and image processing show very good results: 1) TRT preprocessing: speedup of 5 compared to a 300 MHz RISC CPU. 2) S-LINK source and destination: 90% bandwidth, message rates well above 100 kHz. 3) JPEG compression at 20 MBytes/s.

1. RECONFIGURABLE COMPUTING

For high energy physics data processing, custom hardware is often needed because commodity hardware is not appropriate. The ATLAS level 2 trigger, e.g., comprises a number of tasks – e.g. preprocessing and online track recognition – either exceeding the processing power of a computing node or its input bandwidth. Reconfigurable hardware is an interesting solution which provides the required performance without the development of custom hardware. In addition reconfigurable systems can provide an extremely flexible and cost-effective testbed for rapid prototyping or testing of custom modules like high-speed interfaces, protocol engines etc.

1.1. FPGAs – the basis of reconfigurability

The family of FPGA-devices was introduced in 1984 by Xilinx. FPGAs feature a comparably large number of relatively simple elements with configurable interconnects and an indefinite number of reconfiguration cycles with short configuration times. All configuration information is stored in SRAM cells.

The basic processing element (PE) of all current mainstream FPGAs is a 4-input/1-output look-up-table (LUT) with an optional output register. The functionality of the FPGA is thus determined by the contents of the look-up-tables within the PE's and the “wiring” between these elements.

Over the last few years FPGA performance has increased tremendously as it profits from both:
- Increased density by a factor of 24 from 1993 thru 1998 (Xilinx XC4000: 400 to 18400 elements)
- Increased speed by a factor of 3 from 1994 thru 1998 (Xilinx XC4000: 133 to 400MHz internal toggle rate).

This numbers correspond to an annual increase in performance by a factor of 2 roughly which by far beats the annual increase of 1.25 seen with microprocessors[1].

1.2. The FPGA-processor paradigm

The conventional use of FPGAs is to implement some hardwired functions e.g. “glue-logic”, protocol-engines (e.g. ATM cell assembly/disassembly) or the like for special purpose applications.

With the term FPGA-processor we now refer to a system comprising a number of FPGA chips plus memory system and I/O interfaces. In the special context of co-processing the interface between the two processors has a special importance.

In conventional computers an algorithm is executed by a CPU that processes a sequence of standard instructions. Contrary to this an FPGA processor allows the implementation of an algorithm directly in hardware. In one case the processor may look like a SIMD-machine. If done appropriately input data can be shifted through the processor and are processed on the fly. In another case it

\[ \text{Field Programmable Gate Array} \]
\[ \text{CMC: Common Mezzanine Cards (CMC) following the IEEE P1396 specification} \]
\[ \text{S-Link is the unofficial ATLAS standard for high-speed point-to-point links, especially for the ROD to ROB interconnect} \]

\[ \text{The currently largest devices offer approx. 10.000 of these PE's in the internal FPGA array and more than 400 useable external I/O pins} \]
\[ \text{Applications are be classified into a “logic-type” (the one just referring to) and a “processing-type”, described later.} \]
may look like a large pipeline of integer units executing the inner loop of a number crunching algorithm. Thus the hardware of the FPGA processor – the chips on the board – is the same for all applications. However the degree of flexibility is similar to that of a standard CPU, as the configuration data-set is also compiled from a program description.

Since parallel and pipelined processing is implemented easily, even a single FPGA can provide a speedup factor in the range 5 to 100 depending on the algorithm.

Relatively large FPGA-processor systems have been used prior to and during the ATLAS level-2 trigger demonstrator program to implement high-speed pattern recognition and other time-critical tasks[2],[3].

The clock and support circuitry of microEnable implements tasks like configuration and readback of the FPGA, a JTAG port, and provides user-programmable clocks.

1.3. Software

microEnable provides device drivers for the operating systems LINUX and Windows NT 4.0 with the latter one being more advanced.

The device drivers support master as well as slave accesses, two independent gather/scatter DMA channels, and interrupt capability. In order to provide users a simple but fast programming interface, accesses to microEnable are memory mapped into user space.

Maximum throughput however can only be achieved if DMA transfers are used. Using DMA microEnable provides a performance of up to 125 MBytes/s (measured to/from a user application running in user space under WinNT 4.0 on a Pentium II/233). This is about 95% of the theoretical PCI performance! Besides the standard scatter/gather DMA mode where the PCI bridge controls the transfers microEnable also provides a DMA-on-demand mode where transfers are controlled via a simple handshake between PCI bridge and FPGA. Using this mechanism transfer rates comparable to normal DMA rates are possible while protecting the co-processor against data over-/under-run.

2. APPLICATIONS

During the ATLAS level 2 trigger demonstrator program both an I/O oriented and a computing oriented application – S-Link source/destination and preprocessing – have been implemented on microEnable. One of the ongoing projects at Mannheim develops a special version of a Robln prototype which integrates S-Link input, high-speed buffer management and preprocessing, all together implemented into a single microEnable processor.

2.1. TRT-Preprocessing

The preprocessing of the TRT data is an extremely computing intensive task. Preprocessing changes the TRT data format from pixel images with variable pixel length to coordinate lists of constant size. Two steps are necessary to perform the conversion:

1. As input data are not aligned to any fixed boundary a first reformatting step is needed to identify pixels and to compress bunch-crossing information.
2. In a second step zero-supression and indexing is performed.

The preprocessing of the TRT data is an extremely computing intensive task. Preprocessing changes the TRT data format from pixel images with variable pixel length to coordinate lists of constant size. Two steps are necessary to perform the conversion:

1. As input data are not aligned to any fixed boundary a first reformatting step is needed to identify pixels and to compress bunch-crossing information.
2. In a second step zero-supression and indexing is performed.

The Robln work as part of the ATLAS level-2 pilot project is described in a separate paper for LEB98.
The data volume is significantly reduced up to an occupancy of 30%. The execution time of the implemented algorithm is proportional to the number of set pixels. Implementations[5] were done on a 300 MHz DEC Alpha station and a 40 MHz microEnable FPGA processor. Preprocessing times for a single read out buffer (ROB) in the barrel region are 60 to 165 μs with the DEC Alpha compared to 12 to 27 μs with microEnable corresponding to a speedup-factor of 5. Preprocessing takes approx. 15% of the FPGA resources of a microEnable equipped with an XC4028 FPGA.

### 2.2. S-Link

An S-LINK implementation was used during the level-2 demonstrator-A program to supply data to the FPGA-based feature extraction and Region-of-Interest collection systems and to receive the FEX results. microEnable carries either an S-LINK source or destination module and buffers data packets in its on-board memory. Transmission is done autonomously using the control information stored with the user data. Only full buffers are transferred to S-Link (source mode) or to the host (destination mode). This way an S-LINK data-rate of 92MB/s was reached at 25MHz design frequency[6].

From this basic S-Link application a set of higher level hardware applets and software modules have been developed allowing an application to use S-Link as it's I/O interface. microEnable is currently used or intended to be used with these applets:

- at CERN as microSlate [7],
- at CERN in the level-1 data emulator project[8],
- at Nikhef in the Window NT S-Link Software project[9].

With the latest microEnable version both source and destination can – in autonomous mode – transfer 132MB/s at 33MHz which is the current limit of the S-Link specification.

However if an application uses S-Link as a block I/O device the achievable transfer-rates are much lower, limited by the I/O-overhead of the operating system.

### 2.3. RobIn prototype

The RobIn prototype built upon microEnable integrates the S-Link applet, a buffer-management applet and a preprocessing applet. Currently Slink-input and buffer-management are integrated and first results are available. To build the complete system it is necessary to port the TRT-preprocessing algorithm developed in 1996/97 to CHDL. This work will be finished in October/November 1998. With the RobIn data transfers are requested block by block from the controlling host software. With presently available device drivers this limits the bandwidth between microEnable and host to approx. 13MB/s @ 1kB blocks or 33MB/s @ 4kB blocks due to software overheads. On the S-Link input 80MB/s can be transferred.

### 2.4. Industrial image processing

On microEnable a complex image processing application was developed for an industrial customer requiring preprocessing, rotation, JPEG compression, binarisation and fax-G4 compression of 2-dimensional images with a size of up to 3000*2000 pixel and 24 bit color.

The whole task was divided into two different hardware applets running alternately on microEnable.

One applet covered mainly the JPEG compression, the other one a set of further data reduction, monitoring, and preprocessing steps. In the applet described here a couple of different tasks beside the actual JPEG compression had to be realized: rotation of the images in multiples of 90 degrees, cut out of partial images, and reformatting and direct interfacing to commercial frame grabbers. Required was a data throughput above 10 MBytes/s for color images of sizes between 5 and 10 MBytes. JPEG is the most popular lossy compression standard for still images[10]. The algorithm is based on a discrete cosine transform (DCT) of the image (to reduce the computing requirements the image is divided into blocks of size 8*8 pixels). The second processing step is called quantization. The quantized values are compressed by a Huffman coding. The complexity of the algorithm is dominated by the DCT requiring 16 concurrent MACs (multiply and accumulate) per pixel.

The JPEG implementation on microEnable reaches an overall data throughput of 18.3 MBytes/s running at 30 MHz on an XC4036EX. This covers preprocessing time, data transfer to and from memory, and includes additional tasks like rotation and partial image handling.

### 2.4. Prototyping and test-gear

In addition to the above processing-type applications microEnable can also be used as an excellent basis for prototyping and testing. One just has to put the interesting hardware – maybe a new readout chip or link driver – onto a prototype expansion board for microEnable. Now the FPGA can be used to

- emulate the target environment,
- implement a pattern generator or logic-analyzer,
- convert interfaces or protocols,
- etc.

A hardware applet is that part of an application to be executed on microEnable.

The RobIn prototype work as part of the ATLAS level-2 pilot-project is described in another paper submitted to LEB98.

---

*The memory system can operate at up to 40MHz. As a dual-port-emulation is used here the applets can only run at half of this frequency thus limiting the input bandwidth to be 20MHz * 4 bytes.*
Testing can take even further advantage from the close interaction between host-cpu and test equipment.

3. IMPLEMENTING ALGORITHMS

To describe logic-type FPGA designs VHDL is commonly used. However it provides poor support when one tries to program an application distributed between FPGA subsystem and host-cpu. There is no way to compile VHDL into microprocessor code and testing of the VHDL code cannot be done by the host-application itself. To efficiently realize the FPGA processor paradigm a set of tools is need which support all aspects of hardware-software co-design. This is exactly the purpose why CHDL was developed at the University of Mannheim.

3.1. Programming microEnable

microEnable can be programmed with VHDL and this can be reasonable for applications where the on-board FPGA is mainly used for interfacing, prototyping or as a test-tool. In order to support this approach a VHDL library is available together with a set of API functions for communication and data-transfers. The VHDL library can be used with arbitrary VHDL synthesis and simulation tools. In this case the standard VHDL tools – timing simulators, testbenches, waveform displays etc. – must be used for design verification.

However all benefits from microEnable as a co-processor can only be taken when using CHDL. CHDL seen only as a hardware description language certainly doesn’t have all of the features available with a complete VHDL system, in particular behavioral design description and exact timing simulation. CHDL builds upon a C++ class library which implements all basic building blocks (primitives) present in a specific FPGA family, plus a library of macro functions – counters, adders, multiplexers, memories etc. – which are built from the primitives, plus a simple state-machine description method.

As CHDL is not a description language but a class-library a given application can describe both host program and FPGA design in a single C++ project or even in a single C++ source file. Each FPGA class comes with an implementation method and a simulation method. The structural description of the FPGA design is done by instantiation of class members of the FPGA class-library and operations like “-”, “+”, “XOR” etc. In addition to the FPGA classes all important parts of the microEnable co-processor are available as library classes or elements:
- PCI-bridge chip, including master/slave interfaces, various DMA streams, interrupts etc.,
- microEnable RAM-system, including dual-port-, fifo- and ROM (LUT) - emulations,
- external I/O connector pinout,
- Clock control,
- FPGA configuration, including run-time-reconfiguration,
- Additional classes can of course be added by the user.

To anyone familiar with a lower level hardware description language the use of CHDL will be straightforward.

In order to build an entire application in principle three different building blocks must be present:
- ordinary C/C++ code describing the host-cpu functionality,
- instances of the PCI library providing the communication mechanism between host-cpu and co-processor for data transfer and configuration
- CHDL code, describing the co-processor design using instances of the FPGA-, memory- and support libraries.

This C++ code can be compiled by any standard C++ compiler. During execution basically one of three options can be selected:

1. Simulation. All CHDL elements use their simulation methods, the application runs entirely on the host-cpu. This mode will be used until the code has proved a certain stability. The FPGA co-processor doesn’t even have to be present in the system.

2. Implementation. The netlist to be fed into the FPGA vendor Place&Route tool is generated from the CHDL description. The P&R tool outputs the configuration data-set of the hardware-applet.

3. Execution. In this mode the hardware-applet is loaded to the FPGA co-processor and both parts do their work. A number of debugging facilities are available while still in execution mode.

It is worth noting that for the host-part of the application simulation and execution mode are fully transparent. This is achieved by an exception based implementation of the PCI library which can – even dynamically – switch between real mode and emulation mode.

As a special feature currently not supported by any commercial tool CHDL supports dynamic (or run-time) reconfiguration. If the co-processors task is too large to fit onto the available FPGA-resources it might be cut into pieces which can be loaded and executed one after

11 CHDL uses device independent higher-level macros built upon device specific primitive libraries which are currently available for the FPGA families Xilinx XC4000, Atmel AT40k and Lucent Orca 3T.

12 For example the driving and receiving functions for S-Link are user defined classes.

13 Like ABEL, Altera HDL or PALASM.

14 CHDL has been tested with the operating systems: Windows NT 4.0, Linux, Solaris 2.4
3.2. Testing and debugging

CHDL provides a debugging tool well known to hardware designers: the waveform display. Instances from the CHDL code can be added to the display thus showing the sequences of signals during the simulation phase. In a traditional setup the input for this simulation would be controlled by a VHDL testbench or the like. However when debugging an application one is less interested in seeing bits being set or reset but in the overall results, which might immediately be drawn as an image on screen, be dumped to a file or be online compared to predefined values in a reactive way. All this can easily be done because simulation is controlled by the application itself and the full set of C++ debugging tools – break/watch-points, exceptions, variable modification, etc. – is available, at least in simulation mode. But even in execution mode an application may query the internal resources of the FPGA using the readback facility. There is no need to write a separate testbench to examine the FPGA design.

Bypassing the guidelines of object-oriented programming CHDL takes advantage from the fact that host-application and CHDL simulation library are executed as a single process in host memory. This allows fast access to the internal members of the CHDL classes which significantly reduces simulation times. Another speed-up factor is the use of a unity delay simulation model, which will only be replaced by exact timing model if necessary. A representative example design with 1000 PEs executed 260,000 simulation steps within 20 seconds on a Pentium-II/266. During this time 14,400 clock cycles elapsed and 29 kByte were transferred via the emulated PCI interface.

In case run-time reconfiguration is used the download of a new configuration data-set by the application is reflected by the loading of the netlist of the new design into the simulation database. By this means simulation and real execution are consistent even if multiple applets are needed for an application.

4. CONCLUSIONS

A large number of applications has been presented where a single hardware object – the commercial microEnable FPGA co-processor – is successfully used to improve system performance. This strongly supports the guidelines of ATLAS to reduce the number of different components used and to favor commercial solutions.

The concept of reconfigurable computing was introduced and CHDL proposed as the adequate development tool. Even though CHDL doesn’t make a thorough understanding of hardware unnecessary overall design cycles can significantly be reduced even for less experienced persons. For example the S-Link hardware applets were implemented in CHDL within two weeks. Support for co-design and co-simulation of both host and co-processor make it by far superior to any other kind of pure hardware description.

FPGA technology has reached a state of complexity and performance which allows to map significant portions of an algorithm onto FPGA processors. For example all Robln applets including preprocessing and DMA engine fit into a single FPGA of type XC4036 which has less than 30% capacity of the largest device available. The fact that the yearly rated increase in processing power is much higher than for traditional cpu’s (2 to 1.25 per year) make FPGA processors a good choice. As a rule one can consider to use an FPGA co-processor if the algorithm features any of the following:

- High rates of short messages to be assembled.
- Bit and data field manipulations.
- LUTs instead of complex calculations.
- Parallel and/or pipelined dataflow operations.

5. REFERENCES

[8] ATLAS level-1 emulator project: http://www.pa.msdu.edu/people/ermoline/atlas/docs/dg.txt
A REAL-TIME TRACKER FOR HADRONIC COLLIDER EXPERIMENTS

A.Bardi, S.Belforte, W.Errico, G.Galeotti, P.Giannetti, G.Magazzù, F.Morsani, F.Spinella, R.Tripiccione (name.surname@pi.infn.it) INFN, Pisa, Italy
M.Dell’Orso (Mauro.DellORso@pi.infn.it), Dipartimento di Fisica, Pisa, Italy
E.Meschi (Emilio.Meschi@cern.ch), CERN, Geneva, Switzerland
X. Wu, T. Speer, A. Leger (name.surname@cern.ch) Département de Physique Nucléaire et Corpusculaire, Université de Genève, 24 Quai Ernest-Ansermet, CH-1211 Genève, Switzerland

Abstract

In this paper we propose highly parallel dedicated processors, able to provide precise on-line track reconstruction for future hadronic collider experiments. The processors, organized in a 2-level pipelined architecture, execute very fast algorithms based on the use of a large bank of pre-stored patterns of trajectory points.

An associative memory implements the first stage by recognizing track candidates at low resolution to match the demanding task of tracking at the detector readout rate. Alternative technological implementations for the associative memory are compared.

The second stage receives track candidates and high resolution hits to refine pattern recognition at the associative memory output rate. A parallel and pipelined hardware implements a binary search strategy inside a hierarchically structured pattern bank, stored in high density commercial RAMs.

1. INTRODUCTION

Hadronic collider experiments require large online computing power to reach the enormous rejection factor necessary to select events to be written on tape. One of the most demanding tasks is usually the track reconstruction from measured points (detector hits) of particle trajectories. In this paper we propose the use of highly parallel dedicated processors to efficiently execute two fast track finding algorithms [1, 2]. The algorithms are based on the idea of a large bank of pre-calculated hit patterns to be compared to the event [3].

The proposed system is an evolution of the Silicon Vertex Tracker (SVT) [4] currently being built for the CDF experiment at Fermilab. The CDF tracker processes events with a 100 kHz input rate, and an overall allowed processing time (latency) of 10 μsec. Hits from five vertex detector layers can be linked to segments observed in the tracking chamber to reconstruct real time tracks precisely enough to measure b quark decay secondary vertices.

Next generation hadronic collider experiments can exploit technology advancements to realize a more powerful system that can work with the same performances on more complex tracking detectors. The availability of very large, low cost memories allows buffering of many large events. Therefore, new experiments' triggers can have a long latency time and pipelining can be used extensively to subdivide the complex pattern recognition into simpler sequential steps with increasing degrees of approximation.

Figure 1 outlines a computational architecture that takes off from detector hits and goes up to compute track-based physical quantities such as invariant masses and decay vertices. There are significant advantages in splitting the overall computation in two sections (coarse resolution and fine resolution) and applying different mixes of hardware and software technologies for their implementations. High performance commercial CPUs are the best choice for the fine resolution section, where flexibility is a great advantage to handle many variables and specific situations such as local corrections, alignment effects, exceptions etc. Resolutions of few tens of microns are obtained with the use of large data bases updated on a run by run basis. On-line use of standard CPUs can exploit offline software. On the other hand, the coarse resolution section has a lot to gain from the extremely large performance increase obtained from dedicated hardware since a huge combinatorial problem.
must be solved to filter out few relevant track hits from the plethora of detector data. A large fraction of CPU
time is usually wasted in data sorting or similar tasks
consisting of multiple repetitions of simple actions, such
as random accesses to large memories, that could fit well
in dedicated highly parallel architectures.

In the rest of this paper we describe a number of
hardwired blocks that actually implement the coarse
resolution segment of a track finding processor. Part of
these blocks have been designed and developed taking
into account the requirement of present generation
experiments and the constraints of present technology.
The technology improvements in the next 9-10 years is
expected to cover almost automatically a large part of
the future experiment complexity increase.

2. A PARALLEL ARCHITECTURE

The Global Tracker of figure 1 performs the most CPU
consuming part of the pattern recognition. It splits
the problem of finding tracks inside the whole detector into
many simpler problems of finding tracks inside detector
"slices" called fat roads. Depending on applications, the
fat road width spans from 100 µm to 100 mm. The
Global Tracker consists of a Road Finder and a Data
Organizer.

The Road Finder looks for low resolution track
candidates in the whole detector. The resolution must be
low enough to make the problem solvable at high rate,
(for this reason the track candidates are called fat roads).
At this level, multiple hits inside a road are treated as a
single hit, allowing multiple unresolved tracks.

The Data Organizer is a high-speed data traffic node
between the detector, the Road Finder, and the Local
Tracker. At full rate (e.g. 30 MHz in CDF [5]) the Data
Organizer performs the following operations: (a) receives full resolution detector hits in any order, (b)
buffers them in an internal database, (c) sends low-
resolution hits called super bins to the Road Finder (the
super bins are obtained by logically ORing a number of
adjacent detector bins or channels), (d) receives fat
roads from the Road Finder and fetches from the internal
data base all the detector hits contained in the fat roads, (e) sends each fat road with its set of full resolution hits
to the Local Tracker.

Fat roads usually contain several unresolved tracks.
The Local Tracker is powerful enough to deal with large
roads full of tracks at the same rate of the Global
Tracker's output, but with higher resolution. The thin
roads, output by the local tracker, are narrow enough to
hold only few hit ambiguities, if any. These ambiguities
can be solved by sequentially fitting the residual hit
combinations and choosing the best fit. The width of the
fat roads must be optimized for the characteristics of the
specific experiment. Too small or too great widths would
require intolerably high performances respectively to the
Global Tracker or to the Local Tracker.

We propose the use of an Associative Memory (AM)
[1] as Road Finder and of a Tree Search Processor (TSP)
[6] as Local Tracker. A possible implementation of the
Data Organizer can be found in reference [5].

3. THE ASSOCIATIVE MEMORY

3.1 General Description

AM is a dedicated device where parallelism is pushed
to the maximum level since each stored hit pattern is
provided with its private hardware necessary to compare
itself with the event. Matching patterns are identified by
outputting their addresses. The device is so powerful
that tracks can be found during the detector readout. This feature makes the AM a perfect road finder.

The AM pattern bank is limited by the size of the
hardware, mainly consisting of low-density custom
memories. However, the coarse resolution of the Road
Finder prevents divergence of the pattern bank size even
for the complex detectors of the next generation
colliders.

3.2 AM implementations

CDF plans to use a full custom VLSI [7], built with
0.7-µm two-layer metal technology, to house a bank of
4x10^7 patterns in 24 9U-VME boards (AM-boards) for a
detector of 6 layers, with 48000 250µm wide super bins
per layer. An AM-board with 128 custom chips, 128
patterns per chip, was built and tested at 30 MHz [8].

Field Programmable Gate Arrays (FPGA), an easy-to-
upgrade technology, has been recently used to design a
Programmable Associative Memory (PAM) [9]. PAM
offers a high degree of flexibility, a simple architecture,
a prompt exploitation of technology advancement, and
an easy prototype testing and debugging.

Patterns are stored in the FPGA at power on, when the
configuration bit-stream is downloaded in the chip. This
choice allows higher pattern densities since no user-logic
is wasted for download circuitry. This is also a
disadvantage, since patterns must be generated by means
of CAD tools. For convenience, the procedure uses a
placed and routed project, modifying only the pattern
look-up-tables.

A 9U-VME board assembled with PAMs can house the
same number of patterns as the CDF AM-board, although the used FPGA is less dense than the custom
VLSI. This is the result of the following improvements:
(a) the simplification of both the AM readout logic and
the clock distribution that on the AM-board occupy a
large area, (b) the reduction of the pattern size, obtained
by means of data compression. The pattern bank is a
collection of sets of coordinates: several bit fields of
these coordinates are common to many different memory
cells. Decoding and comparing a shared bit field only
once per chip clearly results in data compression. The

compression is paid with complex software for organizing patterns into classes with shared bit fields before chip downloading.

The PAM pattern density depends on the amount of compression and on the choice of the specific FPGA device. The current design places 48 uncompressed patterns into a Xilinx XC5210-STQ144 device (0.6-μm multi layer metal process) [10] for a CDF-like detector. Up to 80 CDF patterns can be placed into a single chip as a mix of uncompressed and compressed patterns.

![Fig. 2: PAM board allocating a PAM unit. White and gray rectangles represent chips respectively on the top and on the bottom side.](image)

To simplify input/output operations, the PAM chips on a PAM board are grouped into PAM units composed of 64 chips. A prototype 9U-VME board has been implemented to test a single PAM unit (see figure 2). The chips of a PAM unit are located on both board sides, 32 chips per side. Matching roads are read out by an output controller called GLUE. The GLUE, an evolution of the corresponding device described in reference [1], is an internally pipelined multiplexer from 8 to 1 controlled by a priority encoder. Up to 8 pattern addresses can be read in parallel from 8 PAM output buses, called Address Buses, and merged inside the GLUE into a single 30 MHz output stream. Each Address Bus is driven by 8 PAMs via three-state output buffers. On the contrary, the input hits are distributed to the PAM array through two internally pipelined fan-out chips called INput Distributors (INDI). The INDI fanout is reduced by a factor four by pipelining groups of four PAM chips. The possibility of moving signals from pin to pin with few constraints is an asset in realizing the layout and routing of the crowded PAM unit, with chips on both board sides and only 4 mm of inter-chip distance. Routing widely profits of regularities introduced with symmetric pin-out of chips on opposite board sides and with daisy chains through short surface connections between facing pins of adjacent chips. The physical size of a PAM unit is only 4.4" × 11" and three of them fit on one board, as shown in figure 2, to reach the same pattern density of the CDF AM-board.

Patterns were downloaded by programming the FPGAs through the VME controlled JTAG port. Chains of eight PAMs each are downloaded in parallel to limit programming time. The VME 32-bit wide data transfer allows to program 32 chains in parallel for a total of four PAM units per board. Downloading time was measured to be few seconds, dominated by the ethernet data transfer from the host computer to the VME controller. The board, provided with a CDF compatible interface, has been successfully tested at 30 MHz in a CDF level 2 trigger test stand [8]. The supply voltage was 5 V. The current was 13 A for a swapping data rate of 30 MHz. Lower power 3.3-V devices [10] may be used on boards with multiple PAM units.

3.3 Evolution of the AM capacity

We can extrapolate the future capacity of an FPGA PAM: the present device, equivalent to ten thousands gates, can be replaced today by a XC530XL (0.35-μm technology) that can allocate 128 CDF patterns in the smaller package TQ100. In a couple of years it will be replaced by new devices based on 0.18–0.25 μm technology, equivalent to several hundred thousands of gates, with an improvement of at least a factor 10 in pattern density.

A high-level language representation of the associative memory allows at any time a fast synthesis of the project in a common gate array or in an ASIC standard cell for further improvements in pattern density. FPGAs feature low development efforts and costs, but their densities are by far lower than those of ASICs. A good strategy is to use FPGAs for the system development, and to switch to a pin compatible ASIC only for system production when the experiment is getting close to data taking.

A Standard Cell Associative Memory (SCAM) has been designed, for a CDF-like system, using the ALCATEL-MIETEC CMOS 0.35-μm technology [11]. An area of 35 mm² contains 1024 uncompressed patterns for an eight layer detector. Since the package TQ144, used for the prototype PAM unit, allows encapsulation of a die larger than 100 mm², we could probably place 4000 patterns in a chip, for a six-layer detector. This corresponds to 32 times the capacity of both the XC530XL chip and the CDF full custom device. Arraying chips with the same density of the PAM unit prototype, today we can have 8×10⁵ patterns on a single board, a factor 50 more than on the CDF AM-board. The forthcoming 0.18-μm technology will provide an additional factor 4 before LHC starts operation.

3.4 Data Flow to the Associative Memory

Figure 3 shows how the Associative Memory could be integrated in modern data acquisition systems. Tracking
data are calibrated and searched for clusters at the Level 1 (LVL1) trigger rate, then they are stored into large memory buffers. These buffers are interfaced by an event builder to a large CPU farm for higher level triggers. The AM, possibly followed by the TSP, spies the cluster centroids on their way to the memory buffers and performs strong data reductions. Interesting candidate tracks are stored into an extra memory buffer and performs strong data reductions. Interesting candidate tracks are stored into an extra memory buffer before the final track fit. Numbers are calculated in a parallel readout of the detector layers. Data could be fed in a new AM chip with a rate of 100 bits every 20 nsec for a total of 5 Gbit/sec, without severe technical problems.

Figs. 3: (a) Hierarchical pattern organization in a tree structure. (b) Parallel architecture of machines distributed in a pipeline corresponding to the tree levels. The machines activated by the matching shower are highlighted.

If the fat roads are too wide to adequately scale down the combinatorial problem, an intermediate step of pattern recognition at higher resolution must be performed by a local tracker before the final track fit. The Tree Search Processor (TSP) is designed to this purpose as it takes fat roads in input and it outputs thin roads.

The TSP algorithm [2] is based on the idea of a pattern bank arranged in a tree structure (figure 4a): increasing depth corresponds to increasing spatial resolution. Each node represents one pattern and is linked to the sub-patterns generated when spatial resolution is improved by a factor two. The set of sub-patterns hanging from one node is called pattern block in figure 4a. We sequentially scan a pattern block (block test) and every pattern matching the event is a track candidate that enables the search at a deeper level, contributing to a matching shower. A refined track candidate, or thin

### Table 1: One fourth of the CMS silicon barrel.

<table>
<thead>
<tr>
<th>Layer R (cm)</th>
<th>Channels per layer</th>
<th>Occupancy (%)</th>
<th>nsec per cluster</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel 7</td>
<td>2.65x10^4</td>
<td>0.034</td>
<td>22</td>
</tr>
<tr>
<td>Pixel 11</td>
<td>4.05x10^4</td>
<td>0.017</td>
<td>29</td>
</tr>
<tr>
<td>Si-strip φ 22</td>
<td>53152</td>
<td>2.67</td>
<td>14</td>
</tr>
<tr>
<td>Si-strip z 22</td>
<td>26624</td>
<td>3.6</td>
<td>21</td>
</tr>
<tr>
<td>Si-strip φ 30</td>
<td>55296</td>
<td>1.6</td>
<td>22</td>
</tr>
<tr>
<td>Si-strip z 30</td>
<td>36864</td>
<td>2.4</td>
<td>22</td>
</tr>
<tr>
<td>Si-strip φ 40</td>
<td>118272</td>
<td>1.2</td>
<td>14</td>
</tr>
<tr>
<td>Si-strip φ 50</td>
<td>96768</td>
<td>0.9</td>
<td>23</td>
</tr>
<tr>
<td>Si-strip φ 58</td>
<td>111104</td>
<td>0.8</td>
<td>22</td>
</tr>
<tr>
<td>Si-strip z 58</td>
<td>55552</td>
<td>1.0</td>
<td>28</td>
</tr>
</tbody>
</table>

As an example of data flow to the AM we report the expected CMS silicon barrel rates [12] on table 1. Numbers are calculated in the hypothesis that 4 AM systems work in parallel, each one receiving data from a quarter of the barrel. Occupancy is defined as the total number of detector channels in reconstructed clusters divided by the total number of channels. The last column is an estimate of the maximum clock period that can be used to transfer cluster centroids to the AM for a 100 kHz event rate. It is assumed that two strips, on average, belong to a cluster and no cluster overlap occurs inside super bins. Even in the very conservative assumption of a 100 kHz level 1 rate, the time for transferring each cluster is reasonable. Should the rate be too high, it is possible to transfer to the AM only a subset of the level 1 triggers. For example, only multi-jet triggers could be analysed to search for b-jets, interesting for low-mass Higgs physics.
recognition is completed, otherwise the possible residual road, is found whenever the tree bottom is reached. If TSP reaches the detector intrinsic resolution, pattern recognition is completed, otherwise the possible residual hit ambiguities must be resolved by fitting all the combinations.

Figure 5 shows the average number of matches found in a road of 8 layers, 32 bins/layer, as a function of the tree level, for events with a variable number of simulated straight tracks. For multiple tracks the number of matching patterns exceeds the number of tracks. Fake matches are due to the combinatorial nature of the problem. The number of fake matches, of course, decreases as the level in the fat road arrives, its full resolution hits are broadcast to the level 1 machines in the intermediate FIFO memory. The level 1 machines, in turn, execute the level 1 tests. Block tests generated by the same fat road at any level in the tree are called road fragments. The process is repeated until exhaustion of all fragments.

Many roads can be handled at the same time. When a road arrives, its full resolution hits are broadcast to all machines in the system. The machines have buffers to store hits from many roads. In this way, they are ready to work on any input road at any time. Different fragments of the same road can pass each other along the tree. On the contrary, events flow in the pipeline maintaining the order they entered TSP. In order to use the computing power efficiently, the number of machines per level and the number of buffers per machine must be optimized. The optimal number of machines in any layer is proportional to the average number of matches at that level. These numbers are reasonably small, even with high occupancy, as shown in figure 5. The machines can be packed efficiently in FPGA devices. The pattern bank is de-localized and distributed into the tree levels; each level stores the structure of the patterns hanging from its nodes. This information is stored in high-density commercial RAMs.

5. CONCLUSIONS

The described processors can find tracks at an event rate of 100 kHz. They are eligible for tracking data reduction in trigger applications. Hits of track candidates, with P_{T} above a threshold of few GeV and with impact parameters compatible with b quark decay, can be filtered among a huge number of other hits. The ambitious goal of trigger selection of b decays at the future hadron colliders can benefit from our architecture.

6. REFERENCES

DETECTOR CONTROL SYSTEMS
Timing set-up strategy for the ATLAS experiment

Ph. Farthouat, CERN, Geneva, Switzerland
(email: philippe.farthouat@cern.ch)

Abstract

In ATLAS, thousands of read-out electronics elements receive timing (LHC clock [BC]) and the Level-1 Accept signal (L1A). The BC and L1A phases must be properly adjusted in order to sample the detector signals at the right time and to read-out the data of the proper bunch crossing. The strategy that ATLAS is defining to set-up these timings in different running configurations (with electronics test pulses and with beam) is presented.

1. INTRODUCTION

Several hundred thousands read-out elements receive timing (LHC clock [BC]), trigger (L1A), synchronisation (bunch counter reset [BCR]) and test (Test-pulse) signals. The phase of all these signals have to be adjusted in order to optimally sample the input signals, read-out the proper event and maintain a coherent BCID and hence synchronisation in the whole experiment. There will be a large number of delay elements to be adjusted and monitored in (most of the time) non-accessible places, and these two tasks may require a lot of time.

Maintaining synchronisation across a big experiment has always been an issue even when the time between crossings is large (for instance in LEP experiments). In the case of LHC where the bunch crossing period is very short and the detector occupancy is high, making sure that all the sub-detector systems are reading out the same bunch crossing when a trigger occurs is a major issue.

The timing set-up is hence seen as critical and some automatic procedures must be defined for various modes of operation:

- Beam-beam collision;
- Beam halo;
- Cosmic-ray trigger;
- Test pulses for test or calibration purposes.

Using the Timing, Trigger and Control (TTC) system, the following timings have to be adjusted (figure 1):

- BC phase at the front-end level (optimal sample of the input signal);
- L1A arrival time at the front-end level (read-out the proper event);
- Bunch Counter Reset (BCR) arrival time (coherent bunch crossing identifier [BCID]);
- Test pulse phase (test or calibration).

Each sub-system must define a procedure to make these adjustments and this work is in progress in ATLAS.

In this article, possible strategy is being presented and discussed in general terms. Later on, each ATLAS sub-detector will produce their own procedure which will be documented and formally reviewed.

![Figure 1. Timings to be adjusted.](image)

This article presents the following:

- The TTC distribution system;
- Timing set-up with beam;
- Timing set-up for beam using test-pulses.

2. THE TTC DISTRIBUTION SYSTEM

The Timing, Trigger and Control (TTC) system allows the timing and trigger signals to be distributed to the readout electronics elements. The timing signals comprise the LHC clock (BC) and the synchronisation signals (BCR, ECR). The trigger signals include the L1A, test and calibration triggers. The TTC allows the timing of these signals to be adjusted.

The ATLAS TTC system is based on the optical fan-out system developed within the framework of RD12 [1] which allows signals to be distributed from one source to up to 1024 destinations. The system is partitionable and sub-detectors can be running with the central ATLAS timing and trigger signals, or independently, with their specific timing and trigger signals. The TTC system receives the LHC 40 MHz clock (BC) and the ORBIT signal from the LHC, the L1A signal from the central trigger processor (CTP) [2], and commands and data from either the CTP or sub-detector-specific electronics. A proper encoding allows this information to be transmitted on a single optical link which is fanned out to up to 1024 destinations. At the receiving end, an ASIC decodes the incoming signal and makes available the BC clock, the L1A signal, the ECR and BCR signals, the L1ID and BCID and the user commands and data.
Provision is made to adjust the timing of all the signals. The context diagram of a partition is shown in Figure 2.

The TTC crate receives electrical signals from the TTCvi and the LHC machine, and performs the encoding and the electrical-to-optical conversion. An optical tree network with optical passive fan-outs distributes the encoded optical signals to up to 1024 destination nodes. These nodes consist of an optical-to-electrical conversion device followed by a receiver ASIC (TTCrx) which decodes the incoming frame and makes available all the timing, trigger and control signals. The TTCvi is a VME module which provides the trigger and control signals to the TTC crate in the form of two encoded signals (A-channel and B-channel). This module allows the user to select the trigger source and to generate commands at known times. A TTC partition consists of a TTCvi, a TTC crate, an optical network and as many receivers as necessary. An example is shown in Figure 3.

3. TIMING SET-UP WITH BEAM

This section describes a possible automatic way to set-up and check the coarse timing (i.e. everything but the fine BC adjustment) of the detector with beam. This can only be applied when there is beam and the next section will show that it is possible to set-up the timing with test-pulses, which is of great interest during the commissioning phase of the experiment.

It is planned to make use of the LHC bunch structure and of the BCID values provided by the front-end electronics (FE_BCID) or the level-1 trigger electronics (BCID) as specified in [6].

The fine BC adjustment procedure is sub-detector dependent and can be done either before or after the coarse timing has been done (by looking at the data and for instance looking for a peak position or the starting point of a signal). In the later case, an iteration on the coarse alignment procedure might be necessary.

Figure 4 shows a simplified block diagram of the front-end electronics circuitry.

The timing and trigger signals are transmitted by the TTC to geographical regions of the sub-detectors which house a large number of channels, and within which there is no need for fine timing adjustment. For instance in the TRT, such a region is 1/32 of a wheel in the end-cap, which corresponds to 200 to 400 channels depending on the type of wheel; in the liquid-argon
calorimeter a region corresponds to a front-end board which houses 128 channels.

The timing adjustment is based on a two-step procedure.

In a first step, random L1A signals will be generated and data read-out. For each timing distribution region, an histogram of the number of hits (in the sense of presence of a signal above threshold) versus the FE_BCID received from the front-end is built. This histogram should reflect the LHC bunch structure but be shifted in time as shown in Figure 5. The BCR timing is then adjusted in order to get FE_BCID=1 at the correct place.

Figure 5. Hits versus BCID.

In a second step, the system will be run with L1A fixed at BCID = 1. The event read-out will generally give a FE_BCID not equal to 1 as L1A timing has not yet been adjusted. The L1A timing is then adjusted in order to get the correct FE_BCID value.

This method can very efficiently be implemented at high luminosity as the time needed to build an histogram will be very short. It can also be used to check the timing alignment at the beginning of a run for instance.

In the case where the FE_BCID is formed after the level-1 pipeline (for instance to save some silicon area) a similar procedure can be used.

At low luminosity, the occupancy of the different sub-detectors may not be sufficient enough to use efficiently this method. Obviously, in the absence of beam this technique cannot be used. This is why some methods allowing to adjust the timing with test pulses are being studied.

4. TIMING SET-UP FOR BEAM USING TEST-PULSES

As mentioned above, it is deemed extremely useful to be able to set-up the timing for beam before the beam is available. Two objectives are being pursued:

- Set-up the timing of the different parts of a sub-detector so that a single global adjustment is needed to align it in time with the others.
- Set-up the timing of each sub-detector with respect to the others. This could be used during the commissioning phase of the detector to have as complete as possible data taking tests.

This section shows that at the expense of measuring the length of the fibres which distributes the TTC signals, both objectives can be reached.

Additional work is still needed to see whether it’s possible to do more with the test-pulses such as the fine BC adjustment. It could be envisaged for instance to tune the test-pulse timing to simulate the timing of the particles coming from the interaction point, including their time of flight and the detector response time. However this part is very much sub-detector dependent and cannot be addressed here.

Two different methods of using test-pulses are being considered. The first method consists of sending a test-pulse followed by a L1A signal after a known time (this functionality is available in the CTP). The second methods consists of sending a test-pulse which will produce a L1A signal through the normal level-1 electronics. This can be used for instance in the calorimeter.

Figure 6 and Table 1 show the different delays involved in three conditions. The timing adjustment with a test pulse will be considered as efficient if the adjustment of the delay applied to the L1A signal is the same in all conditions.

<table>
<thead>
<tr>
<th>Delay</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>d1</td>
<td>Cable delay from CTP to TTCvi</td>
</tr>
<tr>
<td>d2</td>
<td>Fibre from TTCcrate to TTCrx</td>
</tr>
<tr>
<td>d3</td>
<td>Latency on L1A (TTCvi + TTCrx)</td>
</tr>
<tr>
<td>d4</td>
<td>Latency on test-pulse (TTCvi + TTCrx)</td>
</tr>
<tr>
<td>d5</td>
<td>Pipeline length</td>
</tr>
<tr>
<td>d6</td>
<td>Delay between the prepulse and L1A in CTP</td>
</tr>
<tr>
<td>Adj1</td>
<td>Delay adjustment on L1A in TTCrx</td>
</tr>
<tr>
<td>Adj2</td>
<td>Delay adjustment on test-pulse in TTCrx</td>
</tr>
<tr>
<td>Latency</td>
<td>Level-1 latency up to the CTP output</td>
</tr>
</tbody>
</table>

Table 1. Delay elements

In the case of a beam-beam interaction (Figure 6(c)) producing a signal at the input of the pipeline at the time t0, the L1A will be generated at the time t0 + Latency and will reach the front-end at the time t0 + Latency + d1 + d2 + d3 + Adj1 which must be equal to t0 + d5. Hence one must have Adj1 = d5 - Latency - d1 - d2 - d3.

In the case of a test pulse which generates a L1A (Figure 6(b)), one will have the following if one calls t1 the time at which the test pulse is initiated at the TTCvi level:

\[ t1 + d2 + d4 + Adj2 + Latency + d1 + d2 + d3 + Adj1 = t1 + d2 + d4 + Adj2 + d5 \]

i.e. Adj1 = d5 - Latency - d1 - d2 - d3 which is identical to the value obtained with beam.
5. CONCLUSIONS

The strategy for setting-up and controlling the timing with beam is based on the availability of a BCID in the front-end electronics and the LHC bunch structure.

At the expense of the measurement of the TTC distribution fibres, it is possible to approximately set-up the timing with test-pulses.

Each ATLAS sub-system must provide their own timing set-up strategy and the TTC system components must include all the necessary tools to do so.

6. REFERENCES

THE SLOW CONTROL SYSTEM 
FOR THE NA48 EXPERIMENT

R. Fantechi
NA48 Collaboration*

Abstract

The NA48 collaboration at CERN has built an experiment control system using VME and G64 hardware and the commercial software toolkit, FactoryLink, for supervisory functions. Specific front-end software has been developed using object-oriented techniques to handle the input/output to/from the hardware. IndustryPack modules, the proprietary field bus CAENET and G64 hardware has been used to provide the maximum flexibility, which is helped by the use of databases to drive the operation of both the front-end and the supervisor software. The experience with both the hardware and the software is reviewed.

1. INTRODUCTION

The NA48 Collaboration has built a detector to measure the direct CP-violating parameter \( \varepsilon'/\varepsilon \) in neutral kaon decays [1]. The experiment runs in the CERN North Area High Intensity Facility in an underground cavern and its elements are spread down the beamline for about 250m. The collaboration considered the implementation of a slow control system to be necessary not only for the usual and obvious reasons to have one single, remote point of control, but also because the area is inaccessible whilst there is beam. In addition, because the two experiments in the area (NA48 and NA50) get beam alternately, there is little possibility of accessing the equipment outside our scheduled beam time.

Because the detector is spread over such a distance, we have implemented a distributed system with VME crates in specific areas and a supervisor station in the control room.

2. THE REQUIREMENTS

The slow control system should fulfill the following requirements:
- Control of power in racks, crates and power supplies
- Monitor of temperatures, mainly in crates
- Monitor of voltage and currents in crates and power supplies
- Control and monitor of high voltage channels

In addition to these usual items, there have been requests for:

* The NA48 Collaboration:
  - University of Cagliari and INFN-Sezione di Cagliari
  - Cavendish Laboratory, University of Cambridge
  - EP and IT Divisions, CERN, Geneva
  - Joint Institute for Nuclear Research, Dubna
  - Department of Physics and Astronomy, University of Edinburgh
  - University of Ferrara and INFN-Sezione di Ferrara
  - University of Firenze and INFN-Sezione di Firenze
  - Institut für Physik, Universität Mainz
  - Laboratoire de l’Accelerateur Lineaire, Orsay
  - University of Perugia and INFN-Sezione di Perugia
  - University of Pisa, Scuola Normale Superiore and INFN-Sezione di Pisa
  - CE-Saclay-DAPNIA
  - Fachbereich Physik, Universität Gesamthochschule, Siegen
  - University of Torino and INFN-Sezione di Torino
  - Institut für Hochenergiephysik, Vienna
  - Soltan Institute for Nuclear Physics, Warsaw
• Control and monitor of a movable target
• Monitor of the purity of the helium in a big tank
• Detection of sparks in the LKr HV system

The functionality required is basically monitoring and control, without responsibility for safety issues. However, in practice, a first level of safety for sensitive items has been introduced; for example, some crates are switched off if their temperature exceeds a defined threshold. Alarm detection, alarm notification, trending and display of monitored values are available. External interfaces are provided to the DAQ and liquid krypton cryogenics systems.

Table 1 shows the number of hardware channels, the number of database parameters used in the software and the total number of parameters including those relevant for the supervisor. Adding also all the other parameters used by the supervisor, one gets a total of about 70000.

<table>
<thead>
<tr>
<th>Hardware channels</th>
<th>Parameters in Hw DB</th>
<th>Including supervisor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog ch</td>
<td>1000</td>
<td>6000</td>
</tr>
<tr>
<td>HV chann</td>
<td>750</td>
<td>3000</td>
</tr>
<tr>
<td>Digital Out</td>
<td>250</td>
<td>500</td>
</tr>
<tr>
<td>Digital In</td>
<td>120</td>
<td>400</td>
</tr>
<tr>
<td>Fan trays</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>220V sw</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Total</td>
<td>2225</td>
<td>10005</td>
</tr>
</tbody>
</table>

Table 1 – The number of channels/parameters

3. THE HARDWARE

The choice of the hardware has been done keeping in mind the costs, especially for the acquisition of high-volume analog data. There are four VME crates installed in different positions along the experiment, each equipped with a Motorola MVME167 Single Board Computer, running LynxOS. These are diskless and are booted over the network. To improve the accessibility to the front-end crates, remote reset, remote console capability and a connection to a UPS are implemented.

I/O is based on GreenSpring IndustryPack Carriers and a series of IndustryPack modules from different manufacturers (PT100 conditioning, ADC, Digital I/O, GPIB, Relay Multiplexer). Cheap, high-volume analog acquisition is done using G64 Multiplexer/ADCs developed at CERN for Aleph/Delphi and connected to the front-end crates with a VME-G64 interface developed at CERN [2].

The control of the majority of the crates and of the high voltage power supplies is done using the Canet fieldbus, because all the HV power supplies are from CAEN and the fan trays (VME, NIM, CAMAC) are equipped with a Caen interface. Several controllers CAEN V288 are installed to reduce the communication load on the modules.

During 1998, tests were made to communicate with a few fan trays via the CAN fieldbus using a CAN interface on an IP module. Before the run in 1999, there will be a partial conversion to the use of CAN for the control of crates in a specific area.

4. THE SOFTWARE

4.1 Front-end software

The front-end SBC runs a single program, called the Daemon, which provides the control of all the installed I/O hardware. The Daemon is multi-threaded with different threads used for different survey speeds and to manage all parallel activities. It is implemented in C++ with Object Oriented techniques and is configured entirely from a database containing a definition of all the hardware components and other objects. Thus, the same code can run on all four front-ends. The Daemon regularly polls all channels, but only reports changes to the supervisor, which markedly reduces the load on the network and supervisor computer. A value is deemed to have changed if the difference with the previous measurement is bigger than a dead band value specified on a per-channel basis in the database. Full-duplex communication with the supervisor is achieved via remote procedure calls, so that the Daemon can also accept commands from the supervisor and act accordingly.

4.2 Hardware database

The parameters for all front-end objects are defined in a database which is maintained and updated using FileMakerPro. Using this product, an export procedure exists which produces the flat Ascii configuration files used by the Daemons as well as the interface definition files for the FactroyLink supervisor. If required the database can also provide wiring lists for all hardware connections.

The Object Oriented approach is very useful because new hardware can be added with no software changes providing the necessary classes are already implemented. One simply has to add the entries into the database and reload the Daemon.

4.3 Supervisor software

The supervisor station uses the commercial tool FactoryLink, running on an HP 712-80 with HP-UX. FactoryLink is built around a kernel containing a real-time database which communicates with a set of independent tasks. These provides facilities including a Graphical User Interface, Alarm Handler, Data Logger, as well as Trending and so forth. Additional tasks have
been implemented at CERN to communicate with the front-end systems and to interface to the NA48 Data Acquisition System.

4.4 Interfaces to other subsystems
The implemented architecture allows for easy interfacing with other subsystems, both at front-end and supervisor levels. In particular, the front-end provides an interface to the software used at CERN to control power distribution equipment in order to control the power in the main electronics installation.

For a several applications, such as measurement of currents for the drift chambers and calorimeter synchronously with the beam, the front-end software implements a synchronous survey driven by a hardware interrupt generated from the SPS timing signals.

At the supervisor level, a task available with FactoryLink is used to retrieve data from the Liquid Krypton Cryogenics system, also supervised by FactoryLink, so that this is available for display within the experiment control system.

5. IMPLEMENTATION PHASES

The work on the NA48 slow control system started in early 1995 with a formal specification of existing requirements. This was done using ESA FS505 methods and led to a User Requirement Document [3] used for the implementation. At the same time, procurement of the hardware was started and in the summer 1995 a first version was ready, mainly for debugging purposes, with a fraction of the hardware.

During the winter of 1996 almost all the hardware was installed, the FactoryLink applications were improved and bug fixed and a real-life test was started [4],[5]. The system was operated for the first time in an NA48 run, getting a good feedback from the users.

For the 1997 run, effort was spent in improving the reliability with few hardware additions and with extensive training for NA48 physicists. In 1998 there has been the implementation of the liquid krypton calorimeter High Voltage control subsystem and few developments and maintenance are foreseen for the next year.

The experience with ESA methods has been successful, even if not all the items were included at the beginning. This is because the detector was still evolving and some subsystems were designed after the work on the system started. Some inertia was present as well, due to the "quick and dirty" way of working of physicists, who sometimes prefer to have something ready now instead of sufficiently studying the details in order to avoid to do the same work many times.

Some violation of the framework of the URD happened:

- A control loop was added to switch off power under certain conditions to provide a certain level of security. No such system had been foreseen in the URD.
- Some areas of the software have been implemented many times, either because specific hardware was modified or because knowledge of the best way to operate the equipment was refined through prototype tests.
- It has not been foreseen to read data synchronously with the beam.

6. EXPERIENCE WITH THE SYSTEM

6.1 Hardware
The experience with the hardware is very good. In parallel to the front-end software development, a set of small dedicated programs to test the hardware has been written, helping the installation and even the debug of the Daemon software.

As far as CaeNet is concerned, the NA48 installation is a big one, both in terms of high voltage channels and fan trays. Continuous contact with the CERN electronics pool and with CAEN experts helped a lot in fixing software problems as well as hardware hick-ups which we have experienced. CaeNet timing can be a problem with many devices on the same segment.

6.2 Front-end software
The software in the front-ends has been reliable and it is easy to add new devices.

6.3 Supervisor software
FactoryLink is a complete tool for supervising slow control systems: it has an elaborate graphical user interface, consistent sets of colours, icons, graphical objects, etc. However it has few problems which give some troubles to the developer:

- It lacks an object-oriented structure, which could help in mapping the supervisor to the front-end
- It does not provide a multi-user protection mechanism, although this is available from a third party vendor.
- It needs a big investment in training for a good use and efficient development of user interfaces
- It consumes computing resources, although perhaps not more than similar products. In our case, the system grew from the initial expectations and the workstation used is now under-configured for the latest versions of HP-UX and FactoryLink.
- Changes and additions are slow to implement. It is almost impossible during the run to fix quickly a problem during the 8 hours SPS MD periods once a week
7. CONCLUSIONS
The NA48 slow control system has been described. It has been in operation for three years now and has been shown to be useful and reliable. The front-end hardware and software are easily implementable and the supervisor software has good features, even if the changes cannot be implemented as easily as one would like.

The initial specification of user requirements has helped a lot during the implementation and it would have been better if more details should have been described. Many of the requirements and functionality could apply as well to LHC experiments, where the basic principles could be employed, even if at a different scale.

8. REFERENCES

[1] G.D. Barr et al., CERN/SPSC/90-22/P253
FRONTEND I/O VIA CANBUS
OF THE ATLAS DETECTOR CONTROL SYSTEM

B. Hallgren and H.J. Burckhart
CERN, Geneva, Switzerland

Abstract

The ATLAS Detector Control System (DCS) will be organised in several hierarchical levels. The lowest one connects to the subdetector hardware and to the sensors and actuators. This connection will mainly be achieved via the commercial CAN fieldbus, which is very well suited for such distributed readout and control. The concept of the "Local Monitor Box" (LMB) as a modular building block for this work is proposed. The first implementation consists of a CAN bus node and a 16+7 bit delta-sigma ADC for the readout of Ptl00 high precision temperature sensors. The CANopen standard is employed as high-level software protocol. The general implementation will be discussed and results from tests performed with the ATLAS LAr calorimeter and first results from radiation tests will be presented.

1. INTRODUCTION

A distributed control system which uses the CANbus will provide the basic control and monitoring functions for the ATLAS detector [1]. CANbus is one of the CERN recommended fieldbuses [2]. It is especially suited for sensor readout and control functions in the implementation of a distributed control system. Reliability, availability of inexpensive controller chips from different suppliers, ease of use, wide acceptance by industry and the expectation that CAN will be available for a long period of time, were strong arguments in favour of this choice. Unlike traditional networks, such as Ethernet, where performance is measured in terms of throughput of large data blocks, fieldbuses are optimised for controls i.e. exchange of status and command messages. The ATLAS DCS system has particular requirements, which usually are not found in commercial systems. The environment close to the ATLAS detector necessitates the use of components that are tolerant to radiation. The magnetic field around the detector requires that non-ferromagnetic components be employed in the front-end electronics. The number of parameters to measure and control requires multi-channel solutions to be economical.

In the next sections of the paper the main aspects of CAN hardware and of CANopen software is covered. Then the concept of the LMB will be introduced and the results of the first measurements will be discussed.

2. THE CANBUS

Controller Area Network (CAN) [3] is a fast serial bus that is designed to provide reliable and very cost effective links. CAN uses a twisted pair cable to communicate at speeds of up to 1 Mbit/s with up to 127 nodes. It was originally developed to simplify wiring in automobiles.

2.1 Data Exchanges and Communication

A CAN message contains an identifier field, a data field and error, acknowledgement and CRC fields. The identifier field consists of 11 bits for CAN 2.0A or 29 bits for CAN 2.0B. The size of the data field is variable from zero to 8 bytes. When data are transmitted over a CAN network no individual nodes are addressed. Instead the message is assigned an identifier which uniquely identifies its data content. The identifier not only defines the message content but also the message priority. Any node can access the bus. After successful arbitration of one node all other nodes on the bus become receivers. After having received the message correctly, these nodes then perform an acceptance test to determine if the data is relevant to that particular node. Therefore, it is not only possible to perform communication on a peer to peer basis, where a single node accepts the message, but also to perform broadcast and synchronised communication whereby multiple nodes can accept the same message that is sent in a single transmission.

2.2 Arbitration and error checking

CAN employs the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) mechanism in order to arbitrate access to the bus. Contrary to other bus systems CAN does not use acknowledgement messages, which cost bandwidth on the bus. All nodes check each frame for errors and any node in the system that detects an error immediately signals this to the transmitter. This means that CAN has high network data security as a transmitted frame is checked for errors by all nodes.

The error checking include Cyclic Redundancy Check (CRC), Acknowledgement Errors, Frame Errors, Bit Errors and Bit Stuffing Errors. The concept of Bit Stuffing is, that, if more than five consecutive bits are of the same polarity, a bit of opposite polarity is inserted. If an error is detected by any of the other nodes, regardless of whether the message was meant for it or not, the
current transmission is aborted by transmission of an active error frame. An active error frame consists of six consecutive dominant bits and prevents other nodes from accepting the erroneous message. The active error frame violates bit stuffing and may also corrupt the fixed form of the frame causing other nodes to transmit their own active error frames. After an active error frame, the transmitting node begins re-transmission of the frame automatically within a fixed period of time.

2.3 CANbus speed and lengths

Table 1 shows the relation between the bit rate and the cable length:

<table>
<thead>
<tr>
<th>Bit rate</th>
<th>Cable length</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kbits/s</td>
<td>6.7 km</td>
</tr>
<tr>
<td>20 kbits/s</td>
<td>3.3 km</td>
</tr>
<tr>
<td>50 kbits/s</td>
<td>1.3 km</td>
</tr>
<tr>
<td>125 kbits/s</td>
<td>530 m</td>
</tr>
<tr>
<td>250 kbits/s</td>
<td>270 m</td>
</tr>
<tr>
<td>500 kbits/s</td>
<td>130 m</td>
</tr>
<tr>
<td>1 Mbits/s</td>
<td>40 m</td>
</tr>
</tbody>
</table>

The length of a CAN message varies not only depending on the number of data bytes transmitted but also on the contents of the message. This is due to the error checking methods (bit stuffing) described above.

3. CANOPEN

A high level standard is needed to define how the different nodes on a bus segment use the 11-bit identifier and the 8 data bytes. Among the standards, which use the CAN bus, CERN has chosen CANopen. The CAN in Automation (CiA) organisation [3] supports this protocol. CANopen was originally developed from an EEC ESPRIT III project and has found applications in industrial automation applications.

3.1 Device profiles

CANopen uses the concept of device profiles. Manufacturers can produce standardised devices by conforming to the guidelines contained in a CANopen device profile. Modules from different manufacturers can operate together with the same low level software. Basic network operation is guaranteed by defining mandatory device characteristics. It is possible to implement additional functions with the help of the optional and the manufacturer specific part of the profiles. There are a number of standard profiles available, which cover e.g. I/O modules, measuring devices and closed loop controllers. The profiles are implemented in a standardised database called object dictionary. There are software tools available to read, configure and change entries in the dictionary of a device. The object dictionary is not stored in the CANopen node itself; it is defined in an Electronic Data Sheet. In this way a network master will know the data type and size of every object.

3.2 The communication profile

The communication profile defines that in a CANopen network there must be at least one master application. The master performs the boot-up process and maintains the network in an operational state. It can also manage the object dictionary entries and the CAN identifiers of the connected devices. Real-time data transfers are called Process Data Objects (PDO). The communication profile specifies several methods for transmission and reception of messages over the CAN bus. Synchronous data transfers allow network wide co-ordinated data acquisition and actuation. Synchronous transfers are supported by predefined communication objects i.e. synchronisation messages transmitted on a cyclic time period and time stamp messages. Asynchronous or event messages may be sent at any time and allow a device to immediately notify another device without having to wait for a synchronous data transfer to take place. The network master using Network Management (NMT) may dynamically configure PDO messages at network boot up. Although CAN is restricted to transfer a maximum of 8 bytes of information, data transfers larger than 8 bytes in length are also provided for by the protocol and are called Service Data Objects. The detailed specifications of the CANopen communication profile are contained in the CiA DS 301 document [4].

3.3 Minimal Functionality Devices

In order to implement simple slave nodes the CiA DS 301 profile specifies what minimal functionality a CANopen device must provide. Default identifiers are available directly after power up but they can also be modified. Only a limited selection of the CAN identifiers has to be supported by a device node. These CAN identifiers can be pre-configured by means of DIP switches or EEPROM. The 11 bits of the identifier contain in the four most significant bits the function code and in the 7 other bits the node number. After the boot up sequence the device boots into a pre-operational state. NMT messages are used to turn a slave node on or off. A single message from the master then makes the device fully operational. NMT is also used to determine whether nodes are still in operation. The functional status of the device is returned as the reply to a remote frame message. Inhibit times/timouts may also be implemented, i.e. if the master does not receive a reply from a node within a certain time period the node is regarded as not functional and an error flag may be set. NMT services can also be used to bring all or selected nodes into various operating states at any time. For
functions as defined in The LMB CAN controller (Figure 1), like differential ADC module, digital I/O or DAC module. The modules can be connected via a serial bus, which also supplies the power to each module. The LMB is designed to be radiation tolerant for a dose rate corresponding to 10 years of operation in the ATLAS cavern. It contains no components sensitive to magnetic field such as DC to DC converters, chokes and transformers. The LMB has low power consumption. This permits the use of remote power supplies via the CANbus connector and the auxiliary power connector on the housing.

4. LOCAL MONITOR BOX

The local monitor box (LMB) is a general-purpose low cost standardised device for the ATLAS DCS front-end. Each LMB consists of one controller CAN-node and up to 6 I/O-modules of different types, (Figure 1), like differential ADC module, digital I/O or DAC module. The modules can be connected via a serial bus, which also supplies the power to each module. The LMB is designed to be radiation tolerant for a dose rate corresponding to 10 years of operation in the ATLAS cavern. It contains no components sensitive to magnetic field such as DC to DC converters, chokes and transformers. The LMB has low power consumption. This permits the use of remote power supplies via the CANbus connector and the auxiliary power connector on the housing.

Figure 1 Block diagram of the Local Monitor Box.

4.1 The LMB CAN controller module

A CAN slave node is implemented with the minimal functions as defined in the CANopen specification [3]. The LMB CAN controller (Figure 2) consists of one CAN controller SAE 81C91 from Siemens and a CAN bus transceiver PCA82C250 from Philips. These are standard components and are available at low cost from industry. The SAE81C91 manages automatically the CANbus protocol. It contains registers for 16 CAN identifiers. For each of the identifiers there are 8 bytes of dual port RAM, in total 128 bytes. The initialisation of the SAE81C91 consists of loading 12 registers with default values. This task is done by the microcontroller AT90S1200 from Atmel. This contains 64 bytes of EEPROM for the SAE81C91 initial values. The AT90S1200 has been developed to have low power consumption while providing high processing performance. It contains only 512 words of program and costs less than $2 even in moderate quantities. This flash microprocessor can be programmed while mounted in the circuit with the help of a serial programming interface implemented on-chip. As shown in Figure 2 there is a second AT90S1200 working in parallel with the first one. This second processor has as main function to allow reading and programming of the other AT90S1200. This permits the downloading and checking of the program in the LMB CANnode via the CANbus. This can be done even when the LMB is installed in the experiment.

4.2 The ADC module

The module is based on a low-cost 16-bit ADC from Crystal Semiconductor CS5525. The CS5525 ADC combines a differential programmable gain amplifier (7 bits) and a chopper stabilised instrumentation amplifier to ensure signal stability (drift of 5nV/°C) in one integrated circuit. The input range is selectable from ±25 mV to ±2.5V. The ADC, based on the delta-sigma principles, includes digital filters to reject noise at 50 Hz and 60 Hz simultaneously and has a common mode rejection of 120 dB. A CMOS multiplexer with 16 differential inputs is used to augment the number of inputs of the ADC. The selected multiplexer is fault protected to ±35V. The printed circuit board (PCB) contains 16 channels. Four PCBs can be stacked together to make a module with 64 differential channels. As
Figure 3 Combined ADC and Pt100 module.

The resistor RC determines the DC current through the sensor, the measurements are not sensitive to changes in the voltage reference and other common mode changes. The resistor RC determines the DC current through the sensor.

4.3 External power supplies

In order to be able to operate the LMB in a strong magnetic field, the power to the LMB is supplied by the CAN cable or by an external connector. There are two separate power supplies, one analogue and one digital. Low drop voltage regulators are used and therefore the actual voltage supplied to the LMB can be between 5 to 15 V. The current consumption for the digital power supply is 36 mA and from the analogue supply 15 mA per 64 channels.

5. MEASUREMENTS

A series of measurement [5] with the LMB was done in July 1998 at the ATLAS LAr EM End-Cap cryostat in the H6 experimental area in CERN SPS. The setup is shown in Figure 4. A total of 9 sensors were used in the measurements. Eight of them (labelled PT1, PT2, PT8) are standard low-cost Pt100 calibrated probes. One reference probe (labelled PRT) is calibrated to ± 1.5 mK in absolute accuracy.

Examples of the behaviour of the temperature in the cryostat are shown in Figure 5 and 6. The temperature is varying by 20 mK. The Figure 5 shows how the sensor PT5 tracks the precision sensor PRT with a mean value of -3.1 mK and a standard deviation of 0.9 mK. The PRT was measured manually using a 5½ digits precision digital voltmeter. The equithermal sensors PRT and PT5 when measured with LMB show a difference of the order of 1 mK and a standard deviation of 1.2 mK, (Figure 6). This corresponds to an effective resolution of the LMB equal to 0.8 mK per channel. One digitisation step corresponds to 1.5 mK.

Figure 4 The positions of the sensors in the cryostat.

Figure 5 Temperature variations measured by the sensors PRT and PT5.
6 RADIATION TESTS

Radiation tests were done at a CERN beam target area in three periods of 11 weeks in total. It has been predicted that the ATLAS Cavern will have an equivalent dose of about 10 Gy and $10^{13}$ neutrons cm$^{-2}$ in ten years of operation. In the three periods of irradiation the dose rate accumulated were 20 Gy, 50 Gy and 100 Gy respectively with fluences of $10^6$, $10^7$ and $10^8$ neutrons cm$^{-2}$ (equivalent 1 MeV Si). The main results are that the tested optocouplers (IL206A) were influenced as shown in Figure 7. The current transfer ratio (CTR) changed from 90% to 3%. However, all five tested optocouplers were still functional in a test circuit when changing the load resistor from 2.2 kΩ to 35 kΩ. Other effects observed were that in two of the four tested microcontrollers AT90S1200 one EEPROM memory location was erased and a voltage reference was changed by -4 mV. The LMB CAN controller and all other components showed no significant changes due to the radiation.

More measurements have recently been performed at a nuclear test reactor with a similar integrated dose rate of neutrons but without gamma rays. The tests were performed during 5 h and at this test the LMB was powered and continuously read out. A preliminary analysis confirms the results described above.

7. CONCLUSIONS

The practical experience with CANbus in the design and operation of the LMB as part of the future ATLAS front-end I/O has been very good. The high-level CANopen protocol greatly simplified the effort in programming of the CAN slave controller. The measurements of the temperature in the LAr cryostat show a precision of about 3 mK and a resolution of 0.8 mK. These performances are a factor 10 better than is needed for the cryogenics temperature measurements. The radiation tests show that with some design precautions being taken standard commercial components can be used in the radiation environment of the ATLAS cavern.

8. ACKNOWLEDGEMENTS

We are very grateful to the LAr group for giving us the occasion to verify the concept of the LMB and to measure its performance in a realistic environment. L. Poggio organised the LAr part of the test. A. Karlov from the CERN IT/CO group provided the very user-friendly and efficient data taking and visualisation program in the BridgeView framework.

8 REFERENCES


[3] CAN in Automation (CiA), D-91058 Erlangen (Germany), http://www.can-cia.de/


POWER SUPPLIES
RHBIP1 TECHNOLOGY EVALUATION TO TOTAL DOSE, LOW DOSE RATE AND NEUTRONS, FOR LHC EXPERIMENTS AND SPACE APPLICATIONS.

Authors: S. Caruso\textsuperscript{1)}, C. Dachs\textsuperscript{2)}, C. Detcheverry\textsuperscript{3)}, P. Jarrou\textsuperscript{4)}, S. Leonardi\textsuperscript{5)}, E. Noah\textsuperscript{6)}

1) CERN - Geneva (SWITZERLAND), 2) ST-Microelectronics - Catania (ITALY)
3) University of Montpellier - (FRANCE), now with Philips Research, The Netherlands
S. Leonardi, ST-Microelectronics - Stradale Primosole, 50 - 95121 - Catania (Italy)
Phone: +39 95 7407645; FAX: +39 95 7407099; E-Mail: Salvatore.Leonardi@st.com

ABSTRACT. RHBIP1, AN INDUSTRIAL IC TECHNOLOGY, HAS BEEN TESTED AND A FIRST EVALUATION OF ELEMENTARY Bipolar COMPONENTS TO TOTAL DOSE EFFECTS (TID), LOW DOSE RATE EFFECTS (LDRE) AND NEUTRONS HAS BEEN MADE FOR LHC & SPACE APPLICATIONS.

1) Introduction. Space and LHC-CERN electronics need analog electronics components tolerant to total dose effects (TID) and displacement damage. Low dose rate enhancement effect is also a matter of concern for both Space and LHC applications since the operating dose rate is usually in the range of 0.01 rad/s or smaller.

The RHBIP1 process, suitable for both high speed and power analog circuits, has been identified as very tolerant to TID and displacement damage. The present paper presents the results of the investigation of the radiation hardness of this process and discusses the first application of the RHBIP1 technology, a radiation tolerant Voltage Regulator with specifications that fulfill the needs of LHC experiments, and compatible space missions.

Most of the sub detectors of the LHC experiments such as, trackers, calorimeters and muons systems require local powering of their electronic boards and detector modules with associated slow control system in order to get clean and precise low supplies voltages. There are 3 fundamental issues related to the use of voltage regulators in the harsh and confined environment of LHC experiments:

1) The high radiation level in total dose up to 500 krads, and up to a neutron fluence of $2 \times 10^{13}$ n/cm$^2$ or 10 year of operation in the outer detector regions. Tracker regions with a much higher level of radiation are foreseen to be remotely powered from outer regions.

2) Detectors and readout electronics are packed in a confined space where cooling is extremely difficult. The in situ power consumption has to be minimised.

3) Access to these regions is extremely limited, and static or dynamic overload conditions, such as latch up of powered components caused by single event effects, have to be properly monitored and remotely controlled.

2) RHBIP1 Technology. The devices investigated in this paper come from an industrial standard high speed BiCMOS technology [1,2,3].

The technology of RHBIP1 is based on the monolithic integration of complementary vertical high speed NPN and PNP transistors as sketched in fig.1.

The thin intrinsic base width of these transistors makes this process suitable for designing ICs operating in the range of GHz, and with a good radiation tolerance against displacement damage.

The radiation hardness of RHBIP1 technology against total dose effects TID, is obtained by improving the oxide quality over emitter-base depletion region (BiCMOS technology) and by reducing the intrinsic base thickness of all bipolar transistors [4]. In addition, based on preliminary radiation test, lateral pnp transistor has been excluded.

Further features of RHBIP1 technology are the maximum operating voltage up to 12 volts, minimum emitter size of 5microns, the gain Hfe in the range of 100 before irradiation for both transistors, and a transition frequency of 2.5GHz and 6GHz respectively for the vertical PNP and NPN. RHBIP1 is a double metal level process, with double poly layer with high and low sheet resistance, poly capacitors. Contact and via size is 2.0 micron, and metal pitch is 4.5 micron.

3) Radiation tests. All components of the RHBIP1 technology, bipolar transistors, resistances and capacitors, have been tested with x-rays, $^{60}Co$ at different dose rates and total doses. Neutrons irradiation up to a fluence of $2 \times 10^{13}$ n/cm$^2$ have been performed to evaluate the effect of the displacement damage. Sizes and some geometrical dimensions of the bipolar transistors tested are given in table N.1.

Bipolar devices were irradiated with emitter, base and collector connected to ground. It has been verified that these connections corresponds to the worse case conditions. X-ray irradiations were performed at two dose rates, 100 rad/s and 10 rad/s. Gamma irradiation with a $^{60}Co$ source was performed with a dose rate of 4 rad/s. The low dose rate test has been performed at 0.02 rad/s, a typical condition for LHC operation and space environment.
3.1] - Total dose results. The radiation effects on bipolar transistors have been investigated by measuring the $H_{fe} = f(I_c)$ characteristics for total dose values up to 500 krad. The $H_{fe}$ gain is a key parameter for the design of analog circuit. $H_{fe} = f(I_c)$ curves directly determine whether a bipolar transistor is usable or not in a given circuit at a specified collector current, for the maximum total dose expected in the application.

Figures 2 and 3 show the gain evolution of the minimum size bipolar transistors, irradiated with x-rays at a dose rate of 10 Rad/s. At 500 krad and a 10 mA collector current, the $H_{fe}$ gain decrease of minimum size NPN and ICVPNP devices is respectively 28% and 41%, whereas at a collector current of 100 mA, they are respectively 14% and 28%. These $H_{fe}$ gain drops are acceptable in most of the foreseen applications.

Figures 4 and 5 show the results obtained for power NPN and ICVPNP bipolar transistors.

Tab. 1 - Geometrical dimensions of bipolar components

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PNP Power</th>
<th>NPN Power</th>
<th>PNP Min.</th>
<th>NPN Min.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Area ($\mu m^2$)</td>
<td>10 800</td>
<td>4 350</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Emitter Peri. ($\mu m$)</td>
<td>4 536</td>
<td>1 827</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>P/A Ratio ($\mu m^2$)</td>
<td>0.42</td>
<td>0.42</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>Base Area ($\mu m^2$)</td>
<td>28 000</td>
<td>28 000</td>
<td>150</td>
<td>155</td>
</tr>
<tr>
<td>Tot. Area ($\mu m^2$)</td>
<td>67 000</td>
<td>67 000</td>
<td>2 350</td>
<td>750</td>
</tr>
</tbody>
</table>

Tab. 2 - Gain degradation on min. size bipolar transistors at 500 Krad for two different current values.

<table>
<thead>
<tr>
<th>500 Krad results - 10 Rad/s</th>
<th>$I_c = 10 \mu A$</th>
<th>$I_c = 100 \mu A$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$H_{fe}$ PNP prerad</td>
<td>136</td>
<td>130</td>
</tr>
<tr>
<td>% - degradation</td>
<td>28 %</td>
<td>14 %</td>
</tr>
<tr>
<td>$H_{fe}$ PNP prerad</td>
<td>72</td>
<td>70</td>
</tr>
<tr>
<td>% - degradation</td>
<td>42 %</td>
<td>28 %</td>
</tr>
</tbody>
</table>

Tab. 3 - Gain degradation on power bipolar transistors at 500 Krad for two different current values.

By comparing the gain degradation at a given current value ($I_c=100\mu A$, see tables 2 and 3), minimum size transistors show a better behaviour than the power transistors. As expected, the gain degradation is related to the emitter perimeter, which is larger in case of power devices [5]. However, power devices are generally used at a much higher collector current in analog ICs, such as voltage regulator. In the
case of the power NPN, for a constant normalised collector current density, the observed Hfe drop is actually smaller than for minimum size devices.

Postrad Hfe=f(Ic) characteristics shapes indicate that the Hfe is much more degraded at very low collector currents. This can be explained by surface recombination mechanism, which are observed in all bipolar technologies [6]. This result has an impact on the design of radiation tolerant circuit, where analog bipolar configuration circuits with very low bias current should be avoided.

Tested resistors and capacitors have not showed any significant degradation (<1%) after a maximum total dose of 500 krad.

3.2] - Low Dose Rate results. Low dose rate enhancement effect has also been investigated for three dose rates, 10 rad/s with X-ray, and 4 rad/s and 0.02 rad/s with a Co-60 source on minimum and power size transistors. We report here only the results on power devices, which are intrinsically more sensitive to this effect.

Comparison between 4 rad/s results (Fig. 6 and 7) and 0.02 rad/s results (Fig. 8 and 9) on power devices for total dose range of 50 krad to 100 krad indicates no significant low dose rate enhancement effect, less than 10% for NPN devices and almost nothing for PNP devices, in particular for low collector current.

![Co-60 irradiation @approx. 250 rad(Si)/min](image)

Fig. 6 - Hfe of NPN Power irradiated up to 1 Mrad total dose at a dose rate of 4 rad/s.

![Co-60 irradiation @approx. 250 rad(Si)/min](image)

Fig. 7 - Hfe of ICVPNP Power irradiated up to 1 Mrad total dose at a dose rate of 4 rad/s.

However, this results should be confirmed, since prerad characteristics between these two devices were not identical.

3.3] - Neutrons - All RHBip1 components have been irradiated with neutrons at two different fluences. Results of the Hfe decrease for minimum size transistors after a fluence of $10^{13}$ n/cm$^2$, are summarised in Table 4. They indicate that the maximum Hfe degradation is respectively 8% and 11% for NPN and PNP transistors at a collector current of 100 mA.

<table>
<thead>
<tr>
<th>Fluence (n/cm²)</th>
<th>Hfe NPN and PNP Chain</th>
</tr>
</thead>
<tbody>
<tr>
<td>10$^{13}$</td>
<td>8%</td>
</tr>
<tr>
<td>10$^{14}$</td>
<td>11%</td>
</tr>
</tbody>
</table>

Tab. 4 - Hfe degradation by neutrons irradiation on minimum size transistors at 10$^{13}$ n/cm$^2$.

For the same fluence, the Hfe decrease of power devices (Table 5) is not more pronounced than for the minimum size devices, 6% and 8% for respectively the power NPN and the ICVPNP at a collector current of 100 mA. This is explained by the fact that the displacement damage is only influenced by the emitter area (current density) and not by the device perimeter like for surface recombination.
Tab. 5 - Hfe degradation by neutrons irradiation on power NPN and ICVPNP transistors at $10^7$ nrn/cm$^2$.

Fig. 10 - Comparison of Hfe degradation by neutrons and X-ray irradiation on minimum size NPN device.

Fig. 11 - Comparison of Hfe degradation by neutrons and X-ray irradiation on minimum size ICVPNP device.

4) Voltage regulator - The functional blocks of a series voltage regulator circuit is presented in Fig. 12. It consists of a reference voltage element, an error amplifier, and a series-pass element (ballast) [7]. Smart features have been included in the design to enable to remotely monitor and control voltage regulator embedded in detector systems such as remote sensing, digital signal output available to monitor an over-current condition (OCM), inhibit input signal to switch off the regulator for de-latching electronic circuits, temperature protection circuit to turn off device and avoid damage due to environment temperature or over power dissipation.

The circuit design of the voltage regulator has been especially studied to enable operation with the minimum possible dropout voltage, important to minimise the external power dissipation in powering modern VLSI circuits operating at low voltage supplies (3.3V, 2.5V). A maximum drop of 0.5 and 1.5 Volt for 1 and 3A load current respectively in the whole range of temperature outperforms commercially available voltage regulators.

The choice of a series bipolar power device guarantees an independent drop as function of input voltage and a better dynamic behaviour of the Voltage Regulator. Both characteristics are key features in low voltage and high current application. Output voltage accuracy specification is ±2% in the whole range of temperature, from +10°C to +70°C, corresponding to 4.9-5.1 Volt output voltage stability for voltage regulator with 5 volt output.

A dedicated design and layout have been employed with a modification of standard design rules, in particular for spacing rules and biasing operating currents, in order to minimise postrad leakage currents inside and between elementary component. The optimisation of the circuit design has lead to only use a restricted group of well tested and qualified elementary components.

Based on the radiation tests, power devices has been also optimised by using a special ratio between emitter area and emitter perimeter in order to increase the radiation tolerance.

5) Conclusion. An evaluation of elementary devices of the RHBip1 bipolar technology to total dose, low dose rate and neutrons has been made. Hfe gain degradation in terms of total dose and low dose rate enhancement effect has been evaluated on minimum size and power devices. Results indicate that the technology should enable the design of analog and power circuit compatible with the space radiation environment and LHC requirements.

Based on this promising results, the design of a radiation tolerant Voltage Regulator for LHC and Space applications has started.

REFERENCES


A RAD HARD PWM INTEGRATED CIRCUIT FOR POWER SUPPLIES CONTROL

T. Melebeck, M. Mélotte, C. Poncelet, SdM, Charleroi, Belgium (email: melebeck@etc.alcatel.be)

1. INTRODUCTION

PWM controllers are widely used in power conditioning. Many integrated circuits based on conductance (or current) control techniques are available on the market.

They generally make use of variations of peak or peak-to-peak current control techniques.

However, nothing exists for average current control, even in commercial parts.

Therefore, ESA has decided to develop a rad hard chip based on average current control technique. This circuit will become available to all manufacturers of rad hard power supplies, after successful development and evaluation.

2. PRINCIPLE OF OPERATION

In a conventional voltage mode control of a PWM regulator, the error amplifier signal directly interfaces with the PWM comparator.

In the conductance control mode (see fig. 1), the new feature is the introduction of a current measurement and a second error amplifier forming an inner feedback loop, which controls the inductor current as a direct function of the voltage error amplifier output signal.

Such a configuration converts the second order behavior of the classical PWM regulator into a first order system.

The additional benefits, such as ability to parallel power stages, total device and system protection due to the intrinsic current limitation, are major advantages of this technique [1].

3. BLOC DIAGRAM

All the active elements of the conductance control loop excluding the power devices are integrated.

The main features include (see fig. 2):

- a current loop with a current sense error amplifier and a PWM comparator,
- a sawtooth generator, adjustable to the required frequency with external passive components (from 20 to 400 kHz),
- a voltage loop with a voltage error amplifier,
- a current limitation circuit,
- an undervoltage detector,
- a divider by 2 to generate the control signals of push pull drivers,
- driver stages (50 mA).

Dedicated power supply pins are allocated respectively for the analog part of the chip (amplifiers, comparator, limiter, sawtooth) and for the power section (output buffer and push pull drivers).

The purpose is to minimize possible troubleshooting of the analog cells by crosstalk of the power cells.

Another requirement of flexibility and testability dictates a pin allocation where all inputs and outputs of the analog cells are accessible.

Figure 1: Average current conductance control

Figure 2: Functional diagram
4. MAIN CHARACTERISTICS

In order to cover the broadest application domain of space power converters, the preliminary requirements specification has been defined as large as possible for the voltage supply, the switching frequency and the operating temperature ranges.

The main characteristics have been listed hereunder:

Supply voltage range : 8 to 35 V
Power consumption : 10 to 27 mA
Operating temp range : -55 to +125°C
Operating frequency : 20 to 400 kHz
Input offset voltage : ±10 mV
(Volt. amplifier)
Gain Bandwidth Product : 3 MHz min.
(Volt. amplifier)
Drivers rise/fall time : 70 to 120 ns
(Cload = 200 pF)
Radiation hardness : 50 krad min.

5. APPLICATION AREAS

The concept allows a maximum of flexibility in the operation.

The chip implementation leads to several independent building blocks, to be interconnected by the users.

The most classical configuration is the buck regulator, eventually complemented in the smart topology (see fig. 3).

These topologies are mainly devoted to low and medium power DC-DC converters in stand-alone operation (10 to 100 W).

Other configurations are possible like in high power regulators (5 to 10 kW), where a modular architecture is preferred for reliability reason.

In this case, the Conductance Control technique permits parallel power stages with effective current sharing.

Application areas cover the low and medium power DC-DC converters of satellite payloads, as well as the high power (few kW) battery charge and battery discharge regulators.

More generally, the circuit is able to work in a rad hard environment, in power supplies configurations with or without the current loop control.

6. PROCESS SELECTION

A radiation hardness of 50 krad (Si) minimum is required, without any derating. A latch-up free operation is also mandatory.

A complementary bipolar process with Dielectric Isolation from Harris has been selected to meet these requirements.

The selected EBHF process is a 35 V bipolar process with complementary vertical transistors, dielectric isolation and thin film Ni-Cr resistors.

The process is accessible through FASTRACK, an integrated design tool based on CADENCE and allowing schematic entry, electrical simulations and layout of custom and semicustom circuits.

Moreover, the process is used for the production of many rad hard circuits (standard parts and ASICs).

The radiation effects can be predicted by the use of dedicated Spice models (for total dose and neutron) provided by the manufacturer.

The design being targeted to 50 krad minimum, the 300 krad model has been used, and some design margins (ESA derating factors) have been included.

SEU susceptibility is not a concern since the circuit is fully analog, thus excluding any latching function.
7. DESIGN PHASE

The design methodology adopted for this project is a classic one, using standard CAD tools and the cell library of the selected process.

Moreover some special design guidelines related to high rel applications have been observed to assess a safe nominal operation in a harsh space environment:

- thermal simulations of the component have been performed in order to demonstrate that the maximum junction temperature does not exceed 110°C in the worst, case conditions of power dissipation in vacuum,
- electromigration analysis has been studied in order to keep the maximum current density in the metallisation tracks under a specified value which does not affect the long term reliability,
- reliability estimation based on CNET and MIL HDBK217 prediction models has been made in order to assess the failure rate of the component.
- the radiation hardness problem has been addressed by using the Spice models provided by HARRIS (at 300 krad total dose).
- large design margins have been used in order to cope with the ESA derating factors, avoiding any excessive stress to the component in the normal operating mode.

8. TEST RESULTS

The development phase is completed resulting in prototype circuits compliant with the technical specification [2].

Extensive characterization has been done at component level by SdM, while ESA has performed the validation at power supply level.

The tests performed by SdM include the static and dynamic testing of the prototype, over the full temperature range, to check the compliance of the design with the ESA specification.

The tests performed by ESA were application tests, where the component has been mounted in a breadboard of a DC-DC converter (28 V - 10 A - 50 to 200 kHz) in a buck regulator at ambient temperature. Measurements of current consumption, phase and gain margins, and loop delays were performed and compared to a discrete implementation, with excellent results.

Other additional tests have been performed by Alcatel ETCA (Charleroi, Belgium) on a breadboard of a 15 W (at 20 V and 120 kHz) converter in a smart topology.

The line rejection and audio rejection measured over the temperature range with the chip have shown also an excellent behavior, if compared with the discrete implementation (38 to 70 dB).

Based on all these results, the prototypes have been officially approved by ESA, and authorization to proceed to an evaluation phase has been given.

9. EVALUATION PROGRAMME

The purpose of the evaluation phase presently ongoing is to overstress specific characteristics of the component with a view to the detection of possible failure modes [4].

Additionally, a detailed destructive physical analysis must be performed to detect any design and construction defects which may affect the reliability of the component and facilitate the failure analysis activities.

The evaluation must also include a check of the susceptibility of the chip to ESD damage.

An evaluation test plan has therefore been submitted to ESA and includes:

- radiation validation test
- ESD sensitivity test
- electrical tests
- high temperature endurance test (accelerated lifetest)

The radiation tests have been performed using Co60 source up to 100 krad at low dose rate (between 1 and 10 rad/s) and maximum bias conditions [5].

The circuit has demonstrated a full spec operation with negligible parametric drifts at 100 krad total dose.

To assess the reliability of the component, a high temperature endurance test (1000 hours at 125°C) is requested.

It will be complemented by a construction analysis and an ESD sensitivity test.

The result of these tests will be made available at the end of the contract (planned for November 98).

10. STATUS

Samples and a preliminary data sheet of the component [6] are already available for breadboarding and evaluation.

The agreement between ESA, SdM and HARRIS consists in the introduction of the product in the foundry's catalogue as a standard part without any proprietary rights restrictions on behalf of ESA, so as to favor its commercial diffusion.
ESA will support the design through the recommended use of the chip in the development of new DC-DC converters.

This should contribute to increase the production volumes, to lower the unit cost and to ensure higher perennially of the product.

The circuit will be available in 28 pins ceramic DIL and ceramic metal seal flatpack packages, as well as in die form for hybrids.

The Harris product reference is HS-1664RH and the samples are presently available in DIL 28 package.

11. RELEVANCE TO LHC EXPERIMENTS

The PWM chip presented here shows many features which make it suitable to LHC experiments.

If the power supplies are located in the cavern, near the detector, they must be able to withstand radiation (both gamma and neutron), high magnetic field, coupled with a 10 years reliable operation.

The versatility of the chip (many possible topologies), its radiation hardness and the total device and system protection implemented should simplify the work of the power suppliers involved in the LHC experiments.

The evaluation phase shall also assess the reliability of the component, based on the results of the high temperature endurance tests.

12. CONCLUSIONS

A rad hard PWM chip has been developed for power supplies applications. Prototypes are fully compliant with the specification. The evaluation phase is presently ongoing.

The radiation hardness is confirmed up to 100 krad.

Application tests in different DC-DC converters have validated the principle of operation and main advantages of the PWM conductance controller circuit.

13. ACKNOWLEDGMENT

We wish to thank Mr. P. Perol (ESA/Power Systems Dept.) and his team for their valuable support during this contract.

14. REFERENCES

CAEN SY1527: a new LHC dedicated HV Power Supply System

G. M. Grieco

C.A.E.N. S.p.A., Via Vetraia 11, I-55049 Viareggio, Italy
E-Mail GRIECO@CAEN.IT, URL http://www.caen.it

Abstract

LHC experiments represent an enormous technological challenge both for Experimenters and Industrial partners. CAEN has strongly invested its resources, in the last two years, in the development of a Power Supply system totally dedicated to LHC applications. The underlying idea is to provide the Slow Control groups with an extremely flexible system, featuring an enhanced local intelligence to minimize the Slow Control feedback loops.

The new system embeds a completely new approach to the power generation and distribution problem and has been designed with safety, reliability and ease of maintenance criteria. Telnet and WWW access facilities will allow remote debugging and technical support of the system.

Summary

LHC experiments represent an enormous technological challenge both for Experimenters and Industrial partners. Several problems must be faced, including radiation hardness environment and strong magnetic fields. CAEN, thanks to the know-how accumulated in several years of activity, has strongly invested its resources, in the last two years, in the development of a High Voltage Power Supply system totally dedicated to LHC applications. The underlying idea is to provide the Slow Control groups with an extremely flexible system, featuring an enhanced local intelligence to minimize the Slow Control feedback loops.

The new system embeds a completely new approach to the power generation and distribution problem: ordinary High Voltage boards will be used both as direct supplies to the various detectors and as primary channels for remote distributed systems (peripherals). Moreover the control of remote generators and distributors will be performed by "branch controllers" housed in the system mainframe.

The mainframe will be available in three different versions, namely:
- a laboratory version with 6 slots;
- a fully equipped experiment version with 16 slots;
- a low cost experiment version with 16 slots.

The remote control and monitoring of all operational parameters of the High Voltage system is possible via the CAEN traditional built-in links (RS232, H.S. CAENET), via CERN approved Fieldbuses and via Ethernet (TCP/IP). Multimaster data handling and control is foreseen. The User interface encompasses all the usual friendliness of previous CAEN systems. The use of one microprocessor per slot allows fast and accurate setting/monitoring of channel parameters (14 bit resolution on Voltages and Currents). Moreover, each "branch controller" allows to control and monitor up to 1024 parameters of the peripherals.

The system employs modularity criteria: the internal power supply allows different configurations up to 2250 Watts per mainframe. Live insertion of the boards is also available, thus reducing the down time of the global system.

The huge LHC experiments will introduce several problems with the maintenance of the detector electronics: the new system has been designed in order to gain an easy access to the computing core and peripherals. Telnet and WWW access facilities will allow remote debugging and technical support of the system.
Abstract
The high voltage generation and distribution system for the Atlas MDT chambers is described. A high modularity together with a high reliability is required to supply a detector with a large number of tubes (about 370000) for at least 10 years at LHC. Furthermore the capability to reverse the high voltage to cure aged tubes and to disconnect tubes with broken wires (using a fuse per tube) must be foreseen. The layout of the system proposed is based on three main components: the main high voltage generator; the boards for remote regulation, monitor and limiting of tension and current; the hedgehog cards for the distribution of the high voltage to each single MDT tube.

1. INTRODUCTION
The high voltage system for the Monitored Drift Tube (MDT) chambers has to be able to supply the 1200 chambers of the Atlas muon spectrometer.

The MDT chambers perform the precision coordinate measurement in the bending direction of the spectrometer, providing the momentum measurement. A safe and stable operation for 10 years in the high rate environment has to be guarantee.

A MDT chamber is made of two multilayers of high-pressure drift tubes assembled on a support frame. Each multilayer is composed of three or four layers (depending on the chamber) of closely spaced tubes. The number of tubes per layer ranges from 24 to 72 and their length from 1 to 6 m.

In order to achieve a stable space-time relation [1] an overall high voltage accuracy and stability less then 0.3% is required, together with a maximum operating voltage of 4 kV. Moreover, because of the large number of channels involved a high modularity is required; as a consequence the system has to be able to work properly also in case of tubes with broken wires. Lastly the capability to supply MDTs using high voltage with reversed polarity must be foreseen (this point is useful to cure aged tubes).

A crucial point for the HV power supply design is the maximum current that the system has to supply. For MDT chambers this value can be calculated according to the amount of integrated charge for 10 years at the nominal working conditions; this calculation gives an average dragged current of about 1.5 mA for the biggest chamber.

The proposed solution for the MDTs HV generation and distribution is composed of three parts:

- The Main Control System located in the underground counting room USA15;
- The REgulation MOonitoring LImiting (RE.MO.LI.) boards located on racks around the apparatus (these cards are managed by the HV generation boards housed in the Main Control System);
- The Hedgehog cards located inside the faraday cage.

In the following sections the main characteristics of each part are reported.
2. MAIN CONTROL SYSTEM

The operation of the entire MDT high voltage system is carried out by the Main Control System, located in the control room USA15, that generates the high voltage and manages communications and controls.

A modular high voltage system is realised in order to host up the high density HV generation boards and to support the hardware and software communication. For the ATLAS spectrometer each HV generation board hosted in the system has to be provided with a local processor and 10 HV outputs to manage and supply RE.MO.LI. boards (see the following section). RE.MO.LI. board controls can be carried out either by an optical or an electrical line (in this case an optocoupler will be used to avoid ground loop [2]).

One main HV channel is foreseen to supply three chambers, so 40 HV generation boards housed in three crates localised in the USA15 control room will supply the full detector (about 1200 chambers). A block diagram of the whole system is shown in fig.1.

3. RE.MO.LI. BOARDS

These boards, located in racks around the apparatus, have been designed to provide the REgulation, MOntoring and Limiting of tension and current.

The single board (fig.2) is made of two identical sub-systems. Each sub-system supplies three chambers by means of six linear regulators individually adjustable from 0 to 4 kV.

Both tension and current of these channels are monitored; the current limit for each channel is hardware set to 0.7 mA. About 200 boards, located on racks around the apparatus, will be used to supply all MDT chambers.

A local controller, that communicates with the Main Control System through an optical line, manages the sub-system operations. The HV line that supplies each sub-system is also used to blow the fuse (in case of MDT with broken wire) and to cure aged tubes. A network made of passive components is used for the connection between the chamber and the RE.MO.LI. board ground in order to avoid ground loop.
HV RE.MO.LI. BOARD

Fig. 2 High voltage distribution board (RE.MO.LI. board)

HEDGEHOG

Fig. 3 Hedgehog card
4. HEDGEHOG CARDS

These cards are connected directly to the tube endplugs and are used to distribute high voltage to the single MDT tube. A Faraday cage encloses all cards that are used to supply a chamber multilayer; three HV cables have to be connected for each chamber (two cables to supply HV to multilayers and one cable to bring out the diodes common cathode line for blowing fuse or MDT curing option purpose). The broken wire. This current blows the fuse, disconnecting the relative tube.

5. Curing option

In this case (see Fuse Blow option) the high voltage cable relative to the chamber to be cured, has to be disconnected from the main HV generator and connected to a negative high voltage power supply. This generator has to provide an adjustable high voltage from 0 to 3 kV and a maximum current of 30 mA. Both current and tension can be monitored. The diodes polarization, during the curing option, is the same of the Fuse Blow option, while the maximum dragged current is limited to 30 mA.

6. CONCLUSION

The proposed system satisfies all the ATLAS muon spectrometer requirements, providing a safe and stable operation for MDT chambers. During the normal operation, the system is completely controlled by the Detector Control System (DCS). Manual operation is required only few times to disconnect the main generator for the fuse/curing option (remote control of this operation is possible, but too expensive, so at the moment, it is not foreseen).

7. REFERENCES

[3] P.Mockett, Design and Test Results for a Proposed MDT Fuse System, ATLAS internal note MUON-NO-228
POSTERS
READOUT AND PRETRIGGER LOGIC OF THE HERA-B HIGH-P_T PRETRIGGER.

Vladimir Popov (HERA-B Collaboration)
Email: vladimir.popov@desy.de
Institute for Theoretical and Experimental Physics, Moscow, Russia

Abstract
The high-p_T pretrigger has been proposed for HERA-B experiment. Dedicated pretrigger logic is needed for selection events out of data streams coming with typical rate of few 10^{12} hits/s. The paper describes concept of pretrigger logic and data processing which provide necessary speed and flexibility for pretrigger selection criteria.

1 Introduction
The high-p_T trigger provides HERA-B experiment with ability to measure CKM unitarily triangle angles \( \alpha \) and \( \gamma \) by detection of the \( B \rightarrow \pi^+\pi^- \) and \( B \rightarrow K^\pm \pi^\mp \) decays [1]. The expected numbers of reconstructed events are 500 and 750 per year correspondingly. The goal of the high-p_T pretrigger is selection of candidates for particles with the large transverse momentum to initiate the First Level Trigger (FLT) tracks finding process. The high-p_T pretrigger is organized using approximately 19000 pads of different sizes distributed among three layers of chambers located in the magnet. There is a projectivity between position and sizes of correspondent pads in three layers with respect to the vertex position. Pads’ sizes are varying in correspondence with their distance from the beam. The basic track selection algorithm of the high-p_T pretrigger is: each pad of the first chamber layer (PT1) maps to three adjacent pads in the second layer PT2, and each pads of the PT2 maps to two adjacent pads of the PT3 (fig.1). The tracks with high-p_T produce signals in the projective or adjacent pads of three chamber layers. Specific pretrigger logic must provide selection and encoding events and distribution the parameters of few 10^7 tracks out of few 10^{12} possible roads per second.

2 Pretrigger implementation
The main components of the high-p_T pretrigger system are three layers of gaseous pad chambers placed in the magnet, on-chamber front-end electronics, front-end drivers and pretrigger logic. The outer region of detecting layers is covered by straw tube chambers with cathode pad readout. These chambers are developed at Princeton University, Cincinnati [2]. The inner region is covered by gas pads of different sizes assembled in gas pixel chambers developed in ITEP, Moscow [3].

Detailed description of readout and pretrigger logic is given in [5]. The pad signals are routed from the chambers to front-end cards mounted at both sides of the chamber stations’ frames outside the detector fiducial volume. It is done by using low-mass flex cables which have been specially developed for that.

Front-End Driver (FED) fulfills the tasks of interface for FE output signals both to the data acquisition system (DAQ) and to the pretrigger logic, and either synchronization function – labels passing data with timing information (bunch crossing number). It is placed close to the detector. Data are being transmitted from FEDs to the pretrigger logic located outside the HERA-B detector area via optical lines.
Every bunch crossing chamber's data together with
timing information are being transferred to the pretrig-
ner logic. The main task of the pretrigger logic is to
define track candidates by performing coincidences of
pads' signals with required topology and transforming
the result into streams of initial track parameters com-
ing to the appropriate FLT processors. This task is be-
ing carried out in real-time with short delay. Informa-
tion from chambers is being accepted synchronously
with the HERA clock (10.4 MHz), the track param-
eters are being transmitted to FLT processors at a
typical rate of 40 MHz. Some additional facilities to
provide monitoring and testing functions, are imple-
mented either.

3 Readout

The geometry of readout signals from pads to the
front-end cards is horizontal. Such geometry has been
chosen due to two main reasons: to minimize the num-
er of overlapping hits (the hits which involved in coin-
cidence procedures in different boards of the pretrig-
ner logic) and due to arrangement of pads in vertical di-
rection more regular than in horizontal. The ASD8B
chip is used in FE cards[4]. It has 8 amplifier-shaper-
discriminator channels.

Every bunch crossing each FED reads in syn-
chronously 1024 hit signals coming from FE cards.
These data stream are being fan-outed in two paths: trans-
smitted to the pretrigger logic and loaded to
pipeline memory to be output then to the DAQ in
accordance with the FLT request. To reduce the num-
ber of transmission lines data are being transfered in
serial form via high-speed optical link lines. Reduc-
tion factor is approximately 42. To transfer hits out
of 19000 pads to the pretrigger logic 480 optical links
are used. Fast link chips MC100SX1451 (Motorola)
transmit data in serial form with the speed which al-

tows to transfer two 32-bit words per bunch crossing.

4 Pretrigger Logic

Main tasks of the pretrigger logic are:

1. Receive streams of logical signals from front-end
drivers and select data which match to the pretrigger
track selection criteria.

2. Translate selected data into streams of track’s
parameters (messages).

3. Distribute messages among appropriate FLT pro-
cessors in accordance with their regions of interest.

Besides, pretrigger logic must provide ability for
monitoring its performances and performances of in-
put data, and either provide ability for updating of
constant in order to cope with unexpectable operat-
ing conditions.

Essential requirement is flexibility for coincidence
algorithm to provide ability for further optimization
of the pretrigger.

Figure 2: Schematic view of data processing on a pre-
trigger board. Coincidence trees n1 and n3 have at
least one hits' combination which matches to the pre-
trigger algorithm, while patterns n2 and n4 have no
one.

The following concept and data processing algo-

rithm are put into development of pretrigger logic [5].
The pretrigger logic electronics has sectional structure
and is composed of boards of two types - the Pretrig-
ner Boards and the Master Cards. Each section con-
ists of one master card and a number of pretrigger
boards. Two processes run asynchronously in each sec-
tion: filtering and serialization procedure at pretrigger
boards, and serialization-encoding process at the mas-
ter card. Output of the first process is the input for
the second one. A pretrigger board executes filter pro-
cedure for raw data and diminishes output data rate
to acceptable level. A pretrigger board serves com-
plete rows of pads of three chamber layers. It receives
data from six half-layers of chambers and tests them
for coincidence. Data which match to the pretrigger
algorithm are stored for necessary time, data items are
being extracted from stored data and transmitted in
special format to the master card. The master card
acquires data items from a group of pretrigger boards,
transforms them into a number of messages and dis-
tributes messages among FLT processors.

Average rate of messages generated by a master card
can not be more than one track candidate per bunch
crossing. This restriction determines maximal num-
ber of pretrigger boards served by one master card.
According to the above restriction and the results of
Figure 3: Schematic of a Pretrigger Board.

MC simulation of the pretrigger rate distribution over the detection area the pretrigger logic has been divided into independent sections with one master card in each.

Schematic view of data processing at a pretrigger board is shown at fig.2. Data are being processed in items of 'coincidence trees'(CTs). This term means a set of pads involved in the coincidence procedure together with one pad of the first layer. For the basic pretrigger algorithm (fig.1) a CT consists of eight pads - 1, 3 and 4 pads of the 1st, 2nd and 3rd layers correspondingly. The position of fired pad in the 1st layer defines a point of track, the combination of fired pads in the 2nd and 3rd layers are used to determine the direction of track(s). CTs are being encoded at pretrigger boards in the following way - root hit obtains its individual number and the rest seven bits remain as they are. The stream of CTs is being sent to the master card. One or more track roads can be derived from a fired CT at a master card using more detailed algorithm.

4.1 Pretrigger board

The main tasks for a pretrigger board are the following:

Receive 3 streams of logical signals via optical link lines;

The first stage of data selection by performing the coincidence procedure;

Serialization of selected data into a stream of CT items.

Besides, the pretrigger board fulfills the following specific procedures:

Check of synchronization between the data streams coming from different FEDs;

Suppression data with pointed 'VETO-BX' numbers coming from other pretriggers;

Data overflow protection - limitation the number of fired CTs with the same BX# which are being sent to the master card;

Counting average rate of CTs.

The pretrigger board block scheme is shown at fig.3. The numbers given on the picture are related to case when pretrigger board serves 96-pad rows. Every 48 ns three data packs, consists of 96-bit string of chamber's hits and 9-bit timing information each, are coming into a board in serial form. They are being accepted by fast link receivers (MC100SX1451 by Motorola) and arranged into parallel form. Bit-strings are being latched, masked to suppress noisy channels and tested for coincidences. 96-bit string of PT1 is filtered in the following way (illustrated at fig.2). Those bits which match to the coincidence algorithm remain fired, the other bits are cleared. If there is at least one fired road in processed data then the following information are loaded into the FIFO: filtered bit-string of PT1, bit-strings of the PT2 and PT3 as they are, and timing code BXnC. The described procedure can be executed by 7 PLD chips of MACH4 family or 4 PLD chips CY-PRESS 7C388A. Two pipeline cycles are necessary to execute it.

BXnC code consists of 8 least significant bits of full Bunch crossing Number and the transmission Cycle bit. The last C-bit is necessary due to the following. Data are being taken from chambers into FEDs every bunch crossing - each 96ns. Two data transmission cycles can be done via optical links to the pretrigger logic during this time interval. C-bit is used as extension of BX# code to identify 1st and 2nd data transmission cycles. The BXnC codes received from chamber stations must be equal, and thus they are tested for equality. An error signal is generated in case of in-
The next procedure implemented at the pretrigger board is an extraction of the fired CTs from the selected data which are stored in the FIFO. Filtered PT1 hit-string is being loaded into priority encoder and tested to find fired bits. The positions of fired bits are consequently appeared at the output of encoder as 7-bit codes and used to retrieve 3 adjacent bits out of PT2 and 4 bits of PT3 bit-strings. This 7-bit code defines X-position (in the row) while board number together with transmission Cycle bit of BXnC code define Y-position (row) of fired pad in the PT1. These codes together with BXnC code are loaded into the output register to be read by the master card. The time needed for deriving one fired CT in this way is about 96 ns (one bunch crossing time). This time is short enough in respect to the average number of tracks which pass through one row of pads per bunch crossing. This number is expected to be less than 0.1 per bunch crossing and no pile-up is expected at pretrigger boards.

Output data overflow protection is implemented in a pretrigger board. The 'Multiplicity counter' counts fired CTs in the same event. It stops the CT finding procedure in case of this number exceeds the limit.

External 'VETO' signal represents the BX# of HERA-B event which must be rejected. In order to monitor the average rate of CTs generated by the pretrigger board, the 'Events counter' is used.

**Figure 4: Schematic of a Master Card.**

4.2 **Master Card**

A Master Card completes the pretrigger logic process and provides communication between group of pretrigger boards and appropriate FLT processors. It executes the following procedures:

- Acquires data out of pretrigger boards;
- Completes the serialization procedure - extracts roads out of the CTs using optimized algorithm;
- Converts road's code into a set of track parameters;
- Transmits messages to the appropriate FLT processors;
- Distributes VETO-BX# among pretrigger boards;
- Limits the number of track candidates with the same BX# is being sent to the FLT (overflow protection);
- Besides, some additional facilities are foreseen at a master card:
  - Storage of acquired data for necessary time and transmission of data selected by the FLT to the DAQ;
  - Counting of track candidates.

Optimization of roads finding procedure means minimization the number of roads in fired CT which has several neighbour fired pads (see fig.2, CT #n1).

A master card consists of three parts (fig.4) working asynchronously. The first one ('Controller') acquires data out of pretrigger boards via the bus and loads data to the FIFO and DPM in parallel. 'Multiplicity RAM' counts CTs with the same BX#. It blocks FIFO input in case of overload. The 'Veto BX#' from other subdetectors can be easily implemented at a master card.
The 'messages generation' part defines roads in CT, converts them into tracks parameters and distributes messages among appropriate FLT processors. The row and pad numbers coming from pretrigger boards determine Y and X positions of track in the PT1 plane. The symmetry of chamber layers with respect to horizontal axis allows to reduce the addressing space of the Look-Up-Table (LUT) for one bit. Only 5 last bits out of 6 of Y-code are connected to the address inputs of the LUT (Look-Up Table). The 'Serializer' consequently derives roads from CT and generates road codes (RCs). According to the HERA-B FLT message format LUT transforms X, Y and RC codes into 45-bit code which includes initial track parameters. Some parameters in 80-bit message are constant and are being taken from register 'Const'. The 'Message transmitter' divides 80-bit message into four 20-bit words and transmits them to FLT processors.

The third part of a master card provides communication with the DAQ. Dual Ports Memory (DPM) realizes pipeline function, it keeps acquired data during 256 bunch crossings. BX# determines the data location in memory - both for loading data into and for reading data out in accordance with FLT request.

### 4.3 Flexibility, testability

The pretrigger logic is implemented in VME standard. Initialization procedure must be done to provide functionality of the pretrigger logic. Initialization of a pretrigger board includes loading mask codes into the PLDs and setting some other necessary codes. The Look-Up Table and some registers on a master card are to be initialized either. Reinitialization can be done at any time to update parameters.

There is either a facility to change coincidence algorithm by reprogramming PLDs at pretrigger boards and master cards. It allows to change basic coincidence scheme 1-3-2 to 1-4-2 or 1-5-2.

Facilities to test the pretrigger logic via VME bus are foreseen. Test data can be loaded into coincidence PLDs on a pretrigger board, the results of data processing can be retrieve out of FIFOs both at the pretrigger board and the master card.

### 4.4 Prototype

The first prototype of the pretrigger logic section has been designed and is being tested in Hamburg University. The pretrigger logic latency is 0.5 μs. In physics run '98 complete test of the prototype with real data is planned to check its performances and study high-pT pretrigger.

### References


V. Popov, HERA-B note 96-239.
Design of a High Performance, Low Noise Charge Preamplifier with DC Coupling to Particle Silicon Detectors in CMOS Technology

Y. HU* and R. TURCHETTA
LEPSI IN2P3/ULP
23, rue du Loess
67037 Strasbourg Cedex, France

* corresponding author E-mail: hu@lepsi.in2p3.fr
tel: 33 3 88 77 75 17 fax: 33 3 88 28 34 85

Abstract: In this paper, a low noise, low power CMOS charge preamplifier with DC coupling to silicon radiation detectors has been designed. Simulation results show that the detector leakage current can be compensated up to 8 µA. The proposed charge amplifier has been simulated and implemented with a CMOS SOI process. An input referred ENC of 1265 electrons (rms) for a detector capacitor of 10 pF and a DC leakage current of 5 µA, a conversion gain of 2.86 mV/fC with 0.66 mW power consumption have been obtained.

Introduction
Charge amplifiers with low noise and high speed characteristics are key components in most frontends such as pixel sensor amplifiers and preamplifiers for radiation detectors. It is also an active approach for silicon microstrip detector frontends in high energy physics experiments [1-2]. Frontend electronics for the readout of silicon detectors can be AC coupled or DC coupled to detectors. The AC coupling technique is widely used for the readout of silicon detector in which the coupling capacitors and bias resistors are integrated on the detectors. However, such AC coupled silicon microstrip detectors are more complex and expensive in fabrication than simple DC coupled silicon detectors. On the other hand, the leakage current coming from the detectors can be quite high, especially after irradiation, and can cause saturation at a standard charge preamplifier. Several approaches for readout frontend with DC coupling to detectors have been reported in the literature [3-5]. In [3-4], the authors present a pulse charge amplifier in which a high DC current can be compensated. But the noise output is relatively high because a pair of common gate topology for input transistors is used. Another architecture is proposed in [5] in which the DC current compensation range is small (a few hundreds of nA). In this paper, a new design of a high performance, low noise charge preamplifier which allows DC coupling to silicon detectors is described.

Circuit description
The schematic of this amplifier is presented in Figure 1. In the circuit, the charge amplifier is composed of the transistors M1-M6 and capacitor CF. In order to compensate DC leakage current of silicon detectors, the transistors MC1-MC7 are used to provide correct DC bias voltage in the charge amplifier.

The charge amplifier architecture is a single ended folded cascode structure buffered by a source follower because of its high DC gain, large frequency bandwidth and good noise performance. In this amplifier, the DC operating point of the high impedance output (the drain of
transistor M3) is set by means of the differential pair MC1 and MC2 with an exterior control voltage VFC. The DC leakage current can be absorbed by a CMOS current source MC3. Two feedback paths can be found in this amplifier. The first is realized by the transistors MC1, MC2 and the capacitor CF which time constant is \( \tau_1 = CF/g_{mc2} \). The second feedback path is the transistor MC3 and the capacitor C1 via the drain of transistor MC2 in which the time constant is written by \( \tau_2 = C1/g_{mc3} \). In order to ensure a correct damping ratio for step response (phase in domain) in feedback loop, the stability criterion is given by

\[
\frac{C1}{g_{mc3}} > \frac{2CF}{g_{mc2}}
\]  

(1)

**Noise Analysis**

Total noise contribution of the amplifier is mainly determined by the input transistor M1. The choice of the input transistor as well as its bias current are very important. Normally, the noise performance of the input transistor is fully characterized by an equivalent input noise voltage source \( V_e \) with noise spectral density:

\[
S_v(e)(f) = \frac{8K_T}{3g_{m1}} + \frac{K_f}{C_{ox}W_JL_J} f
\]  

(2)

where \( g_{m1} \) is the transconductance of the input transistor, \( C_{ox} \) the oxide capacitance per unit area and \( K_f \) the ficker noise coefficient. In order to minimize the total noise, a PMOS device has been chosen due to its lower ficker noise compared to the corresponding NMOS one. The highest possible \( g_{m1} \) has been selected bearing in mind the power consumption constraint.

Even if the input transistor is the main device tuning the noise, the contribution of the other transistors can not be completely neglected, especially for the compensation circuit (MC1-MC7). Usually, the bias current \( I_{bias2} \) of the differential pair MC1 and MC2 can be made very small (a few nA) and therefore their noise contribution can be neglected. But the noise for the transistor MC3 is important because of its strong bias current (\( I_{bias} + I_{bias2}/2 \)). The output noise spectral density of the current source MC3 is \( 4kT(\frac{2}{3}g_{mc3}) \) when it works in strong inversion. Then the minimum noise is achieved for the minimum transconductance \( g_{mc3} \).

In our design, the minimal transistor gate width \( W_{mc3} \) is limited by the CMOS process used. One efficient possibility to reduce the transconductance \( g_{mc3} \) is to increase of the gate length \( L_{mc3} \). From the drain current given in formula (3)

\[
I_{ds} = \frac{K_n W_{mc3}^2}{L_{mc3}} (V_{gs} - V_T)^2
\]  

(3)

as the ratio \( W_{mc3}/L_{mc3} \) is small, a strong DC leakage current absorbed by the transistor MC3 leads to a high value for \( V_{gs} \). As a result, the charge amplifier does not work because the differential pair MC1 and MC2 is not biased in saturation region. An optimization design has been carried out to trade off between low noise behaviour and strong leakage current compensation.

**Simulation results**

In order to investigate the feasibility of the low noise charge preamplifier discussed above, a simulation has been performed with Cadence 4.3.3 using the SPICE MODEL parameters of the Process DMIll (Durci-Mixe sur Isolant Logico-Linéaire) developed by CEA, France. The main design parameters and characteristics of the amplifier is summarized in Table 1. The simulated transient response is presented in Figure 2 for an input current pulse corresponding to 24000 electrons (3.84 fC). From this figure, a conversion gain (charge-to-voltage gain) of 2.86 mV/fC and a rise time of 10 ns have been obtained. The output noise spectral density \( S_v(f) \) of the amplifier is shown in Figure 3. Total rms output noise voltage \( V_n \) total can be calculated by

\[
V_{n\text{total}}(\text{rms}) = \sqrt{\int S_v(f) df}
\]  

(4)
where \( \Delta f \) is the amplifier noise bandwidth. The typical value for a detector capacitor of 10 pF and a DC leakage current of 5 \( \mu A \) is 0.58 mV. Considering the conversion gain of 2.86 mV/fC taken from Figure 2, the input equivalent noise charge of 1265 electrons has been obtained. The DC leakage current can be compensated up to 8 \( \mu A \) without significant deterioration of the low noise charge preamplifier performances.

**Conclusion**

In this paper, a high performance charge preamplifier with DC coupling to silicon detectors is presented. The advantage of this amplifier is its low noise level, a high speed and a high gain with a very low power consumption. More important, this amplifier can be connected directly to silicon detectors due to its high DC leakage current compensation and can be widely used in particle physics and X ray detections.

**References:**

[1] Willy M. C. Sansen and Z. Chang
"Limits of Low Noise Performance of Detector Readout Front Ends in CMOS Technology"


[2] Suhali Tedja, Jan Van der Spiegel and Hugh H. Williams
"A CMOS Low-Noise and Low-Power Charge Sampling Integrated Circuit for Capacitive Detector/sensor Interfaces"

"ICON, A Current Mode Preamplifier in CMOS Technology for Use with High Rate Particle detectors"

"Current Mode Charge Pulse Amplifier in CMOS Technology for Use with Particle Detectors"
Electronics Letters, 14th March 1996, Vol.32, No.6, pp. 515-516

"Pixel Detectors with Local Intelligence: an IC Designer Point of View"

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>power supplies</td>
<td>vdd = +2 V, vss = -2 V</td>
</tr>
<tr>
<td>bias current of preamplifier</td>
<td>( I_{bias1} = 250 \mu A )</td>
</tr>
<tr>
<td>bias current of compensation circuit</td>
<td>( I_{bias2} = 10 \text{nA} )</td>
</tr>
<tr>
<td>input transistor (M1) dimension</td>
<td>( W/L = 1500 \mu m/1.2 \mu m )</td>
</tr>
<tr>
<td>compensation transistor (MC3) dimension</td>
<td>( W/L = 2.2 \mu m/25 \mu m )</td>
</tr>
<tr>
<td>feedback capacitor</td>
<td>( CF = 0.35 \text{pF} )</td>
</tr>
<tr>
<td>compensation capacitor</td>
<td>( C1 = 2 \text{pF} )</td>
</tr>
<tr>
<td>compensation range of DC leakage current</td>
<td>up to 8 ( \mu A )</td>
</tr>
<tr>
<td>input signal-to-noise ratio</td>
<td>( S/N = 25.5 \text{dB} )</td>
</tr>
<tr>
<td>power consumption</td>
<td>( PD = 0.66 \text{mW} )</td>
</tr>
</tbody>
</table>

Table 1: Main design parameters and characteristics
Figure 1: Schematic of the amplifier

DC current compensation circuits
charge amplifier
bias circuits

Figure 2: Simulated transient response

Figure 3: Output noise spectral density

Transient Response

Noise [$V^2$/Hz]

- Voltage output in Volt
- Output noise spectral density $S_{vn}(f)$

(time $t$ in second)

(freq in Hz)
A 16-channel Digital TDC Chip with internal Buffering and Selective Readout

LPNHE, Universités Paris 6 et 7, T33 RC, 4 place Jussieu, 75252 Paris, France
Zhang Bo
University of Alberta, Edmonton, Canada
October 9, 1998

Abstract

A 16-channel digital TDC chip has been built for the DIRC Cerenkov counter of the BaBar experiment at the SLAC B-factory (Stanford, USA). The binning is 0.5 ns and the full-scale 32 microseconds. The data driven architecture integrates channel buffering and selective readout of data falling within a programmable time window. The linearity is better than 100 ps rms on 90% of the production parts.

1 Introduction

The Front-End electronics of the Detector of Internally Reflected Cerenkov light (DIRC) for the BaBar experiment is presented. Its aim is to measure to better than 1ns the arrival time of Cerenkov photoelectrons, detected in a 11,000 phototubes array and their amplitude spectra. It mainly comprises 64-channel DIRC Front-End Boards (DFB) equipped with eight full-custom Analog Chips performing zero-cross discrimination with 2 mV threshold and pulse shaping, four full-custom Digital TDC chips for timing measurements with 500 ps binning and a readout logic selecting hits in the trigger window, and DIRC Crate Controller cards (DCC) serializing the data collected from up to 16 DFBS onto a 1.2 Gb/s optical link. Extensive test results of the pre-production chips will be presented, as well as the system tests results.

2 Context

2.1 The DIRC in the BaBar experiment
The Detector of Internally Reflected Cerenkov light (DIRC) sub-system of the BaBar Detector [1] is intended to provide particle identification, particularly separate π and K mesons to better than three sigmas for momenta between 0.15 and 4 GeV/c. Cerenkov photons are internally reflected in 144 quartz bars towards 10,752 photomultiplier tubes (PMT). A water tank is used as leverage between the quartz bars ends and the photomultipliers. The Cerenkov angles are deduced from the pattern created on the PMT wall. The momentum is measured in the BaBar Drift Chamber. The noise in the DIRC due to the PMTs themselves is estimated to 1 kHz, the PEP II machine noise is estimated to 30 kHz including a safety factor of ten; for an average bb event, 5.7 primary tracks hit the DIRC and produce each 33 photoelectrons to which must be added six extra hits from background generated by these tracks. An equivalent number of background photons of the order of 200 is generated by secondary interactions between the event tracks and the detector (mostly Compton scattering in the quartz). Therefore, photomultipliers with a 1ns time resolution have been chosen, that the Front-End electronics should not degrade significantly.

The Level 1 (L1) trigger is built from Drift Chamber, Calorimeter, and Muons Detector primitives. Its latency is 12 μs, with an uncertainty of one microsecond. Raw data are stored locally in the TDC chips during the L1 late ncy. A local selection in this chip is furthermore performed so that only data in time with the one microsecond trigger window are sent to the DAQ system after reception of the L1 trigger.

2.1.1 The photodetectors and their signal
The photodetectors are fast PMTs with single photoelectron resolution. Typical timing resolution is 0.7 ns. The typical gain is $1.25 \times 10^7$ using high voltages
between 900 and 1400 V, with a single photo-electron peak to noise ratio of 2.1. Using a threshold of 10% of the single photoelectron response, (2 mV on 50 Ohms) the rate is found less than 100 Hz.

2.1.2 Trigger and Data acquisition

The noise in the DIRC due to the PMTs themselves is estimated to 1 kHz, the PEP II machine noise is estimated to 30 kHz including a safety factor of ten; for an average b̄b̄ event, 5.7 primary tracks hit the DIRC and produce each 33 photoelectrons to which must be added six extra hits from background generated by these tracks. An equivalent number of background photons of the order of 200 is generated by secondary interactions between the event tracks and the detector (mostly Compton scattering in the quartz). The Level 1 (L1) trigger is built from Drift Chamber, Calorimeter, and Muons Detector primitives. Its latency is 12 μs, with an uncertainty of one microsecond. Raw data are stored locally in the TDC chips during the L1 trigger latency. A local selection in this chip is furthermore performed so that only data in time within a one microsecond window around the trigger are sent to the Data Acquisition System. This data driven scheme avoids the buffering of a huge amount of data in the Readout modules: the dataflow from the Front-end to the Readout modules is reduced by a factor of ten, according to the current estimations of the background noise.

2.2 The TDC requirements

The DIRC TDC chip integrates the following functions and features:

- 0.5 ns binning with 250 ps rms precision.
- 32 μs full-scale.
- 32 ns double-hit resolution.
- 59.5 MHz reference clock.
- Simultaneous Read and Write operations.
- Maximum rates:
  - Single channel rate = 10 times nominal background: 100 kHz
  - Maximum random rate on 16 channels simultaneously: 10 kHz
- Selection of data within a programmable time window available at any time for readout.
  - latency from 64 ns to 16 μs (eight bits).
  - window size from 64 ns to 2 μs (five bits).
- Bit pattern flagging the overloads during the trigger window.
- Channel disabling of the noisy channels between 500 kHz to 8 MHz
- Power should be under 200 mW at 100 kHz average input rate.

2.3 The TDC within the DIRC Front-end Electronics

The DIRC digital TDC chip is a building block of the DIRC Front-end electronics. It receives 16 outputs from two 8-channel zero-crossing discriminators timed with the single photo-electrons responses of the DIRC detector PMTs. On any Level 1 trigger (L1) occurrence, digitized time data associated to this trigger are transferred to a Multi-Event Buffer (MEB) and stay until a readout request (Readout Strobe) originated in the central control and timing system occurs.

3 TDC Implementation

A block diagram of the chip is shown Figure 1. Within a 59.5 MHz input clock period, a fine time measurement on 5 bits is achieved using voltage-controlled digital delay lines synchronized on the clock period using a calibration channel generating a reference voltage, to compensate for temperatures, supplies, and process delays variations. This calibration is fully transparent to the TDC operations.

A synchronous counter covers the 11 higher order bits.

In order to allow data-driven operations and asynchronous readout occurring at any trigger time during BaBar runs, sixteen dual port FIFOs allow data to be written from the TDC section.

Three level of buffering in FIFO memories allow to sort data in time with an incoming trigger, and make them available for readout. This feature allow to reduce by a factor of 10 the amount of data to be read from the DIRC detector. Each FIFO overload or
channel disabling during a trigger window is reported at the end of each data block as a sixteen bit pattern.

A maximum average channel input rate of 600 kHz is accepted, as far as there are less than 4 input hits on the same channel within a window of one microsecond, and less than 96 inputs on any of the 16 channels within one trigger latency. Input double pulse resolution is 32 ns.

The chip is manufactured by ES2, using a 0.8 microns CMOS process.

3.1 Time measurement

3.1.1 The time measuring channel

The TDC section integrates one 60 MHz counter, 16 digital delay lines with 32 taps of 500 ps delay each, a calibration channel made of a delay line identical to the measuring channel, locked on the clock using two analog controls stored in the gate capacitors of nMOS transistors controlling the delays of the 32 identical stages, and a time offset.

These analog controls are common to all channels, assuming a good process uniformity within the chip. The uniformity had been measured on previous TDC chips designs using the same technology. [2] [3]

An incoming signal latches the counter state in a 11-bit register. It is also propagated through the delay line. The next clock positive edge latches the state of the delay line in a 32-bit register, the result being binary encoded to five bits. Extra cells on each side of the delay line allow to lock the total delay and offset on the clock period.

The delay lines, the synchronization mechanism between the clock and the time inputs, the 60 MHz counter, the charge pump used as phase feedback have been implemented as full-custom designs, simulated with SPICE, before and after layout.

3.1.2 Phase locking

A state machine sequences the calibration process, sending clock pulses as inputs, tuning the channel to give back zero and full-scale digitizations alternately. This process is basically convergent, and no loss of lock can be observed. Therefore, it is not monitored. Calibration is internally activated at a 1 MHz frequency.

3.2 Layout

The layout has been done using a symbolic editor, drawing the transistors from a stick representation, using the Silicon manufacturer design rules. A compact layout is obtained, allowing to draw the sixteen time channels, the 60 MHz counter, the channel FIFO within half the chip area.

The latency and output FIFOs have been provided by the manufacturer. The associated counters and logic are merged into the standard cells generated by the Synopsys compiler from Verilog hardware descriptions. A post layout simulation has checked the design using the safety margins recommended by the manufacturer.

3.3 Selective Readout

3.3.1 Overview

A block diagram of the selective readout is shown Fig. 3. The TDC section is sensitive to any positive edge applied to the inputs. Datum is stored for one μs at more in a four-deep channel FIFO. There is one FIFO for each channel, they are emptied by a continuous read process at 30 MHz, that extracts the oldest datum among the sixteen channel FIFOs outputs (actually the oldest from each FIFO), and transfers it to a 32 deep latency FIFO (FIFO!), shared by all channels, where it stays until the minimum L1 latency.
It is then transferred to a 32 deep FIFO where it stays until the maximum trigger latency (latency plus half the resolution). During that stage, a L1 accept is followed by a readout command that empties this FIFO and outputs a data packet whose header is the L1 accept time (on 11 bits), followed by the time words ordered by 32 ns slices, and terminated by a trailer flagging input FIFO overloads, or channels that have been self-disabled due to input overload. These informations have been buffered in a dedicated FIFO with the associated time, and processed in the same way as the time data during the selective readout process.

The readout process is sequenced at 30 MHz, and can be managed within the time before another L1 accept comes (1.5 μs). When data is readout, the selective readout process filling the output FIFO is still working. There is no deadtime associated.

3.3.2 Fast sort

The fast sort algorithm is based on a slicing in time windows. Within each of these time windows, data are compared using a binary tree shown Figure 4. From two adjacent channels, two bits from time words (bit 10 and 9) belonging to a window of 256 ns are input to eight comparators, the oldest data being compared again two by two, until the last. There are 128 time windows. Therefore, fifteen two-bit comparators are used. The width of 269 ns is fixed by the response time of the 18 ns response time. The tree returns the address of the oldest time data for transfer to the latency FIFO.

3.3.3 Latency and Output FIFO management

This section sends data from the Latency FIFO to the Output FIFO if they are in time with a just arriving trigger (Figure 4). The current time is first subtracted from the time data, if the result is more or equal to the sum of the latency and half the resolution, the time data is sent after the trigger latency minus half the trigger resolution to the Output FIFO, provided it is not full. If no trigger has come after the latency plus half the resolution, data is lost. The writing rate can be up to 1/32 ns at that stage.
3.4 Expected performance

These three levels of buffering have been implemented in order to cope with the required single channel rates of ten times the nominal background of 10 kHz per channel, and the simultaneous maximum random rate on 16 channels of 10 kHz. The transfer from each TDC section to each channel FIFO is immediate. With the same assumption for the transfer from the channel FIFO to the latency FIFO, the dead time can be estimated for a latency FIFO depth of 32 (Figures 5). FIFO depths of 4 and 32 have been implemented for the channel and the latency FIFO respectively, according to the simulation results, leading to a minimum dead time less than 0.1 % as required for input rates of 100 kHz.

4 Performance tests

4.1 Test bench

Test benches have been set up at each stage of the chip development. First versions were used for checking prototypes linearity and overall functionalities. The last test bench aimed to fully test the production parts within a few minutes. Tests were also performed on the Front-end cards of the DIRC with actual PMTs signals as inputs. The production test bench is shown Figure 6. It makes use of a Pentium PC, a LeCroy precision pulser 9210, and a dedicated printed circuit board housing a hardwired sequencer, digital interfaces to the PC and the chip socket.
4.2 Selective readout

The selective readout process has been checked by sending an input synchronous with the trigger window while a set of PMT generated random noise. A peak at a fixed position within the trigger window is found.

4.3 Linearity

The histogram of the bin widths has been built by sending random inputs. A typical result is shown Figure 8. On channel 14 and 15, the last bin has been found up to two times too wide for a few chips. This is understood as a process dependent layout effect introduced by parasitic components not taken into account in the simulation since the TDC sections have been replicated from channel to channel.

4.4 Monotonicity

A coarse counter slipping by one clock tick was observed on a few channels (3 over 896) when all channels are fired together at the same time. For the reason detailed above, the delay lines of some chips needed to be calibrated on 31 bins instead of 32. Then, the number of faulty channels is reduced to 0.3%. However, in both cases, the overall differential linearity remains less than 100 ps rms.

4.5 Dead time

A good agreement is found between simulated and measured deadtime, both for random events on the sixteen channels, and synchronous events (Figure 9).

4.6 Production for the DIRC

4.6.1 Acceptance criteria

All the chips have been successfully tested by the manufacturer using an 8k test-vector file. Over 1250 chips, 38 were not working properly due to faults in the analog sections, tested using an extra 10k test vectors not accepted by the manufacturer standard flow. As another selection criterion, it was decided to reject chips with a bin 31 larger than the others by 20%, or chips with bin 0 or/and 1 smaller by more than 60% than the average, having selected the best calibration scheme. 805 chips satisfied these criteria.
4.7 Test of the TDC chips on the DIRC Front-End Board.

56 chips from the preproduction set were mounted on 14 DFBs in order to read out one full DIRC sector (896 PMTs). This test bench has been operational at CEA Saclay since October 97 and is used to test the 12 DIRC sectors after the PMTs have been mounted and fully cabled. The PMTs were illuminated by one LED (LEDTRONIC BP280CW1K and both ADC and TDC spectra were recorded. In total, 805 chips satisfied the selection criteria.

4.7.1 Statistics

The distribution of the delay lines differential linearity was peaked at 35 ps when the chips were calibrated on 32 bins. As for preproduction chips, the tail towards high values was mainly due to channels 14 and 15 (i.e. channels far from the calibration line).

The average differential linearity on all chips and all channels in 73 ps. This corresponds to a time resolution of about 196 ps including the binning error.

5 Conclusion

This digital TDC chip is a building-block of the Front-End electronics for the Detector of Internally Reflected Cerenkov light of the BaBar experiment at SLAC (Stanford, USA). Twelve hundred parts have now been fabricated and tested with a very good yield. Resolution and input rate capabilities have been measured within the initial requirements. The readout of data within a programmable time window reduces by a factor of ten the amount of information to be read for the DIRC detector at BaBar.

References


Differential non-linearity compensation in ADC of binary weighted capacitances array type

V.V. Sushkov, present address: University of California Riverside, IGPP CA-92521, USA, tel: +1 (909) 787-3957 fax: +1 (909) 787-4509 E-mail: Sushkov@mail.ucr.edu

1. Introduction
Differential non-linearity (DNL) compensation technique has to be implemented in ADC of CRIAD [1] type to reach performance of that required in tracker of CMS detector at LHC. The technique used for non-linearity compensation in this type of ADC first was proposed in [2]. Later developments of this technique might ensure more rapid performance of the ADC. DNL is outlined as determined. The capacitors with the indices lower than k-th are connected in parallel and this block is connected in series to the reference source Vr (see fig.1). The larger capacitors starting from the k-th are connected to the ground from both sides. In the second stage of the calibration the k-th capacitor is connected to the reference source from the bottom side, while all the other capacitors are connected to the ground from the bottom side too (the connection of the top of the array to the ground is switched off). Due to the charge conservation in the capacitors array the following expression for the residual voltage $V_{rk}$ (potential difference between top of the array and ground) of k-th capacitor mismatch may be obtained:

$$V_{rk} = V_r (C_k - \sum_{i=1}^{k-1} C_i)$$  (1)

The count of the capacitances starts with 1A, because the array begins with two identical capacitors 1A, 1B. This expression shows that if the sum of the capacitances preceding the k-th is equal to the k-th capacitance value (ideal array of capacitors), then the residual voltage is zero. Arbitrary errors $\varepsilon_i$ of capacitance mismatch may be introduced in form:

$$C_i = 2^{i-1} C (1 + \varepsilon_i),$$  (2)

where $C$ represents the whole capacitance of an array divided by full-scale number of the ADC counts.
digitized error voltages are subtracted from natural error voltages; the residual of the above subtraction is a new error voltage, which is now to be used in determining of ADC transfer function. The correction potentials did not applied during the residual voltage determination, thus the residual voltages only store information about capacitance mismatch in non-ideal array of binary weighted capacitors. The techniques how to arrange this information storage, how to extract it and apply correction potentials may be instrumentally realized in different ways and will not be discussed here.

4. Simulation techniques
For an ideal array of binary weighted capacitors the values of each capacitance divided by the bit weight (thus normalized) are equal. The simulation method discussed is applicable to an arbitrary profile of variation of normalized capacitances. A constant gradient of normalized capacitances variation is the most important type of the variation [3] (which is also a first order approximation for the other types of variation). For a constant gradient of g value the ascending sequence of the capacitance values may be represented by:

$$C_i = 2^{i-N} C (1 + (i - 1) g)$$  \(8\)

When calculating the sum of the capacitance values of the array the error of i-th capacitor mismatch due to the gradient g may be found:

$$e_i = \frac{1 + (i - 1) g}{1 + (N - 2) g + g^{2^{i-N}} - 1}$$  \(9\)

More sophisticated errors are easily described in the same manner by polynomial representation of normalized capacitances profile. For the third order approximation the normalized capacitances profile is represented by:

$$C_i = 2^{i-N} C (1 + (i - 1) g_1 + (i - 1)^2 g_2 + (i - 1)^3 g_3)$$  \(10\)

This representation may be useful too, if one has more details about oxide layer variations, the coefficients g1, g2, g3 may be determined when fitting this profile (g1 equal to g for the first order approximation). The error of i-th capacitor mismatch in this case is represented by expression:

$$e_i = \frac{1 + (i - 1) g_1 + (i - 1)^2 g_2 + (i - 1)^3 g_3}{\text{SUM}} - 1,$$  \(11\)

where the expression for the SUM is as follows:

$$1 + g_0 (N - 2 + 2^{i-N}) + g_1 (N (N - 4) + 6 - 32^{i-N}) + g_2 (N (N (N - 6) + 18) + \text{26} (1 - 2^{i-N}))$$

DNL characterizes one bit analog value change associated with one digital count. DNL is usually represented as a result of subtraction of current analog value from a value corresponding to the bin center of digital count (see
corresponding plots in the following discussion). The displacements of the step borders from their perfect positions result in deviation of transfer function from ideal one, i.e. non-linearity. The positions of step borders in non-ideal transfer function are calculated in the developed program by scalar production of vectors formed by digital codes and vectors representing the bit weights, with coordinates:

\[ V_i = V_f \frac{2^i (1 + \epsilon_i)}{2^N}, \]  
(12)

the code vectors scan over the full conversion range of the ADC, the errors \( \epsilon_i \) may be determined by expressions (9), (11).

Rapid evaluation of DNL may be obtained with

\[ V_i = V_f \frac{2^i (1 + \epsilon_i)}{2^N}, \]  
(12)

conversion range. Fig.2 presents the variation in the number of counts due to different gradient values obtained with 8-bits main ADC. The density of the scan corresponds to 512 counts in each bin for an ideal array of binary weighted capacitors. Each remarkable pick at the histograms of the above figure corresponds to switching on the superior bit to 1 (and thus the larger capacitor of the array), while the preceding code was obtained by switching on all the preceding bits to 1. The above representation, when employed, is useful in the rapid DNL evaluation over the full conversion range and for the presentation of the compensation efficiency. Another important case is periodic structure in profile of normalized capacitance array (or texture, which may be analyzed with decomposition in periodic functions). Half

![Fig.2](image1)

![Fig.3](image2)

histogram representation, when the analog range of the converted amplitudes is scanned by the uniformly distributed amplitudes and the step borders of analog-to-digit transfer function being the bin borders for the histogram of digital counts. For an ideal transfer function the number of histogram counts of each digital code are equal, if the amplitudes are uniformly distributed over the sine profile is considered in the next example. The capacitance values here are represented by:

\[ C_i = 2^i C (1 + g \sin[\pi (i - 1)/N]) \]  
(13)

The corresponding to this profile DNL representation is shown in the lowest plot of fig.2 (g equal to 0.01).
The technique of DNL compensation implies cancellation of the error voltages \( V_{ei} \) by weighted sums of digitized residual voltages. However the number of bits compensated in the main ADC, the number of bits of the 5 bit supplementary DAC employed for compensation and the capacitance value used to introduce correcting potentials [2]) impose instrumental limits on the quality of compensation. The priority of error compensation for the larger capacitances (major bits) is evident from fig.2. Fig.3 show DNL compensation efficiency when different number of bits in the main ADC of 8 bit are compensated by 5 bit supplementary DAC with analog range of 1/40 of the range of main ADC, the original errors are caused by 1% gradient in binary weighted capacitors array. Excessive counts for the last code are due to the main ADC overflow (the analog range after non-linearity compensation is slightly reduced, while scan is done for the original analog range). In the simulator the number of bits being compensated in the main ADC is determined by the fact whether original error voltage or compensated error voltage is used in the determination of corresponding step borders of analog-to-digit transfer function.

The complexity of the instrumental realization of the compensation technique depends also on the bit number of supplementary DAC (or several DACs used for compensation). Fig.4 presents histograms showing the DNL compensation dependence on the bit number of supplementary DAC for a fixed number of bits compensated in the main ADC (in this figure DNL for all 8 bits of the main ADC is compensated). Histogram representation is very useful in DNL compensation analysis, however this representation can not show distinctively missing codes, which may appear for example for a sufficiently large negative gradient \( g \).

All the techniques employed in the simulator are in operation, but histogram representation will not be possible until missing code is eliminated. In this case a traditional representations of analog-to-digit transfer function and DNL may be helpful. These representations are also embedded in the simulator. During the scan of uniformly distributed amplitudes over the analog range the corresponding code is assigned in the program if the amplitude value is within the step borders interval of the code. The quality of transfer function representation and DNL representation depends on the density of the amplitudes in the scan. The DNL and transfer function representations in traditional method are shown in fig.5. Fig.5 (low) compares fragments of ideal transfer function with that simulated for 1% gradient in binary weighted capacitors mismatch (analog axis is calibrated in LSB units) the upper plot correspond to traditional DNL representation for the above two transfer functions.
5. Conclusion

Important instrumental limits are naturally recognised from parameterized modeling of DNL compensation technique employed in ADC of binary weighted capacitors type. The developed simulator significantly facilitates ADC designing for tracker where sufficient DNL compensation has to be reached with simplified schematics. It may also be useful in the development of high bit resolution system based on charge redistribution techniques.

7. Acknowledgments

This work was almost completed during short stay at CERN at winter 97-98. The first version of the simulator was built in HiQ programming language. I am grateful to P. Jarron and F. Anginolfi for their rapid introduction into the problems of code correction in charge redistribution technique and their friendly support of this work.

6. References

The modern experiments in elementary particles and nuclear physics demand increasingly sophisticated trigger systems.

Since the early 30s (Rossi's coincidence) the trigger systems have become more and more complex, operating at higher and higher speed and their development committed to a team of people.

Up to now, the design and construction of a trigger system has been based on the experience of its designers and its simulations always based on software programs code.

On the other hand, the transfer of know-how among the members responsible of trigger systems can become very difficult if based on pencil and paper and thousands of lines program code. Therefore an interactive graphical tool becomes an essential part of the trigger design process.

TASS is a simulation program with graphical and interactive interface, it reproduces in a realistic way the commercial Nim, Camac and Vme modules: both the front panel picture and the electrical and logical behaviors are simulated.

The user has access to any hardware and software characteristics like with real modules: he can move switches, push buttons, set Camac functions and so on.

TASS is a program embedded in Object Oriented environments and has been designed to run under Windows 95/NT.

TASS will be useful in different fields:

1. **to design and to document the trigger system in physics experiments.**

   This is the main TASS purpose. The trigger designer can gain a lot of help building his system in virtual environment. He can choose from the library the modules he needs, put them in the crates, do the connections and run the system in simulated way.

   The designer can set and tune in interactive way any parameter of each module. He can stimulate the system sending signals by a waveform generator and see in real time the result of any change using the virtual digital scope.

2. **to debug real trigger systems**

   TASS is extremely useful to identify a bad working module in an already running trigger system doing the cross check between the real set up and the simulated one.

3. **to evaluate the features of new home-made modules**

   The design of a new home-made module can be simpler if the environment where it will be insert has been simulated in advance. Good indications can arise and a better design can be done, avoiding bad surprises at installation time.

4. **to evaluate the dead time and the efficiencies**

   TASS has trace of delay and duration time of signals of any module, cables connection and so on. Stimulating the input with different patterns can be easily performed an evaluation of efficiency and hardware dead time.

5. **to save beam time for trigger set up and tuning**

   Most of beam time spent to tune the real system can be saved if any critical part has been simulated in advance. This can be extremely important in case of short beam allocation period.

6. **to test the Data acquisition program**

   TASS provides a full set of Esone routines. The writing and debug of DAQ program can be simulated gaining in efficiency and time.

7. **to teach the fundamentals of trigger systems**

   TASS offers to students and instructors the ability to quickly design and test a general purpose systems without any real available modules saving, therefore, a lot of time and money.
8. to understand how the modules work

Using mouse and keyboard the user can investigate the features of the modules without the request of expensive laboratory's tools.

- some other LeCroy and Cern
- several tool:
  - digital scope
  - wave generator
  - manual Camac crate controller

End of year foreseen the implementation of full set of Nim, Camac and Vme.

A demo package comprehensive of many samples is available, ready to download, on WWW at:

http://tass.roma1.infn.it
A Multichannel Gb/s Bit Error Rate Tester for the Evaluation of Front End Optical Read-out Link Solutions of the ATLAS Liquid Argon Calorimeter

B.Dinkespiler
Centre de Physique des Particules de Marseille, 163, avenue de Luminy, case 907, 13288 Marseille, France

M-L. Andrieux
Institut des Sciences Nucléaires, 53 Avenue des Martyrs, 38026 Grenoble, France

J. Lundquist, M. Pearce
Royal Institute of Technology (KTH), Physics Department Frescati, Frescativagen 24, 10405 Stockholm, Sweden

R. Stroynowski, J. Ye
Southern Methodist University, Department of Physics, Dallas, Texas 75275-0175, USA

Summary
In the baseline read-out scheme of the ATLAS liquid argon calorimeter, approximately 1600 unidirectional Gigabit/s (Gb/s) fibre-optic links are used to transfer data from the calorimeter front-end boards to data acquisition electronics situated up to 200 m away. The emitter end of the links must be radiation tolerant and the links as a whole must be highly reliable as they are not easily accessible during data taking. When designing, testing and qualifying links the bit error rate of the link is used as measure of the overall quality of the data-flow in the link. Bit error rate testers are available commercially for Gb/s links, but they are prohibitively expensive and only allow a single link to be analysed at a time. We have developed a tool which permits the analysis of up to 16 Gb/s links for a modest cost. At present it has mainly been used to evaluate the 'G-Link' chips-set (a pair of Gb/s serialiser and deserialiser chips manufactured by Helwett-Packard). It can, however, be used to test almost any transmission line where 32 bit words are sent using a 40 Mhz clock. A 32 bit pattern generator sends data into the link serialiser on the transmission board. The data received at the other end of the link is fed into a comparison board. The comparison board is also fed by the pattern generator, allowing errors to be detected through a simple comparison procedure. The modularity of the system means that configurations of between 1 to 16 links can be tested simultaneously. The entire system is overseen by a communication and error handling system which is PC driven and all errors are automatically logged.
LASER TECHNIQUE OF SINGLE EVENT LATCHUP THRESHOLD ESTIMATION
Specialized Electronic Systems
31 Kashirskoe shosse, Moscow, 115409 Russia, aichum@spels.msk.ru

Abstract

Radiation-induced latchup in various CMOS test structures was analyzed by software simulation. Correlation between single particle induced and dose rate latchup was found. Latchup experimental research was performed at laser wavelength of 1.06 μm and 0.53 μm, pulse duration of 10 ps and 10 ns, various locations of focused laser beam and spot sizes. The possibility of single event latchup threshold energy prediction based on the results of nanosecond uniform laser irradiation tests was analysed.

1. INTRODUCTION

Single event latchup (SEL) is one of the dominant failure effects of CMOS ICs under irradiation by high energy nuclear particles [1, 2]. The probability of single particle-induced latchup depends on SEL cross-section and threshold linear energy transfer (LET). Sometimes it is necessary to estimate only the fact whether there would be SEL in CMOS IC or not under certain radiation environment. In this case only threshold LET should be estimated.

SEL threshold prediction by software simulation requires taking into account various parasitic structure characteristics (gains of parasitic bipolar transistors, effective values of substrate and wells resistances, etc.), which are very difficult to identify. The estimation of SEL parameters using direct experimental approaches are rather complex and expensive. For examples, picosecond focused laser simulation tests for SEL latchup threshold evaluation of real IC is rather difficult because of interconnection metallization shadowing and necessity to scan the whole IC chip surface using various pulse laser energy for each laser beam location [3]. This approach can be successfully used for investigation of test structures.

The main issues of this work are to perform experimental research and software simulation of radiation-induced latchup in various CMOS test structures and to reveal latchup threshold dependencies on:

- irradiation pulse duration;
- location of ionized region and its dimensions;
- charge distribution in the ionized region;
- power supply voltage.

Computer simulation was performed using "DIODE-2D" software. Laser simulators with pico- and nanosecond laser pulse durations and relatively long (wavelength \( \lambda = 1.06 \mu m \)) and short (\( \lambda = 0.53 \mu m \)) laser energy absorption lengths were used for experimental research. The devices under test were special test structures and commercial CMOS RAMs.

2. COMPUTER SIMULATION

"DIODE-2D" software simulator was used for investigation of common SEL mechanisms under various ionization conditions.

Two dimensional 40 μm x 100 μm p-n-p-n structure was chosen for simulation. Schematic diagram of the test structure is presented in Fig.1. The lateral transistor’s base width \( W \) was 7 μm. The radiation influence was either uniform within the whole structure or local. In the latter case it was simulated with a narrow ionization strip.

Simulation of the test structure was performed under various conditions: location and size of ionization strip, power supply voltage, irradiation pulse duration and bulk or surface ionization along the strip. Bulk and surface ionization corresponds to laser irradiation wavelength of 1.06 μm and 0.53 μm respectively.

The software simulation results (Fig.2 and Fig.3) represent SEL threshold vs. ionization strip location and width as well as power supply voltage.

The position of the most sensitive to latchup region was determined as a function of ionization strip width in the simulated test structure (Fig.2) and correlates with experimental fact that the most sensitive region is located near well-substrate junction [1, 4]. Similar dependencies were also obtained for \( \lambda = 0.53 \mu m \) and for other base widths. The calculations were performed for twice larger separation distance between the well contact and the anode of parasitic structure. The results were found to be practically the same while the threshold energy values differ from initial ones for not more than 25%. It should
be noted that a charge funnelling effect is not essential because there is practically no difference of latchup threshold energy when laser beam crosses well-substrate p-n junction or is located near depletion region.

The calculated latchup thresholds under the local irradiation were performed for various conditions. The difference in latchup threshold energy for two wavelengths can be attributed to strong dependence of laser radiation absorption factor vs. wavelength: with the decrease of wavelength from 1.06 μm to 0.53 μm the absorption factor in Si increases from ~14 to ~7000 cm⁻¹. Consequently volume ionization distribution changes from practically uniform to that localized within the 1.4 μm from the chip surface. Thus for focused laser beam with λ=1.06 μm the latchup sensitivity can be characterized by LET threshold \( \frac{dE}{dx_{th}} \):

\[
d\frac{E}{dx_{th}} \approx \left( 1 - R_{1.06} \right) E_{1.06} \alpha_{1.06} (e_{1.06}/e_{1.06});
\]

while for focused laser irradiation with \( \lambda=0.53 \) μm - by total absorbed energy (or charge) threshold \( E_{th} \):

\[
E_{th} \approx \left( 1 - R_{0.53} \right) E_{0.53} (e_{0.53}/e_{0.53})
\]

Here \( E \) is laser energy, \( R \) is a reflection factor, \( e_i \) is an electron-hole generation energy (Si: 3.6 eV in Si), \( e \) is a photon energy, \( \alpha \) is a laser radiation absorption factor and "\( 1.06 \)", "\( 0.53 \)" indexes relate to the corresponding wavelengths.

The correspondence between latchup thresholds at various wavelengths and the dependence of laser energy on LET and absorbed energy in Si (expressions 1, 2) gives us the possibility to determine the latchup effective charge collection length \( L_{th} \):

\[
L_{th} = \frac{E_{th}}{(dE/dx_{th})} = 0.5 \left( \frac{E_{0.53}/E_{1.06}}{1/\alpha_{1.06}} \right)
\]

Estimation of \( L_{th} \) gives the value of about 13 μm for the simulated test structure. Taking into account the results shown in Fig. 2 and estimated value of \( L_{th} \) we conclude that the charge collection length is determined by both drift and diffusion processes.

Additionally, software simulation of the test structure showed that the latchup occurrence is determined by the pre-latchup power supply current value (Fig. 4) and is independent of charge generation conditions in the test structure sensitive volume. Therefore, non-focused laser irradiation can be applied for SEL threshold estimation.

The latchup triggering time for typical CMOS ICs is about 10 ns (that corresponds to the carrier collection length about 10 μm and more) due to relatively large switching delay of parasitic structure which depends on the inertial switching characteristics of parasitic transistors. Thus, any temporal ionization is assumed to be "instant" if its time duration is less than the mentioned value.
3. SEL THRESHOLD ESTIMATION

We have analyzed the latchup conditions for various irradiation procedures. According to the analysis of simulation results it should be noted that the power supply transient current amplitude of a single parasitic structure at pre-latchup point does not essentially depend on pulse duration, wavelength and beam width (Fig. 4). Thus, the rough estimation of \( \frac{dE}{dx} \) can be written as [3]:

\[
d\frac{dE}{dx} = k_0 L_{th} P_{th} L_{th} / P_{th},
\]

where \( k_0 \) is a proportionality coefficient. The value of \( L_{th} \) in this formula can be estimated from laser test results (3). Taking into account that \( P_{th} = \text{const} \) (from completes simulation) we can write the following relation:

\[
d\frac{dE}{dx} = k_0 L_{th} P_{th} L_{th} / P_{th}. \tag{5}
\]

The proportionality coefficients can be estimated either from computer simulation or experimental results for special test structure. We calculated the latchup threshold LET from 2D-simulation results for local laser irradiation. Then we obtained the values of \( L_{th}, P_{th}, P_{th} \) and \( P_{th} \) from calculations for uniform nanosecond laser irradiation. The predicted values of latchup threshold LET based on uniform nanosecond laser irradiation were obtained from formula (5) with \( k_0 = 3 \text{ MeV/(mg-mA/cm}^2) \).

It should be noted that the laser energies ratio \( P_{sh}/P_{se} \) is used in the above relations. Therefore, the influence of optical effects, metal shadowing etc. is assumed to be rather small.

4. EXPERIMENT

Two types of laser simulators have been used as the radiation sources [5]. “PICO-2E” pulsed solid-state laser simulator (Nd\(^{3+}\) passively mode-locked, wavelength \( \lambda = 1.055 \mu m \)) was used to generate picosecond pulses with the duration \( T_p = 10 \) ps. “RADON-5E” portable pulsed solid-state laser simulator (YAlO\(_3\):Nd\(^{3+}\), wavelength \( \lambda = 1.064 \mu m \)) was used to generate nanosecond laser pulses with the duration \( T_p = 12 \) ns [6]. For both laser simulators the wavelength conversion to the second harmonic was performed by non-linear KTP crystal.

The devices under test were specially designed test structure TSCLU and CMOS RAM of two types 537RU6 (4Kx1, 3μm p-well process) and 537RU16 (8Kx8, 2μm n-well process). The test structure consisted of several p-n-p-n structures of the same type with different shadowing of sensitive region by metallization (Fig. 5).

Fig. 5. Schematic diagram of test structure TSCLU

During the experiment latchup threshold laser energy was estimated for focused and uniform irradiation as a function of power supply voltage, wavelength pulse duration and beam location (for focused irradiation).

Experiment (Fig. 6) and software simulation (Fig. 2) gave nearly the same position of the most sensitive region of investigated test structure TSCLU is in agreement with software simulation results. Also, there is obvious similarity between latchup threshold laser energy vs. supply voltage dependence for test structure TSCLUXX (Fig. 7) and the results obtained by software simulation (Fig. 3).

Measured 537RU6 and 537RU16 latchup threshold energy values under the focused beam irradiation for two laser wavelengths and two pulse durations are presented in Table 1. According to expression (3) \( L_{th} = 21 \mu m \) for 537RU6 and \( L_{th} = 6 \mu m \) for 537RU16. If \( T_p < \tau_{th} \) (Fig. 7), where \( \tau_{th} \) is a latchup threshold time constant, then this
Higher predicted latchup threshold values were also obtained for 537RU16 due to the additional polysilicon layer. Therefore, it is more preferable to use the 1.06 μm wavelength in this case. The correlation between the measured values in Table 1 and the predicted ones in Table 2 is quite good, as shown in the table below.

**Table 1. Measured 537RU6 and 537RU16 latchup threshold energy E in nJ under the focused beam at various laser wavelengths and pulse durations.**

<table>
<thead>
<tr>
<th>Type of RAM</th>
<th>λ=1.06 μm</th>
<th>λ=0.53 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>RU6</td>
<td>3.36</td>
<td>2.23</td>
</tr>
<tr>
<td>RU16</td>
<td>2.38</td>
<td>2.045</td>
</tr>
</tbody>
</table>

The latchup threshold estimation for p-well 4K (537RU6) and n-well 64K (537RU16) CMOS SRAMs was performed (Table 2). Predicted values dE/dx₀ are based on formula (5) using experimentally obtained values of power supply current Iₘ/Iₚ for relatively low dose rate P₀ and latchup threshold laser intensity Iₘ. The ratio Iₘ/Iₚ for uniform laser irradiation with Tₚ=12 ns and λ=1.06 μm are shown in third column. Values of Pₘ were determined for λ=0.53 μm and λ=1.06 μm laser beams. Rather high predicted latchup threshold values were obtained for λ=0.53 μm laser radiation (sixth column). Such values can be explained by high absorption factor of IC surface polysilicon layers at λ=0.53 μm. Absorption is essentially higher in 537RU16 due to additional polysilicon layer. Therefore, it is more preferable to use λ=1.06 μm in this case. We have obtained correlation with CE²⁵² experimental results: latchup took place in 537RU16 while it was not observed in 537RU6. It is necessary to point out that heavy particles of CE²⁵² have small ranges in device volume (Rₓ<10μm in Si). Therefore for devices with Lₓ<Rₓ, the charge collection is nearly total and we can not use LET approach.

**Table 2. Predicted RAM latchup threshold values in MeV/(mg/cm²) using the uniform laser irradiation with Tₚ=12 ns.**

<table>
<thead>
<tr>
<th>Type of RAM</th>
<th>n₀</th>
<th>λ₀/λ₁ mÅ/(mJ/cm²)</th>
<th>Pₘ(12 ns) mJ/cm²</th>
<th>dE/dx₀ MeV/(mg/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RU6</td>
<td>64</td>
<td>22/0.73 μm μm</td>
<td>6.2 50</td>
<td>145 70</td>
</tr>
<tr>
<td>RU16</td>
<td>256</td>
<td>18/0.28 μm μm</td>
<td>7.1 20</td>
<td>89 15</td>
</tr>
</tbody>
</table>

5. CONCLUSION

Latchup threshold comparative research using focused and unfocused laser beams, picosecond and nanosecond laser pulse; bulk (wavelength 1.06 μm) and "surface" (0.53 μm) laser ionization was performed experimentally and by software simulation. Single event to dose rate latchup correlation was found. The approach was proposed for SEL threshold energy prediction using the dose rate laser simulation test results based on the independence of power supply current amplitude for single parasitic structure on pulse duration and irradiation spot width at pre-latchup point. For real IC this power supply current is proportional to the total number of parasitic structures.

**REFERENCE**


Abstract

Two-parameters model of ion-induced single event upsets is suggested. Saturation cross section of single event upsets and threshold linear energy transfer are required to estimate the cross section as a function of linear energy transfer. Comparison of this two-parameter dependence with Weibull function for various integrated circuits is done. Correlation of these two parameters with two parameters of Bendel approximation or of computer model for proton-induced single event upsets is discussed.

1. INTRODUCTION

Single event upsets (SEUs) are the main reason for functional errors of VLSI in low intensity radiation of nuclear particles [1-3]. The single event upset is a bit flip in a digital element that has been caused either by the direct ionisation from a traversing particle or by the ionisation produced by charged particles and recoiling nuclei emitted from a nuclear reaction induced near the microcircuit element.

The SEU rate prediction needs experimental SEU cross section dependencies on energy for proton irradiation and on linear energy transfer (LET) for ion irradiation. These dependencies are obtained from proton and ion accelerator tests for various energies or LETs. Such approach is rather complex and expensive and it would like to obtain a relation between sensitivity parameters of proton- and ion-induced SEUs. It is possible because of a common nature of proton or ion-induced SEUs. The common reason is a generation of a critical local charge in a sensitive volume of IC elements. The main issue of this work is the determination of correlation between proton- and ion-induced upset cross section dependencies.

2. PROTON-INDUCED SEU CROSS SECTION

The proton-induced SEU prediction methods are based on SEU cross section dependence on a proton energy. Two different approaches to proton-upset cross section calculations are developed now [4]. The first one is concerned with a nuclear reaction analysis in a microvolume of IC elements [5]. The semiempirical approach based on Bendel model is used as the second one [6]. The each model needs only two parameters. As a rule, a prediction of SEU cross section dependence on proton energy needs a threshold energy (Eo) and a sensitive volume value (Vsp) in digital models. Bendel approximation is based on the following expression:

$$\sigma_p = \sigma_{psp} \cdot [1 - \exp(-0.18 \cdot \sqrt{(18/A_p)}(E_p - A_p))]^4;$$  (1)

where $E_p$ is a proton energy; $A_p$, $\sigma_p$ are approximation coefficients; $\sigma_{psp}$ is a proton-induced SEU saturation cross section; $A_p$ is a threshold parameter.

Therefore there are only two independent parameters in both methods. It is clear that there is a connection between them. Let’s determine the threshold proton energy ($E_{po}$) from the condition $\sigma_p = 0.05\sigma_{psp}$. Then one can write:

$$E_{po} = 19.775 \cdot (A_p/10)^{0.7885};$$  (2)

It is necessary to point out that the real value of $E_{po}$ must be more than a threshold energy of proton-induced nuclear reaction in Si ($\approx 15$ MeV). The value of $E_{po}$ estimated from equation (2) may be less than 15 MeV due to formal fitting of Bendel function to the experimental results.

Taking into account the simplest model of proton-induced nuclear reaction in Si the relation between $E_{po}$ and $E_o$ can be written as:

$$E_o = E_{po}/k_{po} \cdot \Delta Q;$$  (3)

where $k_{po}$, $\Delta Q$ are approximation coefficients (satisfactory correspondence are obtained for $k_{po} = 2.9$ and $\Delta Q = 0.69$ MeV).

The connection between $\sigma_{ps}$ and $V_{sp}$ can be obtained from the following equation [7]:

$$\sigma_{ps} = V_{sp} \cdot \sigma_{nst} \cdot f(>E_o);$$  (4)

where $\sigma_{nst}$ is a macroscopic cross section of proton-induced nuclear reaction in Si; $f(\Delta E > E_o)$ is a probability of energy losses more than $E_o$ in a sensitive volume from secondary nuclei;

$$V_{sp} \equiv \sigma_{ns} \cdot d_{sp};$$  (5)

$\sigma_{ns}$ is an ion-induced SEU saturation cross section; $d_{sp}$ is a thickness of a sensitive volume. The equation (4) can be solved digital methods [7]. The approximate decision of the equation (4) can be written as:

$$\sigma_{ps} = k_{sp} \cdot V_{sp}^{(1+Eo/E_1)} \cdot \exp(-E_o/E_2);$$  (6)

where $k_{sp}$, $E_1$ and $E_2$ are approximation coefficients. A satisfactory agreement of approximation curves with
digital calculation curves [5,7] was obtained for \( k_{sp} = 2.5 \times 10^{-14} \text{cm}^2 \); \( E_1 = 18.3 \text{ MeV} \) and \( E_2 = 1.43 \text{ MeV} \) (Fig. 1).

One can use the only typical value of the sensitive thickness \( (d_{sp} \approx 1.5 \mu m) \) because of the mutual correlation between \( \sigma_{ps} \), \( E_0 \) and \( d_{sp} \) [7]. Therefore the physical parameters \( (E_0 \text{ and } V_{sp}) \) of proton-induced SEU cross section dependencies on proton energy can be calculated using Bendel approximation parameters \( (A_p \text{ and } \sigma_{ps}) \) and vice versa. Moreover the correlation of these parameters with ion-induced saturation cross-section is obtained also.

3. ION-INDUCED SEU CROSS SECTION

The ion-induced SEU prediction methods are based on the SEU cross section dependence on LET. Typically, the cross section curve for ion-induced SEU can be fit by the Weibull function with four parameters:

\[
\sigma_i(LET) = \sigma_{i0} \left(1 - \exp\left[-\left(\frac{(LET-LET_0)}{W}\right)^{1/s}\right]\right) \quad \text{for } LET > LET_0
\]

where \( LET_0 \) is a threshold LET; \( W \) and \( s \) are approximation coefficients. It is preferable to decrease the number of parameters in the function (7). The satisfactory results are obtained for two independent IC's SEU sensitive parameters \( (LET_0 \text{ and } \sigma_{i0}) \) and supposing that \( s=1.5 \) and \( W \) depends on \( LET_0 \) and on a peripheral area of sensitive volume of IC elements. The possible approximation for \( W(LET_0, \sigma_{i0}) \) looks as:

\[
W = k_w \cdot LET_0^{2s} \cdot (1+k_p \cdot \sigma_{i0}^\beta);
\]

where \( \sigma_{i0} \) is an ion-induced SEU saturation cross section per one bit; \( k_w, \chi, k_p \text{ and } \beta \) are approximation coefficients.

Only the ion-induced cross section and threshold \( LET_0 \) are used in this case. The simplified Weibull functions for some IC are shown in Fig. 2. Satisfactory agreement between the two-parameter function and usual Weibull curves [2, 8] is obtained. Therefore two-parameter curves can be used for determination of ion-induced SEU cross section dependence on LET.

It is important to point out that \( LET_0 \) is connected with \( E_0 \):

\[
LET_0 = E_0/d_{si}; \quad \text{(9)}
\]

where \( d_{si} \) is an effective thickness of the IC sensitive volume [9]. Taking into account the funnelling effects one can consider that \( d_{si} = (2\text{-}4) \cdot d_{sp} \).

4. CORRELATION PROTON-AND ION-
INDUCED SEU PARAMETERS

It is possible to use heavy ion data for estimating the energy dependence of the proton-induced SEU cross section and vice versa. Really one can assume that a sensitive volume of an IC element is a right rectangular parallelepiped and its area is proportional to SEU ion-induced saturation cross-section per bit. The threshold LET equals to threshold energy divided by an effective thickness of the parallelepiped (9). In addition to one can use the relation (6) between SEU threshold energy and proton-induced saturation cross section.

Proton-induced SEU parameters can be determined both for Bendel function and for digital model. Technique for estimation parameters of digital model consists of the following steps:

- determination of \( \sigma_{i0} \) and \( LET_0 \) from experimental results;
5. CONCLUSION

Simplified two-parameters models of ion-induced and proton-induced single event upsets were considered. The appropriate equations connecting the parameters of these models were suggested. Correlation of the parameters of ion- and proton-induced SEU models was discussed. Examples of a conversion of ion-induced SEU model parameters into proton-induced ones were performed. Comparison of the experimental data was done.

ACKNOWLEDGEMENT

The author would like to thank to M.G. Tverskoy for his assistance in computer simulation and A.I.Sheremetyev for his assistance.
REFERENCES

RADIATION RESPONSE OF HALL SENSOR BASED ON
SOI DOUBLE GATE FIELD EFFECT RESISTOR

A.Y. Nikiforov, A.V. Sogoyan, A.S. Artamonov,1
V.N. Mordkovich, A.D. Mokrushin, N.M. Omelianovskaia2

1Specialized Electronic Systems
2Institute of Microelectronic Technology and High-purity Materials

31 Kashirskoe shosse, Moscow, 115409 Russia, aynik@spels.msk.ru

Abstract

Hall Sensor based on Silicon on Insulator (SOI) Double Gate Field Effect Resistor (DGFER) is presented and its total ionizing dose (TID) radiation response is experimentally analyzed.

The radiation behavior of the device under test was found to be similar to SOI MOSFET's. The device characteristics degradation was mainly due to intensive positive charge trapping in SIMOX layer. The rate of buried oxide positive charge annealing was found to be rather low. It corresponds to the observed hole trapping in SIMOX. The contribution of surface traps in buried oxide to silicon interface was found negligible. The preliminary results didn't demonstrate any significant contribution of deep electron traps at doses up to 4 Mrad.

It was demonstrated that Hall sensors degradation threshold can be essentially increased by the proper device application circuit.

1. INTRODUCTION

SOI devices based on SIMOX process are widely used in radiation environment applications due to their inherent low sensitivity to the dose rate and single event effects. At the same time SOI devices are rather low immune for total dose effects because of the buried oxide layer additional influence on a device radiation response parameters. It should be mentioned that the buried oxide radiation features differs from those of thermal oxides. Most of the published works are concentrated on SOI MOSFET radiation behavior analysis [1-4]. In this paper we present Hall sensor based on the original SOI Double Gate Field Effect Cross Resistor which gives us some additional possibilities to perform comparative experimental research of "top" and "bottom" borders of silicon device layer in SOI structures.

II. DEVICE UNDER TEST DESCRIPTION

Double Gate Field Effect Resistor (DGFER) is a SIMOX SOI structure (Fig.1). The n-type <100> silicon layer has 0.2 μm thickness and 10 Ω-cm resistance. The thickness of the buried oxide layer (SiO₂) is 0.4 μm and the n-Si substrate's thickness is 500 μm.

![DGFER cross-section](image)

Fig.1 DGFER cross-section

![DGFER current-gate voltage characteristics](image)

Fig.2 DGFER current-gate voltage characteristics
The two gate electrodes allows us to vary the channel conductivity in a wide range which give us a good possibility to analyze the sub-threshold operation range in details (Fig.4) and to use standard methods [5] to extract the components of threshold voltage radiation-induced shift, corresponded to oxide ($\Delta V_o$) and interface traps ($\Delta V_t$) charge.

At first we were going to compare the radiation-induced charge build-up rates in buried SIMOX layer and pyrolytical oxide. Two device groups were irradiated with a different combinations of gate biases: $V_{g1}=+10 \text{ V}$, $V_{g2}=0 \text{ V}$ for the first group and $V_{g1}=0 \text{ V}$, $V_{g2}=+10 \text{ V}$ for the second group. The irradiation was performed using Co-60 gamma-source and "REIS-IE" X-ray tester. The measured device threshold voltage shift to total dose dependencies for both groups are presented in fig. 5. The devices of the second group were subjected to postirradiation annealing for 25 hours with the same gate biases ($V_{g1}=0 \text{ V}$, $V_{g2}=+10 \text{ V}$). The threshold voltage shift caused by the annealing was in the limits of the experimental error.

Radiation-induced threshold voltage shift leads to the source-drain conductivity modulation. The dependencies of normalized DGFER resistance on total dose at various gate bias combinations are presented in Fig. 6.

Another set of devices was irradiated with the dose rate 1000 rad(SiO$_2$)/s. At the first step the devices were irradiated at zero gate biases $V_{g1}=0 \text{ V}$, $V_{g2}=0 \text{ V}$ to the total dose of 2800 krad. Then the gate bias was changed to -10V and the devices were exposed to the additional dose of 1200 krad. The measured DGFER threshold voltage shift to total dose dependence is presented in Fig. 7.
The radiation hardness of Hall sensor can be characterized by the radiation induced degradation of device sensitivity which deals mainly with Hall mobility degradation. A Hall sensor failure mechanisms were investigated in the following experiment. The device was irradiated with dose rate 200 rad(Si)/s using X-ray source. In order to minimize the performance point shift during the irradiation the gate bias was periodically cycled: +10V during 75 s and then -10V during the next 150 s, etc. The device transconductance $k$ was measured in each step which was proportional to the effective mobility of charge carriers. At the same time the maximum point of Hall voltage $V_h$ vs. gate bias characteristic was detected and the corresponding $V_h$ to drain voltage dependence was measured. Thus the relative degradation of Hall mobility $\mu_h$ was identified.

The comparative Hall mobility together with effective mobility vs. total dose measured curves are presented in Fig. 9.

The rate of radiation induced interface traps buildup at the buried oxide to silicon interface was investigated in CV-tests as well. DGFER CV-curves were determined before and after $\gamma$-irradiation (Ce$^{6+}$) up to total dose 30 krad. The measurements were performed at 1MHz frequency for Gate 1 - pyroilical SiO$_2$-Si and Gate 2 - buried oxide-Si layers separately. The measured buried oxide capacitance are presented in Fig. 8.

According to the results of low-dose experiment (Fig.5) the rate of positive charge build-up in the buried SIMOX oxide is higher as compared to the thermal gate oxide. This result is in agreement with the other published data [2,4]. It can be explained by the relatively higher density of oxygen vacancies in the buried oxide layer and by the higher thickness of the oxide layer. The low rate of positive charge annealing in the buried layer is also in agreement with the assumption, that the hole traps are located in the bulk of SIMOX oxide [4].
Fig. 7 demonstrates the negligible influence of electron MOSFET parameter degradation under irradiation. One parameter degradation and effect resistor and the appropriate Hall sensor were biases. More research work is to be perform in order to determine the influence of electron traps on the device parameter degradation and to clarify the specific process conditions that may lead to such an effect.

The results of CV-measurements (Fig. 8) demonstrate that the effect of radiation-induced interface traps build-up in the buried oxide is negligible as compared to the positive charge trapping. It should be mentioned that some DGFER based Hall “cross” structures can be used as test structures to clarify in details the particular physical mechanisms of MOSFET parameter degradation under irradiation. One of the most urgent problems deals with the model effective channel mobility ($\mu_{eff}$) radiation induced decrease [5,6]:

$$\mu_{eff} = \frac{\mu_0}{1 + \alpha AN_i},$$  (1)

where $\mu_0$ is initial mobility value, $\Delta N_i$ is the concentration of radiation induced interface traps. This effect is usually interpreted in terms of channel carriers scattering by charged interface or oxide traps [6]. Another approach deals with the recharging of interface states, which energy levels correspond to Fermi level $E_F$ as [7]:

$$\mu_{eff} = \frac{\mu_0}{1 + \beta \Delta N_i + \gamma \Delta D_i(E_F)},$$  (2)

where $\Delta D_i(E_F)$ is the increase of interface traps with energy levels close to $E_F$ density. In the experiment described we tried to determine independently the relative contribution of each mechanism to the final effect of effective mobility degradation. The normalized value of effective mobility was estimated from DGFER voltage-current dependencies, and the "true" mobility from Hall experiments. The obtained test results (Fig. 9) support the assumption of [7] that the dominant mechanism of a MOSFET transconductance radiation induced degradation deals with interface-traps recharge.

Besides, one can see that the powered Hall sensor without the stabilization of the operational current is rather total dose sensitive. But if one will use a feedback circuit to control the operational current then the Hall sensor became rather radiation tolerant. This results should be taken into account in LHC electronics design.

V. CONCLUSION

The radiation response of SOI Double Gate Field Effect Resistor and the appropriate Hall sensor was investigated. The obtained experimental results corresponded to the usual SOI structures behavior. The device characteristics degradation was mainly due to intensive positive charge trapping in SIMOX layer. The rate of buried oxide positive charge annealing was found to be rather low. It corresponds to the observed hole trapping in SIMOX. The contribution of surface traps in buried oxide to silicon interface was found negligible. The preliminary results didn’t demonstrate any significant contribution of deep electron traps at doses up to 4 Mrad.

The Hall cross structure version of the device give us possibility to perform an independent measurements of real and effective carrier mobility degradation under irradiation. This observations can be useful to clarify a physical nature of radiation induced degradation of MOSFET parameters. It was demonstrated that Hall sensors degradation threshold can be essentially increased by the operational current control circuit application.

REFERENCES

Abstract

Both simulation and experimental research of CMOS ICs total dose upsets must take into account the operation modes of IC. Techniques are presented to determine the irradiation and test operation modes of CMOS ICs. Test and simulation results illustrate the specifics of operation mode influence on total dose upsets.

1. INTRODUCTION

CMOS ICs are widely used in LHC electronics and are often irradiated by gamma and neutrons. Total dose degradation of MOS transistors parameters under such irradiation results in both parametrical (supply current, output voltages and currents, leakage current etc.) and functional upsets of ICs. For digital LSI the functional upsets are often of primary interest.

Both radiation tests and calculating simulation can be used for total dose functional upsets of digital CMOS ICs investigation; and in both cases one must take into account the dependence of element dose degradation on operation mode under irradiation. It is well known that CMOS element is most vulnerable for total dose when logical "1" is applied to its input and n-channel transistor is turned on. In the same time the element total dose upset is characterized by output logical "1" degradation because of threshold voltage shift of the MOS transistors. Any CMOS logical element inverts input signal, that is why we can conclude that CMOS IC radiation test procedure should use two operation modes for worst case hardness estimation: (1) operation under irradiation and (2) test operation. It is very desirable for IC under test to have as many logical element inversions for these two operation modes as possible. This technique is applicable for numeric simulation as well.

2. EXPERIMENTAL AND NUMERIC SIMULATION TECHNIQUES

The experiments and simulations were carried out to investigate the influence of operation modes on total dose behavior and upset levels.

2.1. Experimental Technique.

Experimental technique we used for total dose investigation is based on the X-ray simulator. The simulation usage possibility and test results adequacy is discussed in many previous papers (see [1] for example). The "REIS-IE" X-ray simulator demonstrates 50 keV maximum energy, about 10 keV average energy and provides up to 1000 rad(Si)/s dose rate.

We used top-side irradiation in both X-ray and laser simulation tests. That is why all the parts were previously delidded.

The computer based test and measurement tools allowed to control a device under test (DUT) during irradiation and to measure its characteristics after irradiation. The basic version of the control system is also presented in [1].

2.2. Numeric Simulation Technique.

For calculating we used the system of functional-logic numeric simulation based on the criterion membership functions (CMF) method of the fuzzy logic sets theory.

Application of the CMF method for total dose functional failures simulation is based on the following principles:

1. The continuous character of processes in IC elements under irradiation brings to the parametrical character of their failures. It claims the transformation of Boolean logic model with set of signals \( \{0,1\} \) to logic model with signals which are belong to the continuous interval \([0,1]\) for analysis of such processes.

2. The influence of irradiation on element is simulated by introduction of an additional CMF input signal \( \mu(D) \) which is also within the range \([0,1]\). The value of this signal depends on the total dose.

3. The Boolean logic functions are transformed to contiguous functions. Thus, the system of Boolean logic equations of IC operation is transformed into the system of fuzzy logic equations.

The system and the simulation method were presented in detail in the last year Workshop [2].
3. NUMERIC SIMULATION DATA AND TEST RESULTS DISCUSSION

We took some simple CMOS ICs (logics, decoder, multiplexer, counter, parity check circuit) and multifunctional buffer VA1 (analog of CP82C86 by Harris Semiconductor).

Both experimental and simulation results showed that usually there is no total dose upset if irradiation and test operation modes are same. Upsets take place if the modes are different. Some results allow to conclude that the more this difference (number of elements which change state) the lower total dose upset levels.

The experimental data and the numeric simulation results of CMOS multifunctional buffer VA1 are presented in Fig. 1. The output CMF's for two strategies are presented: (a) the test operation mode of the DUT is changed as compared to the irradiation mode and (b) the test mode and the irradiation mode of the DUT are the same.

One can see that there is no total dose upset when the operation mode was not changed for test. Both numeric simulation and experiment demonstrated the total dose failure only when the operation mode of VA1 was changed after irradiation for the test.

The operation mode sensitivity of CMOS IC total dose upsets results in some problems in calculations. When an element of IC changes its state during simulating irradiation (because of input signals change or if "a previous" element failed) we have to switch a model of an element into another one. In many cases these moments can not be predicted in advance and we need to add some "intelect" into the calculation strategy.

4. CONCLUSIONS

One should take into account the CMOS ICs total dose upset sensitivity to operation modes in radiation test and simulation task preparation. The technique presented assumes to use two different operation modes - under irradiation and for functional test. This approach is proved to result in sufficient differences of CMOS ICs radiation hardness levels.

REFERENCES


Figure 1. Output CMF's of VA1: a - test operation mode is changed as compared to irradiation mode, b - test mode and irradiation mode are the same.
A WAY TO IMPROVE THE EFFICIENCY OF LASER SIMULATION TESTS ADOPTED TO SOI/SOS DEVICES

P.K. Skorobogatov, A.Y. Nikiforov, B.A. Akhabaev

Specialized Electronic Systems
31 Kashirskoe shosse, Moscow, 115409, Russia, Pkskor@spels.msk.ru

Abstract

Laser simulation tests are widely used for radiation hardness estimation of the bulk IC for LHC applications. The simulation adequacy of particular device type depends on the chosen laser wavelength \( \lambda \). The requirements to laser wavelength are contradictory. From one hand the quantum energy must be sufficient to obtain silicon bulk ionization. From the other hand the absorption coefficient should not be very large in order to limit ionization nonuniformity within the device depth. These factors restrict the choice of laser sources. In particular for conventional bulk silicon IC the Nd: IAG laser is nearly optimal, with \( \lambda \) in the narrow range 1.06...1.08 \( \mu \)m and a corresponding penetration depth about 700 \( \mu \)m [1-4].

Nd: IAG lasers can generate equivalent dose rates up to \( 10^{15} \) rad(Si)/c with small nonuniformity in active semiconductor regions. However, this advantage results in large loss of laser beam energy in case of thin device layers in Silicon-on-Insulator (SOI) and Silicon-on-Sapphire (SOS) IC. For example only about 0.03\% of laser energy is absorbed in 0.2 \( \mu \)m silicon device layer if one will use 1.06 \( \mu \)m wavelength.

In case of SOS/ SOI IC the laser simulation efficiency may be improved by laser wavelength decrease. Due to the inherent features of SOS/SOI devices the initial nonuniform distribution of radiation-induced carriers relaxes to the uniform state within a few nanoseconds which is less than a laser pulse width [5].

II. RESEARCH RESULTS AND DISCUSSION

In order to check the improved laser simulation technique the specialized SOS test structure was designed and investigated. It consists of complementary MOS/SOS field effect transistors (FET) pair with 0.6 \( \mu \)m device layer, 5 \( \mu \)m channel length and 128000 \( \mu \)m channel width. This extra large channel width give us possibility to increase photocurrent response and consequently to decrease the measurement error. The ionizing current transient response was registered with "Tektronix TDS-220" digital oscilloscope.

The experiments were performed with usage of Specialized Simulation Test System [6]. Pulsed laser simulator "RADON-5E" [7] and its upgrade version "RADON-5EM" [8] were used to generate laser radiation with two wave-lengths: 1.06 \( \mu \)m and second harmonic 0.53 \( \mu \)m The comparative tests for both wave-lengths were performed to analyze the radiation responses.

Software simulator "DIODE-2D" was used to perform numerical analysis of the test structures transient response. "DIODE-2D" is the two-dimensional solver of fundamental system of equations taking into account the electrical and optical processes including multirefection and free carrier nonlinear absorption [2].

The measured and calculated p- and n-MOSFET photocurrent amplitudes to laser intensity dependencies for 1.06 (a) and 0.53 (b) \( \mu \)m wavelength are presented in Fig.1. One can see that p-MOSFET is more radiation sensitive as compared to n-MOSFET because of relatively low doping level and consequently large carrier mobility. The main result is that using 0.53 \( \mu \)m wavelength one can get the same response as with 1.06 \( \mu \)m but at sufficiently less laser intensity.

The comparative simulation results demonstrate that the second laser harmonic application give the gain about 100 times. The experimentally measured gain is near 60 to 70 times due to the additional absorption of 0.53 \( \mu \)m light in polysilicon gate of MOSFET. Consequently, using 30\% efficiency second harmonic converter one can increase...
Fig. 1. Theoretical (curves) and experimental (dots) photocurrent amplitudes vs. laser pulse intensity for p-MOS (1) and n-MOS (2) SOS MOSFET in case of 1.06 (a) and 0.53 (b) μm laser wavelength.

Fig. 2. Distributions of equivalent dose rate in n-MOS SOS structure at two wavelengths: 1, 2 - 1.06 μm (for source (drain) and channel consequently); 3 - 0.53 μm (for all of regions)

difference between drain (source) and body regions is due to the difference of doping levels. The 0.53 μm irradiation has relatively large absorption coefficient in silicon that creates sufficient ionization nonuniformity with slight doping level dependence.

It was supposed that in thin device layer of SOS/SOI the processes of generated excess carriers diffusion and drift can smooth out the initial nonuniformity during laser pulse width (10 to 15 ns). The numerical calculations with «DIODE-2D» two dimensional software simulator confirmed this assumption. The difference between ionizing current waveforms under 1.06 and 0.53 μm lights with the same equivalent dose rates did not exceed 1%.

The equivalence of radiation responses was obtained in comparative tests at two wave-lengths. The comparison of experimental ionizing current oscillograms at two wavelengths does appear sufficient difference as shown in Fig. 3 and 4.

III. CONCLUSIONS

The numerical and experimental results confirmed the possibility of laser irradiation with short wavelength application for dose rate effects simulation in SOS/SOI IC. It is required much less 0.53 μm laser radiation intensity as compared to 1.06 μm laser radiation intensity to get an equivalent dose rate response of SOS/SOI device. Thus the usage of short wavelength laser is proved to be much more efficient for SOS/SOI IC's.

The new laser simulation technique gives us possibility (1) to increase the maximum available equivalent dose rate due to more efficient absorption of laser energy and (2) to extend the range of suitable laser sources including more convenient semiconductor laser devices.
ACKNOWLEDGEMENTS

The authors wish to thank Yury Sitsko - the author of "DIODE-2D" Software Simulator for his assistance in numerical simulation procedure and also Oleg Mavritsky, Andrew Egorov and Igor Poljakov for their help in laser experiments and test structure design.

REFERENCES

DEVELOPING A GIGABIT S-LINK CARD

Zoltán Meggyesi, Erik van der Bij (CERN/EP, Geneva)
Tivadar Kiss, György Rubin (RMKI, Budapest)
György Vesztergombi Jr. (BME, Budapest)

Abstract

Components for Fibre Channel and Gigabit Ethernet are candidates for realizing several thousand small footprint, fast, cheap and reliable data links for the LHC experiments. After having introduced a prototype card two years ago, we integrated the media interface on the link card. Integration of the system elements into one chip or one board, using the latest technology developments is necessary to reduce the size, price and power consumption of a link.

This article introduces an integrated media-interface Fibre Channel - S-LINK interface, shows the design issues and points to our future plans for realizing data links for the LHC experiments.

1. INTRODUCTION

LHC experiments require a large number of small footprint, cheap, fast and reliable data links. The S-LINK specification [1] defines a simple, synchronous FIFO-like user interface which remains independent of the technology used to implement the physical link. Components for Fibre Channel (FC) and Gigabit Ethernet are candidates for implementing cheap, high-speed serial data links. The FCS-Link is composed of a source (LSC) and a destination (LDC) card and a fibre optic cable. The FCS-LINK maps the S-LINK signals to Fibre Channel. Since the user interface of the cards is S-LINK and the physical layer is transparent to the user, the developments have no effect for those who used any previous version of these cards for system prototyping. FCS-LINK cards are used in the ATLAS DAQ/Event Filter Prototype-1 project, testbeams of the MDT and TileCal and in the Trigger Supervisor [2]. It has also been used outside ATLAS: Olivetti and Oracle research laboratories have used it for moving video and keyboard data to and from remote terminals.

The “FCS-LINK2” card is an intermediate step between the first cards and a final S-LINK physical implementation. Its aim is to provide an inexpensive and reliable data link with standard S-LINK interface for data acquisition system developers.

2. FCS-LINK-CARD

The first FCS-LINK card was introduced on the 2nd LEB workshop in 1996 [3]. An FCS-LINK card consists of four main units: Optical interface, Serializer chip, Fibre Channel and S-LINK protocol logic. The first FCS-LINK card (Figure 1) was mounted with a standard plug-in Gigalink Module (GLM) which is responsible for the high-speed serialisation and optical functions and has a 32-bit data interface. The highest clock frequency on the main circuit board and inside the PLD was 53Mhz which was easy to implement. The FC 8b/10b coding scheme and link management was done by a VSC7107 Fibre Channel encoder/decoder (ENDEC) chip, the protocol mapping between S-LINK and Fibre Channel was implemented in an Altera PLD. The size of the board is specified by the S-LINK specification.

A new Fibre Channel - S-LINK card was developed with integrated media interface on the circuit board (Figure 2, 4). The high-speed serial stage is now implemented on the main card resulting a significant decrease in component height. The protocol mapping between S-LINK and FC was improved - the reset protocol was rewritten as software developers required. As a result either side of the link can be reset independently, the opposite side won’t detect any failure in link operation.
These cards were designed to provide flexibility for prototype systems developers. It is possible to use standard Fibre Channel electrical media with the same performance for distances up to 20 m. The media interface - both optical and electrical - can be mounted on either side of the card for use in either PMC or PCI systems (Table 1).

Table 1: Media Options

<table>
<thead>
<tr>
<th>Media</th>
<th>Distance</th>
<th>Mounting</th>
<th>Utilisation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td>20m</td>
<td>Top</td>
<td>Laboratory</td>
</tr>
<tr>
<td>Electrical</td>
<td>20m</td>
<td>Bottom</td>
<td>Laboratory</td>
</tr>
<tr>
<td>Optical</td>
<td>500m</td>
<td>Top</td>
<td>PMC</td>
</tr>
<tr>
<td>Optical</td>
<td>500m</td>
<td>Bottom</td>
<td>PCI</td>
</tr>
</tbody>
</table>

In order to reduce the production price, the same printed circuit board design is used for both source and destination cards, top and bottom mounted electrical and optical media interfaces. Configuration information of the CMOS SRAM protocol chip is downloaded from an EPROM on each power-up. The card behaves as a source or destination depending on the configuration data. The configuration EPROM is a cheap device and can easily be replaced if mounted with a socket.

This gives the flexibility to update the cards by sending EPROMS to users with new configuration data in case any bugs are found or if the user has special requirements for the system.

3. MEDIA INTERFACE

The frequency of the transmission lines between the laser transceiver and the VSC 7126 serializer chip is over 500Mhz which places restrictions on printed circuit board (PCB) design and manufacturing. Calculated line impedances and termination circuits reduce reflection and crosstalk on high-speed data and clock lines. Transmission lines are implemented on both sides of the card to allow mounting the media interface on either side. The wires of the unused side can be cut before mounting the components, avoiding the use of 0 ohm resistors whose pads may cause reflections. If no laser driver is mounted, AC coupling capacitors ensure the connection to electrical media connectors. Figure 3 illustrates the path of the high speed transmission lines.

In order to reduce the production price, the same printed circuit board design is used for both source and destination cards, top and bottom mounted electrical and optical media interfaces. Configuration information of the CMOS SRAM protocol chip is downloaded from an EPROM on each power-up. The card behaves as a source or destination depending on the configuration data. The configuration EPROM is a cheap device and can easily be replaced if mounted with a socket.
Reliability and low price of the laser unit are the most important requirements. The card features an industry standard 1x9 pin configuration and dual SC connector laser driver, which is available from many vendors (HP, Methode, Molex, Siemens, Vixel...). All types provide less than 10^{-12} bit error rate (BER). The maximum distance with a cheap 850nm laser source and multimode cables is 500m. Single mode optics with 1300nm laser sources can span distances up to 10 km. The Vertical Cavity Surface Emitting Laser (VCSEL) has higher reliability, lower power consumption, and higher maximum operating temperature than a CD laser.

4. PROTOCOL CHIP

The FCS-LINK2 protocol chip is implemented in an Altera Flex 8000 PLD. The chip was designed in the Altera AHDL design language. We could simulate the chip with simple AHDL models of the S-LINK and ENDEC within the Max+Plus Altera design system. Figure 5 shows the main blocks of the source card logic.

![Figure 5: LSC Protocol Chip](image)

5. TEST ENVIRONMENT

The FCS-LINK2 cards were tested at full speed using the commercially available S-LINK testing devices [4], a HP logic analyzer and two pulse generators. The cards were plugged to SLITEST testing boards (Figure 6). Different test patterns were generated by the SLIDAS S-LINK data source at 160 Mbyte/s maximum speed (40Mhz clock and 32-bit wide datawords). Data transmission was periodically interrupted by a pulse generator connected to the LEMO connector of the SLIDAS with up to 20Khz pulses, emulating a real-life environment. Data was received by the SLIDAD data drain. The SLITEST features a built-in counter that counts the error pulses coming from the link. A second pulse generator was connected to the SLIDAD’s LEMO connector to emulate random flow control. The received data was sent to a HP logic analyzer from SLIDAD’s logic analyzer connectors which checked the received pattern and triggered on errors.

Walking 1, walking 0, alternating FF/00 and alternating AA/55 patterns were tested. We observed no errors during several days of testing, which is of the order of 100Tbits transmitted data with each pattern. The maximum throughput when no flow control was used reached 100 Mbyte/s, the maximum performance of a Fibre Channel link. The cards were also tested in VME environment and in a PC with LINUX S-LINK drivers.

High frequency signal quality tests were made by the Microwave Telecommunication Department of the Technical University of Budapest [5].

6. PRESENT DEVELOPMENTS

Present developments aim to further reduce the price, size and power consumption of a gigabit link card. This can be realized by a stepwise integration of the system elements into one board or one chip, using the latest and lowest cost technology developments.

6.1 Supply voltage

Small feature size semiconductor components with lower power consumption and faster operation require a lower supply voltage. Gigabit S-LINK cards will follow the trends in reducing the supply voltage. Within a few years most electronic systems will work on 3.3V or 2.5V power sources. On this card the serializer chip is already a 3.3V device. The next generation Gigabit S-LINK card will be able to operate on both 5V and 3.3V supply voltage.

6.2 Integrated functions in one PLD

We are planning to integrate the FC 8b/10b encoding/decoding (ENDEC) and CRC generation circuits together with the S-LINK functions into a high complexity programmable logic device (PLD). Source code for the FC functions has been written for an Altera FLEX10K PLD and is being used in the prototype Fibre Channel cards of the ALICE-DL link. The main elements of the ENDEC macrofunction are the 8b/10b encoder and decoder, CRC generation and check and link initialization modules (Figure 7).
FUTURE PLANS

The rapidly expanding market for Gigabit Ethernet will result in decreased component prices and increased performance. Gigabit Ethernet uses the same physical layer as Fibre Channel, so the FC-S-LINK card can be mounted with standard Gigabit Ethernet components resulting in further cost reductions. Using Gigabit Ethernet technology will increase the performance by 20% because of its higher signaling rate (1.25 Gbaud).

For DAQ systems of LHC experiments it will be possible to integrate more links on one read-out board to reduce the price overhead and converge the link cost to the component price. Figure 7 shows an estimated price projection of the main link components (two cards) for the near future [8]. The figure is based on single unit pricing and does not contain circuit board and manufacturing costs.

6.3 PCI functions

The reduced number of components makes it feasible to implement the PCI functions on the same card, in a separate device or in the same PLD. A destination card, which integrates the FCS-LINK LDC and the S-LINK to PCI units [7] is under development.
8. CONCLUSIONS

The Fibre Channel – S-LINK cards have already been used in several applications within ATLAS and in other experiments relieving users from high-speed circuit design and implementation. We developed the FCS-LINK2 cards to provide a smaller and cheaper reliable data link for prototype systems. Ongoing and planned development projects aim further price and size reductions by integration of the system elements in one board or one chip. The rapidly expanding market for Gigabit Ethernet, new small feature size components and high system integration will result in cheap, small and reliable high-speed serial data links for the LHC experiments.

REFERENCES


[8] Private communication with SIEMENS on laser transceiver price projection


A MIXED SIGNAL DATA RECEIVER/CLOCK SYNCHRONIZER ASIC FOR ANALOG FRONT END CHIPS IN LHC EXPERIMENTS

C. Posch, T. Toifl
CERN – EP, Geneva, Switzerland

ABSTRACT
The analog readout scheme for the ATLAS SCT Semiconductor Tracker requires an off-detector device that receives the data packets from the front end chips (SCT128A) via optical links, prepares them for the conversion and controls the A/D converter and following data processing stages at ROD (Read Out Driver) level. This paper describes the Clock Synchronizer Chip (CSC), an ASIC designed for this task.

The CSC monitors the data line at the output of the optical receiver for the mixed signal data packets sent by the analog front end chips. It recognizes the digital header, synchronizes on the data and creates an encode clock of correct phase for the A/D converter. The clock phase is adjusted at reception of each data packet within a resolution of 1 ns. The device also performs the extraction of additional information, bunch crossover (BCO) number, trigger L1 number and data overflow flag, from the digital trailer at the end of each data packet. The CSC is programmable via serial control inputs to react flexibly on different environmental conditions as clock phase requirements of different A/D converters and data frame formats. As it is designed to work primarily together with the SCT128A analog front end chip, the CSC is fully compatible with the SCT128A mixed signal data format [3], [6] and meets the LHC/ATLAS timing specifications in terms of clock speed (typical 40 MHz) and timing resolution.

The ASIC comprises full custom blocks as well as standard cell logic circuitry and is fabricated in a standard double-metal 0.8μm CMOS process.

1. INTRODUCTION
For the analog readout of silicon strip detectors in the ATLAS Semiconductor Tracker, a 128-channel analog pipeline chip (SCT128A) has been designed and manufactured [2]. The SCT128A comprises three basic blocks: front-end amplifier, analog memory and output multiplexer. At each readout cycle, the multiplexer sends a data packet consisting of a digital header pattern, 131 analog data values and a digital trailer time multiplexed at 40 MHz (thus the length of one time slot is 25ns) to the optical transmitter to be sent to the Read Out Driver (ROD), which is situated off-detector in the cavern typically around 50 to 100 meters from its front end chip. On reception at the ROD, a defined phase relation between the data packet and the local copy of the machine clock has to be established in order to ensure proper A/D conversion of the analog data. Furthermore the additional information on the data, namely the bunch crossing number (BCO number), the level-1 trigger number (L1 number) and an overflow flag, signalling a data overflow in the FIFO derandomizer on the SCT128A, has to be extracted out of the trailer of each data packet and distributed to their respective receivers. As the radiation level in this part of the experiment is sufficiently low [1], a commercial ADC can be used. Figure 1 shows a block diagram of the ROD level conversion unit.

Figure 1. ROD level conversion unit block diagram

The CSC receives the data packets from the optical receiver. After successful identification of the header pattern, the phase of the packet is determined and the appropriate conversion clock phase is sent to the ADC. Control signals for the ADC and for the extraction of the trailer data are generated.

At any time a 5-bit register (PHASE_SELECT) can be loaded choosing any clock phase within one 25ns time slot at a resolution of 1ns relative to the data phase. Generally done at power up, this allows to accommodate timing requirements of different ADCs. One bit (CONFIG) configures the CSC to either one-chip or two-chip readout cycles. In the ATLAS analog readout scheme, two-chip cycles are foreseen. In this case two data packets, corresponding to the same L1 trigger event, coming from two adjacent SCT128A are attached and are treated as one 256-channel packet by the CSC [3], [6].

In order to assure the absolute accuracy of the conversion timing, a self-calibration structure is incorporated in the chip, consisting of a dummy path, an output pad feedback loop and a phase detection unit. This circuit permanently measures the time delay of the signal path through the chip, and corrects the phase of the output conversion clock. Timing accuracy and resolution can therefore be maintained over a wide range of operating
temperatures and process parameter variations and is independent of the load capacitance.

2. CSC ARCHITECTURE

Figure 2 shows the block diagram of the CSC chip architecture. The main building blocks comprise a delay locked loop (DLL), a finite state machine (FSM) for the header identification, the phase detection and clock selection units and a self calibration circuit using a dummy loop. A 9-bit counter controls the generation of the DATA_VALID and the BCO_TR1 signal.

![CSC Block Diagram](image)

### 2.1 The delay locked loop (DLL)

To achieve a low-jitter timing resolution of 1ns, a delay locked loop (DLL) structure was chosen. It consists of a voltage controlled delay line, a phase detector, a loop filter and a charge-pump [5], [4]. The delay line is a chain of 2x25 current-starving inverters. The delay of each individual inverter is controlled by the loop control voltage \( V_C \). The outputs of the delay line are fed into a multiplexer, which puts out the conversion clock, as well as into the phase detection units.

The signal edge coming out at the end of the delay line is compared against the incoming clock signal through a phase-detector, deriving a binary decision whether the signal delay was longer or shorter than one period of the reference clock (25 ns at 40 MHz). The phase detector is implemented as a balanced flip-flop. The decision of the phase detector (either early or late) is used to control a charge-pump, which increases or decreases the charge on the loop-filter capacitor, thus changing \( V_C \) and its associated delay value. Figure 3 shows a block diagram of the DLL.

**Delay line architecture**

Every tap of the delay line, corresponding to a nominal delay of 1 ns, consists of two identical current starving inverter cells. The output of each of these inverters connects to an inverter acting as a buffer between the delay line and the multiplexer. Although only the output of every second buffer is actually used, the other buffers cannot be omitted in order to achieve identical behaviour for rising and falling edges rippling through the delay line.

![DLL Block Diagram](image)

The schematic of a current starving inverter delay cell is shown in Figure 4. The basic current starving inverter structure consists of an ordinary CMOS inverter (T1, T2) being connected to the supply rails via voltage controlled current sources (T3 and T4, with gate voltages \( V_p \) and \( V_n \). Two shunt transistors (T5, T6) were added to linearize the delay vs. voltage characteristic of the delay cell and to assure a finite delay time even if the starving transistors are cut off.

![Current Starving Inverter Cell](image)

To achieve the same propagation delay in all inverter stages it is necessary to consider the matching properties of the transistors. It can be assumed that it is mainly the behaviour of the voltage controlled starving transistors influencing the delay of the inverter, which is a good approximation as long as those transistors work as current sources.

To achieve good matching properties large transistors should be used. Increasing the device width \( W \) is not critical since both current and capacitance increase by the same amount, hence the timing properties of the inverter stay approximately the same. The device length \( L \) cannot be chosen arbitrarily large since increasing \( L \) raises the load capacitance and decreases the drive current. The transistor sizes finally used where found by simulations on the extracted layout with included parasitic capacitances. The length of the starving transistors was chosen to be 1 \( \mu \)m.
Figure 6 shows the schematic of the charge pump.

Phase detector and charge pump

In this design a simple bang-bang phase detector [5] was used where the delayed signal is sampled by the non-delayed clock signal. The decision of the phase-detector therefore is maintained during a whole clock period. The phase detector consists of a symmetrical flip-flop implementation with cross-coupled RS-latches [5]. Care was taken that both input signals are loaded with exactly the same capacitances.

The charge pump conducts small currents to and from the loop capacitor, according to the decision of the phase detector. The change of the control voltage $\Delta V_C$ per cycle calculates to $2.5\text{mV}$ according to

$$\Delta V_C = \frac{I \cdot \Delta t}{C},$$

with $I$ being the current in the charge pump ($2\ \mu A$), $\Delta t$ the integration interval (25 ns), and $C$ the value of the integration capacitor (20 pF). Because of the bang-bang phase detector structure, the control voltage will steadily oscillate around an average value. Hence, the smaller the voltage change per cycle the less jitter is to be expected.

Figure 6 shows the schematic of the charge pump. Transistors T1 and T2 define a reference current, which is taken over by a current mirror (T3-T4) controlling the gate-source voltage (and the drain current) of the PMOS transistor T13, actually pumping charge to the loop capacitor. If transistor T10 is switched on then $V_{GSD}$ of T13 will be lower than $V_{DSS}$, and hence no current will flow to the capacitance. T9 functions as a resistor assuring that $V_G$ of T13 will not be reduced to zero in order to be able to quickly switch on T13. To reduce the amount of charge on the integration capacitor, T14 is used which in turn gets its gate-source voltage defined by current mirrors consisting of transistors T5-T8.

Driver circuits convert the control voltage at the output of the loop filter to the gate source voltages $V_s$ and $V_p$ of the NMOS and PMOS starving transistors. In order to avoid long oscillation cycles in the control loop it is necessary that the gate voltages change as fast as possible. Using big transistors result in small timing constants and fast transient behaviour, but also in high consumption of static power. So there is a trade off between power consumption and jitter. In this design, the time constant of the starving transistor drivers is approximately one clock cycle (25 ns). The second function of the starving transistors drivers is to provide buffering between the control voltage $V_c$ and the gate-source voltages of the delay stages, thus avoiding coupling from the delay channels to the integration capacitor.

2.2. The conversion cycle

Header identification and phase detection

The mixed signal data packet sent by the front-end chip (SCT128A) consists of a 4-bit digital header pattern, 3 calibration levels (used for calibration of the analog optical link), 128 channel-data and a 9-bit digital trailer (Figure 7).
The CSC uses a finite state machine (FSM) with one-hot encoding for header detection and identification. In order to start a conversion cycle, the consecutive reception of a correct bit pattern (0101) is required. This decreases the probability of detecting non-existing data packets due to noise on the data line. The FSM contains a auto-reset circuit.

![Figure 8. Block diagram of the phase detection units](image)

The phase detection units use the 25 clock signals supplied by the DLL to latch the incoming data. The contents of these latches are continuously processed in order to determine the phase of the data packet relative to the local clock. The phase information for every rising edge coming in on the data line is stored for one clock cycle using a 1-of-25 code (Figure 8). In case of a successful header identification these data are sent to the clock selection circuit, which updates the phase of the output conversion clock. Thus the output phase is readjusted for each data packet.

**Generation of the control signals**

On arrival and identification of a data packet, a 9-bit counter is initialized and starts operating depending on the mode set by the CONFIG bit. On the line PACKET, a 25 ns pulse is put out indicating the start of a conversion cycle. The DATA_Valid signal goes active on the first analog data value. At the beginning of the trailer, DATA_Valid is reset and the signal indicating the trailer data becomes active. A 9-bit word (1 bit overflow flag, 4 bit BCO number, 4 bit L1 number) is put out in serial. This constitutes the end of one readout cycle and the CSC goes back to its initial state and starts monitoring the data line for the next data packet. In two-chip mode, 2 data packets from adjacent front-end chips are joined together sequentially. In this case, the trailer of the first packet and the header of the second packet are being ignored by the CSC. The DATA_Valid signal goes low during this period and becomes active again at the beginning of the analog data sequence of the second chip. The additional information is extracted out of the second trailer (both trailers contain identical data).

---

2.3 Self calibration and numerical phase correction

In order to correct the phase of the output conversion clock for changing delays due to temperature or process parameter variation or different load capacitances, a self-calibration structure was incorporated in the chip. It consists of a dummy signal path that represents the path of the conversion clock through the chip including the output buffer. From the output pad, which can be loaded with the actual load capacitance, the signal is fed back into the chip. A second phase detector permanently measures the signal delay in multiples of 1ns and stores the result as 5-bit binary code. This number is utilised to tie the positive edge of the output clock to approx. 1 ns before the end of each data time slot.

The contents of a 5-bit register can be used to select earlier clock phases in 1ns steps to accommodate timing requirements of different A/D converters. The register can be loaded any time and has a separate reset line.

3. MEASUREMENT RESULTS

A prototype version was fabricated in a standard 0.8μm CMOS process (AMS\(^1\) 0.8μm CYE). The chip shows full functionality and performance within the design specifications.

Performance measurements on the prototype ASIC prove that the desired timing resolution can be obtained with sufficiently low jitter and good linearity. The output clock jitter scales linearly with the delay cell number and is mainly due to the up-down cycles in the feedback loop. The jitter was measured to peak at 185 ps r.m.s. for the last delay cell.

![Figure 9. RMS jitter vs. delay cell number](image)

The phase detection circuit actually works as a “phase-to-digital converter” that uses the clock phases from the delay line as timing references. The worst case

---

\(^1\) AMS® – Austria Mikro Systeme International AG, Unterpremstätten, Austria.
integral non-linearity of the converter was measured to be 325 ps (Figure 10). The step width varies from 500 ps to 1375 ps showing a Gaussian-like distribution with a sigma of 156 ps, providing a measure for the differential non-linearity of the phase detector (Figure 11). Due to the locked loop architecture, there is no gain error in the transfer function (the mean of all delay step values is 1).

The characteristic curve of the auto-calibration circuit in Figure 12 shows the correction of the output clock phase as a function of the load capacitance at the EXT_CAP pad.

4. CONCLUSIONS

CSC, a mixed signal data receiver/clock synchronizer ASIC to be used with analog front end chips in LHC experiments has been designed and implemented in a standard 0.8μm CMOS process. The prototype shows full functionality and performance within the design specifications. A ROD level A/D conversion unit for the ATLAS analog readout scheme using the CSC is under construction.

ACKNOWLEDGMENTS

The authors would like to acknowledge J. Christiansen, P. Moreira, E. Cantatore and B. Van Koningsveld for valuable support and discussion throughout the realization of this work.

REFERENCES


[6] J. Kaplon et al., DMILL implementation of the analogue readout architecture for position sensitive detectors at LHC experiments, this proceedings.
TWO 2-STAGE TRANSIMPEDEANCE AMPLIFIERS FOR SILICON DRIFT DETECTORS READOUT

G. Mazza, INFN, Torino, Italy (email: mazza@to.infn.it)
A. Rivetti, Politecnico and INFN, Torino, Italy (email: rivetti@polgen1.polito.it)

Abstract

Two 2-stage transimpedance amplifiers have been developed which match the requirements of the front-end of the Silicon Drift Detectors (SDD) in the ALICE experiment. In this paper the architecture of the circuits is described and lab measurements are presented.

1. DESIGN SPECIFICATIONS

The requirements of the front-end electronics for the ALICE SDD are discussed in detail in [1] and [2] and can be summarised as following:

- Maximum input signal (charge): 10 mip
- Maximum input signal (current): 1.6μA
- Equivalent input noise charge (E.N.C.) < 500 e-
- Input current noise < 2nA r.m.s.
- Power consumption: < 1mW
- Input capacitance (detector capacitance + bonding wires and stray capacitances) < 2pF.
- Capability to work with power supplies down to 3.3 V

In addition, a fast peaking time (< 30ns) is a useful feature that can improve significantly the separation of close tracks.

The presented circuits have been designed to meet all of the previous constraints.

2. DESIGN ARCHITECTURE

When fast peaking times are desired, a transimpedance amplifier is a suitable configuration [3], [4].

Moreover, to decrease the power supplies to 3.3 V, we limited the maximum output signal to 1.5V. If this is the case, the transimpedance gain required can be calculated as:

\[ \frac{V_{\text{out}}(\text{max})}{I_{\text{in}}(\text{max})} = \frac{1.5V}{1.6\mu A} = 940k\Omega \]

For the lowest signals of interest, which are in the nA range, this gain will give an output of few millivolts, thus requiring a waveform digitizer of high sensitivity (at least 10 bits on a scale of 1.5 V)

A possible alternative is to use a non linear amplifier. In CMOS technology a non linear transimpedance amplifier can be easily implemented using a MOS transistor as the feedback element [5]. We found the design proposed in [5] extremely interesting for our application because:

- The non linear transfer function relies on the behavior of a single MOS transistor, which is physically well understood and mathematically well modeled.
- With a proper design of the feedback element, the equivalent transimpedance can be quite high (hundreds of kΩ or more). The contribution of this resistor to the system noise is then very low.
- A second order transfer function is achieved in a single stage, saving area and power.
- The pulse shape can be optimised acting on a bias voltage, which makes the system very robust against variation of the input capacitance.

Our implementation of this scheme is reported in fig. 1.

![Fig. 1 Schematic of the transimpedance amplifier](image-url)
If we look at fig. 1, we can notice that this configuration can provide two outputs: a voltage output at node OUT_V, which is proportional to the square root of the input current and a current output at the node OUT_I, which is proportional to the input current [5]. The second stage can be either a linear voltage amplifier connected to node OUT_V or a transimpedance amplifier connected to node OUT_I.

In the former case a square root signal compression is achieved in the input stage. In the latter, the square root compression can be achieved in the second stage if this has the same circuit topology of the input one.

3. DESIGN IMPLEMENTATION
Both solutions described above were implemented on silicon in a standard 0.8μm CMOS process, in a single chip containing eight channels of each type. Fig. 2 depicts the configuration which uses a voltage amplifier as the second stage. In the technology used, high value linear resistors were not available, so, to minimise power consumption, a differential pair with local feedback was the preferred solution. In this way, also a differential output is provided.

Design guidelines for this kind of amplifiers can be found, for instance, in [8].

Fig. 2. Transimpedance amplifier with voltage gain stage

Fig. 3 depicts the alternative solution, in which the input stage works as a current amplifier. Compared to the previous one, this solution has the advantage that no passive component is required. If we look at fig.2, we see that there is the need to provide a reference voltage to the differential amplifier. On the other hand, in the circuit represented in fig. 3 the dc current flowing from the first into the second stage is so high and needs to be compensated. Both problems were addressed with the use of dummy structures. In this way, there is no ac coupling in the signal path. The amplifier is completely dc coupled to the detector and the detector leakage current can be measured.

The total small signal gain is adjusted to 2MΩ in both circuits for a peaking time of the pulse response of 25ns. The layout area is 100μm x 270μm for the circuit of fig. 2 and 100μm x 220μm for the circuit of fig. 3.

4. LAB MEASUREMENTS
The two circuits were first tested at the bench with a dedicated set-up and then connected to a silicon drift detector used in a test beam at the CERN SPS. The analysis of the beam test data is still very preliminary. We concentrate here on the tests at the bench. The main results are summarised in table 1 for the circuit of fig. 2 and table 2 for the circuit of fig. 3, respectively.

| Tab. 1 Measured parameters for circuit of fig. 2 |
| Small signal gain | 2MΩ (single ended) |
| Current input noise | < 2 nA r.m.s |
| Output voltage swing for | 0.75V(singled ended) |
| power input | 1.30V(differential) |
| Power consumption | 680 μW |
| Power supplies | 3.3V |

| Tab. 2 Measured parameters for circuit of fig. 3 |
| Small signal gain | 2MΩ |
| Current input noise | < 2 nA r.m.s |
| Output voltage swing for | 1V (Only single |
| power input | ended output available in this scheme) |
| Power consumption | 800 μW |
| Power supplies | 3.3V |

Fig. 3 Current amplifier with transimpedance gain stage
The cross talk between channels was below 2% for both circuits.

The small signal gain variation was around 2% for channels on the same chip and 4% for channel on different chips for both circuits as well.

The chip were also tested in a large signal condition, with input signals up to 2µA, in order to study the nonlinear behavior. As we have seen in sec. 2, in fact, this property could be used to compress the signal at the amplifier level, thus decreasing the resolution required for the waveform digitizer (i.e. analog memory + ADC) from 10 to 8 bits [1].

As an example, in fig. 4 we report the fits on the data measured on two channels which use the voltage amplifier as the second stage (see fig. 2).

The output voltage was chosen as the independent variable and the data were fitted by a simple parabolic law: 

$$y = p_1 \cdot x^2 + p_2 \cdot x + p_3$$

It can be seen that a parabolic fit is very good for input currents up to 700nA. In case of the Silicon Drift Detectors in ALICE, this value corresponds to an input charge of about 5 mip. The fact that the data follow a quadratic law is in good agreement with the fact that the nonlinear element is a MOS transistor working in the saturation region.

In fig. 5 is reported the behavior of the two channels for input currents up to 1.6µA, which correspond to a charge of about 10 mip

We notice that here the curves can be better approximated by a polynomial fit of the third order. This indicates that for higher levels of current the nonlinearities in the stages following the input transimpedance amplifier become important.

This effect is basically due to the differential voltage amplifier and results in a stronger compression for the largest input signals.

A more robust voltage amplifier with improved linearity for large signals is now under development. If the second stage is linear also for large swings, in fact, a very simple quadratic function can be used for the whole dynamic range. The homogeneity of the compression curve between different channels is improved as well.

---

**Fig. 4** Fit of the non linear input-output relationship of two different channels of the circuit of fig. 2. Compared to fig. 4 the input signal is extended to 1.6µA (10 mip)

**Fig. 5** Fit of the non linear input-output relationship of two different channels of the circuit of fig. 2. Compared to fig. 4 the input signal is extended to 1.6µA (10 mip)
In fig. 6 is reported the input-output curve for the circuit of fig. 3. Here the parabolic fit is a good approximation for the whole dynamic range.

![Graph](image)

Fig. 6 Fit of the non-linear input-output relationship of the circuit of fig. 3.

5. CONCLUSIONS

Two non-linear transimpedance amplifiers have been designed in a 0.8μm CMOS technology.

The basic features of the circuits are a fast peaking time, a low noise and a low power consumption.

The lab measurements show that these circuits can meet the specifications required for the front-end of the Silicon Drift Detectors in the ALICE experiment.

6. REFERENCES


DEVELOPMENT OF MEDIA INTERFACES FOR GBIT/S FIBRE-OPTIC LINKS

Tivadar Kiss, Bertalan Eged, István Novák, Attila Teleggy, István Gelencsér
TU of Budapest (BME MHT), Goldmann Gy. tér 3., H-1111 Budapest, Hungary;
György Rubin, CERN, CH-1211 Geneva 23, Switzerland;
Zoltán Meggyesi, László Szendrei, György Vesztergombi, KFKI-RMI, H-1525 Budapest, P.O.Box 49, Hungary

Abstract
An experimental 1.0625 Gbit/s fibre-optic media interface has been developed within the framework of the ALICE collaboration. First it has been used on the Destination Interface Unit (DIU) card in the ALICE Detector Data Link (DDL) project. The results of this development have also been applied in the design of the 2nd version interface cards in the Fibre Channel S-LINK project. These applications raised different constraints for the design of the PCB layout, signal routing, cross section, and power supply. The different realizations of the same media interface circuit gave us the opportunity to carry out thorough tests and measurements to compare and evaluate the different solutions used in the design of these PCBs.

1. INTRODUCTION
In a previous project, two media interface test boards (MI1 and MI2) were built in order to test the available electrical and optoelectronic interface components and gain experience about designing PCBs of digital circuits working at gigabit/s signalling speed. On MI1, we used Vitesse VSC7125 10-bit electrical transceiver chip and Methode MDX-19 optical transceiver module, on MI2 we used HP HDMP-1526 electrical transceiver chip. On MI1, we tried the so-called buried capacitance technology to improve the power supply decoupling.

The following tests and measurements were carried out on the experimental MI test boards:

Bare board measurements
  • Buried capacitance evaluation
  • Matched-trace impedance verification
  • Impedance-limit verification

Component measurements
  • Bypass capacitors
  • Decoupling inductors
  • Optical transceiver input impedance

Signal integrity tests
  • Noise amplitude and spectrum
  • waveform measurements

As the result of these tests we chose the Vitesse chip against the HP one, and decided to keep the 'buried capacitance' when other constraints on the PCB cross section allow this.

After these preliminary studies we started to design the media interface part of optical link interface cards in the ALICE DDL project. The same results were used in the S-LINK project, too, building the new version of the S-LINK interface cards.

In the DDL project, the DIU (Destination Interface Unit) has been designed first. To help the designers of the logic parts of these cards, we chose a 20-bit wide data interface at 53.125 MHz clock speed instead of the 10-bit wide interface at 106.2 MHz. This had become possible, because Vitesse released the 20-bit version of his transceiver chip, VSC7126. Otherwise, this chip has the same characteristics as the 10-bit VSC7125.

In the S-LINK project, the first version of the Fibre Channel S-LINK cards used a standard GLM (Gigabit Link Module) daughterboard as the media interface. As this daughterboard requires a lot of space and costs a lot, we improved the FC S-LINK cards by integrating the media interface on the board. With VSC7126 we were able to keep the original 20-bit data interface, did not have to move to 10-bit.

The DDL SIU (Source Interface Unit) card is the next link card where the same media interface will be applied.

These link cards have the following common block diagram. Figure 1.
The media interface circuit has TTL compatible, 20-bit-wide data interface at 53.125 MHz clock speed. The Fiber Channel compatible electrical transceivers make the serialization/deserialization of the encoded data. The serial encoded data is transmitted and received at the rate of 1062.5 Mbit/s. These differential PECL signals are connected to the optical transceiver module that can be Fiber Channel or Gigabit Ethernet compatible. (FC optical transceivers are designed to work at 1062.5 Mbit/s, while Gigabit Ethernet transceivers can work up to 1250 Mbit/s.) The optical interface is a duplex SC connector compatible with Fiber Channel and Gigabit Ethernet standards. For the simplest test setup, the optical signal can loop back to the receiver.

The main features of the media interface design on the DIU card can be seen in Figure 2.

These applications raised different constraints on the design of the PCB layout, signal routing, cross section, and power supply. We laid emphasizes on the careful layout design keeping the general rules of high-speed board design and the instructions in the application notes of the components used. However, it was not possible to keep every rule without compromise everywhere because of the constraints of the actual physical arrangement.

The main difficulty in the design of the FC S-LINK card has been that the same single PCB layout has to serve 4 different mounting options. These are the combinations of the following two alternatives:

- copper media (skipping the optical transceiver module) – optical media
- Media connector mounted on the top side – bottom side of the PCB.

This was possible only with multiple signal traces and cutting the unnecessary traces off from the signal path to prevent harmful stubs.

The DIU card is a small form factor PCB populated with components very densely. This raised difficulties for the optimal routing of the signal traces. The SIU card will have an even smaller size meaning a real challenge to design and route the PCB.

2. MEASUREMENTS

The different realizations of the same media interface circuit gave us the opportunity to carry out thorough tests and measurements to compare and evaluate the different solutions used in the design of these PCBs.

We carried out a lot of measurements on the DIU and FC S-LINK boards. We measured the followings:

- Waveforms of the critical signals.
- Jitter of the high-speed serial signals
- Power supply noise amplitude and spectrum

The following instruments were used in these measurements.

- HP 54120 oscilloscope mainframe
- HP 54121T TDR unit
- HP 8593E

2.1 Measurement of the serial signals

In this paper I would like to show some of the measurement results. We looked at the signal quality of the serial transmit signals (TX+, TX-) at the input of the optical transceiver module, and the receive signals (RX+, RX-) at the input pins of the deserializer while
using different optical cables and optical attenuators to loop the light back to the receiver.

On the S-LINK card we used the MDX-19-6-1-S optical transceiver from Methode. On the DIU card we tried two different ones: MDX-19-6-1-S from Methode and 86990-9010 from Molex. They are pin compatible and both are compliant to the Fibre Channel standard.

The setup for measuring the waveforms of the serial signals can be seen in Figure 3.

![Figure 3](Image)

We tested the receive signals (RX+, RX-) at different conditions of the input optical signal. As the reference, we used a short (5m) optical cable to loop back the light to the receiver. The optical budget (simply: the maximum attenuation of the optical signal along the optical cabling) can be 6dB according to the Fibre Channel standard. We inserted about 7.3dB attenuation in the optical cable and looked at the degradation of the signal at the electrical output of the optical receiver. We also tested this with about 240 m long optical cable. (The maximum distance in the ALICE DDL setup is 200 m). This caused much less attenuation but more dispersion of the optical signal received.

These measurement results can be seen in Figure 4 – Figure 11. Typical signal waveforms can be seen in these figures. The reason for the small distortions on the transmit waveforms were identified. On the transmit lines it happens because of the reactance of the internal input terminations of the optical module.

The signal shapes are clean, noise and jitter are quite low. Although the test setups were not always exactly the same as it is required in the standard (we had limitations on the instruments available) we can say that these components satisfy what they promise in the datasheets and in the standard.
DIU: Molex OT - 5m cable

DIU: Electrical loopback with microcoax (OT is removed)

DIU: Molex OT - 5m cable and cca. 7.3 dB attenuation

DIU: RX+ jitter measurement

DIU: Molex OT - cca. 245 m cable

DIU: Noise Spectrum at Different Points on the Card

Figure 7

Figure 10

Figure 8

Figure 11

Figure 9

Figure 12
2.2 Noise measurements

The power supply noise levels were measured at several places on the board. The amplitude of the noise is low, it is below the level that can cause problems in the operation of the media interface. The peaks of the noise amplitude are less then <150mV during long periods of collecting measurement data while transmitting "worst case" data patterns that cause the maximum simultaneous switching in the circuits of the board. Some typical noise spectrum figure can be seen in Figure 12. There is very few noise propagated back to the power supply.

3. CONCLUSIONS

The media interface circuit on these prototype link interface cards work well, and they can be used in the next versions of these cards, too.

Signal integrity questions can be handled in such 1Gb/s serial media interface card designs. With careful PCB design the harmful distortions and noise can be avoided. Buried capacitance and careful placement of the discrete decoupling capacitors make quiet board.

4. REFERENCES

6. Fibre Channel Physical and Signalling Interface (FC-PH); ANSI X3.230-1994
8. Gigabit Ethernet (1000Base-Sx); IEEE-802.3z
Test of Alice DDL: Test Setups and Test of ALICE DDL Integration to ALICE TPC Test System

Péter Csató, Ervin Dénes, György Rubin, János Sulyán, Dénes Tarján, Balázs Vissy for ALICE Collaboration, KFKI - Research Institute for Particle Physics, Budapest, Hungary

Abstract

The Detector Data Link (DDL) has been developed to constitute a standard interface between the ALICE sub-detectors and the DAQ system.

In this paper we present the test environment and the application software library made for supporting the DDL development and its integration into the ALICE detector system.

The test setups contain VME64 crates, MVME processor cards, a VMETRO analyser, a logic-analyser and Read-out-Receiver (RORC) and Destination-Interface-Unit (DIU) cards. They made possible to measure the maximum throughput of the full read-out chain and also to measure the transmission latencies. They support the functional and long-term stability tests as well.

1. INTRODUCTION

The ALICE Detector Data Link (DDL) [1] will interface the Front-end Electronics (FEE) of all the sub-detectors to the Data Acquisition System (DAQ). The DDL consists of a Source Interface Unit (SIU) connected to the FEE, a Destination Interface Unit (DIU) connected to the Read-Out Receiver Card (RORC) [2] located in the counting room, and a physical medium which is a duplex optical fibre. Instead of SIU-DIU configuration, DIU-DIU configuration can be used as well, so VME crates can be used at both sides. For test purposes we used the DIU-DIU setup.

2. THE AIM OF THE TEST TOOLS

The aim of the test tools developed in KFKI-RMKI is

- to support the debugging and the low level hardware tests of the DDL components, the RORC and the FEEs;
- to provide test routines for the complete functional tests of the DDL components and the RORC;
- to provide test procedures for the long term stability, the performance and the qualification tests of the complete DDL chain (the RORC is included);
- to provide library routines for the software developers of the front-end and the DAQ sub-systems of the TPC test system.

3. THE TEST SETUPS

The DDL developers and users can use the following setups to execute DDL functionality and stability test:

![Figure 1: The DDL concept](image1)

![Figure 2: Test setups](image2)
4. SUPPORTED HARDWARE

During our tests we used VME64 crate using two different single board computers running under three different operating systems:
- MVME2604 PowerPC under AIX 4.1
- MVME2604 PowerPC under LynxOS 2.5.1
- Motorola VME166-6840 under OS9 V24

5. STABILITY AND TIME MEASUREMENT TESTS

For the task-to-task stability and time measurement test we used the following setup:

In 64-bit block mode in one direction the maximum throughput was 34 MB/s.

During measurements several hundreds GBytes data have been transferred without any error.

We used different data patterns, such as:
- Incremental data
- Chess board pattern
- Walking 0's and 1's
- Random data.

For the average time for sending one command we got 6.4 μs.

We also made successful stability test with random data length.

6. STABILITY TESTS USING THREE RORCS

Figure 5 shows the test setup we used for three RORCs tests.

We used the above test setup because a similar configuration is to be used in ALICE TPC prototype test. Several GBytes data have been transferred without any error.

Data patterns used:
- Incremental data
- Walking 0's and 1's

We also made successful stability test with random data length.
7. DDL INTEGRATION IN ALICE TPC PROTOTYPE (NA49)

The first version of DDL will be integrated and tested in ALICE TPC prototype test beam run in September 1998 [3]. A DIU-DIU setup will be used as shown in figure 6.

Figure 6: The DIU-DIU configuration used in DDL integration

The 2 versions of the integration setups:

Two different use of DDL will be possible.

Version 1.
- All (max. 32) events in one spill are measured and data stored with local event numbers in the Front-end Crate’s LynxOS memory.
- When the central DAQ requires a given event the Receiver Crate’s processor requests it and the Front-end Crate transfers it to the Receiver Crate’s RORC memory, where the further move of the data is carried out by the central DAQ side.

Version 2.
- The Front-end Crate collects data when the trigger arrives
- and transfers this data to the RORC memory of the Receiver Crate automatically without any command from the Receiver side.

Results of time measurements using the integration setup:

We made time measurements for both possible use of DDL. We got the following results:

In the case of version 1 the time between the data request and event arrival into the Receiver Crate’s RORC memory was measured:

<table>
<thead>
<tr>
<th># of words</th>
<th>Time in ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>0.14-0.15</td>
</tr>
<tr>
<td>500</td>
<td>0.21-0.22</td>
</tr>
<tr>
<td>10000</td>
<td>27-0.28</td>
</tr>
<tr>
<td>50000</td>
<td>88-0.89</td>
</tr>
<tr>
<td>10000</td>
<td>1.65</td>
</tr>
<tr>
<td>50000</td>
<td>7.75</td>
</tr>
<tr>
<td>60000</td>
<td>9.25</td>
</tr>
</tbody>
</table>

In the case of version 2 the time between the SW trigger and event arrival into the Receiver Crate’s RORC memory was measured. This time contains two VME transfers and the DDL transfer time.

<table>
<thead>
<tr>
<th># of words</th>
<th>Time in ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>17665</td>
<td>8</td>
</tr>
<tr>
<td>66000</td>
<td>26</td>
</tr>
</tbody>
</table>

8. SUMMARY

We can summarise the results of DDL stability and integration tests as
- No problem found during functional and stability tests, all tests were successful.
- The transfer speed reached the limit of the operating systems and the hardware.
- ALICE TPC prototype integration requirements fulfilled: data arrives to DAQ side in 70 ms after the trigger.

REFERENCES:

Abstract

The ALICE Inner Tracking System (ITS) will be equipped with two layers of silicon strip detectors. The experiment is designed to cope with high particle multiplicity anticipated at $dN/dy = 8000$ for Pb-Pb collision. In this case, silicon strip detector cannot be daisychained, and each detection channel has to be connected to one readout channel. It has been proposed to connect the front end electronics to the detectors with micro-cables [1]. Due to the large number of channels ($2.6 \times 10^9$), it is necessary to find an industrial solution for this type of connection to reach a good yield. TAB (Tape Automated Bonding) is a low cost packaging technology, widely used in the microelectronics industry. Not only is this technion suited for this application, but it also allows to test the electronics in realistic conditions.

1. TAB

TAB is a packaging technology developed mainly for the MCM (Multi Chip Module) domain. It consists in replacing the classical bonding wires with a tape of kapton on which copper strips have been etched (see fig. 1).

![fig 1: example of a chip bonded with TAB cable.](image)

The assembly procedure is the following:

- a bare die is bonded on the tape, ILB step (Inner Lead Bonding),
- a plastic frame can be added to each module to make the manipulation easier,
- the module chip + TAB is glued on a substrate (hybrids, printed circuit board).

The only serious disadvantage of this process is to add solder bump on the die bonding pad. To avoid it, Bull and Dassault developed a new process which allows to bond the copper strips directly to the pads. The TAB bonding is fully compatible with the classical wedge wire bonding with a pressure of around 20 grammes.

![fig 2: top view of a TAB flex.](image)

2. ALICE DESIGN PROPOSAL [1]

2.1 SSD layer main requirements for ALICE

The SSD layers in ALICE experiment have the following requirements:

- the OLB area (Outer Lead Bonding) of the TAB is bonded on the substrate.
- Figure 2 shows a top view of a TAB flex.
- This technics has multiple advantages:
  - handling of the chips is easy,
  - full electrical test is possible in realistic conditions allowing Known Good Die concept
  - characterisation can be performed for sorting the chips out (by family gain for example).

The SSD layers in ALICE experiment have the following requirements:

- the OLB area (Outer Lead Bonding) of the TAB is bonded on the substrate.
- Figure 2 shows a top view of a TAB flex.
- This technics has multiple advantages:
  - handling of the chips is easy,
  - full electrical test is possible in realistic conditions allowing Known Good Die concept
  - characterisation can be performed for sorting the chips out (by family gain for example).

The only serious disadvantage of this process is to add solder bump on the die bonding pad. To avoid it, Bull and Dassault developed a new process which allows to bond the copper strips directly to the pads. The TAB bonding is fully compatible with the classical wedge wire bonding with a pressure of around 20 grammes.

![fig 2: top view of a TAB flex.](image)
• double sided silicon strip detector: 42 mm * 75 mm,
• 35mrad stereo angle between P and N sides,
• 95μm pitch for the micro-strips,
• each detector equipped with its own front end electronics (6 chips per side),
• 768 strips per side of detector,
• 2.6 x 10^6 channels,
• FEE cooling required,
• minimum of material (radiation length).

Bonding directly from the detector to the FEE is not possible due to the pitch mismatch (44μm for the FEE).

2.2 Technical solution

In order to achieve the requirements listed above, the design of silicon strip layers has to follow these constraints:

• flexible connection between FEE and detector to allow the readout electronics to be on the same side of the detector for cooling and cabling considerations,
• pitch adaptation from 95μm (detector) to 44μm (FEE),
• industrial process to achieve a yield of more than 97% of good channels.

The following design is the result of this analysis. It has been proposed for the SSD at STAR of which R&D is common with ALICE (fig. 3).

In order to connect the silicon strip detector to the FEE, the TAB must be bonded on pads in staggered row. Figure 4 shows that it is feasible.

Another problem to solve was to fabricate a tape with the pitch of the FEE, ALICE128C [3], which is 44 μm and far below the standard of the tape manufacturer (100μm). A solution using the fact that the front end electronics input pads are also in staggered row has been accepted (figure 5) and is in prototype phase.

![fig 4: TAB bonded in staggered row (photography provided by Bull).](image)

The 2nd and 3rd quarter of the input lines are going straightforward from the detector to the FEE, while the 1st and the 4th quarter are routed in a kind of U-turn. This will add certainly some difficulties in the readout order, but should not be a big issue.

![fig 4: schematic view of the TAB design](image)

The windows opened in the kapton tape are for two purposes:

3. TAB DESIGN SOLUTION

3.1 Tape design

A solution to connect the double sided silicon strip detectors of ALICE and STAR to the front end electronics is being developed. The use of micro-cables led to the TAB technology.
to allow the copper strip to be bonded,
to allow the tape to be bent, in order to achieve
the module as previously shown in figure 3.

An extra window has been designed, called ‘Bending
lines for input tracks’. Its purpose is to avoid the input
lines to run over the chip close to the output of the
preamplifiers, by bending the lines on top of the others.
The reason of this extra window is to avoid crosstalk
from the preamplifier or shaper outputs to the inputs
which could generate noise or even worse, oscillations.

3.2 Radiation length

The material involved gives a radiation length for the
tape of 0.056 % which is mainly due to the strips made
of 17.5μm copper. This result can be improved if an
aluminium technology is used, available in Ukrainia,
but still in development to automatize the assembly
procedure.

4. ASSEMBLY AND TEST SCHEDULE

To perform several tests in realistic conditions, extra
lines can be designed on the tape including a pitch
adaptator to standard JEDEC pads. Once the chip is
bonded on the tape, the module is mounted on a plastic
frame and can be inserted in a ZIF socket for testing.
All of this extra material is cut and removed before the
assembly on the substrate. With those extra lines, it is
possible to have a direct access to the input pads of a
preamplifier and then to inject charges in the same way
as a detector does. This will allow the users to test the
connection and to perform the calibration of the
electronics, for example.

A scenario of the different steps of the FEE-detector
assembly can be the following:

- GO-NOGO test of the electronics on the wafer
  with a probe station (performed by the founder),
- detector test (leakage current, capacitor ...),
- ILB bonding of the electronics on the tape,
- test, calibration and burn-in of the electronics,
- FEE mounting on the hybrids and OLB bonding,
- bonding of the detector.

5. CONCLUSION

The use of the TAB technology seems to be very
promising for vertex detectors where a large number of
connection is necessary with a strong constraint of
room and radiation length. A prototype is in preparation
to fully demonstrate the feasibility of the concept.
Figure 5 shows the design of the tape approved by the
tape manufacturer.

REFERENCES

IRes, SUBATECH, August 1998
[3] ‘ALICE128C : a CMOS Full Custom ASIC for the
Readout of Silicon Strip Detectors in the ALICE
Experiment’ Proceedings of the Third Workshop on
Electronics for LHC Experiments, London, September
1997.
A Standard Cell based Content-Addressable Memory System for Pattern Recognition

A. Cisternino, I. D'Auria, W. Errico, G. Magazzu, F. Schifano
I.N.F.N. - Sezione di Pisa
(email: gmagazzu@galileo.pi.infn.it)

Abstract

We have designed a single chip processor for track finding based on a Content-Addressable Memory (CAM) architecture. The processor has a rather large CAM bank and all the glue logic needed for easy interfacing to a DAQ system. Our design has been tailored to the requirements of a present generation experiment. Our design methodology (logical synthesis on a Standard Cell technology) makes upgrades to new technologies or to different environments straightforward and quick to implement.

1. INTRODUCTION

Track finding in high energy physics experiments is an extremely demanding combinatorial and computational task. In this area however substantial benefits derive from dedicated hardware systems for pattern recognition.

One possible approach to the problem is to enumerate (at least in principle) all the configurations of hits in the various layers of the detector and to store all the "interesting" ones, i.e. those compatible with tracks associated to physically relevant events.

When an actual event occurs, one particle track is found if the actual set of hits matches one of the stored configurations. All kinematic parameters of the track are immediately available.

Comparing actual tracks to stored configurations is a computational demanding task which lends itself very well to a full parallel implementation in hardware, as done in Content Addressable Memories (CAM), where each interesting configuration (pattern) is stored as a given set of coordinates (hits), one to each layer. Data coming from detectors are compared with them on the fly, keeping up with detector readout speed. The result of the comparison is the address of the matched pattern.

In practice track enumeration is not possible at full resolution in present (or future) generation experiments. Combinatorial complexity can be reduced combining adjacent detector channels in large bins ("fat bins"): in this way a coarse track finding is obtained that requires further more traditional processing to extract all the physical parameters. The post-processing becomes obviously simpler if large sets of patterns can be stored (that is, if large CAM devices are available).

Unfortunately CAMs are not readily available as off-the-shelf components. Several groups have tried to develop custom CAMs in recent years.

A full custom VLSI [1,2,3] approach produces high density and high performances, but requires high development efforts and costs. Also, upgrades to new VLSI technologies require a full redesign. This is probably the single most serious drawback of this approach. Commercial FPGAs feature low development efforts and costs [4,5], but their densities are by far lower.

A Standard Cell VLSI design is a balanced approach, optimizing a combined measure of density and technology scalability.

We have explored this option, designing a complete CAM system, centered around a Standard Cell ASIC which uses a state-of-the-art CMOS technology. We are mainly interested in two issues: the number of patterns that can be stored in a reasonably sized system and the effort going into the design of the ASIC, since these parameters are important to assess the potential applications of a similar (suitably-scaled) system in an LHC environment.

With the aim to make our exercise a project complete in all the details, we have followed the specifications of the Silicon Vertex Tracker (SVT) of the CDF experiment, whose architecture use the CAM system developed in [2].

2. A STANDARD CELL BASED CAM SYSTEM

2.1 Specifications for a CAM system

The CDF SVT architecture is described in details elsewhere [6,7]. For our purposes is important to remark that SVT has six layers (and could be upgraded to eight). Each layer is divided into a large number of bins. As seen by the CAM based track finder, bins are grouped together into fat bins. These are addressed by 12-bit within each section of 30° of the detector. Three more address bits identify the layer.

CDF plans to use 32K patterns for each detector section on which track finding is performed. One pattern is identified by six (eight) 12-bit words.

At run time each CAM system receives 15-bit input data words representing actual hits on actual layers.

In the framework of our exercise one may ask either if the size of the data bank can be substantially increased or if the complexity of the hardware can be reduced keeping the data bank size fixed.
2.2 The CAM system building block

We have designed a Standard Cell based CAM system centered on an ASIC which uses a state-of-the-art technology. Our building block is made by a memory bank with an integrated matching logic which compares each pattern with input data associated to actual events and by a readout logic. Our goals were a high density pattern bank and an easy to upgrade system.

A schematic design of our architecture is shown in Fig.1. The Memory Bank contains the patterns to be compared with actual events searching possible matches. We can imagine the Memory Bank divided into rows. Each row (labelled by its own address) is loaded at startup with one pattern. At run time actual events arrive onto the chip layer by layer on the Data_in bus and are compared on the fly with the contents of the corresponding layer of all the rows. The Memory Block produces in output the list of matched layers. An independent list is available for each row. The list is accumulated on the output of the Memory Bank, as successive hits belonging to the same event arrive to the chip.

The Filter module uses the information coming from the Memory Bank according to algorithms and for each row produces the address of the corresponding pattern in case of a match. A pattern is matched when there is a match in at least \( n \) among a given subset of \( N \) layers. Several combinations of the threshold value \( n \) and of the subset specification can be stored in the chip at startup and used in sequence on the same event.

Both patterns and algorithms are loaded at startup via JTAG user-defined instructions.

The Collapse module receives the addresses of the matched patterns and presents them in output according to a fixed priority order.

The Readout Logic selects between the output of the Collapse module and the address of a pattern matched in another ASIC. This architecture has two additional benefits: it keeps the results of the comparisons within the chip till the readout logic is able to collect them and makes daisy chaining of several devices logically straightforward and electrically simple.

The Memory Bank represents the largest fraction of the chip in terms of area: different logic structures have been accurately tested in order to minimize the area. Global routing has been reduced as much as possible: the only global signals in the array are input data (vertical lines) and writing/reading controls (horizontal lines) needed to store the patterns. This allows to avoid routing channels and to reach a standard cell density about 25% higher than the average value suggested by the silicon foundry.

The Memory Bank has been physically mapped into an array of Standard Cells. Each row of the array (see Fig.2) contains 12 modules which work in parallel on the 12 bits of the input data. Each module contains 8 latches (one for each layer), a multiplexer 8to1 which selects the value of the stored pattern in the current layer and a XOR gate which compares the input data with the selected stored data. In case of a match in all the 12 bits of the input data the register associated to the current layer is set.

The handmade placement of the array and the locality of connections lead to a very dense structure: this extra effort is however not large in term of time, since the manually placed section of the chip is inherently very regular. In the ALCATEL-MIETEC CMOS 0.35 micron technology we have evaluated an area of 32 sq. mm for an array of 1K pattern: this corresponds to a pattern density of about 3K patterns in one sq.cm. A memory bank of 4K patterns can be therefore made in a die with reasonable dimensions.

Both the Filter module and the Collapse module have been synthetized starting from a VHDL model. No particular efforts in their placement and routing is needed since these blocks represent less than 2% of the area of the chip.

The final device has 1K patterns (eight 12-bit layers for each pattern) in a die-size of 40 sq.mm. About 99% of the total area is used for the memory bank and for the matching logic.
Clock frequency up to 50 MHz can be reached with no particular efforts.

The storage capability of one chip is about 20 times larger than a system which uses state-of-the-art FPGAs.

We have chosen a 1K pattern device in a TQFP100 package as the best trade-off between stored patterns and package dimensions. If a bigger number of I/Os (e.g. if all the layers had to be handled in parallel) were required, a larger package could be used; we could design a chip 4 time larger within the limits of the chosen silicon technology.

A fully scalable system can be built starting from the basic 1K pattern device. We have designed a 32K pattern module (Fig.3) which consists of one array of 4 columns of 8 chips each, plus the necessary glue logic mapped onto programmable devices. Up to 4 modules can be housed in one Extended-VME PCB board: three boards are enough for CDF requirements.

3. CONCLUSIONS

In this paper we have described the design of an integrated track-processor chip, based on a CAM array, that fulfills the requirements of a large present generation experiment.

The device has been designed in a state-of-the-art CMOS technology with a silicon-compiler approach, starting from a functionally tested VHDL model. This approach translates into a fast design turnaround time of the order of 2 to 3 months.

The basic merit of our design are:

- an architecture closely tailored to the application
- a design methodology that allows easy and fast redesign of the device, in order to follow technological developments. We can expect a transition from 0.35 to 0.18 micron CMOS technology in the next few years. We expect therefore that devices with up to 16K patterns can be built in the near future.

Our basic design system could be easily rescaled and adapted in order to meet LHC requirements [8]. For instance LHC experiments may require to handle all the layers of the detector in parallel. This may lead to larger packages with a large number of stored patterns. The pattern density can be unaffected: the same number of patterns can be stored in a smaller number of larger devices. Otherwise one can imagine to use still small packages working in parallel on different subsets of layers.

A different application of our architecture could be the development of a PCI board containing the CAM processor, to be used as a PC-coprocessor for pattern recognition.

A final comment concerns the recent development of off-the-shelf CAM devices, tailored to the needs of network switches. Devices with up to 8K patterns (80 bit wide) have been announced. We remark that the density of these components is not much larger than that available in our design. The main drawback however is that match information cannot be stored in the device. Use of these devices in our architecture would probably need more complex glue circuitry with a (today) limited density advantage. If however large CAM arrays become available in the future, they may make CAM based processors even more attractive.

We thank members of the CDF collaboration for providing us details about the SVT system. Special thanks for illuminating discussions to Paola Giannetti and Stefano Belforte.

4. REFERENCES

FAST PARTICLES IDENTIFICATION IN PROGRAMMABLE FORM AT LEVEL-0 TRIGGER BY MEANS OF THE 3D-FLOW SYSTEM.

D. Crosetto, 3D-Computing, Inc., 900 Hideaway Pl., DeSoto, TX
(email: crosetto@bonner-ibm2.rice.edu)

Abstract

The 3D-Flow Processor system is a new, technology-independent concept in very fast, real-time system architectures. Based on either an FPGA or an ASIC implementation, it can address, in a fully programmable manner, applications where commercially available processors would fail because of throughput requirements. Possible applications include filtering-algorithms (pattern recognition) from the input of multiple sensors, as well as moving any input validated by these filtering-algorithms to a single output channel. Both operations can easily be implemented on a 3D-Flow system to achieve a real-time processing system with a very short lag time. This system can be built either with off-the-shelf FPGAs or, for higher data rates, with CMOS chips containing 4 to 16 processors each. The basic building block of the system, a 3D-Flow processor, has been successfully designed in VHDL code written in “Generic HDL” (mostly made of reusable blocks that are synthesizable in different technologies, or FPGAs), to produce a netlist for a four-processor ASIC featuring 0.35 micron CBA (Cell Base Array) technology at 3.3 Volts, 884 mW power dissipation at 60 MHz and 63.75 mm sq. die size. The same VHDL code has been targeted to three FPGA manufacturers (Altera EPF10K250A, ORCA-Lucent Technologies OR3T165 and Xilinx XCV1000). A complete set of software tools, the 3D-Flow System Manager, equally applicable to ASIC or FPGA implementations, has been produced to provide full system simulation, application development, real-time monitoring, and run-time fault recovery. Today’s technology can accommodate 16 processors per chip in a medium size die, at a cost per processor of less than $5 based on the current silicon die/size technology cost.

1. TECHNICAL OBJECTIVES AND APPROACH FOR A TECHNOLOGY-INDEPENDENT IMPLEMENTATION

1.1 Area of application

The purpose of this project is to design a programmable, scalable, and modular solution for high-speed, front-end applications. Not long ago, front-end electronics were built with analog techniques using discrete components. Later, with the rapid advances in digital technology, Digital Signal Processors (DSPs) replaced analog circuitry up to certain speeds. However, in many applications the user still had to design a specific hardware to implement an algorithm on the front-end signal from a detector (or sensors) because the DSPs were not fast enough or flexible enough.

The throughput of this system can fetch as many input data (16-bit for a 16-bit-wide bus structure of the processor) per second from a device (detector) as clock cycles of the technology implementation, yet unlike currently available systems of comparable speed, it is fully programmable and extremely flexible.

1.2 How to design a technology-independent application

The quality and the level of a technology-independent solution are determined by several factors, the most important of which is avoiding the selection of an architecture that leaves insufficient margins in speed or performance beyond the present requirements.

This decision comes at a very early stage, when a solution to a problem is conceived. For example, in the case of the problem of processing thousands of input data at a continuously sustained input data rate of 40 MHz, use of the approach of the 3D-Flow system and selection of a processor speed of at least 80 MHz places the user in a safe position because:

a) the architecture approach allows in principle the acquisition of input data at the same processor speed, and the factor two between input data rate and processor speed is a safe margin;

b) the architecture allows one to run more complex algorithms simply by adding 3D-Flow layers (see Section 2.4) to the system, without having to redesign the entire system. This provides cost optimization for each application without the need to replace the original processors with faster ones;

c) besides de-coupling the parallel processing system from the sensor device, the FIFOs memory at each input port enables the system to sustain input data at a higher peak rate for short periods of time with respect to the nominal 40 MHz.

Other factors that will determine the quality and level of technology independence of a system include:

1. The code should be written in "Generic HDL."
2. The coding "style" should be targeted to ASIC without having an architectural knowledge of the basic elements and routing characteristics of one FPGA versus another (e.g., CLBs from Xilinx versus LEs from Altera versus PFUs from Lucent Technologies).
3. When implementing a design using FPGAs, it is best not to make use of macros (besides the memory blocks), or to manually floor plan the design. The use of macros makes the design not ready for simulation; on the contrary, an HDL behavioral model equivalent to the functionality of the macro must be written. One should submit the same HDL code to the powerful tools provided by the different vendors (Altera, Lucent Technologies and Xilinx) and let the tools optimize the floor plan and routing. In the event one would like to modify the circuit, the additional time needed to go through some manual phases will cost more than purchasing the new component with increased performance.

4. In the case of an implementation in ASIC, it is worthwhile to synthesize the design using different vendor libraries (Cell Base Array, Gate Array, etc.). Some companies are providing tools that help to submit a design using different vendor libraries, keeping track of file handling and results handling for an easy comparison of different technology performances on a specific design.

1.3 Advantages of a technology-independent application versus "ad hoc" FPGAs or ASICs solutions

The cost and time required to design a circuit is minimal with respect to the time required to develop all the tools for testability, simulating, troubleshooting, writing documentation and maintenance of the circuit, and for making provisions to easily implement modifications that one might think beneficial in the future.

The 3D-Flow System Manager (see Section 3) provides the same information and features to the user regardless of the technology chosen to implement the circuit (FPGA: Altera, Xilinx, Lucent Technology, or ASICs).

The same VHDL code is used in all cases: the same tools to initialize the circuits, to download the algorithm through RS232, and to monitor the system in real time through the scratch pad register file in the silicon that memorizes consecutive cycles (see Section 7).

The tools to create a new application with a different system size, different algorithm, different speed, and different input data rate, and to display all information of the system remain the same.

The only variable is the filtering algorithm (consisting of 10 to 20 lines of code that the tools of the 3D-Flow System Manager help the user to generate) that will be downloaded into the system, while an "ad hoc" circuit (FPGA or ASIC) implementing a specific algorithm will require one to develop a set of different tools for testability, accessibility, and maintenance for each application in addition to the need to change the circuit.

2. A SINGLE COMPONENT FOR SEVERAL APPLICATIONS

The main characteristics of the 3D-Flow system architectures based on a single 3D-Flow component are the following:

2.1 System level

Objective:
Oriented toward data acquisition, data movement, pattern recognition, data coding and reduction.

Design considerations:
- Quick and flexible acquisition and exchange of data, but not necessarily in fully bi-directional manner.
- Possibility of dedicating small area to program memory in favor of multiple processors per chip and multiple execution units per processor, data-driven components (FIFOs, buffers), and internal data memory. (Most algorithms that this system aims to solve are short and highly repetitive, thus requiring little program memory.)
- Balance of data processing and data movement with very few external components.
- Programmability and flexibility provided by enabling downloading of different algorithms into a program RAM memory.
- High priority of modularity and scalability, permitting solutions for many different types and sizes of applications using regular connections and repeated components.

2.2 System architecture

The goal of this parallel-processing architecture is to acquire multiple data in parallel (up to the clock speed of the technology implementation) and to process them rapidly, accomplishing digital filtering on the input data, pattern recognition, data moving, and data formatting.

The system is suitable for "particle identification" applications in HEP (calorimeter data filtering, processing and data reduction, track finding and rejection).

The compactness of the 3D-Flow parallel-processing system in concert with the processor architecture allows processor interconnections to be mapped into the geometry of sensors (such as detectors in HEP) without large interconnection signal delay, enabling real-time pattern recognition. This work originated by understanding the requirements of Level-1 (and Level-0) triggers for different experiments, past and present, as well as future trigger designs. Each one has been studied in some detail, with visits to the site of the experiment when possible and attempts to define a system architecture, processor architecture, and assembly architecture that had the commonality features to implement all of them. To maintain scalability with regular connections in real time, a three-dimensional
model was chosen, with one dimension essentially reserved for the unidirectional time axis and the other two as bi-directional spatial axes (Fig. 1).

The system architecture consists of several processors arranged in two-orthogonal axes (called layers; see Fig. 2), assembled one adjacent to another to make a system (called a stack; see Fig. 3). The first layer is connected to the input sensors, while the last layer provides the results processed by all layers in the stack.

Data and results flow through the stack from the sensors to the last layer. This model implies that applications are mapped onto conceptual two-dimensional grids normal to the time axis. The extensions of these grids depend upon the amount of flow and processing at each point in the acquisition and reduction procedure.

Four counters at each processor arbitrate the position of the bypass/in-out switches in order to achieve the proper routing of data. An image-processing application fits this model quite closely. When new data arrive or when the reduction possible with the program executing in one plane is finished, the intermediate data are transferred to the next plane, which has a number of processing elements compatible with the new data extension. Higher-dimensional models were considered too costly and complex for practical scalable systems, mainly due to interconnection difficulties.

2.3 Processor architecture

The 3D-Flow processor is a programmable, data stream pipelined device that allows fast data movements in six directions with digital signal-processing capability. Its cell input/output is shown in Figure 1.

![Figure 1. 3D-Flow input/output.](image)

The 3D-Flow operates on a data-driven principle. Program execution is controlled by the presence of the data at five ports (North, East, West, South, and Top) according to the instructions being executed. A clock synchronizes the operation of the cells. With the same hardware one can build low-cost, programmable Level-1 triggers for a small and low-event-rate calorimeter, or high-performance, programmable Level-1 triggers for a large calorimeter capable of sustaining up to one event per clock.

The 3-D Flow processor is essentially a Very Long Word Instruction (VLIW) processor. Its 128-bits-wide instruction word allows concurrent operation of the processor's internal units: Arithmetic Logic Units (ALUs), Look Up Table memories, I/O busses, Multiply Accumulate and Divide unit (MAC/DIV), comparator units, a register file, an interface to the Universal Asynchronous Receiver and Transmitter (UART) used to preload programs and to debug and monitor during their execution, and a program storage memory.

The high-performance I/O capability is built around four bi-directional ports (North, East, South and West) and two mono-directional ports (Top and Bottom). All of the ports can be accessed simultaneously within the same clock cycle. N, E, S, and W ports are used to exchange data between processors associated with neighboring detector elements within the same layer. The Top port receives input data and the Bottom port transmits results of calculations along successive layers.

A built-in pipelining capability (which extends the pipeline capability to the system) is realized using a "bypass mode." To bypass mode, a processor will ignore data at its Top port and automatically transmit it to the Top port of the processor in the next layer. This feature therefore provides an automatic procedure to route the incoming events to the correct layer. Several 3D-Flow processing elements, shown in Figure 1, can be assembled to build a parallel processing system, as shown in Figure 2.

![Figure 2. One layer (or stage) of 3D-Flow parallel processing.](image)

2.4 Introducing the third dimension in the system

In applications where the processor algorithm execution time is greater than the time interval between two data inputs, one layer of 3D-Flow processor is not sufficient.

The problem can be solved by introducing the third dimension in the 3D-Flow parallel-processing system, as shown in Figure 3.

In the pipelined 3D-Flow parallel-processing architecture, each processor executes an algorithm on a
set of data from beginning to end (e.g., the event in HEP experiments, or the picture in graphics applications).

Data distribution of the information sent by the calorimeter as well as the flow of results to the output are controlled by a sequence of instructions residing in the program memory of each processor.

Each 3D-Flow processor in the parallel-processing system can analyze its own set of data (a portion of an event or a portion of a picture), or it can forward its input to the next layer of processors without disturbing the internal execution of the algorithm on its set of data (and on its neighboring data set at North, East, West, and South that belongs to the same event or picture).

The programming of each 3D-Flow processor determines how processor resources (data moving and computing) are divided between the two tasks or how they are executed concurrently.

A schematic view of the system is presented in Figure 3, where the input data from the external sensing device are connected to the first layer (or stage in Fig. 3) of the 3D-Flow processor array.

![Figure 3. General scheme of the 3D-Flow pipeline parallel-processing architecture.](image)

The main functions that can be accomplished by the 3D-Flow parallel-processing system are:
- Operation of digital filtering on the incoming data related to a single channel;
- Operation of pattern recognition to identify particles; and
- Operations of data tagging, counting, adding, and moving data between processor cells to gather information from an area of processors into a single cell, thereby reducing the number of output lines to the next electronic stage.

In calorimeter trigger applications, the 3D-Flow parallel-processing system can identify particles on the basis of a more or less complex pattern recognition algorithm and can reduce the input data rate and the number of input data channels.

In real-time tracking applications, the system calculates track slopes, momentum, pt, and the extrapolated co-ordinates of a hit in the next plane.

Figure 4 shows the timing (at the bunch crossing rate) of the input data to each layer (or stage) and the algorithm execution time (latency) in the 3D-Flow pipelined architecture.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Time</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>200 - 500 ns</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>16.67 ± 16.67 ns</td>
</tr>
</tbody>
</table>

![Figure 4. Timing diagram of four 3D Flow pipelined layers (or stages).](image)

3. 3D-FLOW SYSTEM MANAGER FOR A TECHNOLOGY-INDEPENDENT IMPLEMENTATION

The 3D-Flow System Manager is a set of tools that allows the user to:

1. create a new 3D-Flow application (called project) by varying size, throughput, filtering algorithm, and routing algorithm, and by selecting the processor speed, lookup tables, number of input bits and output results for each set of data received for each algorithm execution;

2. simulate a specified parallel-processing system for a given algorithm on different sets of data. The flow of the data can be easily monitored and traced in any single processor of the system and in any stage of the process and system; and

3. monitor in real-time a 3D-Flow system via the RS232 interface, whether the system at the other end of the RS232 cable is real or virtual.

A flow guide helps the user through the above three phases.

A system summary displays for a 3D-Flow system created by the 3D-Flow System Manager the following information:

1. characteristics such as size, maximum input data rate, processor speed, maximum number of bits fetched at each algorithm execution, number of input channels, number of output channels, number of layers filtering the input data, number of layers routing the results from multiple channels to fewer output channels;
time required to execute the filtering algorithm and to route the results from multiple channels to fewer output channels.

A log file retains the information of the activity of the system when:
1. loading all modules in all processors;
2. initializing the system;
3. recording all faulty transactions detected in the system (e.g., data lost because the input data rate exceeded the limit of the system or because the occupancy was too high and the funnelling of the results through fewer output channels exceeded the bandwidth of the system);
4. recording any malfunction of the system for a broken cable or for a faulty component.

A result window can be open at any time to visualize the results of the filtering or pattern recognition algorithm applied to the input data as they come out at any layer of the system.

The generation of test vectors for any processor of the system can be selected by the user at any time to create the binary files of all I/O's corresponding to the pins of a specific FPGA or ASIC chip. These vectors can then be compared with those generated by the chip itself or by the VHDL simulation.

4. IMPLEMENTATION USING OFF-THE-SHELF COMPONENTS

Figure 5 illustrates an implementation of the 3D-Flow system using off-the-shelf components.

For a lower input data rate, the entire 3D-Flow system can be built with off-the-shelf components by using:
a) any one of the following FPGAs: Altera EPF 10K250A, Lucent Technology OR3T165, or Xilinx XCV300 to implement the 3D-Flow with an 8-bit-wide bus structure and 16-bit precision; the Xilinx XCV1000 can implement the 3D-Flow with a 16-bit-wide bus structure and 32-bit precision. The speed performance (without any macro instantiation, besides memory blocks, and without floor planning manual optimization) ranges from 12 to 16 MHz.
b) chips from National Semiconductor 16-40 MHz 10-Bit Bus LVDS (Low Voltage Differential Signaling) Serializer and Deserializer DS92LV1021 and DSLV1210 chip set for board-to-board communication. It features 400 Mbps serial bus bandwidth (at 40 MHz clock). It may transmit data over heavily loaded back-planes, or 10-meter cable, or unshielded twisted pair cable. The LVDS low-differential voltage is 350 mV at 3.5mA.

The same VHDL code for one 3D-Flow processor with 8-bit bus width has been targeted to any of the three FPGAs mentioned above from Altera, Lucent Technologies or Xilinx.

5. 4-VERSUS 16-PROCESSOR ASIC

For applications with higher input data rate, from four to sixteen 3D-Flow processors can be implemented into a single ASIC, and the LVDS Serializer, Deserializer function can be incorporated into the ASIC’s I/O pin drivers/receivers.

The VHDL code for the chip is written in "Generic HDL" using a "style" targeted to ASIC. The netlist for a 3D-Flow ASIC of four 16-bit processors exists for a 0.35 micron CBA technology at 3.3 Volt. The simulation shows dissipation of 884 mW at 60 MHz and a die size of 63.75 mm sq.

Figure 5. One board with 16 3D-Flow processors implemented using off-the-shelf components.
With the use of the LVDS interface technology now available from a few silicon vendors, the number of I/O pins required for the inter-chip and inter-board communication between 3D-Flow processors is a simplified problem, resulting in lower cost in connectors and ASIC packaging.

LVDS can transmit data quickly and at low power. For example, the commercially available component DS90LV031A LVDS quad CMOS differential line driver has an idle power state of 13 mW, and the 3.5 mA loop current from the driver will develop a differential voltage of 350 mV across the 100 ohm termination resistor, which the receiver detects with a 250 mV minimum differential noise margin.

With the availability of the LVDS driver, the 3D-Flow chip is not an I/O bound chip; thus the die can easily accommodate 16 identical processors (the circuit shown in Figure 5 accommodating 16 FPGAs—3D-Flow processors—on a printed circuit board, could be implemented into a single ASIC), lowering the cost per processor to less than $5 based on the current silicon die-size/technology cost.

6. TIMING AND SYNCHRONIZATION

The 3D-Flow system is synchronous. This makes it easier to debug and to build.

The most important task is to carry the clock, reset and trigger signals to each 3D-Flow component pin within the minimum clock skew. (The overall task is easier if each component accommodates 16 processors.)

This task can be accomplished without using special expensive connectors, delay lines, or sophisticated expensive technology since the processor speed required to satisfy the design is running at only 80 MHz. The expected worst clock skew for the distribution of one signal to up to 2,916 chips (equivalent to a maximum of 46,656 processors), using components PECL 100E111L or DS92LV010A Bus LVDS Transceiver, is less than 1 ns according to the worst skew between different components.

This task is not difficult to achieve with the aid of today's powerful printed circuit board layout tools that can make required traces of equal length.

The other consideration in building the 3D-Flow system is that all input data should be valid at the input of the first layer of the 3D-Flow system at the same time.

All other signals in the 3D-Flow system are much easier to control than for any other system (given the modularity of the 3D-Flow approach) because they are of short distance, reaching only the neighboring components.

7. HOST COMMUNICATION AND MULFUNCTION MONITORING

An essential part of the 3D-Flow design is that every single processor is individually accessible by a supervising host, via an RS-232 line. In addition to providing the ability to download and initialize the system, this feature also provides the capability to periodically test the processor's performance by downloading test patterns and/or test programs. A continuous monitoring can be performed by reading through RS232 the status of eight consecutive cycles of all processors and comparing them with the expected ones. These status bits are saved into a silicon scratch pad register at the same time in all processors at a pre-recorded trigger time corresponding at a selected line of the program executing the filtering algorithm in a selected layer.

In the case of suspected or detected malfunction, the processor performance could be tested remotely and its performance diagnosed. In the event of catastrophic malfunction (e.g. a given processor completely failing to respond, or a broken cable), normal operation, excluding the sick processor (or connection), can still be maintained by downloading into all the neighbors a modified version of the standard algorithm, instructing them to ignore the offending processor.

Obviously physics considerations would dictate whether such a temporary fix is acceptable, but it is a fact that the system itself does contain the intrinsic capability of fault recovery, via purely remote intervention.

8. ACKNOWLEDGMENTS

This work was supported by DoE contract DE-FG03-95ER81905. The author would like to acknowledge also Sergio Conetti, Brad Cox, Albert Werbrouck, Billy Bonner, Abdul Akbari, Duccio Lugari, Shi Bing, Gloria Corti, Jeannine Robertazzi, and Walter Selove.

9. REFERENCES

NOVEL ELECTRONIC SENSORS AT CMS

J. Moromisato, Y. Musienko, S. Reucroft, D. Ruuska, J. Swain, E. von Goeler
Department of Physics, Northeastern University, Boston, Mass. 02115

Abstract

We summarize work on three sensors and their applications in CMS: avalanche photodiodes for the detection of scintillation light, solid state temperature sensors, and an optical beam sensing device able to measure transverse displacement with accuracy of a few microns. Radiation hardness studies for the first two devices appropriate to the CMS context are provided. For the optical position sensor, an analog readout prototype with a set of four linear CCD arrays arranged around a square aperture, and illuminated by a cross-hair laser, is described. We achieve a linearity and reproducibility of better than five microns throughout an active transverse range of over 20 mm.

1 AVALANCHE PHOTODIODES

The avalanche photodiode (APD) has been chosen as the baseline photodetector for the electromagnetic crystal calorimeter (ECAL) of the Compact Muon Solenoid (CMS) Detector at the Large Hadron Collider (LHC) at CERN in Geneva, Switzerland. The ECAL consists of some 60,000 lead tungstate (PbWO₄) crystals, each to be read out by a pair of APD’s. Among the reasons for choosing APD’s are their insensitivity to high magnetic fields, their high quantum efficiency and their weak response to charged minimum ionizing particle interactions, also known as the nuclear counter effect.

Three different types of APD were irradiated in 1997. The APD’s were produced by Hamamatsu and EG&G in the context of the CMS crystal readout photodetector R&D program. Many groups [1] have been involved in the ongoing APD research and development program for CMS, including Rome, Saclay, RAL, PSI, Northeastern University, University of Minnesota. In this section we will restrict our attention to devices irradiated with 252Cf as part of radiation hardness studies carried out by the latter two groups.

One APD was from Hamamatsu with a p⁺⁺⁺⁻p⁺⁻n⁺⁺⁻n⁻ structure, produced by epitaxial growth on a low resistivity silicon substrate. The light entry surface of this APD is coated with a thin SiO₂ anti-reflective layer and protected with 0.5 mm of transparent silicone rubber. The package is ceramic with two pins (cathode and anode). This Hamamatsu device has a circular sensitive area 5 mm in diameter and a fully depleted region only 25-30 μm thick.

The two APD’s from EG&G utilized a p⁺⁺⁺⁻p⁺⁻n⁺⁺⁻n⁻⁻ structure produced by ion implantation and diffusion processes on high resistivity (> 3 kΩ-cm) thick (196 and 243 μm) silicon. These APD’s are coated with a thin, (10-60 nm) Si₃N₄ anti-reflective layer to enhance the sensitivity of these devices to 450-550 nm light. They are packaged in a ceramic case with 3 pins (cathode, anode and guard ring). The EG&G APD’s have a square 5 by 5 mm sensitive area and depletion regions nearly equal to the thickness of their substrate wafers.

The main junctions of both types of structures are located 4-5 μm from the light entry surface. This junction depth was chosen to optimize the APD’s behavior for such parameters as the excess noise factor, nuclear counter effect response and radiation resistance.

Sketches of the structures of both devices and the electric field profiles are shown in reference [2].

Summaries of the bias voltage required for a gain of 50, the bulk dark current Ibulk, the capacitance C, and the quantum efficiency (Q.E.) at a wavelength of 480 nm of Hamamatsu BC-16 and EG&G APD’s are shown in table 1.

<table>
<thead>
<tr>
<th>APD</th>
<th>Bias at Gain 50 [V]</th>
<th>Ibulk [nA]</th>
<th>C [pF]</th>
<th>Q.E. at 480 nm [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC-16</td>
<td>183.5</td>
<td>6</td>
<td>140</td>
<td>63</td>
</tr>
<tr>
<td>EG&amp;G-15</td>
<td>365</td>
<td>9.2</td>
<td>25</td>
<td>78</td>
</tr>
<tr>
<td>EG&amp;G-3</td>
<td>420</td>
<td>16.2</td>
<td>20</td>
<td>83</td>
</tr>
</tbody>
</table>

Table 1: Parameters of APD’s measured at 20 C before irradiation.

Gain and dark current as functions of bias voltage for the APD’s studied are shown in figures 1, 2, and 3. For the EG&G APD’s, the guard ring structure allows us to separately specify bulk and surface components of the dark current.

For detailed descriptions of the irradiation setup, and radiation hardness studies, we refer the interested reader to the article on radiation hardness of APD’s in this volume (Y. Musienko et al. [2]) and the longer papers [3, 4, 5].

2 TEMPERATURE SENSORS

Temperature sensing is an important part of any high energy physics experiment which requires environmental control. Aside from such properties as mechanical robustness and fault tolerance, temperature sensors for such applications may have to be extremely radiation hard. As part of an on-going research program into radiation hardness of various devices for the CMS project [6], we have irradiation two types of solid state temperature sensor: one active and one passive.
Figure 1: Gain and dark current as functions of bias voltage for Hamamatsu BC-16 APD measured before irradiation.

Figure 2: Gain and dark current as function of bias voltage for EG&G-15 APD measured before irradiation.
Laboratory. The irradiation available in the future. The device, and newer radiation-hard devices are expected exposed observed for all four sensors. Discuss!

The active devices were four Analog Devices AD590KH bipolar "Proportional to the Absolute Temperature" (PTAT) sensors. These are small devices which sense temperature by its effect on current flow in semiconductors. They provide 1μA per degree Kelvin when suitably powered [7].

The passive devices were miniature platinum RTD's manufactured by R&D Corp. in New Hampshire, USA [8]. They are made of platinum foil sealed between two layers of Kapton and have two, three, or four-wires depending on how they are to be read. Their resistance is proportional to the temperature and can be read using a Wheatstone bridge or any other standard technique. We note that there are two standard temperature coefficients in use, and this should be kept in mind when ordering or using these devices.

Both types of sensor were connected to appropriate circuitry to give an analog signal proportional to temperature and exposed to neutrons from 252Cf at Oak Ridge National Laboratory. The irradiation setup was the same as that used for a detailed study of radiation hardness of avalanche photodiodes described in detail in references [3, 4], as are the general characteristics of 252Cf as a neutron source. All electronic circuitry other than the devices themselves was shielded from radiation.

The results of irradiation of two of the four AD590KH temperature sensors are shown in figures 4 and 5. After a fluence of about 6 × 10^{12} neutrons/cm^2 each device began to fail, registering a progressively decreasing temperature as the irradiation continued. The same behaviour was observed for all four sensors. Discussions with the manufacturer suggested the failure of one particular JFET in the device, and newer radiation-hard devices are expected to be available in the future.

The RTD's showed no indications of a change in output or linearity for the same irradiation.

In its present form, the AD590KH should be used with great caution in situations where high neutron fluences are expected. The RTD seems, as one might hope from its simple structure, to be radiation hard up to 10^{13} neutrons/cm^2, and despite its being more difficult to read out, appears to be an excellent choice for high radiation applications.

3 COPS: A TOTALLY TRANSPARENT ALIGNMENT SENSOR

We have developed a totally transparent optical beam sensing device which can measure transverse displacements with an accuracy of a few microns over many meters[9], and which is applicable to endcap muon chamber alignment for CMS. Four linear CCD arrays are arranged around a square aperture through which a diverging cross-hair shaped laser beam passes. The part of the laser beam which passes through the square hole is completely unaffected by the CCD arrays, which detect the position of the crosshair from its outer edges.

Many of these devices can be placed one after another along distances of over ten meters, with only a small loss in intensity of the beam with distance. A prototype has been constructed with linearity better than 5 microns throughout an active range of over 20 mm. Reproducibility of the measurements was better than 2 μm, and the long-term stability was 5μm.

1A Lasiris crosshair diode module with wavelength 670 nm and a five degree fan-out angle was used.
Figure 4: Ambient temperature and temperature as measured by AD590KH as a function of neutron fluence.

Figure 5: Ambient temperature and temperature as measured by AD590KH as a function of neutron fluence.
The prototype can be read out and analyzed at 1.5 Hz, but no attempt was made to optimize speed. Readout rates of a few Hertz should be possible.

The total transparency of the device comes at a price, which is a possible shadowing effect where one CCD array can shadow the next. It is, however, possible to arrange the window sizes and the spacing between detectors so that this is not a problem. A newer design, under investigation, mounts the CCD arrays perpendicular to the plane of the square aperture, with a prism to deflect light onto the array. This offers a reduction of the shadowing problem as well as the possibility of using the system with light passing through the aperture in either direction.

4 CONCLUSIONS

The CMS experiment involves numerous novel detectors, among them 1) avalanche photodiodes, which have demonstrated reasonable resistance to irradiation, 2) temperature sensors, for which great care must be taken as some seem to fail at relatively low fluences in a slow and insidious manner faking a slow drop in temperature, and 3) novel optical systems for position measurement.

5 ACKNOWLEDGEMENTS

We would like to thank the following people for their assistance in this project:

From Northeastern: Steve DiCaccio and Keith Flynn of the Physics Department machine shop for helping get the mechanical portion of these experiments out the door on time. Matt Marcus, an undergraduate who made cables, built circuits, helped drive the truck and generally helped make it all work.

From ORNL: Chuck Alexander for his keen interest and depth of knowledge in things nuclear. Robert McMahon, Ed Smith and Gary Owen for providing source handling expertise and helping provide means to solve the thousand little things that always still need to be done, and always with a welcome sense of friendliness and humour.

From Fermilab: We would also like to thanks D. Eartly, T. Droge, and D. Prokofiev for their involvement in the COPS system.

We also thank Roger Rusack and all our CMS ECAL colleagues for collaboration, and the National Science Foundation and the United States Department of Energy for their support.

6 REFERENCES

HIGH READOUT SPEED PIXEL CHIP DEVELOPMENT AT FERMILAB
G. Cancelo, D. Christian, J. Hoff, A. Mekkaoui, R. Yarema, S. Zimmermann
Fermi National Accelerator Laboratory, Batavia, IL 60510

Abstract
Pixel detectors are becoming a very important part of high energy physics experiments, including those at the Tevatron and the LHC. At Fermilab, a pixel detector for the BTeV experiment is proposed for installation a few millimeters from the beam. Its information will be used in on-line track finding for the lowest level trigger system. This application requires pixel chips with high readout speed. The architecture of the pixel chips being designed at Fermilab will be presented, and future proposed developments and simulations will be summarized.

1. INTRODUCTION
At Fermilab, the BTeV experiment has been proposed for the C-Zero interaction region of the Tevatron [1, 2]. The innermost detector for this experiment will be a pixel detector composed of 93 pixel planes of 100×100 mm each, divided in 31 triple-stations perpendicular to the colliding beam and installed a few millimeters from the beam. This detector will be employed for on-line track finding for the lowest level trigger system [3] and, therefore, the pixel chips will have to read out all detected hits. Simulations have shown that, given a luminosity of 2×10^33 cm^-2 s^-1 (which corresponds to two interactions per crossing), a pixel chip of 8×7.2 mm active area placed 6 mm from the beam (the innermost chip), will be hit by one or more tracks in approximately one 132 ns bunch crossing (BCO) out of four [4]. At this luminosity, it is estimated that an average of approximately five 50×400 μm pixels will be hit in the innermost chip in those crossings with any data [5]. Therefore, this pixel chip has to sustain an average readout rate of 1.25 pixels per BCO. To account for statistical fluctuations and other effects (for example, the same simulations have shown that more than 20 pixels can be hit in just one BCO) the chip has to be capable of even higher data transfer performance.

Another very important factor that impacts the required data transfer rate is the need for analog to digital conversion (ADC) of the detected pulse height. Simulations have shown that a 50×400 μm pixel with a two or three bit ADC may be enough to achieve the necessary resolution [6]. Experiments that are now being arranged for a test beam should help to confirm the final chip requirements. Though there is no final agreement about the pixel size within the BTeV collaboration, there is a reasonable consensus that the experiment will require analog readout.

The pixel chip will be installed very close to the beam and therefore will have to be implemented in a radiation hard technology. We intend to use the new 0.5 μm process from Honeywell to accommodate this very severe constraint. Prototype chips will be made using the Hewlett Packard 0.5 μm CMOS process.

The pixel chip development described here is a succession of steps and submissions toward a chip that meets the BTeV requirements, each achieving specific engineering goals. The chips resulting from these steps have been dubbed FPIX0, FPIX1, and so on. In the next sections we will describe FPIX1, which represents the first step towards the final pixel readout architecture necessary for the BTeV experiment. Its primary purpose is to determine how fast the chip can process information internally and therefore, allow accurate extrapolation to the ultimate possible readout speed. Previous steps included FPIX0 [7, 8] and Pre-FPIX1, which were designed to test different front-end configurations and cross-talk management ideas. We anticipate that enhancements to the FPIX1 architecture will be necessary to achieve the readout speed required by BTeV. Simulations based on our experience with FPIX1 will guide the design of these enhancements.

2. FERMILAB PIXEL CHIP 1 (FPIX1)
The FPIX1 is a column based pixel chip with 50×400 μm pixel cells arranged in an array of 160 rows by 18 columns. Following an idea presented by Wright, et al. [9], FPIX1 stores hit information awaiting readout in the pixel unit cells, and uses an indirect addressing scheme to reference the hits to BCO numbers held in registers at the end of each column. However, rather than using pointers to accomplish the indirect addressing, FPIX1 uses a command driven design, which is described below. The chip can be divided into three mutually dependent pieces: the Pixel Cell, the End-Of-Column (EOC) Logic and the Chip Control Logic [10] (Figure 1). The responsibility of the Chip Control Logic is to control and maintain all features that are common to the chip such as the clocks, the “current” and “requested” BCO number, and the status of off-chip communication. Each one of the eighteen EOC Logic cells controls one column. The EOC Logic responds to information from the Chip Logic, and from the 160 pixels in a column by broadcasting

Work supported by the U.S. Department of Energy under contract No.DE-AC02-76CH03000. Fermilab conference paper No. 98/278.
commands to the Pixel Cells, and by arbitrating with the other EOC Logic cells for control of the on-chip data bus. Finally, each Pixel Cell connects to one sensor pixel and responds to commands from the EOC Logic. The commands used in this architecture are the following: the “input” command instructs a Pixel Cell to accept hits from its sensor pixel and to respond to a hit by alerting the EOC. In the absence of an input command, the hit is ignored. The “output” command instructs the Pixel Cell to prepare to write its information onto the bus. The “reset” command instructs the Pixel Cell to reset its contents. Finally, the “idle” command instructs the Pixel Cell to do nothing.

Each EOC Logic cell consists of four EOC command Sets, each one capable of generating its own commands. When a Pixel Cell receives a hit, it immediately associates itself with whatever EOC Set is broadcasting the “input” command. From that point until it is reset or output, the Pixel Cell only responds to commands from its associated EOC Set. Meanwhile, the EOC Set holds the timestamp. The EOC Set can then issue the “output” or the “reset” command. The hit information is stored inside the Pixel Cell until readout.

The Chip Command Logic supports two readout modes. The first one, the “continuous” readout mode, requires no external trigger. This mode is expected to be used in the BTeV experiment. The other readout mode is the external trigger mode, in which an external system must provide the timestamp of the hits that should be read out. This mode is applicable for pixel detectors with external trigger, and for diagnostic purposes.

The pixel cells hold the front-end electronics and the digital interface with the EOC Logic. The FPIX1 front-end is based on a design implemented in the FPIX0 and Pre-FPIX1 test chips. Reference [8] reports in detail on measurements of FPIX0, both unbonded and bonded to an ATLAS test sensor. The front-end (Figure 2) contains a charge sensitive amplifier (CSA) and a second amplification stage. The DC feedback used in the CSA is similar to the one described in [11]. The average discharge time of the CSA can be adjusted from 50 ns to 1 ms by an external current source without requiring any reset signals to be transmitted across the sensitive analog region. The output of the second stage connects to a flash ADC and a discriminator.

![Figure 2. Front-end](image)

The discriminator output Hit is asserted when the signal at the input of the discriminator is higher than the threshold (Thr). The flash ADC consists of three comparators directly connected to SR flip-flops inside the pixel cell. The four thresholds (common for all pixel cells) are input to the chip as DC levels. During readout, tri-state buffers connect the outputs of the ADC flip-flops to the EOC Logic, where they are encoded into two bits.

The digital interface of the pixel cell is depicted in Figure 3. It has two major components; the Command Interpreter, and the Pixel Token and Bus Controller. The Command Interpreter has four inputs, corresponding to the four EOC command Sets. Commands are presented by the EOC Logic simultaneously to all pixel cell Interpreters in a column. When an Interpreter is executing the input command and the Hit output from the discriminator is asserted, the Interpreter associates itself with the particular EOC Set that is issuing the input command. Simultaneously, it alerts the EOC Logic to the presence of a hit via the wire-or’ed HFastOR signal. After the association to a particular EOC Set has been made, the Interpreter ignores commands from all other EOC Sets. The pixel hit information is stored in the cell until the associated EOC Set issues an output or reset command.

When the associated EOC Set issues the output command, the Interpreter issues a bus request and asserts the wire or’ed RFastOR signal. This operation is executed independent of the Master Clock (McIk). The balance of the readout proceeds synchronous with the McIk. The EOC Logic provides a column token on the bottom of the column as a means to regulate bus access. The token quickly passes pixel cells with no information until it reaches a cell that is requesting the bus. This propagation to a hit pixel is done in less than one clock cycle, even if the pixel is the last in the chain. After the next rising edge of the McIk, the hit pixel with the column token loads its data onto the bus and drives it to the EOC logic for one clock cycle. In parallel, the column token is transmitted to the next hit pixel, pipelining the output of the Pixel Cell with the token passing. This allows the readout of
one Pixel Cell per clock cycle, without any wasted MCik cycles. The data is composed of the ADC count Bits[3:1] and the row address Radd[7:0]. As the hit pixel is read out, it automatically resets itself and withdraws its assertion of the RFastOR. The RFastOR returns to its inactive state while the last of the hit pixels is being read out. This way, the EOC Logic is able to detect when the last hit pixel in the column is being output. At the next rising edge of the MCik, control of the on-chip bus is transferred to the next column with hit data.

2.2 End of Column Logic

Figure 3 shows a block diagram of the EOC Logic. It consists of a Priority Encoder and four EOC command sets. The EOC Sets themselves consist of a timestamp register, a state machine for generating the appropriate EOC commands, and two comparators.

The Priority Encoder selects one EOC Set to issue the input command. When there is a hit somewhere in the column, the RFastOR signal is asserted, and the state machine inside the assigned EOC Set responds by latching the Current BCO (CBCO) in its EOC timestamp register and by issuing the idle command at the next rising edge of the BCO clock. This ensures that all pixels that have not been hit continue to monitor all four EOC Sets, waiting for a coincidence of hit and input commands.

The Chip Logic controls the features associated with the whole chip. It consists of the Current BCO counter (CBCO), the Readout BCO counter, a multiplexer, and a chip controller. The CBCO increments synchronously with the BCik and is delivered to the EOC logic. The multiplexer multiplexes the Readout BCO counter or the External Request BCO (in case external trigger is used). The output of the multiplexer forms the RBCO number that is delivered to the EOC logic. When the chip is operating in the “continuous” readout mode, the multiplexer connects the Readout BCO counter to the RBCO, and this counter will provide the timestamp number that should be used to compare with the timestamp latched in the EOC Timestamp registers. The clock of the Readout BCO counter is not a free running clock. The Readout BCO counter lags two counts behind the CBCO, in order to avoid comparisons in the EOC.
logic of an event that did not yet stabilize inside the pixel cells. The Readout BCO counts in parallel to the CBCO counter (using the BC1k) until the EOC Sets detect a match between the RBCO and the timestamp latched in the EOC Timestamp register. Then the clock stops and the chip controller starts the read out of the chip by issuing a ETkin to the first EOC Logic. When the read out of that specific timestamp finishes (i.e., the Chip Logic detects that ETkout of the last column was asserted), the controller quickly increments the Readout BCO Counter (using the MC1k) until another match is detected or the Readout BCO counter reaches two counts behind the CBCO.

Other functions of the Chip Logic include external bus arbitration, which is done again by a token passing from chip to chip, the control of the configuration of the chip, and data “throttling”. The configuration is programmed using a serial bit stream to set features like pixel cell kill (to disable noisy pixels) and pulse inject select (for enabling programmable pixel cells to accept charge inject directly into the front-end using an external voltage source). Data throttling is the following: there is an external input to the pixel chip that allows one to command the pixel cells to disregard a bunch crossing, even if it contains hit information. The DAQ can monitor the timestamp of the data as it is read out. If the timestamp gets too delayed with respect to the current BCO, creating the possibility of recorded hit losses, the DAQ can command the pixel chip to disregard future bunch crossings (creating dead time, but no data bias), until the delay drops to an acceptable value.

3. FERMILAB PIXEL CHIP 2 (FPIX2)

Before we can choose the final FPIX2 architecture, we need to decide how many bits of analog information are actually necessary for the BTeV experiment. The present plan is to use FPIX0, bump bonded to ATLAS detectors, in a test beam in order to collect information that will provide an experimental basis for this decision. As described above, FPIX1 implements a two bit flash ADC inside the pixel cell. We have confidence that a three bit ADC could fit inside a slightly larger cell, for example 50 ×450 μm. However, if the test beam shows that four or more bits of analog to digital conversion is required, the ADCs will have to be moved to the periphery of the chip. Analog pulse height information will have to be transmitted for digitization from the pixel cells to the column periphery.

As we have designed FPIX1, we have also considered and simulated features, which may be included in the future to increase the readout speed. We will now present some of them. Clearly, one possibility is to increase the readout clock frequency (MC1k for FPIX1), but this is constrained by the internal speed of the chip and by power dissipation. Another option is to increase the width of the output data word, but this is also constrained by the complexity and mass of the multichip module interconnect and the chip power dissipation. A third option is to achieve some form of data compression inside the chip. The data alignment by timestamp implemented in FPIX1 already achieves an initial degree of data compression. During readout, the timestamp has to be transmitted just once for all the hits that occurred simultaneously. In the next FPIX generation, we hope to implement what we have named “group” reading. The concept is that instead of reading a column by individually reading each pixel cell, we will read groups of consecutive pixel cells in parallel. So, in this sense, we will not have pixel row address, but actually pixel group address, and the row position of several pixels can be uniquely identified with just one row address. Simulations described in next section have shown a data compression by a factor of 2.36 with respect to a pixel by pixel readout. Another option for data compression is the transmission of the column address just once for all the hit data in a given column.

Another method to increase the readout speed is to use two readout clocks. One, the bus readout clock, operates at higher frequency, and is associated just with the output data bus logic of the chip. The other, the internal readout clock, operates at some lower frequency compatible with the microelectronics process and some reasonable power dissipation (for example, the bus readout clock operates at twice the frequency of the internal readout clock). The problem which then must be solved is how to deliver enough hit information to the output data logic to optimize the utilization of the output data bus. If the chip has hits and has control over the data bus, it should transmit data continuously over the bus without wasting readout clock cycles. We have considered two approaches to the solution of this problem. One is to use multiple buses inside the pixel chip, which can transfer hit information from more than one column in parallel to the output data bus logic. The output logic then multiplexes at higher rate the hit data of different internal buses to the output data bus. This approach does not look attractive for the BTeV experiment, since simulations have shown that, in 60% of the BCOs with tracks, only one column is hit. Therefore, simultaneous readout of multiple columns will in general not avoid waste of readout clock cycles [5]. The second option is to use a very wide internal data bus. The chip would transmit all information associated with a group (group column and row address and four ADC conversions) in one internal readout clock cycle and in parallel to the data output bus logic. The output logic would then divide this word into narrower words, and transmit them at a higher frequency. This second approach looks very attractive, since it addresses the concern previously raised by the simulations. Furthermore, it takes advantages of features already implemented in FPIX1, specifically the set of pipeline features that allows the chip to read at full clock speed.
even when the chip finishes the read out of one column and starts the read out of the next.

Finally, we are also considering pipelining incrementing the Readout BCO Counter with the readout of data associated with a previous timestamp, or even some faster method to locate the next stored timestamp. Future submissions will also contain outputs to signal internal error states, and digital to analog converters to allow the thresholds to be downloaded to the chip along with other configuration data.

4. SIMULATIONS

We have done extensive simulations of different enhanced FPIX chip architectures. We will describe here a simulation that assumes two or three bit flash ADCs inside the pixel cells. For a more complete description of these results, see Reference [12]. The objective of the simulations was to determine if the proposed FPIX2 chip architecture could achieve the necessary data rate to avoid dead time in the BTeV experiment. The conditions for the simulations were as follows: The delays used for the internal logic of the chip are set by Verilog and Spice simulations of FPIX1. We simulated the performance of the pixel chip that will receive the maximum fluence in the detector. We assumed a pixel size of 50x400um and a chip with 160 rows by 18 columns, four pixel "grouping", a wide internal bus operating at 26.5 MHz and an output bus operating at 53 MHz with a half the width of the internal bus. The hit input was provided by a Monte Carlo simulation of minimum bias events of approximately 5000 BCOs, assuming n+ on n sensors and discriminator thresholds set at 2000 e-. The total number of interactions per BCO is a random number chosen from a Poisson distribution with mean 2. This is equivalent to a luminosity of \(2 \times 10^{31} \text{cm}^{-2} \text{s}^{-1}\), the highest luminosity expected for the BTeV experiment. The number of pixels hit by each track is affected by the fact that the sensors are located in a 1.6 T magnetic field [5]. A total of 1240 BCOs with hits, and a total of 6152 hits, were simulated. This represents an average of approximately five pixel hits per bunch crossing with tracks. The results of the simulations show that reading groups of four consecutive pixels results in a data compression of 2.36 with respect to a pixel by pixel readout. The data rate did not approach the maximum possible rate; the output bus was only approximately 40% of the time utilized. This gives us a reasonable margin to account for other effects not included in the Monte Carlo simulations.

5. CONCLUSION

In this paper we have described the FPIX1 chip. We have also described proposed enhancements that we plan to incorporate in the future in order to increase data compression and readout speed. Finally, simulations have demonstrated that the FPIX architecture should be capable of achieving the hit readout rate required by the BTeV experiment.

6. REFERENCES

Semi-Custom Gate Arrays and Standard Product Suitable for use in Radiation Environments up to 10Mrad(Si)

J. M. Benedetto D. B. Kerwin and R. Sharman
UTMC Microelectronic Systems
Colorado Springs, CO 80132

Abstract

The radiation response of the UTMC Microelectronic Systems (UTMC) FA01 gate array standard evaluation circuit (SEC) was measured up to a total ionizing dose of 10Mrad(Si) using a Co-60 source. The radiation response of UTMC's JC01 SEC was measured up to a total ionizing dose of 300krad(Si). Each SEC consists of 9 functional blocks, all of which remained fully functional throughout the accumulation of total dose. In addition to functional testing, the SEC was monitored for parameter shifts in quiescent current (QDD), propagation delays, input buffer data transition voltage, and output buffer drive voltage.

Introduction

High energy physics, nuclear power, and some medical applications can require electronics to be radiation hardened up to a total dose of 10Mrad(Si). Many of these applications also require the implementation of custom designs through a gate-array architecture. UTMC Microelectronic Systems (UTMC) offers a 0.8µm, 200,000 usable gate application specific integrated circuit (ASIC) built at Lockheed-Martin Federal Systems (LMFS) using their dedicated radiation-hardened process line which is fully qualified to a total dose of 1Mrad(Si), and is capable of meeting total doses in excess of 10 Mrad(Si).

For applications which require high-reliability along with radiation tolerance (up to 300krad(Si)) UTMC offers a 0.6µm lower cost radiation tolerant process built at American Microsystems Inc. (AMI) using a minimally invasive process module to achieve total dose hardness.

This paper discusses the total dose radiation response of the UTMC FA01 ASIC standard evaluation circuit (SEC) built at LMFS to a total ionizing radiation dose of 10Mrad(Si) [1]. Details of UTMC's 0.6-µm radiation tolerant process have already been published [2,3].

0.8µm Radiation Standard Evaluation Circuit

The LMFS 0.8µm radiation hardened CMOS technology is fabricated on an advanced semiconductor process that borrows many of its features from a 0.5µm CMOS design. This allows the 0.8µm process to offer enhanced performance and reduced power consumption [4]. An ion implanted retrograde N-well, coupled with thin epitaxial layer, assure latch-up immunity by suppressing parasitic bipolar action. The same features reduce charge collection from single-event hits by limiting the charge funnel length. A radiation enhanced LOCOS field isolation process minimizes total dose induced parasitic leakage between transistors and along the transistor edge. A radiation hardened gate oxide minimizes trapped holes and interface state build-up.

The SEC is organized as eight modules: a flop RAM module organized as 128 words with 32 bits/word containing 4096 DFAPCB d-flip flops, an SEU immune flop RAM module organized as 64 words with 16 bits/word containing 1024 SDFF d-flip flops, a RAM macro module organized as 256 words with 32 bits/word with built-in self test (BIST) capability, a noise test module used to test output switching, a delay module containing four different delay chains of NAND2 and NOR2 cells, a test performance module containing all of the cells used in the UTMC library excluding macros, a NAND tree module that allows for VIH, VIL measurements and comparison to JTAG, and a module with UTMC's implementation of JTAG.
Experimental Conditions

All 9 of the discrete blocks from two different FA01 SECs were evaluated for functionality prior to irradiation and at 1Mrad(Si) increments up to a total accumulated dose of 10Mrad(Si). In addition to functional data a selection of parametric data, including quiescent current (QIDD), propagation delays, input buffer data transition voltage, and output buffer drive voltage was also measured as a function of total dose.

The parts were irradiated at room temperature in a Shepherd Model 484 Co-60 source containing two 6000Ci rods. The temperature inside the Shepherd source was continuously monitored during the exposures. This test used a dose rate of 333 rad(Si)/s. The Co-60 source was calibrated immediately prior to irradiating the UTMC FA01 test devices using radiochromic film traceable to the National Institute of Standards and Technology (NIST).

The DUTs were packaged in hermetically sealed ceramic packages with Kovar lids and placed inside of a lead-aluminum box to minimize dose enhancement effects. The parts were statically biased during irradiation with a 5.5V supply voltage (Vdd); the worst case bias condition within the specified operating voltages. To minimize annealing effects, the test devices were measured within one hour following radiation exposure (both functional and parametric tests).

Results of Total Dose Exposure

Functionality

The functionality of each individual test block on the FA01 samples was verified after each successive radiation dose (within one hour after the end of the radiation exposure as mentioned above). All the test blocks within the FA01 SEC remained fully functional following each radiation exposure, up to 10Mrad(Si). Because of time constraints the test was terminated at 10Mrad(Si) without observing any functional failures.

FA01 SEC Parametric Data

Figure 1 shows stand-by (or quiescent) current (QIDD) as a function of total dose for two representative FA01 test devices, designated device 1 and device 2. The dotted line is the QIDD data for device 1 and the dashed line is the QIDD data for device 2 as a function of total dose. The solid line at the top of the plot is the QIDD maximum specification limit (set by UTMC at 1000μA). As seen in the figure both devices are well below the QIDD specification at each total dose increment. The current peaks at approximately 9Mrad(Si) and falls approximately 100μA with the addition of 1Mrad(Si) (to the final dose level of 10Mrad(Si)).
Figure 2 shows the data transition voltage as a function of total dose for the FA01 CMOS Input Buffer. The diamonds are the average $V_{IH}$ data and the squares are the $V_{IL}$ data. The solid black and gray lines are the maximum and minimum specification limits, respectively. As the data clearly shows, the data transition voltage is reduced as a function of total dose but stays above the minimum specification limit out to 10 Mrad(Si).

Both the CMOS and TTL output buffer voltage drive was measured as a function of total dose. Figure 4 shows the TTL output buffer voltage drive versus total dose. The diamonds are the $V_{OH}$ drive voltage and the solid black line is the $V_{OH}$ minimum Specification. The squares shown in figure 4 are the $V_{OL}$ drive voltage and the solid gray line is the $V_{OL}$ maximum limit. There is no measurable change in the output drive voltage as a function of radiation. Similar results were obtained on the CMOS drive buffer, i.e. no measurable change with radiation (the figure was omitted for clarity).

Figure 3 shows the data transition voltage as a function of total dose for the FA01 transistor-transistor logic (TTL) Input Buffer. The diamonds are the average $V_{IH}$ data and the squares are the $V_{IL}$ data. The solid black and gray lines are the maximum and minimum specification limits, respectively. Similar to the CMOS input buffer discussed above, the data transition voltage is reduced as a function of total dose but stays above the minimum specification limit out to 10 Mrad(Si).

Figure 4 shows the TTL output buffer voltage drive versus total dose. The diamonds are the $V_{OH}$ drive voltage and the solid black line is the $V_{OH}$ minimum Specification. The squares shown in figure 4 are the $V_{OL}$ drive voltage and the solid gray line is the $V_{OL}$ maximum limit. There is no measurable change in the output drive voltage as a function of radiation. Similar results were obtained on the CMOS drive buffer, i.e. no measurable change with radiation (the figure was omitted for clarity).
of the FA01 were measured using a 96 gate NAND chain and a 96 gate NOR chain with both high-to-low and low-to-high transitions. Both the low-to-high and high-to-low transitions were within specification as a function of total dose (with the high-to-low transition being worst case). Figure 5 shows the radiation response of the NAND chain and figure 6 shows the radiation response of the NOR chain. In both cases the propagation delay increases with increasing radiation but stays well below the specified maximum limit. The NAND propagation delay starts at approximately 30ns (or 0.3ns per gate) and steadily increases to a maximum propagation delay of approximately 50ns at 10Mrad(Si) (or 0.5ns per gate). Not unexpectedly, the behavior of the NOR chain is almost identical to that of the NAND. The NOR propagation delay begins at approximately 40ns and increases to just under 60ns following 10Mrad(Si) of total dose radiation.

Figure 5. Propagation delay versus total dose for a 96 gate NAND chain (high-to-low transition).
96 Gate NOR Chain (high-to-low transition)

![Graph showing propagation delay versus total dose for a 96 gate NOR chain (high-to-low transition).](image-url)

Figure 6. Propagation delay versus total dose for a 96 gate NOR chain (high-to-low transition).

**Summary/Conclusions**

The radiation response of the FA01 was characterized to 10 Mrad(Si). Functionality and parametric test data was taken versus total dose using packaged parts in a Co-60 chamber. At all total dose increments the UTMC FA01 SEC easily met specified limits. This data clearly shows that the 1 Mrad(Si) UTMC ASIC 0.8μm product manufactured by LMFS is capable of meeting total doses far exceeding the specified limit of 1 Mrad(Si).

**References**


THE HELIX128 READOUT CHIP FAMILY FOR SILICON MICROSTRIP DETECTORS AND MICROSTRIP GASEOUS CHAMBERS

Christian Bauer, Wolfgang Fallot-Burghardt¹, Karl-Tasso Knöpfle, Bernhard Schwingenheuer, Edgar Sexauer, Ulrich Trunk²
Max-Planck-Institut für Kernphysik, Heidelberg
Martin Feuerstack-Raible, Boris Glass³, Sebastian Hausmann, Sven Löchner, Katharina Müller, Ulrich Straumann
Universität Heidelberg
Ruud Kluit
NIKHEF, Amsterdam
Harald Deppe, Ulrich Kötz
DESY, Hamburg
Roberto Carlin
Università di Padova
Robert Sacchi
Università di Torino
¹ now at Philips AG, Zürich ² trunk@asic.uni-heidelberg.de ³ now at ETH Zürich

Abstract

This paper presents a description of the HELIX128-2 frontend chips that are used for the readout of the silicon microstrip detectors and the microstrip gaseous chambers in the HERA-B experiment. Tests in the laboratory and in the experiment show good performance characteristics and full compliance with specifications including moderate radiation tolerance.

A newer version 3.0 is under development and will also be used by the ZEUS experiment.

I. THE HELIX128-2.2 AND HELIX128-3.0 CHIPS

HELIX128-2.2 and HELIX128-3.0 are 128 channel pipelined readout chips [1] used for the HERA-B Silicon Vertex Detector, the microstrip gaseous chambers (MSGC) of the HERA-B Inner Tracking Detector and the ZEUS Microvertex Detector. The HERMES experiment will also use this chip for a vertex detector upgrade. A stripped-down version (without pipeline and analog readout) called CHIP will be used for H1's Central Inner Proportional Chamber upgrade. The chip is manufactured in the AMS CYE (0.8 µm CMOS) process and features the same architectural concept as the FElux chip [2] developed by the RD20 collaboration.

As depicted in Fig. 1, each input channel features a low-noise, low-power charge sensitive preamplifier (CSA) frontend and a shaper. These folded cascade [3] designs are optimized for 100 ns fall time to comply with the HERA bunch-crossing clock of 10 MHz. The output of each frontend channel feeds its signal into a capacitor array (pipeline) and into an AC-coupled differential amplifier type comparator circuit with a common reference voltage for all 128 channels. The outputs of these comparators are ORed together in groups of 4 channels, latched and brought off-chip via open drain pads to derive a level-1 trigger signal. The pipeline consists of 141 cells per channel, which allows a maximum trigger latency of 128 samples and implements a derandomizing buffer for 8 triggered events. The oldest triggered event is read out of the pipeline via a resetable CSA (pipeamp). The signals are then serialized and brought off-chip by means of a 2-stage multiplexer and a current driver. The output stages operate at up to 40 MHz readout clock frequency. All amplifier stages feature forced bias currents to ensure a sufficient radiation tolerance. These currents, as well as the voltages that adjust the feedback resistances of CSA, shaper, and the comparator threshold, are generated with on-chip digital to analog converters (8 bit resolution). The DACs, together with digital circuits adjusting the trig-
nals allow the daisy-chained readout of two or more readout daisy-chain. Figure 2 shows the layout of the HELIX128-2.2 chip.

Figure 1: Schematic of the HELIX128-2 and HELIX128-3.0 chips

Figure 2: Layout of the HELIX128-2.2 chip

Pulse shape measurements under different input load conditions have been made. These measurements cover the full range of preamp bias currents and shaper feedback control voltages. The results (Figs. 3 and 5) show that an undershoot-free pulse with 100 ns fall time can be achieved for input load capacitances up to ±30 pF.

With the recommended receiver circuit, the gain of the chip was measured as 110 mV/MIP without load, dropping to 75 mV/MIP for 16 pF load. \( I_{pre} \) was adjusted to preserve a fall time of ±100 ns. The measured noise characteristic of 338 e\(^-\)+38.4 e\(^+\)/pF is depicted in Fig. 4. It closely resembles the simulated value of 287 e\(^-\)+35 e\(^+\)/pF [5].

The comparator threshold resolution was measured to correspond to an input charge of 267 e\(^+\) [6], which is small compared to the nominal signal of 35000 e\(^-\) for the HERA-B MSGCs. In previous versions severe crosstalk between the switching comparators and the analog input was observed. Improvements in the power supply and the guarding structures healed this problem.

Three chips from different HELIX128 revisions were irradiated up to 2 kGy with a \(^{137}\)Cs-source. Except for the HELIX128-2.1, whose pipeamp required a special clock pattern, all chips were fully functional after the irradiation. A fourth chip recovered to functionality after 60 hrs of annealing at 85°C. This chip was further irradiated up to 4 kGy and proofed fully functional thereafter. The pulse shape of this chip is depicted in Fig. 7. The power consumption of the chips was found to increase with the accumulated dose from 2.2 mW/ch before irradiation to 2.4 mW/ch at 2 kGy as shown in Fig. 8. The discharge of the pipeline storage capacitors due to leakage currents was found to be unaffected by irradiation up to 4 kGy (Fig. 9). More detailed tests are under way.

II. PERFORMANCE AND RADIATION TOLERANCE

Pulse shape measurements under different input load conditions have been made. These measurements cover the full range of preamp bias currents and shaper feedback control voltages. The results (Figs. 3 and 5) show that an undershoot-free pulse with 100 ns fall time can be achieved for input load capacitances up to ±30 pF.
Figure 3: Pulse shapes of a HELIX128-2.2 chip at the input load capacitance of 1.6 pF for different bias currents of the preamplifier.

Figure 5: Pulse shapes of a HELIX128-2.2 chip at the input load capacitance of 16.3 pF for different bias currents of the preamplifier.

Figure 4: The equivalent noise charge (ENC) of a non-irradiated HELIX128-2.2 chip as function of the capacitive input load.

Figure 6: Scans of HELIX128-2.2 output signals for the input equivalent to that of a minimum ionizing particle (MIP) with (light curves) and without (dark curve) switching comparators. Vertical lines indicate the edges of the sampling (left) and comparator (right) clocks.
III. Design of Detector Readout Systems

The Inner Tracking and the Silicon Vertex Detector Systems of HERA-B exhibit the identical DAQ front-end architecture: a central Front End Driver (FED) controller provides the digital control signals (sampling and readout clocks, trigger and reset signals) for the chips, while individual 12 channel FED modules are used to digitize the analog data. In both systems pairs of HELIX128-2 chips are daisy-chained resulting in a total of more than 1000 analog signal paths. Both the digital and analog signal lines are implemented by optical links.

A MSGC tracking superlayer of the HERA-B Inner Tracking System consists of 4 MSGC planes; superlayers issuing also a level-1 trigger consist of 8 planes. One quadrant of a MSGC detector plane is shown in Fig. 10. The plane is read out by 3 pairs of HELIX128-2 chips, and each pair is mounted in chip-on-board technology on a multilayer printed circuit board. The connections between detector and chips are implemented with flexible microadaptors and thin film hybrids that integrate also the resistors for spark protection.

The HERA-B Vertex Detector System will have 7 superlayers that are implemented as a Roman pot system within a 2.5 m long conical shaped vacuum vessel. Each quadrant of a superlayer is housed in a removable pot and consists of two double-sided silicon detector modules with readout electronics. A 150 μm thick Al cap separates the HERA ring vacuum from the secondary Si detector vacuum and serves as protection against rf pick-up from the beam. A partial view of the n-side of a detector module is shown in Fig. 11. The 1280 n-side strips are connected by a 4 cm flexible microadaptor to 10 HELIX128-2.1 readout chips that are mounted together with blocking capacitors onto a 3-layer Alumina hybrid produced in thick film technology. The whole assembly is water-cooled. The three Kapton cables that are just visible at the r.h.s. of the figure connect the n- and p-side (1024 strips, 8 readout chips) hybrids via vacuum feed-thrus to the outside. Prototypes of such modules have been successfully operated at HERA-B since May ’98. At present (Oct ’98), 17 detector modules with a total of 290 readout chips are installed in the HERA-B Silicon Vertex Detector. Event data from one of these detector modules are shown in Fig. 12.
Figure 10: One quadrant of a HERA-B MSGC detector with HELIX128-2.2 based readout system

Figure 11: A partial view of a HERA-B double-sided Si detector module (from left to right): detector, flexible microadaptor, readout chips and blocking capacitors mounted on n-side hybrid and Kapton cables for power and signal transmission. The detector and the hybrids have different cooling paths.

Figure 12: Raw (top) and pedestal corrected (bottom) event data from an n-hybrid of a Silicon Vertex Detector Module installed at HERA-B. Five hits in the processed data are clearly visible.

References


HIGH PERFORMANCE IMAGE SENSORS

Jacques CHAUTE MPS, Nicolas JANVIER, Gilles BOUCHARLAT

THOMSON-CSF Semiconducteurs Spécifiques
B.P. 123
Avenue de Rocheplaine
38521 SAINT-EGREVE Cedex
FRANCE

Abstract: Thomson-CSF Semiconducteurs Spécifiques (TCS) is involved in electronic imaging through high quality image sensor products built on its now famous CCD technology. A lot of products are nowadays integrated in various scientific experiments, thanks to their high level performance capabilities, and to their versatility in driving and signal exploitation.
Numerous standard products will be presented as well as a large range of customizing design capabilities, offered to the continuously increasing field of specific high demanding applications. Performances in severe environment will be presented.

Summary:
Since the early seventies, Thomson-CSF Semiconducteurs Spécifiques (TCS) has been involved in high end CCD image sensor technology development and product manufacturing. All our best efforts are continuously done in order to achieve high electro-optical performances (such as high resolution, wide dynamic range, low noise level, very low dark signal, . . .), and mechanical ones (optical plane flatness, pixel grid geometrical accuracy, optical plane reference, temperature homogeneity, . . .), as well as high reliability and quality levels. TCS’s products are actually present on the high end market through a wide range of scientific imaging products.

As regards its industrial facilities, at the beginning of 1997, TCS has turned its 100 mm wafer diameter manufacturing clean room into a 150 mm one, now totally devoted to manufacturing of high end CCD image sensors (n-MOS CCD technology).
Large devices up to 10 cm² (e.g. the TH7899M, 2048 x 2048 pixel area array image sensor) are currently manufactured through two main processes (2.5 and 1.5 µm design rules) and these new large wafer manufacturing facilities will allow TCS to develop a new CCD sensor generation, and especially very large area arrays.

Our current technologies and design skills allow development and production of various products, such as area arrays and frame-transfer sensors as large as the wafer size (up to 10 x 10 cm²) with good uniformity and very low defect density.
CCD image sensors with MPP mode are also available. This operating mode leads to drastically decrease the dark signal without need of specific cooling [a factor of 30 in dark current is noticed between MPP and standard mode] and then induces a better behaviour under ionizing radiation. Four phase transfer and specific features maintain charge handling capability at a high level, even in MPP mode.

TCS can offer flexible device architectures (multiple-port outputs, numerous readout registers, split imaging zones), and our sensors can combine high speed readout capability in conjunction with low noise performances (typically less than 5 electrons at 1 MHz readout frequency / 20 electrons at 20 MHz on TH7899M), leading to wide dynamic range.

TCS expertise in product design and in micro-electronic Silicon manufacturing technologies is complemented by a strong expertise in specific manufacturing add-on steps for packaging: X-ray and UV scintillator deposition, in-package Peltier thermo-electric cooler integration, focal plane design and buttable processes, hybridization of InGaAs together with Silicon devices, anti-reflective glass windows, specific package and/or materials for achieving specific customer requirements, as radiation hardening through extra pure silica window. Among them, optical fiber plate and taper (up to 90 cm) sealing processes are also available. This conduct to large focal plane elaboration.
COMPONENTS OF FAST ANALOG INTEGRATED MICROCIRCUITS FOR FRONT-END ELECTRONIC SYSTEMS

A.Goldsher, V.Kucherskiy, V.Mashkova
State scientific-research institute 'Pulsar", Russia, 105187, Moscow, Okruzhnoy proezd 27

Abstract

A basic set of analog integrated microcircuits (ICs) for front-end electronic systems, which have been developed and introduced into experimental production in Russia, is presented.

In the capacity of active components the ICs employ n-p-n transistor structures including those with Schottky diodes, p-n-p lateral transistors, p-n-p vertical transistors with the collector in the substrate, field-effect p-n junction transistor structures, precision diodes with the Schottky barrier. Resistors (low- and high-Ohmic) and capacitors on the basis of MOS-structures are used as passive components of the ICs.

The design principles of the IC active components have been described, the dependencies of main parameters of the typical (library) components on bias and temperature have been considered.

1. INTRODUCTION

By the present time in Russia, the following items have been developed and introduced into experimental production:

- ICs containing a fast comparator and a D-trigger, which are intended to be used in time-of-flight systems of plastic wall type;
- the four-channel ICs of an amplifier-shaper with differential inputs and outputs for use with wire detectors and intended for the amplitude data processing (amplification, filtration);
- the four-channel ICs of a differential low-power comparator of the nanosecond range, which is intended for analog signal discrimination;
- the four-channel ICs of a differential comparator of the nanosecond range, which contains a circuit for the hysteresis regulation.

The following developments are at their final stage:

- the eight-channel LSI circuits containing analog and discrete-analog channels for radiation detector data processing;
- the ICs of a fast sample-hold, which are intended for signal sampling before analog-digital conversion, analog-digital processing (filtration, commutation) of rapidly changing signals.

The circuit-engineering of the pointed microcircuits has been developed by the specialists of the Electronics department at Moscow Engineering-Physics Institute (University).

In the capacity of active components the ICs employ n-p-n transistor structures including those with Schottky diodes, p-n-p lateral transistors, p-n-p vertical transistors with the collector in the substrate, field-effect p-n junction transistor structures, precision diodes with the Schottky barrier. Resistors (low- and high-Ohmic) and capacitors on the basis of MOS-structures are used as passive components of the ICs.

General questions of the design of similar active components are expounded in reports [1,2]; and those of passive components, especially of high-Ohmic resistors, are in literature [3].

However, the circuit-engineering of each type of the microcircuits pre-determines specific requirements to their components. The most complicated among the IC components are: transistor structures with the Schottky barrier, p-n-p lateral transistors, field-effect p-n junction transistors. Let us consider the principles of their design and the results of investigation of each among them.

2. EXPERIMENT AND RESULTS

2.1. Transistor structures with the Schottky barrier (TS)

Simulation and calculation of microcircuits by using a PC have shown that the values of working currents \( I_c \) in TS amount to 0.3-5 mA. On taking this fact into account, in the IC lay-out development two typical (library) structures have been used, one of which has been calculated for the collector working current \( I_c = 0.3...1 \) mA and the other has been calculated for \( I_c = 3-5 \) mA. They are different only in geometrical dimensions especially in the perimeter of the emitter \( P_e \).

The two structures are implemented with two basic contacts and one collector contact.

Cross section of the transistor with the Schottky barrier is presented in fig.1.

Fig.1. Cross section of the transistor with the Schottky barrier
Molybdenum which possesses a value of the work function of approximately 0.2eV less than that of aluminum (\( \phi_a = 0.5 \) and 0.7-0.72 correspondingly) is used as the barrier metal here. This permits approximately 0.2 V reduction of the forward voltage drop in case of molybdenum metallization (at the identical areas of diodes). Hence, employment of molybdenum as the barrier metal makes it possible to reduce the area of the Schottky diode (DS) and, correspondingly, its stray capacitance \( C_{DS} \). Besides, molybdenum performs a role of the barrier metal in the emitter region preventing interaction between silicon and aluminum and excluding shorts in the emitter p-n junction, which could arise because of electromigration. Technological peculiarities of microcircuits for front-end electronics which have been developed in Russia are expounded in report [4].

Criterion of an optimum area of the diode in the transistor with the Schottky barrier is the difference in the forward voltage drops between the p-n junction and the diode, which is ensured at a level of \( U_{FOR} = 0.1 \ldots 0.15 \) V in the range of working current densities and working temperature. Besides, from the viewpoint of ensured dynamic parameters, the difference in \( U_{FOR} \) between the collector p-n junction and the diode with the Schottky barrier must be not less than 0.1-0.15 V; and, from the condition of a minimal value of the collector-emitter voltage reached in the saturation mode \( U_{cesat} \), the difference in \( U_{FOR} \) between the emitter p-n junction and the diode with the Schottky barrier must be not larger than 0.1-0.15 V.

One of the main characteristics of TS, that considerably determines the IC parameters especially the speed, is the current amplification cut-off frequency \( f_c \). Typical dependencies of \( f_c \) on the emitter current \( I_e \) for the two types of the library transistor structures are given in fig.2 and 3.

Measurements of \( f_c \) were carried out by using the results of checking the phase angle of the current transmission factor in the common-base circuit \( \arg(h_{21b}) \). The phase angle \( \arg(h_{21b}) \) between vectors of the collector and emitter currents is linearly increasing with the increase in the measurement frequency \( f \) and can be described by the expression

\[
\arg(h_{21b}) = \frac{180}{\pi} \frac{f_c}{f} \quad \text{[grad]}
\]

\[
\frac{f_c}{f} = \frac{\phi_e}{\pi r_c C_e} + \frac{f_m}{f}
\]

The cut-off frequency represents itself as the transconductance of the phase-frequency characteristic.

From fig.2 and 3 it can be seen that the two structures possess a maximal value of \( f_c \) which amounts to the order of 7 GHz directly in the range of the working currents.

From the dependence \( f_c = f(I_e) \), by means of constructing a graphical dependence of \( 1/2\pi f_c \) on \( 1/I_e \), the information about the emitter junction capacitance of the transistor structures biased in the forward direction and about the parameter "cut-off frequency of the transistor theoretical model" \( f_{CTM} \) has been obtained. The delay of the signal transmission from the emitter to the collector can be represented by the following expression:

\[
T_{oe} = \frac{1}{2} \frac{f_c}{f_c} = \frac{r_e C_e}{f} + \frac{1}{f_{CTM}}
\]

where: \( r_e = 26 \text{mV} / I_e \) - is the resistance of the emitter;

\( C_e \) - is the capacitance of the emitter junction biased in the forward;

\( 1/f_{CTM} \) - is the delay which is determined by transmission of a signal through the base, the collector junction and the collector bulk and which is not dependent on the emitter current in the considered range of currents.

Calculated values of \( C_e \) have made up 0.07 and 0.2 pF correspondingly.

The calculation of the microcircuits by using PC have shown at the same time that, apart from a high value of \( f_c, \) the transistor structures must be characterized by a value of the current transmission factor \( b_{21e} \) of not less than 50 (at \( t_{sub}=25\pm10^\circ C \)) in the range of working currents \( I_c \).

Dependencies of the \( b_{21e} \) value on the collector current \( I_c \) for the two types of structures are represented in fig.4 and 5 from which it is seen that the \( b_{21e} \) value amounts to 70 in the range of working currents \( I_c \) at \( t_{sub}=25\pm10^\circ C \).
dependencies of the emitter are caused by the influence of recombination components of the base currents. At the same time Fig. 4 and 5 show that at \( t_{mb} = -60^\circ C \) the decrease is also approximately two-fold increase of the \( h_{2le} \) value is observed in comparison with the \( h_{2le} \) value at \( t_{mb} = 25 \pm 10^\circ C \); and at \( t_{mb} = -60^\circ C \) the decrease is also approximately of two fold. Therefore the microcircuit calculation must be carried out by taking the minimal value \( h_{2le} = 30 \) i.e. the worst exploitation conditions.

Thus, the performed investigations have shown that the typical (library) transistor structures are characterized by: low stray capacitances of the isolation, collector and emitter junctions (in particular, they make up 0.3; 0.2; 0.07 pF correspondingly in the structures of the I type); a high value of the current amplification cut-off frequency \( f_c \) (7GHz); the current transmission factor \( h_{21e} = 70 \).

2.2. P-n-p lateral transistor structures

In fast sampling-hold microcircuits, the p-n-p lateral transistor structures are used as the current-setting components. The lay-out fragment of the IC containing such structures is shown in Fig. 6. As a rule, the regions of the collector and emitter are created at the same time with the base doping diffusion into n-p-n structures, i.e. the both types of the transistors are compatible in the manufacturing technology.

![Fig. 6. The IC lay-out fragment](image)

Dependencies of the current amplification factor \( \beta \) on the collector current \( I_c \) are given in Fig. 7 for three types of the p-n-p lateral transistors which are identical in the lay-out but different in the technological regimes.

![Fig. 7. Dependences of the current amplification factor \( \beta \) on the collector current \( I_c \) for three types of the p-n-p lateral transistors.](image)
FETs are largely determined by regimes: \(Q=0.5 \mu \text{Coul/cm}^2\), \(E=100 \text{keV}\) and reach the pinch-off voltage \(U_{p}\) of 2 V the channel and gate ion doping. The fabrication of p-n-p structures is previous to the creation of n-p-n structures. In the first case \(h_e=1 \mu \text{m}\), in the second case \(h_e=1.5 \mu \text{m}\), in the third case \(h_e=1.7 \mu \text{m}\).

Analysis of the presented data has shown that the main parameter which influences the current amplification factor \(\beta\) is the emitter junction depth \(h_e\) (at \(N_s=1.5...3.3 \times 10^{19} \text{ at/cm}^2\)). When the collector junction depths are less (\(h_c<1.5 \mu \text{m}\)), the processes of the complementary transistor structures creation must be separated. This requirement becomes especially actual in cases when the current amplification cut-off frequency \(f_c\) in the n-p-n structures is the factor which determines increase of the IC speed.

The structure marked in fig. 6 by a dotted line has been chosen as a basic structure and has been calculated for the working current \(I_c=1 \text{mA}\). Designing of structures working at high currents (of the order of 2.4 mA) was carried out by means of parallel connection of a few basic structures. Employment of such a principle has permitted the required current setting in the microcircuit to be reliably reproduced (even when the absolute value of \(\beta\) has some fluctuations).

2.3 Field-effect p-n junction transistors (FETs)

The circuit-engineering basis of the fast sampling-hold IC is the set-up structure of the double-correlated sampling [5] where the amplification module has been constructed on the basis of the circuit of the three-stage voltage follower with an input stage fabricated on a field-effect transistor with p-n junction and p-channel.

Simulation and computing of the microcircuit functional modules have permitted us to define the requirements to parameters of their components. In particular, it has been proved that the FETs must be designed so as to reach the pinch-off voltage \(U_{p}\) of not larger than 2 V; the initial saturation current \(I_{sat}\) of not less than 2 mA; the source-drain breakdown voltage \(U_{sd}\) of not less than 25 V.

The design of structures which possess such a combination of parameters is connected with compromising solutions. Besides, the parameters of FETs are largely determined by the regimes of the channel and gate ion doping.

In the calculation and experimental investigations it has been found out that in order to reach the pinch-off voltage \(U_{p}\) of 2 V the channel and gate ion doping must be carried out in the following regimes: \(Q=0.5 \mu \text{Coul/cm}^2\), \(E=100 \text{keV}\) and \(Q=10 \mu \text{Coul/cm}^2\), \(E=100 \text{keV}\) correspondingly and with the subsequent annealing at \(T=1100^\circ \text{C}, t=60 \text{ min}\) to form the channels (boron) and at \(T=1050^\circ \text{C}, t=15 \text{ min}\) to form the gates (arsenic).

The value of the initial saturation current \(I_{sat}\) is determined by the geometrical dimensions of the channel region and by the number of gates. In particular, in order to increase \(I_{sat}\) it is necessary to reduce the channel length \(L_c\) to extend its width \(Z\) and to increase the number of gates.

3. CONCLUSIONS

1. Criterion of an optimum area of the diode in the transistor with the Schottky barrier is the difference of the forward voltage drops between the p-n junction and the diode, which is ensured at a level of \(U_{FOR}=0.1...0.15\) V in the range of working current densities and working temperature. Besides, from the viewpoint of ensured dynamic parameters, the difference in \(U_{FOR}\) between the collector p-n junction and the diode with the Schottky barrier must be not less than 0.1-0.15 V; and, from the condition of a minimal value of the collector-emitter voltage reached in the saturation mode \(U_{cesat}\), the difference in \(U_{FOR}\) between the emitter p-n junction and the diode with the Schottky barrier must be not larger than 0.1-0.15 V.

2. In the experimental investigations it has been found out that the main parameter which influences the current amplification factor \(\beta\) is the emitter junction depth \(h_e\) (at \(N_s=1.5...3.3 \times 10^{19} \text{ at/cm}^2\)). When the collector junction depths are less (\(h_c<1.5 \mu \text{m}\)), the processes of the complementary transistor structures creation must be separated. This requirement becomes especially actual in cases when the current amplification cut-off frequency \(f_c\) in the n-p-n structures is the factor which determines increase of the IC speed.

3. The design principles for p-n lateral transistors have been proposed. They are based on the parallel connection of a few basic structures (\(I_c=1 \text{mA}\)), that has permitted the required current setting in the microcircuit to be ensured (even when the absolute value of \(\beta\) has some fluctuations).

4. In order to reach the pinch-off voltage \(U_{p}\) of 2 V in the field-effect transistor with p-n junction and p-channel, the channel and gate ion doping must be carried out in the following regimes: \(Q=0.5 \mu \text{Coul/cm}^2\), \(E=100 \text{keV}\) and \(Q=10 \mu \text{Coul/cm}^2\), \(E=100 \text{keV}\) correspondingly and with the subsequent annealing at \(T=1100^\circ \text{C}, t=60 \text{ min}\) to form the channels (boron) and at \(T=1050^\circ \text{C}, t=15 \text{ min}\) to form the gates (arsenic). Besides, a good concurrence of the calculated and experimental results has been achieved.

Employment of circuit-engineering solutions which take into account peculiarities of specific physical experiments, in particular, ‘Hades’ (GSI, Darmstadt), the development of the original lay-outs defended by protection documents, optimization of the technological processes of the microcircuits manufacturing have permitted the creation of the set of...
ICs which are not inferior in their main electrical parameters to the best foreign functional analogs.

The work has been performed in the framework of the project financed by the International Science and Technology Centre.

REFERENCES


DISCRIMINATOR ICS FOR TRACKING AND TIME-OF-FLIGHT DETECTORS

Department of Electronics, Moscow Engineering Physics Institute, 115409, Kashirskoe shosse 31, Moscow, Russia, e-mail: atkin@eldep.mephi.ru

ABSTRACT

Proceeding from the analysis of the present state of front-end electronics there have been stated the requirements to the parameters of discriminator ICs, being part of the time-processing channels for signals of LHC tracking and time-of-flight detectors.

The structure, contents and basic parameters of new ASICs is described. Among them are:
- two versions of four-channel comparator ICs;
- an eight-channel IC, containing a base line restorer and comparator, supplemented by an "OR" circuit;
- a new ASIC, intended to implement the units of time reference to signals of nanosecond duration and with an amplitude of 5mV..2.5V at an accuracy of tens of picoseconds. It can be used to implement CFD, LED, window and extrapolation discriminators.

1. FOUR-CHANNEL COMPARATOR ICS

Comparators are widely used in the equipment of nuclear physical experiments both in amplitude and, especially, time channels. One may recall the fast comparators for the timing circuits and time spectrometry, economical comparators of the nanosecond range, used in the time processing channels for signals of LHC tracking detectors.

The given section considers comparators for time processing channels, which, as the literary sources show, should meet the following requirements:

Firstly, an extremely large channel number imposes tough restrictions on power consumption which should not exceed 20...30 mV.

Secondly, the comparator should have a low-resistance differential output for connection with a high-resistance differential input of a time to digital converter. Output logic levels should be compatible with small logic step standards, for instance GTL, which are preferable from the viewpoint of speed and consumption.

Thirdly, in order to provide the required accuracy of measurements, the duration of the leading and trailing edges should not exceed 1...3 ns at a capacitance load of each output of about 5 pF relative to ground - a typical value for the printed circuit boards. For the same reason the offset voltage is to be provided in the limits of 1..3 mV.

Fourthly, in order to prevent false triggering it is desirable to have a small (0,5...3 mV) hysteresis.

Besides the enumerated basic requirements, it is useful to be able to control the hysteresis, have at disposal an additional latch function and a base line restoration (BLR) circuit. In a multichannel chip it is expedient also to have a circuit of the "common OR" kind, switched on/off by supply voltage.

With account of the above presented there have been designed and manufactured in Russia three versions of comparator ICs.

The first of them is a 4-channel micropower comparator. Each comparator channel is built as a differential circuit with two gain stages and intermediate emitter followers. Output followers are included to reduce output impedance. Internal positive feedback is applied to the input stage, what increases DC gain and provides a hysteresis. The output stage is fed through a separate lead of the positive supply source (+2,0...+3,0 V) and provides the GTL-standard. The main parameters of the comparator are adduced as follows:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption per channel, mV</td>
<td>18</td>
</tr>
<tr>
<td>Supply voltage, V</td>
<td>±3</td>
</tr>
<tr>
<td>Offset voltage, mV</td>
<td>3</td>
</tr>
<tr>
<td>Built-in hysteresis, mV</td>
<td>2.5</td>
</tr>
<tr>
<td>Propagation delay, ns</td>
<td>8</td>
</tr>
<tr>
<td>Rise-time, ns</td>
<td>5</td>
</tr>
<tr>
<td>Fall-time, ns</td>
<td>7</td>
</tr>
</tbody>
</table>

The three latter time characteristics for the given comparator and others were measured at the load capacitance of 5 pF, threshold voltage of 30 mV and a signal over threshold overdrive of 50 mV.

The second version of the 4-channel comparator is built similarly to the first one, except the additional circuits controlling the hysteresis and the output logic. The hysteresis is changed in the range of (0...4,5) mV. Depending on the supply voltage of the output stage (separate pin), the output signals may correspond to the GTL, ECL, or TTL standards as needed. Due to the circuit complication, occurred thereat, the power consumption has increased by 30 mW per channel.

Both versions were implemented in limits of a single planar full-custom bipolar process. The chips differ only in their platings.
2. AN EIGHT-CHANNEL IC, CONTAINING A BASE LINE RESTORER AND COMPARATOR.

The given section describes the third version of comparator IC. The 8-channel IC contains in each channel a circuit of base line restoration (BLR) and high speed voltage comparator. The circuit of one channel is shown in fig.1.

The channel is intended for operation from a single-ended signal of positive polarity, taken from the shaper output [1]. The use of the shaping capacitor simultaneously as a DC decoupling one allowed to eliminate the bias voltage originating in the previous stages.

![Figure 1: The circuit of one comparator channel](image)

The BLR circuit has a small inherent bias voltage with a small temperature coefficient. Particularly this is achieved by introducing an internal voltage stabilizer (transistors Q6-Q9 and resistors R3, R5-R7). The actually obtained bias voltage of the BLR circuit together with the comparator does not exceed 2-3 mV, what can be neglected in comparison with the standard value of threshold (~10 mV).

The restoration of base line in the designed circuit takes place much faster, than in ASD/BLR designed by Pennsylvania University [2]. The time resolution for pulses of close amplitude makes up < 60 ns (< 100 ns for ASD/BLR). For the worst case (a small-pulse superimposed on the tail of a large one) the time resolution makes up < 200 ns (<600 ns for ASD/BLR).

The comparator circuit is built according to the classic circuit with differential input and output. However, some of its peculiarities should be marked.

Since the microwave transistors of the semicustom array have small base current amplification (~35), a Darlington circuit was used at the comparator input in order to reduce the input bias current. The first differential stage has positive feedback, that provides a noise suppressing hysteresis loop (ΔV) about 2 mV wide. The output stage is built as a quasi-push-pull circuit, where the signals of positive polarity are transferred by transistors Q21 and Q25, whereas the ones of negative polarity – by Q22, Q23 and Q24, Q26. The pair of Shottky diodes connected opposed in parallel provides output logic levels of the GTL standard.

The speed of comparator is best of all displayed by the switch-over transients at overdrive levels Vod=5, 20 and 100 mV, presented in fig. 2. Since the comparator output is differential, the duration of transients from logic unity to logic zero and vice versa, is as it should be expected, practically equal. Therefore in fig. 2 there are presented only the plots of transients from logic unity to zero. The corresponding results are tabulated in table 1. Right there are presented also the static parameters of comparator.

<table>
<thead>
<tr>
<th>Table 1: Basic parameters of the comparator.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{od}$</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>5 mV</td>
</tr>
<tr>
<td>20 mV</td>
</tr>
<tr>
<td>100 mV</td>
</tr>
</tbody>
</table>

Figure 1: The circuit of one comparator channel
The given 8-channel IC contains one more interesting peculiarity — it is added by a circuit implementing the logic OR function for all 8 channels. This, for instance, becomes useful at the stage of calibrating, adjusting multichannel experiments, as well as at choosing useful events. In the given case this has been reached by combining the outputs of eight channels, as shown in fig. 3. The output of the “OR” circuit is implemented as an “open collector” one (Q19), what allows to increase the number of the outputs, combined into one “OR” circuit, directly on the printed circuit board. The circuit is provided by an internal voltage stabilizer and gate with transistors Q21, Q22, which allow to disable the “OR” circuit through its supply voltage in case of necessity.

The 8-channel IC was implemented on the basis of a semicustom bipolar array.
3. AN ASIC FOR TIMING DISCRIMINATORS

The LHC multichannel detector systems require an increase of the processing channel number (tens and even hundreds thousand), what inevitably entails a reduction of space, allotted for the electronics of a channel, processing preliminary the signals of a detector, as well as a reduction of power consumption. Requirements are set thereat to preserve or even improve the main precision and energy parameters of electronics, achieved with standard (NIM, CAMAC, VME) units. A success in solving these problems with standard general application ICs appears often extremely difficult.

The structure, contents and basic parameters of a new ASIC, intended to implement the units of time reference to signals of nanosecond duration and with an amplitude of 5mV...2,5V at an accuracy of tens of picoseconds, is described. It can be used to implement CFD, LED, window and extrapolation discriminators.

In the course of design there has been worked out an optimal set of IC components. One chip contains two similar channels of timing discriminators.

The structure of one channel is shown in fig. 4. It is a development of the previous design of the timing discriminator [3]. One channel, along with the most principal cells, namely comparators and D-flip-flops, comprises voltage stabilizers, supply filters, input signal monitoring circuits, buffer amplifiers for driving low-ohmic loads. This all has the purpose of raising the integration scale of the timing discriminator as a whole.

![Figure 4: The structure of the timing discriminator channel.](image-url)
4. CONCLUSIONS

In this paper the requirements to the parameters of discriminator ICs, being part of the time-processing channels for signals of LHC tracking and time-of-flight detectors, are described.

Also the structure, contents and basic parameters of new ASICs are presented. Among them are two versions of four-channel comparator ICs, an eight-channel IC (comprising a base line restorer and comparator, supplemented by an «OR» circuit) and ASIC for the implementation of the units of time reference to signals of nanosecond duration with amplitudes of 5mV...2,5V (it can be used to implement CFD, LED, window and extrapolation discriminators).

The greatest attention was given to reduction of power consumption, minimizing crosstalks, increasing channel characteristics reproducibility as well as to the simplicity of their adjustment, because these discriminators are intended for using in multichannel experiments.

REFERENCES


2. M.Newcomer, A.Romaniouk ASDBLR chip operational properties studies at CERN. RD6 Note, January 1996.

16 CHANNEL PRINTED CIRCUIT UNITS FOR PROCESSING SIGNALS OF MULTIWIRE CHAMBERS. A FUNCTIONALLY ORIENTED SEMICUSTOM ARRAY

Department of Electronics, Moscow Engineering Physics Institute, 115409, Kashirskoe shosse 31, Moscow, Russia, e-mail: atkin@eldep.mephi.ru

ABSTRACT

The matters of designing, studying and testing the printed circuit units (PCU), intended to read out and process preliminary the analog signals of wire chambers (the range of detector capacitances 5...20 pF and that of signal currents 1...200 µA), are discussed. The units were designed as 16 channel SMT daughter boards (dimensions 90*40 mm sq.).

Also a version of the bipolar semicustom array (SA) is described, which is a functionally oriented one, that is a one intended especially to implement ICs of front-end electronics. The given chip has two modifications (for accommodation of 4 or 8 analog channels) and contains npn- / pnp- transistors with unity-gain frequencies over 2/1.5 GHz at currents about 0.5 mA.

1. INTRODUCTION

The requirements to PCUs, containing front-end electronics, on their channel number, electrical and mass-dimensional characteristics quickly change and become with time more and more hard. Under such conditions the close interaction of designers and manufactures of ICs and PCBs is highly topical. Particularly that allows to alter flexibly and correspondingly the design of these items with the aim of implementing the most compact versions of PCUs.

The next section deals with the design of 16-channel PCUs. And after it follows a section, considering the approach to the design of front-end ICs, based on especially developed functionally oriented semicustom arrays.

2. 16 CHANNEL PRINTED CIRCUIT UNITS

Specific PCUs UP2540 (two versions denoted by -L and -U) have been designed as daughter boards, mounted on mother-boards and fixed to the multiwire chambers of the spectrometer, being developed at present in the framework of the International Project HADES (GSI, Darmstadt, Germany). The given PCUs (see the photo in fig. 1) have been manufactured in the Scientific Research Institute of Pulse Technology (Moscow) and are a development of the PCUs UP2542 [1], done in accordance with the new specifications (http://dslep01.gsi.de/~hades/docs/mdc/notes-02-98.htm).

Figure 1: The photo of UP2540 PCUs (-L and -U modifications)

The basis of new PCUs are the Russian application specific ICs of a 4-channel amplifier-shaper and a 4-channel comparator, having, besides the main differential outputs, an additional common logic OR output. Both ICs have been manufactured in the State Research Institute "Pulsar" (Moscow) by means of a bipolar n-p-n full-custom process.

16 channels, each of which is a series connection of a preamp, shaper and comparator, are placed on a 4-layer PCB with the dimensions of 90*40 mm sq. In order to raise the mounting density approximately twice, the
PCUs are mounted on the mother board in the form of a bookstand structure, using the HIROSE board to board microconnectors of type FX4BH-40 and the HARWIN FPC input connectors of type F10-210 for connecting to the drift chambers. Besides that, a separate application of different UP2540 PCU versions is possible. Since at such a board disposition a considerable area of the boards was occupied by connectors, there were studied and compared several versions of chip packaging:

- in metal-ceramic SMT cases;
- on a ceramic substrate;
- on a polyimide flexible film;
- in a caseless construction with compound encapsulation.

To implement the version in SMT cases we used the Russian case H09.28-1B, having 28 pins. This case has proved itself well from the viewpoint of screening the chip against external electromagnetic disturbances. Moreover, the Russian case H09.28-1B, having 28 pins. This case in comparison with the one with ceramic substrate reduces the occupied area. For its full utilization at test preliminary the ICs.

The version with flexible polyimide film has a small area and allows preliminary chip testing, what is especially important at serial production. However the accuracy of manufacturing this kind of encapsulation even at a pitch of 0.5 mm raises considerably production costs in comparison with the one with ceramics.

The caseless design provides the lowest costs and occupies the smallest area. But the replacement (repair) of a damaged IC covered by compound is then complicated. Moreover there is required the capability of welding simultaneously the leads to chip pads and to PCB pads.

The basic electrical characteristics of UP2540 are presented in the table 1.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transresistance, kOhm</td>
<td>20</td>
</tr>
<tr>
<td>Input resistance, Ohm</td>
<td>160</td>
</tr>
<tr>
<td>Shaper output rise time, ns</td>
<td>10</td>
</tr>
<tr>
<td>Output pulse duration at base level, ns</td>
<td>40</td>
</tr>
<tr>
<td>Shaper output full swing, V</td>
<td>1.4</td>
</tr>
<tr>
<td>Comparator threshold setting, mV</td>
<td>10-180</td>
</tr>
<tr>
<td>Comparator rise time, ns</td>
<td>5</td>
</tr>
<tr>
<td>Comparator fall time, ns</td>
<td>7</td>
</tr>
<tr>
<td>Comparator propagation delay, ns</td>
<td>8</td>
</tr>
<tr>
<td>Power consumption per channel, mW</td>
<td>50</td>
</tr>
<tr>
<td>Supply voltage, V</td>
<td>±3</td>
</tr>
<tr>
<td>Comparator output logic</td>
<td>GTL</td>
</tr>
</tbody>
</table>

The UP2540 (-L,-U) in comparison with UP2542 accomplishes an additional logic function of a common OR, that is it shapes an output pulse at the signal arrival to at least one of the 16 inputs. The OR function is implemented at two levels: by joining 4 channels inside the IC and by joining 16 channels at the PCU level. The common OR, may be switched on/off by means of an external TTL signal coming from the mother board. Moreover the daughter board OR signals can be simply summed on the mother board level as a wired OR.

The PCUs are regarded to be the prototypes for reading out the signals of wire trackers of ATLAS.

3. FUNCTIONALLY ORIENTED SEMICUSTOM ARRAY (FOSA)

The part of SA in manufacturing front-end ICS has been limited up to the present moment by the creation of experimental samples or prototypes of future full-custom ICS. This status, bound with the inadaptibility of the produced analog and analog-digital SAs to the implementation of front-end channels, can be changed by developing and manufacturing application specific (functionally-oriented) SAs.

The advantages, common for SAs (reduction of design and manufacture times and of electronic product prices), can be thus extended over the new semi-custom front-end ICS, manufactured on the basis of new SAs, including the ready for use ones. The described approach to designing and manufacturing front-end ICS, along with the traditional approaches, has been developed during the last few years by MEPhI together with a number of Russian technological enterprises. The characteristics of these semicustom ICS and the very possibility of their competition with full-custom ICS are largely defined by the peculiarities of the technology employed.

In [2,3] one of such chips has been described, named an application specific semicustom array - ASSA, and an example of its application has been presented. The ASSA is intended to accommodate up to 8 front-end channels on a chip, but is not a complementary one (contains only npn-microwave transistors).

The version of SAs, here described, uses a complementary bipolar technology with component isolation by pn-junctions and foresees the capability to arrange all necessary connections both in a single- and double-layer plating. This available technology has been chosen for its simplicity and relatively low cost. These SAs have been called functionally-oriented ones (FOSA) and in prospect will include two modifications (the minor and major chips - for 4 and 8 channels respectively). The transition to complementary technology allows to improve essentially the relationship between such important channel parameters, as speed, power consumption and dynamic range at reduced supply voltages. Besides that, the capabilities of SA are extended to implement both all the basic and many auxiliary functional arrangements of a channel, necessary for various applications and having sufficiently good characteristics.

In the general case the front-end channel (and a single FOSA channel, as far as it is available with the technology employed) can comprise the following arrangements:
- a low-noise preamp or a differential instrumentation amplifier;
- a shaper;
- a base line restoration (BLR) circuit for operation at high input rates (if a differential shaper signal is necessary to be processed, two such circuits are necessary - one for each polarity);
- a comparator (actually several "elementary" comparators may be required, if for example a "constant fraction" mode is necessary);
- an input section of ADC or output logic with current switches, which actually can be accommodated only on a chip large enough by its size;
- auxiliary arrangements (like a built-in supply voltage stabilizer, reducing the influence of stray couplings inside and between the channels, caused by a common bus).

The overall structure of the minor area FOSA with the designation of the separate regions for functional arrangement disposition is shown in fig. 2.

Figure 2: General view of the chip (only the two upper channels are shown) with the designation of the separate regions for placing the functional arrangements in each channel [OA - regions for placing the operational amplifiers with a voltage (U) and current (I) feedback].

Remark: The components of the positive supply voltage stabilizers are accommodated in the gaps between particular channels, as well as between the outer channels and the contact pads.

Besides functional completeness, at designing the FOSA there were considered the requirements to the total number of components in a channel, which must be sufficient to accommodate a spectrometric channel. A preliminary development of the spectrometric channel for one of the semiconductor detector types has shown, that this channel is comparatively complicated (contains about 200 transistors) and supposes the use of a certain number of mounted external components (a FET at the charge sensitive amplifier’s input, high ohmic resistors etc.). That means the necessity of a sufficient number of free contact pads. Therefore the minor area FOSA (4*5 mm sq.) contains a maximally available number of contact pads (84).

In order to place a maximal number of components and functional arrangements in the FOSA there is implemented a non-standard for most of SAs solution – an unsymmetrical (oriented at routing the schematic circuits, developed in advance) lay-out for the internal parts of a channel, whereto the requirements are
practically independent of the specific application.

The much less complicated time processing channel, which structural diagram is shown in fig. 3,

![Structural diagram of the time processing channel](image)

The simulated characteristics of the time processing channel, designed for the wire tracking detector, are the following:
- input resistance ...............about 330 Ohm;
- transimpedance...............(20...30) kOhm;
- inherent rise and fall time........not exceeding 8 ns;
- maximal input rate of the processed signal..............10 MHz;
- output logic levels................compatible with GTL;
- power consumption (at the supply voltages of ±3.3 V)........not exceeding 40 mW.

The variety of components in the channel of FOSA (minor chip), their number and particular characteristics are presented in table 2. One should note, that the isogradient structures, having an improved within-pair matching of components at the expense of symmetrical lay-out and increased dimensions, as well as Schottky diodes are absent in the majority of SAs produced, what hinders the improvement of front-end channel parameters.

<table>
<thead>
<tr>
<th>Component variety</th>
<th>Component characteristics</th>
<th>Number of components</th>
</tr>
</thead>
<tbody>
<tr>
<td>kind</td>
<td>type</td>
<td>in channel</td>
</tr>
<tr>
<td>Transistors</td>
<td>npn-/pnp-of minimal area</td>
<td>β̂=100, f̂ ≥ 2 GHz(npn)/1/5 GHz(pnp) at Ie=0.5...2 mA, rε ≤ 200 Ohm, Cn ≤ 0.1 pF, Cc ≤ 1 pF</td>
</tr>
<tr>
<td></td>
<td>isogradient npn-/pnp-structures of 4 low-noise transistors</td>
<td>rε ≤ 50 Ohm</td>
</tr>
<tr>
<td></td>
<td>npn-/pnp- structures for increased working currents all types in total</td>
<td>Iε,ref= 5 mA</td>
</tr>
<tr>
<td>Shottky diodes</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Resistors</td>
<td>based on polysilicon (specific resistance about 50 Ohm/&quot;and 1 kOhm/&quot;), including isogradient structures</td>
<td>basic range of resistances 50 Ohm...8 kOhm (without account of possible connections), high-ohmic resistors with a resistance about 40 kOhm</td>
</tr>
<tr>
<td>Capacitors</td>
<td>with a structure of metal-dielectric-polysilicon</td>
<td>total capacitance per channel ≥180 pF</td>
</tr>
</tbody>
</table>

Table 2. The set of components of FOSA (minor chip).

Remark: Particular values in the table may be altered in the course of further development.
4. CONCLUSIONS

In the given paper there are presented the results of designing two types of items for implementing front-end channels.

Firstly, there are the finished PCUs UP2540 (two versions denoted -L and -U), containing 16 channels each, as distinct from the earlier designed and manufactured UP2542 with 8 channels. The UP2540 has thereat an area almost twice smaller and includes an additional logic OR circuit.

The second type of items are the bipolar functionally front-end oriented semicustom arrays (FOSA). The FOSA, differing essentially from the produced SAs in the component set and structure, may serve as a good basis to implement semicustom front-end ICs.

The joint development of FOSA, front-end ICs on their basis, PCBs and PCUs provides a great flexibility - available becomes a choice of the structural versions of IC implementation, right up to a judicious pin assignment, conforming with stringent requirements to the configuration of mother- and daughter-boards. In the case of a successful FOSA approbation the solutions, set in it, can be implemented on the basis of the updated versions of bipolar technology (Russian or Western), which can provide better (comparing to FOSA) parameters of front-end channels.

REFERENCES


2. A. Goldsher et al. A semicustom array chip for creating high-speed front-end LSICs, Third Workshop on Electronics for LHC experiments, CERN/LHCC/97-60.

3. A. Arkhangelsky et al. An application specific semicustom array for the implementation of multichannel front-end ICs, Third Workshop on Electronics for LHC experiments, CERN/LHCC/97-60.
A Fast and Simple Trigger for High Energy Conics

H. Gemmeke, D. Tcherniakhovski, FZK, Karlsruhe, (email: gemmeke@hpe.fzk.de) and V. Klinger, DESY, Hamburg, Germany, (email: klinger@desy.de)

Abstract

A massive parallel trigger system for efficient data reduction and event recognition is under design for the 14400 channels of the AUGER fluorescence detector. The trigger is combined with a cost-effective control and readout by PCI devices. The first level trigger includes a count-rate dependent trigger-threshold and suppresses Cerenkov pulses, and the second level trigger will identify straight tracks of cosmics in the AUGER fluorescence detector. Configurable FPGAs are used to enable parallel processing and yields a cheap high-speed data handling solution. Furthermore, the use of one PCI-board type for the readout allows a very cost-effective solution for the overall system. By digital pulse-shape recognition more than 90% of the Cerenkov pulses will be suppressed. Due to fast hardware event-pattern recognition of three adjacent pixels within the detector we expect an excellent noise reduction of about \(3 \times 10^5\).

1. INTRODUCTION

We are developing a trigger-system for the Fluorescence Detector (FD) proposed for the PIERRE AUGER Project [1]. The FD works in correlation with the Cerenkov ground detector array [4] to be installed. The FD identifies unambiguously the energy of cosmics with energies more than \(10^{19}\) eV and the source(s) of emission by the angular distribution of these events. The detector is looking with a pixel camera with 4800 photomultipliers (PMT). Each pixel covers a cone of 1.5 degrees in the sky. Straight tracks of cosmics have to be identified in the presence of a high level of background noise (200 Hz) for each pixel, starlight and Cerenkov events. The actual design consists of 100 PMTs per sub-mirror, four sub-mirrors per mirror system and 12 mirror systems per eye (see fig. 1). For the identification and reconstruction of cosmics with very high energy a continuous film of the signals at each PMT has to be taken with a minimum digitization rate of 10 MHz.

Because of the overall involved number of readout channels the system costs and power consumption are important factors for the design. Low power consumption will be implemented as far as possible by using 3.3 V technology. At the same time low power consumption spares money for active cooling and helps to keep temperatures of components as low as possible, necessary for an experiment with a long lifespan (= 20 years). On the other hand the symmetry of the system facilitates low costs. The number of different boards to be developed is low. The main task for the trigger is fast data reduction and therein minimizing the amount of necessary buffer storage and readout speed.

2. SYSTEM CONCEPTS

This paper concentrates on the optimization of the system under cost constraints while a former paper [5] concentrates on the methods to suppress background. The costs of the electronics for the AUGER fluorescence detector will be mainly influenced by four factors:

1. physically necessary dynamic range of the ADC-system,
2. trigger and necessary memory buffer to guarantee data integrity,
3. gain control by high voltage at PMTs or with programmable gain at preamplifiers, and
4. readout system.

These topics will be discussed in the following sections.

2.1 Dynamic Range of Fluorescence Signals

The high dynamic range of the fluorescence signals \(10^4\) to \(10^5\) or 14 to 16 bit) and on the other hand the necessary low relative resolution of 6 to 7 bits lead to two 10 or 12 bit ADCs or three 8 bit ADCs as the most economic solution for the digitization. An amplifier with a non-linear characteristic would be another smart solution. But the necessary precise calibration and temperature stabilisation is a difficult problem in the rough, non-temperature stable environment of FD electronics. Digital solutions with ADCs delivering constant relative resolution (5 bit mantissa and 3 bit exponent) are under test for CMS [2], but have an unacceptable high power consumption (1.3 W/channel) and insufficient number of bits for our application. We chose two 12 bit ADCs.

Figure 1: Schematic view of one eye of the fluorescence detector

Fluorescence Detector
4800 PMT's per eye
100 PMT's per submirror
1.5° per PMT
Eye
(12*4 mirrors)
2.2 Optimum Buffer Memory Size

The necessary size of the buffer memory, the speed of the readout, and the quality of the trigger are strongly correlated. For a positive trigger of each contributing PMT a film of 100 μs with time slices of 100ns resolution has to be taken. The trigger rate for each PMT will be limited to 100 - 200 Hz after first level trigger. By optimization of the trigger (see next chapter) the size of the buffer memory was limited to eight 1k*16bit ring buffers. An organisation of this buffer in one dual port memory was taken.

2.3 Gain Control of Each PMT Channel

The gain of each PMT channel may be controlled by the high voltage at the PMT or by a digitally adjustable gain at the preamplifier. A multiplying DAC or a programmable amplifier is today state-of-the-art and may be cheaper than an individual programmable high voltage supply. We will study this line in the design. Furthermore a low gain PMT with only 6 or fewer dynodes has a lower gain spread than a multi-dynode PMT at the same gain, because the tube with a lower number of dynodes has to be driven nearer to saturation. That gives in addition a good single electron resolution.

Also the lifetime of the PMTs in such a large dark current environment is an important limitation for the design. Conservative estimates of the lifetime of PMTs are given by a maximum drawn charge in the range of 300 - 1000 C [3]. With a low gain tube, gain 1 - 5*10^3 we won't reach ageing limits within 20 years, the possible lifetime of the AUGER experiment. For a background of 3 pe/100ns, gain 5*10^3, 20 years of operation, only at night time (at 1/3 of the day) the collected charge will be of the order of 50 C. That gives enough safety, even if we include stars of 2^nd order of magnitude in the sight of the PMTs. We would get an additional factor of 2.65 higher charge collection, safely within the range of 300 C.

Following this simple overall concept we may use a very cheap collective HV-systems for each mirror system.

2.4 Selection of Readout System

Due to the geometrical organisation of the detector, see fig. 1, one data concentrator is necessary in each of the mirror systems. To obtain a good price-performance ratio we select a simple industry PC. In our conception a single industry PC controls one mirror system consisting of 4 sub-mirrors with 4 * 100 PMTs guaranteeing a profitable and flexible control design (< 1000S). This PC is connected via PCI bus to a passive PCI backplane with the locally installed sub-mirror electronics, designed for 100 PMTs as shown in fig. 2 and 3. The front-end system is a proprietary 6U Euroboard system. The mirror systems are not equipped with a disk to guarantee better long term stability, but contain 256 Mbyte of memory to allow comfortable operation and to provide sufficient buffer space. The CPUs are equipped with passive cooling instead of fan units to yield a longer mean time between failures.

With the developed trigger the data rate per eye will be lower than 1 Mbit/s. Due to this fact it is sufficient to...
connect the PCs of one eye by Ethernet. The mirror client PCs boot from the eye server, which is equipped with a disk system. The operating system will be LINUX because of its fast context switching speed and low costs. Currently a PC system with two clients is under test to learn the software problems and the performance of the overall system. For the connection to central computing of the ground detector a mono mode fibre FDDI has to be provided because of the long distance (≥ 20 km). Furthermore, the triggers of the eyes have to be correlated with the trigger of the ground detector at the central computing station.

If the Cerenkov suppression is not sufficient, we leave a free PCI-slots on the mirror level to install a very fast neural network board [6], which is capable to handle our size of input patterns of 400 pixels, as given by the mirror size. The board is equipped with four SAND/1-chips and has a processing power of 8*10^6 connections per second.

3. TRIGGER

In the following we describe the front-end electronics and the first- and second-level trigger in more detail.

3.1 First Level Trigger

Ten channels of PMTs are digitized and pre-processed on one front-end board. By integrating the 1st level trigger of these ten channels into one single FPGA (field programmable gate array) we have reduced the amount of analogue electronic and improved the modularity and flexibility of the design. This FPGA contains the digital integration and Cerenkov detection, see fig. 4. After a 10 MHz ADC on each photomultiplier channel a sliding boxcar running sum for 10 time slices is inserted to improve the noise performance of the adaptable trigger threshold. Due to the tenfold digital summation the signal to noise ratio for the trigger threshold can be improved by a factor \( \sqrt{10} \) without losses in the time resolution given by the 100ns conversion time of the ADC's. The chosen Altera FPGA has enough free space left for reprogramming to a larger integration time (eg. 2 μs) to improve signal noise ratio further if it is necessary.

The threshold ThSum in fig. 4 is controlled by the trigger rate. The trigger rate is prescaled on the same FPGA in a hit-rate counter and then readout and accumulated via PCI in the mirror PC. For larger deviations from the standard value (100-200Hz) the PC will correct the threshold to avoid insensitivity or high noise rates.

Parallel to the integrator a finite-state-machine (FSM) rejects fast Cerenkov pulses with 90 to 95 % probability. Cerenkov pulses are recognized by their short duration and high charge in one 100 ns trigger slice. This signature results in most cases in a 010 trigger pattern at consecutive time slices discriminated with sufficient high digital thresholds, see fig. 4. If a Cerenkov pulse is detected, the ADC data will be cleared to the actual value of the noise level. Due to this provision the sum-energy trigger is corrected. Two additional registers (-2,-1) in the sum-energy pipeline correct for the time delay of this decision.

Together with some bookkeeping and control electronics 2400 logic cells or 14 k equivalent gates on an Altera FPGA were used to install the described algorithms for ten PMTs.

3.2 Second Level Trigger

The pixel trigger generated by the sub-mirror electronic is processed in the second level trigger. The event detection combines a geometrical and a timing criterion, which have to be fulfilled by an air shower. All criteria are integrated into an FPGA hardware present for each sub-mirror system (100 PMTs) once.

A shower at a maximum distance of about 20 km should trigger 3 PMTs at least, what is defined as a minimum event. Due to the continuous tracks of the cosmos three adjacent hits of PMTs in succession are taken as geometrical criterion. To guarantee overlap the signals are extended by approximately 3 μs (see fig. 5) and by the coincidence of a neighbouring PMT avoiding unnecessary signal extensions – enlarging the probability for noise triggers. This trigger function is a completely

![Figure 4: 1st level trigger: boxcar running sum and Cerenkov pattern recognition.](image-url)

![Figure 5: Neighbourhood coincidence for each pixel.](image-url)
local task and can be executed in parallel on the FPGA yielding together with the following geometrical scan a delay of 1 μs only.

Our trigger concept is based on areas of 9 pixel (3 × 3) pixels. A look-up table (LUT, see fig. 6), for economic realization and maximum flexibility implemented into the internal FPGA-RAM does the event detection within this minimum area. In a scan one sub-mirror is covered by all possible arrangements of these minimum areas. We have realized the scan by 10 LUTs implemented into the internal FPGA-RAM scanning in each step 10 minimum areas in parallel, see fig. 7. Therefore we need 9 steps to evaluate the whole mirror and the adjacent PMTs from the neighbour mirrors. This scan is a compromise between fast event detection and an optimized hardware. Using this principle we calculated an excellent noise reduction of about 3 × 10^5 by the hardware.

The time criterion rejects all events, which have duration of more than 60 μs. This function is realized with a finite state machine implemented into the FPGA, too. In addition the FSM determines the end of a trigger and controls the data control for saving the valid events. Furthermore the FSM generates all read and write addresses for the dual port memories and the time stamp for each detected event.

Both designs – the first-level and the second-level triggers – are described using the hardware description language VHDL and both designs are automatically synthesized. Working with state of the art design tools we are easily able to adapt to changing evaluation parameters in the future.

4. CONCLUSION

We have presented the concept for an efficient trigger system for the Pierre Auger fluorescence detector. The hybrid system design is based on configurable and programmable hardware for the first-level and second-level trigger and software for the higher-level triggers. Using a modular structure an efficient data management is possible reducing memory requirements. In addition the number of different boards is minimized. All aspects of our system concept reduce on the one hand the logistic problems for maintenance and bring down on the other hand the system costs. Moreover these hardware based triggers yield an excellent noise reduction and allow a flexible event detection. The actual FPGA trigger designs are finished and synthesized.

At the moment we are preparing a first prototype system to evaluate our concept presented in figure 2. The boards for the second-level trigger with the PCI interface to the diskless PCI computer are under design. A prototype experiment at Gran Sasso end 1999 will evaluate the presented designs. The massive parallel trigger concepts and simple PCI structure and overall cheap system solution may be also of some stimulation for other projects.

5. REFERENCES

2. A. Baumbergh et al., Charge integrator and encoder ASIC for readout of the CMS Hadron calorimeter photodetectors, Proc. of the 4th workshop on electronics for LHC experiments, Rom 1998, in session electronics for calorimeters.
3. Philips Photonics, Photomultiplier tubes: principles and applications, Philips International marketing BP520, F-19106 Brive, France, p. 4-33.
TDC Chip and Readout Driver Developments for COMPASS and LHC-Experiments


Universität Freiburg,
Fakultät für Physik, Hermann-Herder-Str. 3, D-79104 Freiburg, Germany

*EMAIL: Horst.Fischer@cern.ch

Abstract

A new TDC-chip is under development for the COMPASS experiment at CERN. The ASIC, which exploits the 0.6μm CMOS sea-of-gate technology, will allow high resolution time measurements with digitization of 75 ps, and an unprecedented degree of flexibility accompanied by high rate capability and low power consumption. Preliminary specifications of this new TDC chip are presented.

Furthermore a FPGA based readout-driver and buffer-module as an interface between the front-end of the COMPASS detector systems and an optical S-LINK is in development. The same module serves also as remote fan-out for the COMPASS trigger distribution and time synchronization system. This readout-driver monitors the trigger and data flow to and from front-ends. In addition, a specific data buffer structure and sophisticated data flow control is used to pursue local pre-event building. At start-up the module controls all necessary front-end initializations.

1 INTRODUCTION

The COMPASS experiment at CERN will investigate hadron structure by deep inelastic scattering processes and in addition pursue different aspects of hadron spectroscopy using hadron beams. Comparison with calculations based on operator product expansion or lattice techniques and with model predictions based on chiral symmetry or effective degrees of freedom will help to improve our understanding of hadrons. To reach this objective a new state-of-the-art fixed target spectrometer, capable of standing beam intensities of up to 2 \cdot 10^8 particles/spill and with excellent particle identification, will be put into commission in the year 2000.

These challenging physics goals of the COMPASS Experiment can only be met, if at highest possible beam rates large data statistics can be recorded. This leads to the requirement of an experiment with negligible dead time, which can digest data rates of several Gigabyte per second. This is at the edge of today’s digitization and bandwidth technologies.

The initial approach of the experiment was to minimize dead time by reading digitized data through pipelines where applicable. Availability of and resolution requirements on digitization units have made this goal not feasible for every detector component. The present scenario assumes a maximum dead time of 500 ns for analog sensitive front-end electronics which will digitize signal amplitude or charge with a precision better than 10 bit.

The readout architecture of the COMPASS experiment is summarized in Figure 1. Data are digitized right at the detector by the front-end electronics wherever possible. In case of analog readout the pedestal subtraction and zero suppression is performed by the front-end at the detector. To suppress background for time measurements only those hits are transferred to the data recording units which have a correlation to a trigger time.
The data are transmitted from the front-end to CATCH modules (CATCH = COMPASS Accumulate, Transfer and Cache Hardware). The functionality of the CATCH will be described below.

From the CATCH data are transmitted via a standardized link to the read-out buffers (ROB) which can store all data from one spill. The backbone of this data transfer is the S-link [1] interface and the S-LINK data transfer protocol. Presently about 128 S-LINK connections are foreseen to transmit data with a maximum total bandwidth of about 12 GB/s.

The read-out buffers combine data which belong to one event, check consistency of the data and perform sub-event-building. In a next step they transmit the sub-events via HiPPI [2] or Gigabit Ethernet to filter computers. Here the final event-building is performed and events are reconstructed. The filter farm will reduce the data based on physics cuts by a factor of 5 to 10 and a continuous rate of 12 to 24 MB/s will be transferred to the central data recording facilities at CERN.

2 THE $\mathcal{F} 1$ TDC CHIP

A key element in the experiment is a new developed dead time free TDC chip, the $\mathcal{F} 1$. It will be used to digitize the data from a large majority of detectors. Table 1 shows that the required specifications vary significantly for the foreseen applications of the $\mathcal{F} 1$ chip. Certainly the most challenging demands are defined by the scintillating fiber (SCIFI) detectors. Count rates up to 6 MHz per channel and time resolution better than 100 ps are on the edge of today's technology. When count rates and background become too high, existing limitations in bandwidth on data-links between TDC and the data recording system require on-chip event selection. Detector components like Plastic Iarocci Tubes ($\mu$-Detector 1) or MWPC do not ask for precise timing but require lowest cost/channel due to the large number of channels involved. Thus multiplexed input is desirable for this kind of detectors.

We were forced to develop a new multi-purpose TDC Chip, because no integrated TDC circuit is currently on the market with a sufficient degree of integration and flexibility to fulfill all requirements of COMPASS. In spite of the short time available for the R&D phase for COMPASS we decided to develop a TDC in collaboration with acam [3], a recently founded German enterprise specialized in the development of time measurement devices and applications.

The development of the $\mathcal{F} 1$ resulted in a highly programmable eight channel TDC ASIC based on a low cost 0.6μm CMOS sea-of-gates process. The reasons for only eight channels in a single chip are driven by financial considerations as well as physical limitations. Eight channels in a chip optimize savings due to density on the die and costs for bonding and chip package. In addition chip prizes depend strongly on the number of produced chips and less on the die surface. Hence 6000 chips with 8 channels are more cost efficient than 1500 chips with 32 channels.

The scheme utilized in the $\mathcal{F} 1$ avoids the use of high-speed clocks and shift registers and, therefore, results in very low power consumption. Signal propagation times in gate arrays have very large variations as a function of temperature and operation voltage. Furthermore signal propagation within gates have a spread strongly dependent on the production process. To overcome these disadvantages the $\mathcal{F} 1$ exploits a self calibrating method utilized by voltage controlled delay elements as part of an asymmetric oscillator in a phase locked loop (PLL).

An outline of the chip is shown in Fig. 2. Non-perspective displayed boxes - like trigger counter, PLL or interface FIFO - refer to units which are shared between the eight channels, whereas the perspective displayed boxes - like hit buffer, trigger matching and readout buffer - indicate logic units in the chip which come eightfold and are not shared between the channels.

The preliminary specifications for the TDC are listed in Table 2. The $\mathcal{F} 1$ can be considered as a real multi-purpose chip with very different modes of operation in terms of resolution and functionality.

In the standard mode the $\mathcal{F} 1$ is an eight channel TDC chip with a digitization uncertainty of 150 ps. When a leading or trailing edge of a LVDS-signal [4] is present at one of the channel inputs the time relative to the last reset of the TDC is derived from a PLL and a coarse counter. The time stamp is written into the hit buffer. When a TTL signal edge is present at the trigger input the time relative to the last reset is measured for the trigger signal. In a next step the time stamps, which are stored in the hit buffer, are compared to the time stamp of the trigger time. Data within a pre-set time window are accepted for readout and copied to the output buffer. An 8 or alternatively 24 bit parallel bus is used for readout of the chip. The data bus can be operated at a maximum frequency of 50 MHz.

In the high resolution mode two channels are interleaved by 1/2 least significant bit (LSB) delay. Hence in this mode the $\mathcal{F} 1$ has four channels with a resolution of 75 ps and the

Table 1: Possible applications for the $\mathcal{F} 1$ TDC-chip in the COMPASS experiment.

<table>
<thead>
<tr>
<th>detector</th>
<th>channels</th>
<th>time resolution [ps]</th>
<th>background rate [kHz]</th>
<th>event rate [kHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Straws</td>
<td>37000</td>
<td>1000</td>
<td>600</td>
<td>100</td>
</tr>
<tr>
<td>$\mu$Mega Chambers</td>
<td>15000</td>
<td>&lt;500</td>
<td>&lt;100</td>
<td>&lt;100</td>
</tr>
<tr>
<td>$\mu$-Detector 1</td>
<td>9000</td>
<td>50</td>
<td>&lt;1</td>
<td></td>
</tr>
<tr>
<td>$\mu$-Detector 2</td>
<td>3000</td>
<td>2000</td>
<td>130</td>
<td>&lt;1</td>
</tr>
<tr>
<td>MWPC</td>
<td>18000</td>
<td>600</td>
<td>600</td>
<td>100</td>
</tr>
<tr>
<td>SCIFI</td>
<td>1280</td>
<td>320</td>
<td>600</td>
<td>6000</td>
</tr>
<tr>
<td>Beam Scintillators</td>
<td>512</td>
<td>&lt;100</td>
<td>600</td>
<td>6000</td>
</tr>
<tr>
<td>Recoil-Detector</td>
<td>5000</td>
<td>&lt;100</td>
<td>&lt;100</td>
<td>&lt;100</td>
</tr>
<tr>
<td>Hodoscope</td>
<td>1200</td>
<td>&lt;100</td>
<td>&lt;100</td>
<td>&lt;100</td>
</tr>
</tbody>
</table>
Table 2: Preliminary technical description of the $F1$ based on pre-layout simulations.

**Number of channels:**
- 4 for high resolution mode
- 8 for standard resolution mode
- 32 for pattern recognition mode

**Time bin size:**
- 75 ps for high resolution mode
- 150 ps for standard operation mode
- 5700 ps for pattern recognition mode

**Reference-clock frequency:**
- Between 500 kHz and 40 MHz
  (Clock is used for self-calibration only)

**Differential non-linearity:**
- Less than 0.05 LSB for high resolution mode
- Less than 0.2 LSB for standard mode

**Integral non-linearity:**
- Less than one time bin

**Variation with temperature:**
- Less than one time bin

**Dynamic range:**
- 16 bits

**Double pulse resolution:**
- Typical 22 ns

**Digitization and readout dead time:**
- None

**Hit buffer size:**
- 32 measurements for high resolution mode
- 16 measurements for standard mode
- 16 measurements for pattern recognition mode

**Output buffer size:**
- 8 measurements

**Readout Interface:**
- 16 measurements

**Trigger buffer size:**
- 4

**Power Supply:**
- 5.0 V, optional 3.3 V with reduced resolution
- 30 mA - 80 mA, depending on trigger load

**Temperature range:**
- -40 to +85 degree centigrade

**Hit input:**
- LVDS or TTL

**Package:**
- 160 PQFP

hit buffer for a single channel is increased by a factor of two. Otherwise the principle of operation is the same as in the standard mode.

The third way to operate the chip is the pattern recognition or latch mode. In this mode 32 input channels are connected to eight groups of fourfold latch-registers. Once a leading edge of a signal is detected on a input channel the fourfold input register is activated for the duration of a pre-set time interval and subsequent hits on the other inputs can be registered as well. When the pre-set time has passed, the register is copied to the hit buffer and cleared for new recording. While this transfer is realized a time-stamp with reduced resolution is taken and added to the information from the register.

In the fourth mode the chip can be used like any other normal common-start TDC. After a start-signal on a dedicated start-input has been applied all subsequent time measurements are relative to this start-signal. In this mode the time-stamps are immediately passed to the output bus and not stored in the hit buffer. This mode does not make use of the trigger-matching possibilities of the TDC.

Initialization of the $F1$-chip is performed via a 10 Mbps serial connection. The interface for this link is integrated in...
the TDC chip and no additional external control is needed. As an additional feature the F1 has eight eight-bit registers and a dedicated interface to an eight channel digital-to-analog converter (AD8842) [5], which can be used for threshold control of discriminator units placed on the front-end cards. The integration of the register and the interface in the TDC avoids additional memory and controller units on the front-end board.

3 READOUT DRIVER BOARDS FOR COMPASS

The basic philosophy behind the COMPASS readout architecture design was to unify as much hardware components as possible to save on spare parts and manpower during preparation and during the data-taking phase of the experiment. Having this concept in mind we decided to concentrate the data as close as possible to the front-end into few high-bandwidth data streams. A logic consequence was the development of a standardized data multiplexer board, the CATCH, for all the different components of the COMPASS detector. The CATCH functions mainly as a derandomizer and must provide enough memory for intermediate storage of several events. To concentrate a large number of channels we decided to build the CATCH as a 9U VME board. However, the VME bus will only be used for power distribution, for transfer of set-up data during detector initialization and to spy on a sub-sample of events parasitically - but independent of the data acquisition system - during data taking.

Data input to the CATCH can be performed in several ways. The data-interfaces to the CATCH are designed as mezzanine cards following the IEEE CMC standard [6]. The advantage of mezzanine cards is that they allow easy and fast exchange without hardware modifications and thus give the highest degree of flexibility. Currently we design four different types of mezzanine cards: One card contains four 30 MByte/s HOTLink de-serializer receiver-chips [7] which will be used for front-end boards mounted on the detector; a second card contains F1-chips to assemble TDC boards; a third mezzanine card which contains several FPGA to implement fast 200 MHz dead-time-free scalers and a fourth card which will serve as an interface to the silicon detector readout boards.

The output of the CATCH module is connected through the P2 connector to a S-LINK multiplexer board mounted on the backplane of the VME crate. This multiplexer board is used to optimize the transmission rate on the S-LINK to the available S-LINK bandwidth, which is 100 MB/s/link. Figure 3 illustrates, as an example for the data flow on the CATCH, the use of the Cypress HOTLink receiver-chip as data input source. In this example 24 bit data words are transmitted in three words of one byte each.

The data interfaces are scanned continuously for arriving events. All data are reformatted to 32-bit words and, if necessary, additional hardware addresses are added. These are transferred by the front-end only during the initialization process for unambiguous identification. Next all data from a trigger are packed between a S-LINK header and S-LINK trailer. The S-LINK header and trailer contain a unique bit pattern for identification. Furthermore a S-LINK header contains an event- and spill-number and describes the data source and event type. For each individual event the information contained in the header is received by the CATCH from the Trigger Control System (TCS). The data for one event are passed to the ROB when all front-end cards, which are connected to a CATCH, have transmitted either valid-data or an empty-data word for a particular trigger-number.

The CATCH module can also be used to erase data based on second level decisions from the readout stream. To implement this feature in an experiment the trigger numbers of events, which are rejected by the higher trigger level, have to be distributed to the CATCH boards via the trigger control system. The latency of the second level trigger decision and the total data rate per CATCH determines the memory needed to store events before they are passed to the ROB. Currently the implementation of several data compression methods on the level of the CATCH modules are discussed as a possibility for further reduction of data rates.

Figure 3: Data flow in the CATCH module illustrated for wire chamber readout via HOTLink receivers.
The handling of trigger signals from TCS on the CATCH board is illustrated in Figure 4. The CATCH-module receives trigger signals and a reference clock from the TCS via optical data transmission. The TCS interface board contains an optical or copper cable receiver and a unit to decode the time-division multiplexed signals transmitted by the TCS. The TCS receiver board can be mounted to the P2 connector on the backplane of VME crates. Once the CATCH receives a trigger signal from the TCS it encodes the signal as a pulse with the length of one clock cycle. The encoded trigger signal is passed immediately to the front-end cards synchronous to the COMPASS reference clock (38.88 MHz). To check data for consistency a local event number is generated and compared to the event numbers transferred with the data headers from the front-end.

The physical network layer between front-end and CATCH is realized in standard S/STP CAT 6 [8] cable. This cable is widely used in Ethernet links between wall outlets and personal computers. The great demand for this kind of cable makes it the cheapest solution to connect two points with four differential lines up to frequencies of 700 MHz. In our application one differential line is used to distribute the COMPASS 38.88 MHz reference clock to the front-end. The second line is used to distribute up to four different user signals to the front-end. The signals are distinguished by their length with respect to the COMPASS reference clock. One of the four possible signals is the trigger-signal and another is a time synchronization reset at the beginning of a spill. The remaining two can be defined according to user requirements. A third line is used for a serial link to down-load initialization data to the front-end electronics at start-up. This serial line is operated at 10 Mbps. The fourth line is used to transfer the serialized data from the HOTLink transmitter (front-end) to the HOTLink receiver (CATCH).

4 ACKNOWLEDGEMENT

This work would be impossible without the significant efforts by the staffs of the collaborating institutions, in particular those involved in front-end electronics development. The developments described in this report are supported by the German Bundesministerium für Bildung, Wissenschaft, Forschung und Technologie.

5 REFERENCES

[3] Address: acam-messeleletronic gmbh, Haid-und-Neu Str. 7, D-76131 Karlsruhe; EMAIL: support@acam.de.
DMILL IMPLEMENTATION OF THE ANALOGUE READOUT ARCHITECTURE FOR POSITION SENSITIVE DETECTORS AT LHC EXPERIMENTS

J. Kaplon (email: jan.kaplon@cern.ch)
F. Anghinolfi, P. Jarron, C. Lacasta, J. Lozano, C. Posch, P. Weilhammer
CERN, Geneva, Switzerland
W. Dabrowski, P. Grasela
Faculty of Physics and Nuclear Techniques, UMM, Cracow, Poland
R. Szczygieł
Institute of Nuclear Physics, Cracow, Poland

Abstract

The SCTA128HC chip with analogue readout architecture for position sensitive detectors at LHC experiments has been developed using the DMILL process. The chip comprises all functional blocks required for the analogue readout architecture, preamplifier, shaper, analogue pipeline, derandomising buffer, analogue multiplexer and readout circuitry. It suits well for the readout of silicon detectors in a wide range of detector capacitance (from 0 to 25 pF). The design has been manufactured successfully in the DMILL technology. The design and the test results from the prototypes are presented.

1. INTRODUCTION

Following the demonstrators of the analogue readout architecture, SCT32A and SCT128A, developed in the course of implementation of the DMILL technology we have designed and manufactured a 128-channel prototype chip using the stabilised DMILL process [1]. The new design follows the architecture of the SCT128A chip [2], however, some blocks have been redesigned and some other added in order to make the chip compatible with the overall detector readout system [3][4]. The number of external control signals necessary to operate the chip has been reduced by implementation of a 40 MHz serial interface (only one clock and one command line). All signals to control readout of the analogue memory (Analogue Data Buffer – ADB) and the output multiplexer are generated in the chip by an internal sequencer. To improve the testability of the chip an internal calibration circuit has been implemented.

In order to be able to use the chip with detectors of various capacitances and to optimise the front-end noise performance for a given input capacitive load, the internal bias generators controlled by DACs integrated in the chip have been implemented. This solution allows for compensations of the bias drifts due to radiation effects expected in the devices used. The front-end circuit supports both, the positive and the negative polarity of the input signal.

2. THE ARCHITECTURE

Figure 1 shows the block diagram of the SCTA128HC chip architecture. The chip comprises five basic blocks: front-end amplifiers, analogue pipeline (ADB), control logic including the derandomizing FIFO, command decoder and output multiplexer.

![Fig.1. Block diagram of the SCTA128HC chip.](image-url)
The bias currents of the input transistor, integrator and readout amplifiers are controlled by 5-bit DACs. In order to improve the testability of the chip an internal calibration circuitry has been implemented. The circuitry allows to generate calibration pulses with the amplitudes controlled by an 8-bit DAC and the delay with respect to the clock phase controlled by an internal delay circuit. One of the four internal calibration lines can be selected by a 2-bit address. Communication with the chip is provided with the command decoder which controls all mentioned above circuits as well as the readout logic.

3. READOUT PROTOCOL

The readout logic is designed in such a way that two 128-channel chips can be read out via one analogue link. Upon receiving the trigger signal the data is sent first from one chip while the second one connected to the same fibre waits for the appropriate number of clock cycles before sending the data. The data package from each chip consists of a 4-bit header, three analogue values which can be used for calibration of the optical links, 1-bit FIFO overflow flag, 4-bit BCO counter and 4-bit Level-1 trigger counter. Figure 2 shows the scope view of a read-out sequence at nominal readout speed of 40 MHz.

The 4-bit BCO counter and L1 counter returned by the chip can be used for synchronisation of each trigger with the physical data from the detector. In the case of overflow of the readout buffer the control logic issues an overflow bit which is bundled with the physical data. After detection of the overflow error the chip should be reset by means of the soft-reset command.

The maximum clock rate of the multiplexer and the readout circuit is the same as the rate of sampling the data, i.e. 40 MHz. The chips can be read out with a lower rate (40 MHz divided by 2, 4 or 8) which is programmable. All communication with the chip i.e.:

- sending the level 1 triggers,
- sending the software reset,
- loading the DACs,
- issuing the internal calibration pulses
- programming the speed of the output MUX

is executed via the fast 40 MHz serial interface.

4. LAYOUT

Figure 3 shows the layout of the SCTA128HC chip. The front-end channels and the analogue pipeline are laid out with a pitch of 42 μm. Input bonding pads are laid out with 60 μm pitch. The bond pads for supply voltages and control signals are located on both sides of the chip. The die area is 7.9x8.0 mm² of which about 30% is occupied by the storage capacitors in the ADB.

5. TEST WITH CALIBRATION PULSE

The evaluation of the chip performance has been done using a test set-up built of a VME sequencer module (SEQSI) and a VME data acquisition module (SIROCCO) running under OS9 system or via a PC-VXI interface. All presented tests have been done using internal calibration circuitry. The noise measurements have been done using statistics of 500 triggers for each scan point. The data has been analysed using the ROOT package.

5.1 Front-End Performance

The concept of the SCT128HC design is based on a fast front-end circuit providing the peaking time of 25 ns which matches the sampling frequency of 40 MHz. This way only one sample of the peak value for each pulse is stored in the ADB.
The pulse shape at the output of the shaper can be reconstructed by scanning the delay of the calibration signal with respect to the clock phase so that a different time slice of the pulse is readout for each scan point. Because the internal delay register is built as a simple chain of inverters it is not designed for an absolute delay value. Since the range of this register is about 50 ns, allowing delay scans across latency of two consecutive triggers, a cross calibration with an external 40 MHz clock is possible. For the present batch a factor of 1.2 has been obtained. Figure 4 shows the result of one delay scan for a particular channel of the SCTA128HC chip. The injected charge was 6 fC. The obtained peaking time matches very well the design value of 25 ns.

Varying the amplitude of the calibration signal for the optimum value of delay, the linearity of the gain has been obtained. Figure 5 shows the gain linearity measured for one particular channel. The SCTA128HC chip has good linearity up to 12 fC which is sufficient for tracking applications.

The noise measurements have been performed for the full chip operating at the clock frequency of 40 MHz. The noise was measured by random reading of cells of the pipeline so the measured value includes cell-to-cell variations in the pipeline. Figure 7 shows results of the noise measurements obtained for different currents in the front-end transistor. The two groups of channels at the edges of the chip were connected to a 6 cm long strip detector with total strip capacitance about 9.5 pF while the inputs of the central part of the chip were left open. For the channels with open inputs one can notice dependence of noise on the base current in the input transistor. For the channels connected to strips the resulting noise is the sum of the parallel noise and the series noise which vary in opposite directions with the bias current of the input transistor. As a result the noise is almost constant over quite wide range of the input transistor current.

In figure 8 the mean values of noise for the open and the loaded channels are plotted as a function of the load capacitance, 0 and 9.5 pF respectively. For the bias current of 200 μA in the input transistor the obtained noise figure of ENC = 757 + 38 e/pF is in a good agreement with the results obtained for the previously developed SCT32A prototype [2].
5.2 Analogue pipeline performance

Since the SCTA128HC chip performs very simple voltage sampling where only analogue information is stored/retrieved from the pipeline the pedestal spread between ADB cells contributes as an additional noise source. By varying the delay between software reset (reset of the write/read pointer in the ADB) and the trigger sent to the chip it is possible to obtain the ADB pedestal map. Figure 9 shows the ADB pedestal map (128 cells × 128 channels) for one particular SCTA128HC chip. From the presented figure one can extract the cell-to-cell pedestal variation as well as variation of the DC offsets between channels.

The spread of the DC offsets between channels is in the range of 20 mV peak-to-peak while the spread of the pedestals along one channel of the ADB is in the range of 5 mV peak-to-peak. The distribution of the pedestals in one particular channel is shown in Fig. 10. The spread value of 1.2 mV rms has to be compared with the gain of 25 mV/fC which gives an additional contribution of 300 e\(^-\) rms to the noise generated in the front-end. For a low bias current in the input transistor and a low detector capacitance the additional contribution is about 10% of the overall noise at the output. For higher detector capacitances and respectively higher currents in the input transistor required for optimisation of noise this contribution becomes negligible.

6. CALIBRATION WITH \(\beta\) PARTICLES

In order to perform absolute calibration of gain and noise the chip was connected to a small 1×1 mm diode. The thickness of the diode was 300 \(\mu\)m and the capacitance was 1 pF. The response to \(\beta\)-particles from a \(^{109}\)Ru radioactive source was measured at the detector bias of 150 V. For each trigger event provided by a scintillator the delay with respect to the clock phase was measured by a TDC module. For the analysis presented below only the events from a 5 ns wide time window around the peak were taken. No signal clustering and no common mode subtraction algorithms have been employed in data analysis.

The distribution of the signal amplitude is shown in Fig. 11. By fitting this distribution to the Landau distribution one obtains the peak value of 89.7 mV which corresponds to the gain of 24.9 mV/fC (89.7 mV/3.6 fC). The above value of gain is in good agreement with the gain of 25.5 mV/fC as obtained from the electronic calibration (see Fig. 6). This result indicates that the parameters of the internal calibration circuitry, i.e. the calibration DAC and the test capacitors are close to the nominal designed values.
It must be mentioned that the most probable charge (peak of the Landau distribution) deposited by $^{106}$Ru $\beta$ particle here is assumed to be 22500 eh pairs. Other measurements indicate that the true value is around 20000 eh pairs, as expected from the energy of the $\beta$ particles being at the minimum of the ionisation curve. Final calibration which is in the progress, may increase therefore the value for the voltage gain by about 10%.

7. PERFORMANCE OF THE SCTA128HC CHIP WITH A STRIP DETECTOR

In order to demonstrate the performance of the SCTA128HC chip when used for the readout of a silicon strip detector a bench test was performed using $\beta$-particles from a $^{106}$Ru radioactive source. The chip was connected to a 6 cm long, 350$\mu$m thick p-type detector with the strip pitch of 25 $\mu$m. The readout pitch of 50 $\mu$m was used with one intermediate strip providing capacitive charge division. The total strip capacitance was about 9.5 pF. The detector was biased at 200 V. The input transistor was biased at 200 $\mu$A.

The histogrammed result of clustered signal/noise is shown in Fig.12. The Landau peak of the signal/noise is equal to 22.2. The measured common mode noise was about 1.3 mV RMS and contributed additional 5% to total noise of the system.

The cluster multiplicity is shown in figure 13. One can see that due to relatively narrow pitch and charge division structure in the detector majority of events result in 2-strip and 3-strip clusters. The mean signal is about 15% smaller compared to the value obtained from the small pad detector mostly due to charge loss on intermediate strips via their capacitance to the backplane.

In the readout logic of the SCT128HC chip a special feature has been implemented which allows for reading of up to 8 consecutive triggers. Using this feature we can see a snap shot of a single pulse along the channel of the ADB. Figure 14 shows a typical response to a single $\beta$-particle along the ADB cells. One bin corresponds to 25 ns.

Fig.12. Distribution of clustered signal/noise for $\beta$-particles measured with the strip detector.

Fig.13. Histogram of signal cluster width.

Fig.14. Snap shot of a single $\beta$ particle signal along the ADB cells. One bin corresponds to 25 ns.

One can see that all the signal is stored in a single 25 ns time slot. Small undershoot is visible as expected. The system can easily provide double pulse resolution of 50 ns as required.

8. CONCLUSIONS

A prototype readout chip with complete analogue architecture has been developed and manufactured in the DMILL technology. The architecture of the design and the implemented readout protocol make the chip compatible with the requirements for the readout electronics of silicon strip detectors in the LHC experiments. The noise and timing performance of the front-end circuit has the required performance for application in a LHC Si tracker.

REFERENCES


Development of a Radiation Tolerant 2.0 V standard cell library using a commercial deep submicron CMOS technology for the LHC experiments.

K. Kloukinas, F. Faccio, A. Marchioro, P. Moreira,
CERN/EP-MIC, CH1211, Geneve 23, Switzerland.

Abstract

A standard cell library was developed using a commercial 0.24 µm, 2.5 V CMOS technology. Radiation tolerant design techniques have been employed on the layout of the cells to achieve the total dose hardness levels required by LHC experiments. The library consists of digital core cell elements as well as a number of I/O pad cells. Additionally, it includes a pair of differential driver and receiver pads implementing the LVDS standard. The library cells have been fully characterised and the necessary descriptions to facilitate simulation have also been generated. The presented library features 5 times increase in speed accompanied by 26 times reduction in power consumption as well as an increase of 8 times in gate densities when compared to a currently available 0.8 µm CMOS technology. To prove the concept and to evaluate the radiation tolerance of the cells, a few demonstration circuits were implemented. The results of the radiation hardness tests are being reported.

1. INTRODUCTION

The collisions of TeV protons in the planned LHC collider at CERN will create a severe radiation environment inside the experimental equipment affecting the detector electronics [1]. For CMOS technologies the predominant damaging phenomena are threshold voltage shifts, transconductance and noise degradation and creation of leakage paths. Transient ionizing radiation effects like Single Event Upsets (SEU) and Single Event Latchup (SEL) are also of great concern.

With the use of thin gate oxides in deep submicron CMOS technologies the threshold voltage and the transconductance of the transistors are becoming less sensitive to radiation. Gate oxides with thickness in the order of 5 nm for gate lengths of about 0.24 µm become insensitive to charge trapping and interface state generation [2], [3]. The oxide trapped charge is roughly proportional to $\text{Tox}^2$ in this oxide thickness range, and its contribution to the total ionizing dose degradation becomes less important with advancing technology [4].

The hole trapping in lateral and field oxides, which are typically thick, is left as the main failure mechanism in submicron commercial technologies [5]. By introducing special layout techniques that aim to block all possible leakage paths that can be turned on due to the radiation these advanced technologies can become immune to irradiation.

The design of digital circuits of a significant size and complexity relies on the existence of a digital standard cell library and powerful CAE tools. This study presents the work that has been performed in order to implement a radiation tolerant digital standard cell library on a commercial deep submicron CMOS technology. Radiation tolerant design techniques have been employed on the layout of the cells.

2. RADIATION TOLERANT LIBRARY

2.1 Description of the Technology

We have chosen to implement the digital library cells on a commercial 0.24μm, 2.5V CMOS technology. Irradiation tests have been performed on this technology have demonstrated the hardness of the thin gate oxide [6]. The basic features of the selected technology are given in Table 1.

<table>
<thead>
<tr>
<th>Table 1: Technology features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Lithography:</td>
</tr>
<tr>
<td>Leff:</td>
</tr>
<tr>
<td>VDD:</td>
</tr>
<tr>
<td>Gate Oxide Thickness:</td>
</tr>
<tr>
<td>Process:</td>
</tr>
<tr>
<td>Device Isolation:</td>
</tr>
<tr>
<td>Ti salicidation:</td>
</tr>
<tr>
<td>Interconnectivity:</td>
</tr>
</tbody>
</table>

2.2 Radiation Tolerant Layout Techniques

Certain layout techniques have been proposed in order to increase the radiation tolerance of deep submicron technologies [6]. These techniques involve:

- the use of "edgeless" or "enclosed" NMOS transistors that prevent the leakage current along the edges of the devices (edge leakage is eliminated since only thin oxide interfaces between source and drain) and
- the extended use of guardrings that isolate all n+ diffusions that are at different potentials.

Figure 1 shows the use of these techniques in the layout design of an inverter and a 2-input NOR. The PMOS devices are as well drawn using the enclosed
geometry. The enclosed PMOS devices occupy less area and at the same time offer smaller drain capacitance than the conventionally drawn devices. There is no significant role of the enclosed PMOS in the radiation tolerance of the cell.

shown in subsection 2.6 the area penalty is mitigated by the small feature size of the technology.

2.4 Library Contents

A set of digital standard cells consisting of core logic as well as I/O pads have been prepared and included in the library. In order to ease the library maintenance we decided to implement only a minimum set of cells that will enable the digital designing. The list of the standard cells that has been included in the presented library is shown in Table 2.

Table 2: List of digital library standard cells

<table>
<thead>
<tr>
<th>Core Logic</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter 1X Drive</td>
<td>Buffer X4 Drive</td>
</tr>
<tr>
<td>Inverter 2X Drive</td>
<td>Buffer X8 Drive</td>
</tr>
<tr>
<td>Inverter 3X Drive</td>
<td>NOR</td>
</tr>
<tr>
<td>Inverter 4X Drive</td>
<td>XNOR</td>
</tr>
<tr>
<td>2 Input NAND</td>
<td>2 Input NOR</td>
</tr>
<tr>
<td>3 Input NAND</td>
<td>2 Input NOR</td>
</tr>
<tr>
<td>4 Input NAND</td>
<td>2 Input NOR</td>
</tr>
<tr>
<td>2-Wide 2-In AND-OR</td>
<td>2-Wide 2-In OR-AND</td>
</tr>
<tr>
<td>2-Wide 3-In AND-OR</td>
<td>2-Wide 2-In OR-AND</td>
</tr>
<tr>
<td>3-Wide 2-In AND-OR</td>
<td>2-Wide 2-In OR-AND</td>
</tr>
<tr>
<td>Static D-F/F</td>
<td>Static D-F/F, Set</td>
</tr>
<tr>
<td>Static D-F/F, Reset</td>
<td>Static D-F/F, Set, Reset</td>
</tr>
<tr>
<td>Dynamic TSPC D-F/F</td>
<td>Static D-F/F, Scan</td>
</tr>
<tr>
<td>2-Input MUX</td>
<td>4-Input MUX</td>
</tr>
<tr>
<td>4-Bit Register, Clear</td>
<td>1-bit Adder</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input pad, CMOS</td>
<td></td>
</tr>
<tr>
<td>Output, 8 mA drive</td>
<td>Output, 8 mA, slew rate</td>
</tr>
<tr>
<td>Output, 16 mA drive</td>
<td>Output, 16 mA, slew rate</td>
</tr>
<tr>
<td>Output, 20 mA drive</td>
<td>Output, 20 mA, slew rate</td>
</tr>
<tr>
<td>LVDS driver</td>
<td>LVDS receiver</td>
</tr>
</tbody>
</table>

The combinatorial core logic consists of simple gates like inverters and buffers with different driving capability, as well as NANDs, NORs and XNOR gates. More complex gates like AND-ORs, OR-ANDs and multiplexers have also been included.

Latches and flip/flops are the basic building blocks of sequential digital circuits and, to large extent, determine circuit speed and power dissipation. A static master/slave pseudostatic D-type Flip/Flop (D-F/F) has been included in the core logic of the presented library. A few other D-F/F cells based on this design that offer RESET, SET, and combined RESET-SET capabilities have also been included. A static 4-bit register with clear capability and a 1-bit adder have been included as well.

A dynamic True Single Phase Clock D-type Flip/Flop (TSPC D-F/F) has been designed according to the

![Figure 1. Layout patterns of a) a minimum size inverter and b) a 2-input NOR gate, as implemented in the Radiation Tolerant library.](image)

![Figure 2. Cell layout style.](image)
architecture proposed in [7] and included in the library. It requires only one clock signal and is positive edge triggered. This circuit is often the choice in pipelined datapaths and register files for signal processing circuits offering reduced power dissipation and less layout area when compared with the static D-F/F. Figure 3 and Figure 4 presents the layout of both the static and the dynamic D-F/F for comparison.

![Figure 3. Layout pattern of the static D-F/F.](image1)

![Figure 4. Layout pattern of the dynamic D-F/F.](image2)

A small set of I/O pads is included in the library. All pads offer ESD protection. Radiation Tolerant layout techniques have been also applied in the design of the ESD protection circuits. There are three types of output pads with different driving capability. Each type has a standard version and a version with a skew rate control output.

A set of "glue cells" have been developed to ease the design and enable the automated place & routing. These cells are: "cap cells" that closes the guardrings at both ends of the cell rows, corner cells for the chip power rings, power feedthrough cells etc.

2.5 CAE Tools

The availability of appropriate models, correct extraction rules and, in general powerful CAE tools to handle the deep submicron technologies, is a key issue in modern chip design. Special physical design verification rules have been added to check for inconsistencies in radiation tolerant designing (openings in the guardrings around n' diffusions etc). Special device extraction routines have been inserted in the extraction rules file that enable a more precise extraction of the size (W/L) of the enclosed geometry transistors. The library technology file has been set up with the necessary rules to allow generation of cell abstracts for the automated place & route.

Timing parameter extraction using SPICE simulations has been performed on the cells and models that enable the digital simulation have been developed.

2.6 Performance Characteristics

The gate delay of an inverter in the presented library is estimated from SPICE simulations to be 50 ps at 2.0 V (F.O.=1). This gives an improvement in speed of about 5 times when compared to a currently available 0.8 μm technology.

The estimated power consumption in the presented library is estimated to be 0.15 μW/MHz/gate (F.O.=1), which is 26 times lower than what is achieved in a 0.8 μm technology.

In order to reduce further the power consumption, as the intrinsic speed of the technology is high, we propose to use the library cells at 2.0 V rather than 2.5V, which is the nominal operating voltage of the technology.

Table 3 shows the estimated propagation delay (Tpd) and the associated power dissipation of a simple inverter (F.O.=1) cell at 2.5 V and 2.0 V. The speed of the technology even after a reduction of 25% will still overwhelm the requirements for the circuit operation in the LHC environment. At the same time the power dissipation is almost halved relaxing the power budget constrains for the detectors front-end electronics. All the cells in the presented library have being characterised at a typical operating voltage of 2.0 V.

<table>
<thead>
<tr>
<th></th>
<th>2.5 V</th>
<th>2.0 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tpd</td>
<td>36 ps</td>
<td>48 ps</td>
</tr>
<tr>
<td>Power</td>
<td>0.24 μW/MHz</td>
<td>0.14 μW/MHz</td>
</tr>
<tr>
<td></td>
<td>-25 %</td>
<td>-42 %</td>
</tr>
</tbody>
</table>

The penalty that the radiation tolerant techniques introduce in the library cells is estimated to be about 70%. For comparison a sample of a few digital cells were drawn, on the selected deep submicron technology, using standard and radiation tolerant layout techniques. The area of the layout of each cell as well as the associated penalty in the area can be seen on Table 4. The comparison shows also that more complex cells exhibit higher area penalty.

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>Rad-Tol</th>
<th>Penalty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>33.6 μm²</td>
<td>50.9 μm²</td>
<td>34 %</td>
</tr>
<tr>
<td>2-in NAND</td>
<td>46.0 μm²</td>
<td>119.0 μm²</td>
<td>61 %</td>
</tr>
<tr>
<td>2-in NOR</td>
<td>47.8 μm²</td>
<td>80.0 μm²</td>
<td>41 %</td>
</tr>
<tr>
<td>Static D-F/F</td>
<td>153.0 μm²</td>
<td>533.1 μm²</td>
<td>71 %</td>
</tr>
<tr>
<td>Static D-F/F SR</td>
<td>188.1 μm²</td>
<td>572.0 μm²</td>
<td>75 %</td>
</tr>
</tbody>
</table>
Despite the area overhead, the gate density offered by the presented library is still 8 times higher when compared to a 0.8 µm standard cell technology. Figure 5 shows the layout of a ring oscillator consisting of 1,280 minimum size inverter cells drawn on a 0.8 µm standard cell technology and on the 0.24 µm technology using the radiation tolerant standard cell library. Both designs were routed using 2 metal layers. The design in the 0.24 µm technology was found to be 7.9 times smaller than the one in 0.8 µm. The fact that the presented library features up to 5 levels of metal for wiring purposes, presents an advantage for the high density designs.

3. DEMONSTRATOR CHIP

3.1 Test Chip

In order to evaluate the radiation tolerance of some of the designed standard cells as well as to demonstrate the functionality of the developed design kit we have designed a few digital circuits that were fabricated on the referring technology. The circuits were:

- a Ring Oscillator consisting of 1000+1 minimum size inverters,
- a Static Shift Register consisting of 2,048 static D-F/F cells,
- a Dynamic Shift Register consisting of 1,024 TSPC D-F/F cells,
- an SEU Tolerant Static Shift Register consisting of 2,048 specially designed D-F/F cells and
- a pair of LVDS receiver and driver.

Figure 6 shows part of the layout of the submitted chip presenting the layout design of the static and the dynamic shift registers.

All the implemented circuits were tested and found to be functional.

3.2 LVDS receiver and driver

The receiver was designed to operate at a nominal power supply of 2.0 V, however, it was possible to operate it successfully at power supply voltages between 1.5 V and 2.5 V. Since the allowed common mode range for an LVDS signal in the input of an LVDS receiver is 0.2 V to 2.2 V and the receiver was designed for a 2.0 V nominal power supply, its input stage was designed as a true rail-to-rail amplifier. The tests showed that the receiver can be operated with common mode voltages between 0 V and the power supply voltage. Tests were carried out for frequencies up to 120 MHz. The receiver displays a nominal delay of 830 ps for an input
differential signal of 300 mV amplitude. Figure 7 shows an eye diagram measurement of the receiver.

The LVDS driver was also tested but it was verified that, due to a "missing connection", only one of the differential outputs was operational. This prevented further testing and qualification of the driver and required the use of a commercial LVDS driver to test the receiver. The "missing connection" was due to an inconsistency in the technology file used to verify the circuit before fabrication. This verification problem has now been identified and corrected.

![Eye Diagram of the LVDS Receiver](image-url)

**Figure 7.** Eye diagram of the LVDS receiver.

### 4. RADIATION HARDNESS TESTS

Hereafter we present the results of total dose irradiation tests performed on the ring oscillator and the LVDS receiver. Results of total dose irradiation tests performed on the three shift registers are presented separately [8]. The three shift registers were also studied for Single Event Upset (SEU) and Single Event Latchup (SEL) effects. The results of these studies are also presented in [8].

#### 4.1 Ring Oscillator

For the total dose irradiation tests on the ring oscillator we have used a 10 KeV X-ray machine. The dose rate was 29 Krad/min. The irradiation was performed at room temperature having the circuits under bias at 2.0 V. A step irradiation was performed at 1, 3, 5, 10 and 30 Mrad. The operation frequency and the power consumption of the ring oscillator were measured at every irradiation step. After the total dose of 30 Mrad the device under test was left for 24 hours under bias at room temperature for annealing and then another set of measurements was performed. After the 24 hours annealing period the device was kept under bias for a weak in an oven at 100°C and measured again. This procedure complies with the ESA qualification procedure described in [9].

Figure 10 shows the measured power delay product (Pw) of the inverter as a function of the power supply voltage (VDD). The Pw before irradiation and at 2.0 V was found to be 0.15 µW/MHz which is in very good agreement with the estimated value from SPICE simulations. The stability of the power delay product curve indicates that there is no increase in the leakage currents associated with the total dose radiation. This result demonstrates the effectiveness of the radiation tolerant layout techniques.

![Inverter Propagation Delay](image-url)

**Figure 8.** Inverter propagation delay (Tpd) as a function of the power supply voltage (VDD) at different irradiation levels.
delay (Tpd) at different irradiation levels. The LVDS receiver showed no observable degradation under bias and supply voltage. The irradiation levels of 16.2 Krad/min. The irradiation steps: one up to a total dose of 1 Mrad and the other up to 10 Mrad. In both cases the receiver was tested after irradiation with the performance showing no observable degradation after the 1 and the 10 Mrad irradiation steps.

**5. FURTHER WORK**

To fully utilise the presented digital standard cell library a proper interface with a logic synthesis CAE tool is necessary.

Interconnect width and spacing are also scaled down with device scaling making the 3D fringing fields significant in the multi-level interconnect capacitances. A tool that will be able to extract interconnect parameters (RC) accurately is of great importance. Especially for full chip global critical paths, the interconnect modelling has to be accurate. Conventional parameter extraction tools from commercial vendors use 2D approximation for 3D capacitances. 3D fringing fields are significant in the multi-level interconnect capacitances.

Another fabrication test run will be required in order to extract the timing parameters for the designed digital cells from measurements leading to more precise timing models.

**6. CONCLUSIONS**

We have developed a radiation tolerant 2.0 V standard cell library using a commercial 0.24 µm CMOS technology. The selected technology was found to be natively radiation resistant mainly due to the utilisation of thin gate oxide and possibly by the utilisation of STI between the devices. With the introduction of special layout techniques in the cell design we have increased further its radiation resistance leading to total dose radiation levels which are compatible with LHC design requirements.

Moreover, the use of an advanced deep submicron technology presents many advantages in terms of speed power and area utilisation over currently available technologies.

We have shown that despite the area overhead implied by the radiation tolerant layout techniques, the presented library is still superior in gate density of about 8 times when compared to a 0.8 µm technology.

We have developed a design kit to support the standard cell library that offers digital simulation capabilities as well as layout extraction and verification. The functionality of the design kit was tested and demonstrated with the implementation of a number of digital circuits in a test chip. The circuits consisted of a ring oscillator, a static shift register, a dynamic shift register and a novel design of a static shift register that features reduced rate of single event upsets. The test chip was fabricated and the circuits were tested and found to be fully operational.

The radiation performance of the standard cell library has been demonstrated with the submission of the ring oscillator in total dose irradiation tests. Only 5.2 % degradation in speed was measured after 30 Mrad of total dose, while there has not been any leakage current turn-on.

Differential signalling transmission will find its use in clock distribution on the detectors front-end electronics, where good timing information, low power and low noise emission is of concern. The availability of a pair of differential I/O pads that follows the LVDS signalling standard is of an advantage for the presented library. We have demonstrated the functionality of the differential receiver pad. The tests showed that the receiver is able to operate with a common mode from rail-to-rail (0.0 V to 2.0 V) at maximum frequency of 120 MHz.

**7. REFERENCES**

2. A. Acovic et al. “Effects of X-ray irradiation on channel current and GIDL in N- and P- channel
Mosfets in ultra-thin gate oxide 0.25μm CMOS technology", in Proceedings of the MCNC Workshop on Radiation and Process Induced Defects, 1991.


LOW POWER BiCMOS CHARGE AMPLIFIER
WITH CURRENT CONVEYOR FEEDBACKS

G. Bertuccio, M. Chisari, L. Fasoli, P. Gallina and M. Sampietro,
Politecnico di Milano, Dipartimento di Elettronica, P.zza L. da Vinci 32, 20133 Milano, Italy
(email: bertucci@elet.polimi.it and sampietr@elet.polimi.it)

Abstract

Based on a minimum noise approach, a low-power preamplifier and shaper circuit fulfilling LHC requirements is presented. The circuit, integrated in BiCMOS technology and intended to cope with a diamond microstrip detector of about 5 pF capacitance, uses a bipolar transistor input stage to obtain a noise level of about 650 electrons r.m.s. with a peaking time of the output signal of 20 ns. The circuit is powered with single supply at 1.6 V with a total power consumption of 310 pW/ch. The DC feedback and reset of the preamplifier and the shaper architecture are performed by current conveyors that minimize power dissipation because of a current re-use design.

1. INTRODUCTION

In this paper we present original circuit solutions for preamplifying and shaping, demonstrated by experimental results obtained from test chips manufactured by AMS in BiCMOS technology. The presented front-end has the following characteristics:

- single power supply
- low bias voltage operation at 1.6 V
- low power consumption of 0.3 mW/ch
- peaking time of 20 ns
- fast return to zero of about 60 ns
- immunity to variation of detector leakage current

Although the circuit design is flexible and can easily be adapted to various detectors and experimental conditions, we have designed it for a 5 pF detector capacitance, as it is the case in microstrip diamond detectors.

2. THE PREAMPLIFIER

2.1 Current conveyor feedback

A schematic of the charge preamplifier section is shown in Fig. 1. It is made of a cascode input stage, an active load and an emitter follower. The feedback path for the signal is provided by the feedback capacitance C_f. The collector current of the follower, proportional to the output voltage through the resistance R, is reduced by a factor γ (in our realisation γ=50) and mirrored to the input node by a MOSFET stage (M5, M6). This novel configuration provides an equivalent feedback resistance of R_f = R/γ so to give a fixed time constant discharge of the feedback capacitance [1, 2]. This configuration also provides the DC base current to the input BJT and a feedback stabilisation of the circuit working point. Thanks to the 100% re-use of the current from the output follower, already available in the circuit, this current conveyor feedback is intrinsically a zero-power added solution. The power consumed by the preamplifier is therefore mainly due to the input BJT collector current, which is rigorously set by noise and bandwidth considerations [3]. In our case, the choice of a peaking time of 20 ns has given an optimum collector current of 90 μA.

The presented current conveyor feedback is based on the same principle already employed in other amplifiers [4] [5], but in our case with an evident much more compact and simple design, with the conveyor practically integrated in the preamplifier circuit itself.

Figure 1 - Schematic of the charge amplifier. The current conveyor feedback is performed by the transistors M5 and M6. The output to the following stage is the current in M7.
2.2 Cold feedback resistance

The noise of the resistance $R$, of relatively low value ($R=1 \, \text{k} \Omega$ in our realisation) and therefore easy to be obtained in integrated technology, is dumped by a factor $\gamma^2$ in its spectral power density and is therefore lower by a factor $\gamma$ with respect to the noise of a feedback resistor of value $R_f=R\gamma$. In addition, the noise added by the MOSFET connected to the input node can be made very small with respect to the shot noise of the base current of the input BJT by properly choosing its W/L factor. In our realisation, this active feedback have a current noise equivalent to a 350 k$\Omega$ resistor by occupying the area of only a 1 k$\Omega$ resistor plus two MOSFET’s.

2.3 First shaping stage within the preamplifier

The key point of having an active feedback resistance, with a much lower noise than a resistor of equal value, is that the feedback capacitance discharge time constant can be chosen to directly produce one of the poles for the pulse shaping. This eliminates the need of a pole-zero cancellation circuit in the following stages of the shaper, with advantages in term of simplicity and stability of the entire amplifying circuit.

Finally, note that the output signal is made available to the following stages as a current signal at M7, with advantages in terms of reducing the noise contribution of the following stages.

3. THE SHAPER

3.1 Active resistor pole

In addition to the first shaping pole already included in the preamplifier, a second pole is obtained by the stage indicated in Fig. 2. This stage is a current amplifier with a bandwidth defined by a pole made with an active resistor. The current pulse, made available from the preamplifier through M7, is integrated on the capacitor C1. The capacitance is connected to a feedback structure (M8-M11) whose effect is to present at the input node $A$ a resistance equivalent to $(1/g_mBf+R_1)\cdot \alpha$, where $\alpha$ is the multiplication factor of the two current mirror stages M8-M9 and M10-M11. In our case $R_f=2 \, \text{k} \Omega$, $C_1=0.3$ $\text{pF}$ and $\alpha=10$ in order to give a time constant of $\tau=10$ ns. This solution allows for the setting of the desired time constant with a minimum area occupation. In our case, for example, the proposed solution should be compared with a resistor of about 30 k$\Omega$.

3.2 Current amplification architecture

The use of MOSFET’s only in current mirror configurations makes the circuit almost insensitive to variations of their threshold voltage, therefore stabilising DC bias, gain and time constant. The mirror architecture makes also available the output signal as a current pulse to drive the following stage. This can be either another shaping stage equal to the previous one (if one wants to introduce one more pole to the overall transfer function, in order to obtain a more symmetrical output pulse) or a final current comparator to detect signal overcoming a given threshold. A current comparator adapted to our circuit and with variable threshold has been designed and is presently under fabrication.

4. EXPERIMENTAL RESULTS

The preamplifier and shaper have been produced in 0.8 $\mu$m BiCMOS technology at AMS [6]. Figure 3 shows the experimental voltage pulse at the output of the shaper loaded with $R_2=30$ k$\Omega$ and $C_2=0.3$ $\text{pF}$. The figure refers to an input charge of 25000 electrons. The pulse has a peaking time of 20 ns and a fast return to zero within about 60 ns, in agreement with the design of the 3...
poles circuit. The pulse is strictly unipolar thanks to the DC coupling of the circuit stages. The dissipated power of a single channel is 310 μW.

Figure 4 reports the output pulses for increasing values of the input charge, showing a output swing of at least 240 mV. This value is imposed by the limited voltage excursion of the gain node of the preamplifier due to the low value (only 1.6 V) of voltage supply. This voltage is the only one required to power the whole circuit. The current source in the preamplifier is obtained using a PTAT (Proportional to Absolute Temperature) circuit, also shown in Fig. 2, which can bias a large number of channels, with a negligible power consumption per channel of less than 10 μW/ch.

The chip is under test for noise measurements. The expected value of Equivalent Noise Charge is about 650 electrons r.m.s. with 5 pF input capacitance.

5. ADDITIONAL REMARKS

The presented circuit is almost insensitive to detector leakage current variations since these are summed to the base current of the bipolar input transistor (about 1 μA); a detector leakage current variation from 0 nA to 100 nA would produce an output level shift of only 10%.

Although not directly addressed in our first prototype, the circuit has good potentials in term of radiation tolerance. This is not only due to its compactness and limited number of transistor used, but also to the choice, whenever possible, of p-MOSFET’s, that are more insensitive to radiation in term of both DC characteristics and noise. The n-MOSFET in the preamplifier can be easily replaced by a npn-BJT, with the only drawback of requiring an additional reference voltage for its base; concerning the n-MOSFET’s in the shaper, they can be made radiation tolerant by choosing enclosed designs and guard structures [7].

6. ACKNOWLEDGEMENTS

This work has been supported by Italian INFN (Istituto Nazionale di Fisica Nucleare) and CNR (Consiglio Nazionale delle Ricerche).

7. REFERENCES

[6] Austria Mikro Systeme International AG, Unterpremstatten, Austria
MCM PRODUCTION: TESTING AND RELATED ASPECTS

R. Mariani, S. Motto, S. Giovannetti, CAEN Microelettronica, Viareggio, Italy
email: r.mariani@caen.it

Abstract

A careful strategy must be planned to bring complex multi-chip systems, as multi-chip modules (MCMs), into production. The different production and testing strategies must be characterized in term of parameters like production yield, Know-Good Dies (KGD) quality and Early Failure Rate. In any case, MCM yield depends strongly on the goodness of its individual components, i.e. on the Fault Coverage (FC). In this paper the production strategy and the testability activity adopted for the FERMI microsystem is presented. It is also shown as the intensive use of Design-for-Testability (DfT) methodologies, both at the chip and at the system level, is fundamental to achieve high production yield of dense multi-chip modules.

1. INTRODUCTION

The quest for higher integration levels in systems and competitive pressures to reduce system manufacturing costs make the Multi Chip Modules (MCMs) always more appealing in today's applications. A MCM is an electronic system or subsystem with two or more bare integrated circuits (bare die) or Chip Sized Packages (CSP) placed very close to each other and electrically connected to a common substrate with very dense lines (up to 10-25 µm spacing) [1]. The substrate provides mechanical support and interconnections: it is composed of multilayer conductors separated by suitable insulating dielectric material and vias connect different layers; wiring densities cover up to 90% of substrate, while in conventional boards it rarely exceeds 10%. The metatization technology can be either thick film (additive stacking on ceramic substrates of dielectric and conductive layers; the metallization is formed by deposition, drying and firing) either thin film (subtractive method; the metallization is formed by sputtering and selective phototetching) having a better stability and noise characteristics [1].

Three basic technologies are available for microwiring substrates:

1) MCM_L (Laminated). Essentially an advanced form of PCB technology with copper conductors on laminated base dielectric. The MCM_L is not always the best solution for every application. Especially with respect to long term reliability and wide temperature ranges MCM_L technology has a smaller application range than MCM_C and MCM_D technologies. MCM_L are less expensive than MCM_C and MCM_D.

2) MCM_C (Ceramic). There are two different processes in MCM_C categories: several conductive layers deposited on a ceramic substrate and embedded in glass layers or several conductive and ceramic layers cofired at high (HTCC) or low (LTCC) temperature. The minimum line to line pitch is about 150 µm, the minimum line width about 75 µm, the conductor thickness about 8 µm and the dielectric thickness about 40 µm.

3) MCM_D (Deposited). The technology is also known as Thin Film Technology: the interconnections are realized by thin film deposition of metals on deposited dielectrics, which may be organic polymers or inorganic dielectrics. The minimum line to line pitch is about 50 µm, the minimum line width about 10 µm, the dielectric thickness ranges between 3-15 µm and the via diameter ranges between 10-50 µm. The main advantages of the MCM_D are the very high wiring density, the improved thermal management (up to 10 W) and a higher mechanical stability with reference to MCM_L and MCM_C; on the other hand the cost of MCM_D is certainly higher than MCM_L and MCM_C.

The use of MCMs leads to performance enhancement and cost benefits at system level. The reduction of the average interconnection length between components causes a reduction in the line impedance and the shorter chip-to-chip interconnections and bare die allows increased operational frequencies, a reduction of the power need to drive line capacitances, a higher signal to noise ratio, a lower cross-talk and an overall reduction of decoupling capacitors, resistors and drivers [IBM source].

The cost saving at system level is mainly allowed by the increased assembly process yield for MCM (1 PPM vs 100 PPM for SMT version per solder joint measured at test [IBM source]), a thermal management enhancement and a reduced board complexity. On the other hand the development of MCMs is much more complex than the development of a PCB; the design has to start with a detailed specification including function, environmental and mechanical specifications, partitioning of the electric functions into standard circuits or ASICs and especially with a test strategy that has to be taken into account since the early stage of the project [2]. To produce high-quality and cost-effective MCMs, test and fault diagnosis has to be included as critical requirements early in the design cycle; treating test as an afterthought in this process may result in high costs. But if incorporating test and fault diagnosis as critical design requirements is necessary to achieve high-quality, high-reliability and cost-effective multichip systems, it takes considerably study to evaluate where and when to test and to decide upon the best test method and level; in fact it is necessary to determine a trade off between cheap test solutions with inferior quality and high quality with effective and highly expensive test solutions.
2. MCM production flow and related aspects

In the figure 1 a complete production flow for MCM is shown: the component and substrate production is done in parallel (left and right branches) and then the MCM is assembled (central branch).

![MCM Production Flow Diagram](image)

Fig. 1: MCM production flow

Every step of the production flow has to be carefully planned to obtain high-quality and cost-effective MCMs, the cost and the resultant quality of an MCM depending mainly upon [3]:
- the yield of the chips;
- the number of chips in the module: a careful partition of the system should be planned at the very beginning of the project and the discussion should involve engineers expert in system design, circuit design, layout, manufacturing, assembly, test and quality;
- the yield of the interconnection structure;
- the yield of the bonding and assembly processes;
- the effectiveness of the testing and rework process in detecting, isolating and repairing those defects: this aspect is also very closely related to the level of testability of the components assembled on the substrate.

If various chip types (1,2,...,n) are used within a module, then the first pass MCM yield can be expressed as it follows:

\[ Y_{mcm} = (y_1)^A \cdot (y_2)^B \cdot \ldots \cdot (y_n)^N \cdot Y_S \cdot Y_A \]

where: \( Y_{mcm} \): first pass MCM yield; \( y_1, y_2, \ldots, y_n \): yield of chips 1,2,...,n (probability of chip 1,2,...,n being good); A,B,...,N: number of chips of each type 1,2,...,n respectively; \( Y_S \): Known-Good probability of substrate; \( Y_I \): Known-Good probability of die interconnects; Q: number of interconnects; \( Y_A \): yield of bonding and assembly.

Chip yield plays a very important role: for example (figure 2) a 8-chip MCM with a 95% chips yield results in a 65% first pass MCM yield without considering any other source of yield loss. This means that 35% of the assembled MCMs must be diagnosed and repaired, a costly and time-consuming task. The chip yield of bare chips must be pushed to nearly 100% to produce a module yield high enough to have cost-effective MCM process.

![Chip Yield vs MCM Yield](image)

Fig. 2: Chip Yield vs MCM Yield; \( n \) is chip number housed on the MCM

3. Chip yield: Fault Coverage (FC) and Design for Testability (DfT)

As underlined in the previous paragraph, high quality bare dies are needed to produce cost-effective MCMs; a high chip yield is achieved during wafer manufacturing, through process control-based approaches, and after manufacturing with bare die test and Burn-In to make the weak dies fail (infant mortality), increasing the confidence that each device is reliable and will continue to function for an extended period of time [1].

Provided a test pattern for the bare die test, the Fault Coverage (FC) is defined as the ratio between the faults detected by the given test pattern and the possible faults of the device under test and it plays a very important role in determining the quality of the bare die test therefore the chip yield; defining the Defect Level (DL) as the percentage of chips of the same type shipped which passed the test, but may be faulty (DL=1-y_n with the notations used also in the previous paragraph), the following formula relates the Defect Level DL to the process yield \( Y_p \) and to the Fault Coverage FC [4]:

\[ DL = 1 - Y_p^{1-FC} \]

The Fault Coverage FC depends on the goodness of the generated test patterns and on the use of DfT (Design for Testability) structures implemented on the device under test: a chip yield of 99% (a DL of 1%) and a process yield \( Y_p \) of 80% results in a FC of 98% (figure 3).

An approach to alleviating the need of sophisticated testers at all levels of integration is to incorporate the tester into the circuit under test itself; hence the notion of DfT and Built-In-Self-Test (BIST). These approaches (often called On-chip ATE, Automatic Test Equipment) eliminate the need for expensive testers an provide a mechanism for accessing and exercising internal design circuitry [3]. In the following sections, these approaches are briefly described and applied to the design of the MCM-V3.
4. Design for Testability in the design flow

As mentioned in the previous section, the yield of the components mounted on the MCM must be pushed to 100% in order to reach a cost effective MCM. Therefore, the standard design flow must be changed to insert some steps aimed to improve the component testability (what is usually called Design For Testability).

The figure 4 shows how the standard CAEN MicroElectronica design flow (left side) has been integrated with a typical testability flow (right side). Proper CAE tools (fault analyzers) implement the “Testability Analysis”: a detailed map of the circuit in terms of Controllability and Observability (CO) values is computed, with different fault models (Single-Stuck At, Bridging Fault, IDDQ, etc...). Using these data and CAE tools (test synthesizers), scan logic (and Boundary Scan) can be inserted into the circuit to increase the CO values. Then Fault simulators and Automatic Test Pattern Generators (ATPG) are used to automatically generate the test patterns with the desired coverage. It is worth noticing that very often (especially with complex circuits), the tools are not able to reach high coverage; in these cases DFT rules must be used since the beginning of the design (at the HDL level) and “ad hoc” test structures must be inserted.

In very complex design using Deep-Sub-Micron (DSM) technologies, many parts of the chip are built using automatic tools (synthesizers) that often introduce redundancies and untestable nodes, therefore the use of testability CAE tools is more and more needed. On the other hand to use these tools in a smart and useful way means to educate design engineers on test related issues.

The use of TestGen (Synopsys), ex-Sunrise, one of the most powerful testability CAE tools currently available on the market, has allowed CAEN Microeletronica to considerably enhance the time-to-market and the quality of the shipped components.

Several methods exist to improve the circuit testability [5] and some of the most commonly used are listed below:

- Structured techniques, as Scan logic: A sequential circuit can be symbolized with a set of combinatorial circuits divided by flip-flops. This type of circuit is clearly difficult to be tested. For example it’s difficult to insert a value in the last flip-flop or to observe a value of the first combinatorial circuit. With the insertion of the scan logic, it becomes easy for the ATPG program to insert the value in each flip-flop (FF) during an initial phase in which all the FF are serially loaded, and then is easy to read the result during a final phase in which all the FF are read by a serial shift. There are many kinds of scan techniques: Level Sensitive Scan Design (LSSD), Full Serial Scan, Partial Scan and Parallel Scan.
- Ad Hoc techniques, for example to reduce the number of Un testable faults. Un testable faults are faults that cannot be tested by the ATPG. This type of fault is found when a redundant part exists in the circuit. Another example of this fault is the case in which some nodes are tied to GND or VDD. They have to be removed redoing the design or using “ad hoc” testing structures: partitioning large sequential circuits, adding extra tests points, adding multiplexers.
- BIST (Built-In Self Test). Ad hoc blocks are inserted in the circuits to allow self-checking operations proving correct functionality, in general at-speed. There are many kinds of BIST: signature analysis and BILBO (Built-In Logic Block Observation), memory self-test.
- IDDQ testing, i.e. the monitoring of VDD supply current quiescent, mainly used to test bridging faults.
- Boundary Scan.

It is worth noticing that DfT and BIST are not free; they require an investment in chip area and in certain cases may themselves cause additional delays. These techniques will be briefly described in the following section applied to one of the MCM-V3 ASICS, and it will be shown as DfT structures can be employed without significant area and speed overhead if properly managed by the designer.

5. Application: MCM-V3

A MCM (MCM-V3) containing 14 bare dies flip-chipped on a MCM_D substrate (figure 5) was realized by FERMI collaboration [6]. Five complete channels are implemented: at the input of the MCM, non-linear data are applied to a linearising stage built around an adder for
offset correction and a multiplier for gain adjustment. The lineariser also includes a RAM that can be used as a Look-Up Table (LUT) and as a test pattern input for testing. The linearised data of the five channels are added and filtered in the level 1 filter ASIC, which will be described in the following paragraph. The lineariser data are stored in a pipeline during the level-1 trigger loop latency and is then, in case of a positive decision of the level-1 trigger, written into an event buffer. The readout filter (filter 2) contains three parallel Finite Impulse Response (FIR) filters and a non-linear order statistics operator; it can process one single channel at the time, and it offers a greater suppression of different artifacts, as timing jitter, in the input data stream, than a single FIR.

![Fig. 5 : MCM-V3 structure](image)

A well-detailed test strategy was planned before and during the design phase: a top-down strategy was adopted to specify the testability requirements at board level, MCM level and components level. The next section will introduce the activity and results carried out in the design of the LVL1 filter device, highlighting the concepts described in the sections 3 and 4.

6. Application: Testability of the LVL1

The Level 1 trigger filter chip (LVL1) [7] operates at the sample rate (40 MHz) on the sum of five channels and performs three different operations: identification of the event time, measurement of the pulse amplitude and identification and flagging of overlapping pulses. LVL1 consists of two parallel FIR filters: the energy filter shapes the input data to measure the amplitude, and the timing filter shapes the data to identify the time of the pulse event. A three-point maximum finder produces the pulse flag and two pile-up flags (near and far) with programmable overlapping distances. The filter can be fully programmed by a serial interface.

The filter has been synthesized from a VHDL description and realized by using the AMS 0.8μm CMOS technology. A standard IEEE 1149.1 Boundary Scan path is included, with the I/O scan register and the bypass register. The whole filter is composed by about 460000 equivalent gates with a silicon area of about 58 mm² and 159 I/O pads. A few first prototypes have been fabricated and successfully tested by using functional test vectors. For this ASIC, seven main activities concerning testability have been carried out:

- **Analysis of the faults in the circuit.** The fault analysis with Single-Stuck-at-Fault (SSF) model showed that about 2% of the circuit nodes were untestable, mainly because of some VDD or GND tied nodes at the input of a block used in different part of the circuit. Other untestable nodes were due to tri-state bus logic.

- **FC measurement using the functional test vectors.** This analysis showed that the FC (with SSF model) was 74.34% using a test-pattern of 180K functional test-vectors.

- **Test-vectors generation and FC measurement using the ATPG.** Running the ATPG tool without any scan insertion was not possible due to a very slow convergence of the algorithms implemented in the tool. The main problems were due to the circuit initialization mainly concerning the serial interface decoder. In fact, running the ATPG on the circuit excluding the decoder removed the convergency problem and a test-pattern was generated allowing a FC of about 81%.

- **Insertion of DFT structures.** To solve the problems shown in b) and c) (i.e. low coverage and ATPG convergence problems due to complex structures not easily testable), a Full-Scan chain (a Mux-scan methodology with a single scan chain) was implemented. The Full-scan methodology was preferred to the Partial-scan because it is easier to implement and it leads to a better ATPG efficiency (defined as # of detected faults plus # of untestable divided by # total nodes); on the other hand the Full-Scan methodology introduces an higher area overhead if compared with the Partial-Scan methodologies, but the use of DSM technologies makes this aspect less demanding. A Full-scan chain with a single scan allows a minimum I/O overhead: only 5 additional I/O are needed. Another possible approach was the use of a multiple scan chain, shortening the test-time but with a considerably increased I/O number.

- **Test-vectors generation and FC measurement using the ATPG after insertion of DFT structures.** The results obtained are shown in the following table:

<table>
<thead>
<tr>
<th>Statistic</th>
<th>Comb</th>
<th>Seq</th>
<th>2-Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault coverage</td>
<td>94.87%</td>
<td>97.58%</td>
<td>96.98%</td>
</tr>
<tr>
<td>Testable FC</td>
<td>99.19%</td>
<td>99.46%</td>
<td>98.77%</td>
</tr>
<tr>
<td>Efficiency</td>
<td>99.23%</td>
<td>99.47%</td>
<td>98.79%</td>
</tr>
<tr>
<td>ATPG Vectors</td>
<td>358</td>
<td>23308</td>
<td>940</td>
</tr>
<tr>
<td>Scan Chains op.</td>
<td>358</td>
<td>456</td>
<td>132</td>
</tr>
</tbody>
</table>

In the table above are shown the fault coverage FC, the Testable FC (obtained eliminating the untestable faults from the total number of faults), the ATPG Efficiency, the number of parallel ATPG vectors (i.e. in each vector the scan elements IO pins are considered as primary IO) and the number of scan chains serial operations (each operation consists of a full shift of the scan chain). These figures were calculated using a pure combinational ATPG, a pure sequential ATPG and a two-pass ATPG, where a first very fast combinational ATPG step is followed by a sequential ATPG step. In the last case, 940 parallel ATPG vectors are needed to reach a 96.98% FC, with a 96% reduction of the ATPG vectors needed in case of pure sequential ATPG.
f) Untestable nodes reduction and insertion of “ad hoc” structures. The untestable faults due to VDD and GND tied nodes were eliminated adding some “injector" structures (multiplexers and extra pins), increasing the controllability; the untestable faults due to the tri-stated bus logic were removed using injector and output multiplexers, increasing the observability and controllability. With these modifications, the number of untestable nodes were reduced by a factor equal to 81%.

g) Test-vectors generation and FC measurement using the ATPG after insertion of “ad hoc” structures". The results obtained are shown in the following table:

<table>
<thead>
<tr>
<th></th>
<th>98.51%</th>
<th>98.84%</th>
<th>98.85%</th>
<th>1008</th>
<th>145</th>
</tr>
</thead>
<tbody>
<tr>
<td>fault coverage</td>
<td>Testable FC</td>
<td>Efficiency</td>
<td>ATPG Vectors</td>
<td>Scan Chains op.</td>
<td></td>
</tr>
</tbody>
</table>

It is important to notice that the untestable node reduction has led to a 1.5% enhancement of the FC on respect to the previous table.

h) Area and speed overhead. The results obtained are shown in the following table:

<table>
<thead>
<tr>
<th>Area</th>
<th>+9%</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/Os</td>
<td>+5</td>
</tr>
<tr>
<td>Speed</td>
<td>unaffected</td>
</tr>
<tr>
<td>Vectors</td>
<td>~200K</td>
</tr>
</tbody>
</table>

The area and I/O pads overhead does not significantly affect the design. Besides the delay on the critical paths was unaffected. Also the number of ATPG vectors needed to test the ASIC is relatively small, and it can be easily exercised by modern ATE. On the other hand the testability of the components was highly improved.

7. Future works

In the framework of the “Low cost Large Area Panel Processing of MCM-D substrates and packages” (LAP) ESPRIT Project [8], we are investigating a new partition for the system implementation on the MCM-V3, in order to reduce the number of components housed on the MCM and to obtain a higher general-purpose peculiarity of the MCM component leading to an increased opportunity to address different experiments. The main idea is to group together the Lineariser and the Pipeline in a single ASIC and to implement only the data acquisition (DAQ) path of the system. More investigation will be done for the ASIC FC, using IDDQ analysis (bridging fault), allowing further improvements for the chip yield. As concern the insertion of BIST structures, we are developing a modular solution for realizing RAM BIST, composed by a BIST controller to execute a test of the memory, a Test Pattern Generator and an Address Generator. We are going to implement the BIST controller as a programmable BIST processor, the Test Pattern Generator as a module generator, and the Address generator as an up_down counter. As concern the system level testability, different tests will be applied at each level (Die, MCM, Board, Crate and System) at different moments during the system life cycle: end of production, power-on, in-field and finally on-line. At each level of the hierarchy will be necessary to analyze the trade-off between constraints and goals and try to maximize the reuse.

8. Conclusions

In this paper we have introduced the MCM assembling technique and its advantages in term of system complexity and performance as compared to standard assembling techniques. However, we have also shown as the MCM approach needs a careful planning of the production flow in order to be cost effective. The topic role of chip yield in the production quality and therefore the need to push the component fault coverage to 100% has been discussed and it has been shown how the Design for Testability concepts must be included in the standard design flow at each level. Some results obtained in the case of the MCM-V3 design have been reported, and it has been shown how the use of testability CAE tools together with the design experience has allowed to reach high FC, without meaningful area overhead and performance degradation.

Acknowledgements

We thank all the FERMI Collaboration members for their continuous support to the project.

References


SIGNAL-INTEGRITY MEASUREMENTS ON VME320 BACKPLANE

Bertalan Eged, Attila Telegdy, István Gelencsér, Csaba Soós, Technical University of Budapest, H-1111 Budapest, Goldmann ter 3., Hungary (c-eged@nov.mht.bme.hu); László Szendrei, KFKI-RMKI, H-1525 Budapest, P.O.Box 49, Hungary

Abstract

Using high-speed buses in data-acquisition systems is widespread very much. The bus topology and performance is one of the key factors in the overall performance of the hole system. The limitation of the speed which can be achieved on a backplane-like bus is determined by the signal-integrity behaviour of the bus and the driver and receiver of the daughter cards. The paper deals with the profound evaluation of one of the latest VME-like backplanes. Measurement results are presented for the impedance profile, frequency-domain response, skew, eye-diagram and BER of the transactions.

1. INTRODUCTION

At the beginning of last year the VME community was surprised that a new type of VME backplane was announced which could handle data transfer up to 320Mbyte/s: the VME320. In DAQ systems of experiments the VME is extensively used so it is very important to extend our knowledge in this new technology.

In this sub-project we would like to evaluate the latest VME backplane technology. The purpose of the measurements is to determine the limitations or weak points of this technology and to receive basic experiences to design high-speed boards and systems using this type of backplane.

2. LIMITATION OF BANDWIDTH

First of all we should find the reason of the bandwidth limitation on a VME backplane. The key factors are the followings:

- Data width, Handshake protocol
- Signal settling time, Backplane delay
- Backplane skew, Circuit delay and skew
- Set-up and hold time
- Synchronization time, Bus acquisition time, Interrupt response time

Several improvements were done on the VME backplane to achieve higher data throughput. In the latest draft standards describe up to 64 bit wide transaction with 2eVME protocol instead of the original BLT protocol. [1]

The electrical characteristics of backplane and bus drivers of the cards are very important to achieve clean, undistorted signal to reach the highest speed enabled by the protocol. The designing of such high-speed cards and systems require deep knowledge of the electrical properties of the system components and extremely careful design focusing on the signal-integrity problems.

3. VME BACKPLANE TOPOLOGIES

3.1 Traditional backplane

Conventional backplane design uses slot to slot wiring scheme. Figure 1. In this topology the backplane looks like a long transmission line from slot #1 to slot #21. The unloaded characteristic impedance is near 60-70 ohm but it can be as low as 20 ohm in a fully loaded system.

The transmission is distorted by the reflection from the end of the long transmission line. [2] The main improvements use incident wave switching drivers with tighter input voltage range and limiting of the slew rate of the pulses driving the backplane. With the 160 pin connector which contains more ground pins we can reduce the crosstalk and ground bounce. The requirements can be seen in [3]. A lot of simulation and measurements were done which show that the system can be used to achieve high-speed data transmission and there are not any basic signal-integrity problems. [4] The theoretical data throughput is 160Mbyte/s with 64 bit wide data bus and 2eVME protocol.
3.2 The VME320 backplane

The new topology which is used by VME320 backplane instead of slot to slot wiring uses a star routing and all of the slots are directly connected to slot #11 at the centre of the backplane. [5][6] Figure 2.

The TDR profile was measured in all of the other slots. At the ends of the backplane we can see some additional delays before the lumped behaviour. Figure 4.

4. BASIC MEASUREMENTS

4.1 The TDR measurement

The impedance profile was measured on the backplane with TDR oscilloscope. In slot #11 the response looks like a lumped capacitance. See Figure 3.

In some connection combinations there is a peek resonance in the frequency domain response. This can show ringing in the time-domain. Basically the frequency of the resonance is higher than the signalling rate of the backplane and the low pass behaviour of the backplane attenuates the value signal which can generate the ringing.

This low-pass behaviour also can help to improve the EMC issues of the backplane and shows less radiation of the high-speed signals.

4.2 The frequency-domain measurement

The transmission on the backplane was measured in frequency-domain, too. Basically we can see low-pass response which will help in decreasing the slew rate of the signals in the backplane. Figure 5.
5. SKEW MEASUREMENTS

Using the 2eSST protocol requires a low-skew signal transmission to achieve a theoretical maximum speed.

For the skew and transmission measurements a 3U VME testcard was designed and manufactured. This card contains the ETL bus drivers with optionally installable RL filter network and it is compliant with VITA ETL draft standard. [3] Beyond the drivers there are some connectors for Pattern Generator and Logic Analyser which was used as a data source and receiver at the source and destination card respectively. The test set-up can be seen in Figure 6. Detailed information about the card can be found at our web: http://hstt.mht.bme.hu.

![Skew measurement setup](image)

Figure 6.

With the test set-up two kinds of skew were measured and one was calculated on rising and falling edge of the signals. First the skew of the 32 output bit of the HP Pattern Generator was measured by measuring bit by bit delay to a reference clock signal. The skew was determined as the difference between the earliest and latest signal. The second measurements series were done at the output of the receiver on the destination card. See Figure 7. and Figure 8.

![Measured source skew](image)

Figure 7.

The third skew was calculated from the two previous measurements. The base of the calculation was the subtraction of the delay of each bit. In this way we can give a delay of each bit from the source (the input of transmitter bus driver) to the receiver (output of receiver bus driver). The difference between the minimum and maximum is the total transmission skew caused by bus transceivers and backplane itself. The results are the followings:

<table>
<thead>
<tr>
<th>SKEW [ns]</th>
<th>Rising</th>
<th>Falling</th>
</tr>
</thead>
<tbody>
<tr>
<td>source</td>
<td>0.5</td>
<td>0.9</td>
</tr>
<tr>
<td>Destination</td>
<td>1.6</td>
<td>2.2</td>
</tr>
<tr>
<td>Transmission</td>
<td>1.85</td>
<td>2.2</td>
</tr>
</tbody>
</table>

Table 1.

Please note that these kinds of skews are different from the skews which are determined by the 2eSST draft. [7] There we can see the source skew which should be measured by the output of the card (real data source plus transmitter driver), backplane and receiver skew.

We think that our explanation and measurements show a little bit more realistic picture about the real development problem. The 2eSST draft may be based on the hypothesis that the real source skew can not be minimalised to such a low level as it was in our measurements, so registers should be used in the output driver. (like ABT16646, ABT646 or V320) In this way, really the output skew of the backplane driver is the main determining factor. But we consulted our digital designer and the preliminary simulation showed that the output skew of the digital core logic could be minimized under 1ns with special high-speed design techniques in the FPGAs and ASICs. In this way it is possible to use bus drivers without registers. And with tight input
From the signal integrity point of view check the 
DS1* line was monitored and eye-diagram was collected 
before one setup time of the earliest data strobe, and the 
measurement 40Mt/s speed. But please 
interference (ISI) presenting 
is the reason why we can see 
pattern, so it gave us a view of the intersymbol 
configurations should be checked.

It should be ensured that the latest data bit arrives 
before one setup time of the earliest data strobe, and the 
earliest data is clocked at least one hold before the 
transition of the latest data strobe. The measurements 
show that the 1-3ns setup and hold time can be fulfilled 
easily and the transmission can be safe at the proposed 
40Mt/s speed. But please note that it was only one 
measurement in one configuration and lot of other 
configurations should be checked.

6. WAVEFORM MEASUREMENTS

With the designed and manufactured test cards we can 
generate transaction up to 100Mt/s on the backplane. 
From the signal integrity point of view checking the 
clean and monotone rising and falling waveform is one 
of the most important measurements.

The waveform was measured on the receiver card at 
the pins of the 160 pin VME connector. The A1 and 
DS1* line was monitored and eye-diagram was collected 
synchronising to the master clock of the transmitter. This 
is the reason why we can see two data strobes because the 
scope was triggered at all rising edges of the master 
clock which has got double frequency as the data strobe. 
The eye pattern was made with a pseudo random bit 
pattern, so it gave us a view of the intersymbol 
interference (ISI) presenting in the system.

The transmission was stable up to 80Mt/s. As we can 
see from the scope pictures unfortunately the data strobe 
signal timing is not good. The transition of the strobe 
should be at the centre of the data window. This is the 
reason of transmission errors beyond 80Mt/s. The proper 
set-up time of the receiver cannot be fulfilled with this 
timing. With properly aligned data strobe the 
transmission can be stable far beyond 80Mt/s. See 
Figure 9.-10.-11. for eye-diagrams of different speed 
transmissions.

7. BIT ERROR RATE MEASUREMENTS

Measuring such high BER as 10E-12 to 10E-15 which 
is required for physics experiments can be quite difficult. 
In a good system we should wait long days for errors. 
One of the useable ways is measuring the low BER 
segment of the BER curve. BER measurements were 
based on the measuring of mean time between errors 
(MTBE). Slot #1 to slot #21 transmission was made 
using HP Pattern Generator as a source. HP Logic 
Analyser was used to monitor the sent word, to capture 
the received word, to compare them and measure the 
time between wrong words. The first 4096 wrong words 
were captured on 32 bit wide bus (3U card). The 
measurements were done at different speeds and the 
BER was calculated as:

\[
BER = \frac{1}{MTBE \times 32 \times \text{Speed}}
\]
The following table and figures show the results.

<table>
<thead>
<tr>
<th>BER Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed[Mt/s]</td>
</tr>
<tr>
<td>MTR[ns]</td>
</tr>
<tr>
<td>bit/s (3U)</td>
</tr>
<tr>
<td>BER</td>
</tr>
</tbody>
</table>

Table 2.

![Calculated BER at high speed](image1)

Figure 12.

![Calculated BER at lower speed](image2)

Figure 13.

8. CONCLUSIONS

The basic behaviour of the VME320 backplane was measured in frequency- and time-domain. Some resonances require future investigations.

The test set-up was built to generate transactions on the backplane, measuring the signal waveforms, skew and BER performance. The test set-up uses HP Pattern Generator and Logic Analyser for data source, acquisition and mean time between error measurement. The test cards use ETL bus transceivers for driving the bus without registers.

The time domain waveforms, skew and BER were measured only in one backplane configuration from slot #1 to slot #21, unloaded backplane.

The measured skew cannot be compared directly to the skew defined in draft standards, but they are under the limitation.

The time-domain waveforms show clear signal with monotone rising and falling edges.

Transaction can be done safely at the suggested 40Mt/s (320Mbyte/s on 6U cards) speed and far beyond this speed at the measured configuration.

Future plans

- Correcting the data strobe timing
- Measurements on other backplane configurations
- Measuring other VME backplanes for reference
- Building a stand alone test card

9. ACKNOWLEDGEMENT

The authors would like to express their special thanks to Pierre Vande Vyvre, Christopher Parkmann, George Rubin for supporting the work, Andrew Berding, Istvan Novak, Tivadar Kiss for extremely useful consulting and suggestions, Zsolt Polgar and Norbert Gerecs for routing the test cards.

10. REFERENCES

[1] VME64x, VITA 1.1-1997/D2.1 VME64x draft standard
[3] ETL, Vita 2-199x/D0.5 ETL draft standard
[7] 2eSST, VITA1.5-199x/Draft 1.5 2eSST (Source Synchronous Transfer) draft standard, [http://www.vita.com](http://www.vita.com)
FOUR CHANNEL FIBRE OPTIC TRANSMITTER AND RECEIVER MODULES FOR CMS DETECTOR TRACKER READOUT LINKS

M. Magliocco, P. Nugent
Italtel Spa, Castelletto di Settimo Milanese, I-20019.
Tel : +39.2.43889288  Fax : +39.2.43889021
e-mail : peterowen.nugent@italtel.it

Abstract

We report on the realisation of compact four channel optical transmitter (Tx) and receiver (Rx) modules which have been developed in collaboration with CERN’s EP/CME division. Custom modules with pigtailed Fabry-Perot laser diodes and PIN photodiodes have been designed and fabricated using the Silicon Optical Bench (SiOB) technology. Both Tx and Rx modules are assembled in a compact 14 pin DIL ceramic package. The four optical fibre pigtails are bundled in a common jacket, terminated in a ribbon and connectorised with an MPO4-T angle polished connector. TheTx modules are hermetic and epoxy free. Both Tx and Rx modules exhibit good linearity, low noise and good temperature stability.

1. INTRODUCTION

Four channel optical transmitter (Tx) and receiver (Rx) modules have been developed for the CMS detector tracker readout link. The CMS central tracker consists of approximately 12 million detector channels from which data will be transferred over an analogue optical link at 40 Msamples/s. Each link transmits 256 time multiplexed analogue samples. Therefore, approximately 50000 links will be required. The link will be composed of Tx modules inside the LHC transmitting data over optical fibres to Rx modules in the data-logging room at a distance of about 100m. Furthermore, there will be a few thousand digital links to and from the tracker for transmission of clock and control signals [1]. This paper outlines the assembly of custom four channel modules in part 2. Part 3 covers the electro-optical characterisation of these modules while part 4 reports some initial results of reliability testing.

2. MODULE DESIGN AND ASSEMBLY

Due to the nature of the application and severe operating environment (analogue link, a 4T magnetic field, the presence of nuclear radiation, limited space) a number of requirements must be fulfilled [2]:

1. Low noise, high linearity transmitter and receiver
2. Compact package
3. Low mass, non magnetic packaging materials
4. Hermetic and epoxy free Tx modules for high reliability
5. Radiation hardness
6. Temperature range of -20 to +70 °C

A solution has been developed based on the Silicon Optical Bench (SiOB) technology available in Italtel to meet these requirements. A 1300 nm Fabry-Perot laser diode is aligned to a singlemode (SM) optical fibre using a custom silicon submount in the case of the Tx; while in the Rx a PIN photodiode is aligned to a SM optical fibre using another custom submount. The resulting pigtailed optical sub-assemblies (OSAs) are then packaged in groups of four. The laser OSA is shown in Fig.1. The laser chip is die-attached to the submount by means of evaporated AWSn eutectic solder. The die-attach is a batch process and takes place in a reducing atmosphere. The solder is confined during the die-attach process by means of evaporated Ti solder dam. The laser’s p contact is accessed by means of a gold wire-bond. At the front of the laser submount is another bond pad where the metallised angle cleaved fibre is actively aligned and attached using a AWSn solder preform. The preform is melted by driving current through a Cr resistor running under this bond pad. This resistor is thermally isolated from the rest of the submount by means of a thick oxide layer and is electrically isolated from the fibre bond site by another thinner oxide layer.

Fig. 2 shows the PIN submount. The die attach and wire bonding processes are similar to those of the laser. The optical fibre is placed in an etched v-groove and actively aligned to the back-illuminated PIN by means of a 54° turning mirror at the end of the v-groove. Once coupling efficiency has been maximised the fibre is fixed in place using thermally cured epoxy.
The ceramic lid which is supplied with a Sn/Pb solder preform is soldered to the package in a reducing atmosphere, using a customised process. During the development of this process trials were carried out on test modules which were then subject to gross and fine leak hermeticity tests according to MIL STD 883D Method 1014. As a result, optimised process conditions were identified which allow the realisation of hermetic modules.

It was therefore possible to assemble completely epoxy free hermetic Tx modules as required.

Fig. 5 shows in detail the lid soldered to the package. The solder meniscus is continuous and shiny in appearance indicating a good seal.

Finally, a bend limiter is fixed to the ceramic ferrule and the fibres which are colour coded according to channel number are bundled in a common jacket and terminated with a MPO4-T angle polished connector. Fig. 6 shows the finished module complete with connector.
3. MODULE TESTING

Two automatic test stations, which can measure up to 5 Tx and Rx modules at a time, are used to perform the measurements. All modules are tested at 25°C and then burned-in to stabilise behaviour and to identify weak devices. Following burn-in the functionality of the Tx modules is verified from -20 to +75°C and that of the Rx modules from -40 to +85 °C. Fig. 7 shows the Tx module test station.

As these modules will be used in an analog link, the modules should have high linearity and low noise. Fig.8 shows a typical laser P/I curve at 25°C while Fig.9 shows the laser RIN (Relative Intensity Noise) vs. frequency. Table 1 shows some typical receiver characteristics. Results for the full analog link are reported elsewhere at this conference [3].
modules which will be inside the LHC and due to mechanical shock and fibre pull tests which should give an indication as to the robustness of the modules when subject to handling during installation are currently underway.

<table>
<thead>
<tr>
<th>Responsivity (1310nm)</th>
<th>0.85</th>
<th>A/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dark current (-5V)</td>
<td>0.1</td>
<td>nA</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>&gt;30 V</td>
<td></td>
</tr>
<tr>
<td>Linearity</td>
<td>&lt;1%</td>
<td></td>
</tr>
<tr>
<td>Capacitance (-5V)</td>
<td>1.5</td>
<td>pF</td>
</tr>
<tr>
<td>Optical back reflection</td>
<td>-55</td>
<td>dB</td>
</tr>
</tbody>
</table>

Table 1: Typical Rx electro-optic characteristics at 25 °C

4. RELIABILITY

Due to the nature of the application, module reliability is of utmost importance particularly in the case of the modules which will be inside the LHC and to which there will be limited access during the lifetime of the experiment. Three Tx/Rx pairs were subject to thermal cycles from -20 to +70 °C with a ramp time of 1 minute and dwell times of 15 minutes. This test should provide information about the module mechanical integrity i.e. if there are any residual stresses on the fibres this is likely to show up in a variation in chip to fibre coupling efficiency. Laser threshold current and slope efficiency and PIN responsivity and dark current were tested before and after each of the aforementioned tests. The results are shown in Figs. 10 and 11. If we use the Bellcore standards [4] as a guideline then the pass/fail criteria are variations of ± 10% in PIN responsivity and laser slope efficiency, no obvious change in laser threshold current (Ith) while the acceptable change in dark current (Idark) is not specified. Considering these guidelines the results shown below are quite satisfactory with no variations above the 10% limit, while variations in Idark and Ith are below the measurement error. Mechanical shock and fibre pull tests which should give an indication as to the robustness of the modules when subject to handling during installation are currently underway.

4519

5. CONCLUSIONS

Four channel optical transmitter (Tx) and receiver (Rx) modules have been successfully developed and realised. These devices are assembled in a mainly ceramic package which has been developed in collaboration with Kyocera Fineceramics. The Tx modules are hermetic and epoxy free. Both the active components (laser or PIN chips) and optical fibres are aligned on silicon submounts which have been specifically designed and fabricated for this project. The dimensions of the 4 channel module of 10x17x4 mm compare favourably with those of the industry standard single channel mini-DIL package of 7.6x13.2x3 mm.
Several new packaging processes were developed to fulfill CERN’s requirements. These include:

- assembly of four devices in a single package, including the development of custom mechanical fixtures for placement of the four OSAs and fibres.
- soldering of the ceramic lid to the package (the standard process consists of a metal lid seam sealed to the package).

The modules have been extensively tested and shown to meet the electro-optical specifications. Results obtained after temperature cycling of the modules are encouraging and further reliability tests are planned.

ACKNOWLEDGEMENTS

This project has been financed by and carried out in collaboration with F. Vasey’s group at CERN’s EP/CME division. The authors gratefully acknowledge the very valuable contributions of our colleagues in the Wafer Fab and Packaging Groups. We particularly thank E.Cadamosti and C.Garavaglia for module assembly and L.Brioschi, F.Fusari and G.Ongaro for Silicon wafer fabrication.

REFERENCES

RESULTS FROM AN FPIX0 CHIP BUMP-BONDED TO AN ATLAS PIXEL DETECTOR

A. Mekkaoui, D. Christian, S. Kwan, J. Srage, R. Yarema
Fermi National Accelerator Laboratory, Batavia, IL 60510

Abstract
Results are presented of tests performed on the first pixel detector readout ASIC designed at Fermilab (FPIX0).

1. INTRODUCTION
An effort has begun at Fermilab to develop a pixel detector readout ASIC appropriate for use at the Fermilab Tevatron Collider. The readout ASIC must be radiation hard so that it can be used close to the beamline, and it must be optimized for the 132 ns time between crossings planned for future Tevatron operations. Our development plan calls for a series of test chips, fabricated using standard CMOS technologies. We expect the final design to be realized using the radiation hard Honeywell 0.5μ SOI process. In this paper we report the results of measurements made on our first test chip (FPIX0), which has been indium bump bonded to an ATLAS n*-on-n pixel sensor [1].

2. FPIX0 DESIGN
The FPIX0 is a column based pixel chip with 50μ x 400μ pixel cells arranged in an array of 64 rows by 12 columns. It has been fabricated using the HP 0.8μ CMOS process. The cell geometry was chosen to be compatible with test pixel sensors designed by the ATLAS collaboration. This first prototype pixel detector readout chip was designed with three goals: 1) Establish a front end design appropriate for use at the Tevatron collider. 2) Verify that the analog and digital sections of the chip can be isolated from one another. 3) Verify that coupling through the sensor is not a problem (metal 3 is used as a shield between the sensor and the readout chip).

FPIX0 consists of an array of pixel unit cells together with relatively simple digital logic that provides a zero-suppressed readout of the chip. Each unit cell includes an amplifier with test input, a discriminator with programmable kill, a peak detector, and readout logic. The amplifier consists of two folded cascode stages, AC coupled to one another. The first stage is a charge amplifier that uses a current controlled feedback circuit [2]. The feedback current controls the return to baseline time and compensates for sensor leakage current. The second stage provides additional gain and is DC coupled to the discriminator. The discriminator is a classic two stage comparator. When the discriminator fires, a set reset flip flop is set and a fast-OR signal asserted. Upon receipt of a token, the cell places its address on an output bus and connects the output of its peak detection circuit to a global analog output line. An externally controlled token advance signal is used to release the token to the next hit pixel cell. This signal also causes the cell that releases the readout token to reset itself.

Two of the 12 columns contain amplifiers with lower first stage feedback capacitance (10 fF instead of 20fF). These cells have higher gain than the standard cells and correspondingly lower dynamic range.

3. MOUNTING ON SENSOR
Four FPIX0 IC's have been indium bump bonded (by Boeing North America) to ATLAS test sensors. Each sensor consists of an array of 160 rows by 18 columns of 50μ x 400μ pixel cells. The FPIX0 chips have been bonded to one corner of the sensor array, as shown in Figure 1. Eleven of the twelve columns in FPIX0 are bonded to sensor pixels and one column is left unbonded. This allows us to compare the performance of bonded and unbonded cells. Amplifier and discriminator outputs from one row of pixel unit cells are routed directly to pads on two sides of the FPIX0. The outputs from four of these cells are accessible in the bonded assembly. These include three cells bonded to sensor pixels and one unbonded cell.

Figure 1. Photograph of an FPIX0 bonded to an ATLAS test pixel sensor.

Work supported by the U.S. Department of Energy under contract No.DE-AC02-76CH03000.
All of the measurements reported on here were made on a single FPIX0 bonded to a Seiko test sensor. Plans are being made to beam test the other three devices during the 1999 fixed target run at Fermilab.

4. CONNECTIVITY AND SENSOR IV

The IV characteristic of the bonded Seiko “STI” [1] and the current in the n-side guard ring are shown in Figure 2. At sensor bias voltages below the full depletion voltage, the guard ring current is very sensitive to the biasing of the guard ring relative to the pixels. These curves show that full depletion is reached at approximately -45 V. All of the tests described below were performed with a sensor bias voltage of -75 V.

The bump bond yield was measured by illuminating the sensor with a Sr’⁵⁰ source and plotting the number of times each pixel unit cell registered a pulse above a threshold of ~3000 e⁻. All pixels were found to be connected and no pixel was noisy.

5. NOISE AND DISCRIMINATOR THRESHOLD MEASUREMENTS

Fluorescence x-rays from a number of metal foils were used to provide an absolute calibration of the FPIX0. For example, the sensor was illuminated with Terbium x-rays, and a pulse height spectrum was collected using one of the direct amplifier outputs. The Kα peak (44.5 keV) was easily identified. Since a 44.5 keV x-ray creates 12300 mobile e-hole pairs in depleted silicon, the peak in the spectrum can be interpreted in terms of the number of electrons input to the amplifier. The rms noise observed with no source illuminating the sensor also can be converted directly into an equivalent number of electrons input to the amplifier (these measurements agree with the noise values inferred from the discriminator threshold scans described below). We have also verified the linearity of the FPIX0 amplifier response to small input signals using a variety of characteristic x-rays.

The x-ray spectra obtained using the three direct amplifier output signals also allow us to interpret the response to an injected test signal in terms of electrons input to the amplifier, or equivalently, to determine the value of the charge injection capacitor. This, in turn, allows us to rigorously interpret discriminator threshold scans of all of the pixel cells in the array in terms of electrons input to the amplifiers (assuming only that C_finput is the same for all cells). It also allows us to interpret the dynamic range of the amplifier in terms of the input in electrons. For FPIX0 cells with C_f=20 fF, the dynamic range is approximately 52000 electrons at the input.

A discriminator threshold scan was performed for each pixel cell by holding the discriminator threshold constant and scanning the injected test pulse voltage through the threshold. The fraction of the time that the discriminator fired was recorded for each value of the injected pulse. The resulting curves were fit to the integral of a Gaussian distribution, yielding an rms noise and discriminator threshold (50% point). The discriminator threshold rms was calculated directly from the resulting distribution of 50% points.

Figure 4 shows noise distributions inferred from these measurements for three columns of pixel cells. The top histogram corresponds to a column of bonded pixel cells with the higher gain version of the amplifier. The middle histogram is for a standard bonded column. The bottom histogram shows the noise of the unbonded column of pixel unit cells. Two conclusions can be drawn. First, there is a trade-off between the larger dynamic range associated with the standard front end and the lower noise and reduced discriminator threshold dispersion of the higher gain front end. Second, the bonded cells are only slightly noisier than identical
unbonded cells. If all of this noise difference is attributed to the difference in input capacitance, then a SPICE simulation indicates that the total input capacitance of the sensor pixel and bump bond is approximately 180 fF.

We have measured the pixel to pixel cross talk both in the short direction of the pixel cells and in the long direction. When a pulse is injected into an FPIX0 front end which is bonded to a sensor pixel, the neighboring cell in the long direction registers a signal ~2% as large as the cell which received the charge injection. When an unbonded cell is selected, the cross talk to the neighbor in the long direction is ~1%. This indicates that the cross talk through the sensor is ~1%. We believe that the balance of the cross talk occurs through the charge injection network itself. Cross talk has also been measured on several bare FPIX0 chips (not bonded to sensors). In this case, the cross talk in the short direction is almost exactly the same as for the bonded chip.

6. ANALOG READOUT

We have verified that the normal readout sequence (including the analog information) works as designed, except that the token fails to get reset after readout. This means that a chip reset must be issued after each event is read out. This operation involves only the resetting of a single flip flop.

7. PICKUP AND CROSS TALK

We have not been able to measure any pickup of the digital activity associated with readout. With the metal 3 shield grounded there is no significant coupling through the detector. The capacitance between the metal 3 shield and a sensor pixel has been inferred to be approximately 1.8 aF/µ. This capacitance was deduced by disconnecting the shield from its ground, injecting a pulse on the shield, and measuring the output voltage from a single pixel unit cell.

8. CONCLUSIONS

Results have been presented from an FPIX0 prototype pixel readout chip bump bonded to an ATLAS pixel sensor. With these results in hand, we are continuing our effort to develop a readout chip optimized for use at the Tevatron collider. Subsequent designs will use an amplifier design based on the FPIX0 front end, probably using even lower feedback capacitance (than in the high gain cells of FPIX0) to further decrease noise and discriminator threshold variation, at the expense of reduced dynamic range.

FPIX0 chips bonded to ATLAS sensors will be used in beam tests during the 1999 Fermilab fixed target run to study the use of analog information to improve spatial resolution using charge sharing information. Simulations done by the BTeV collaboration indicate that a significant improvement in resolution over binary readout can be obtained by a very coarse digitization of the analog information [3].

9. REFERENCES


KEY INDUSTRIAL TECHNOLOGIES FOR ALICE TPC DETECTORS
AND OTHER DETECTOR APPLICATIONS

A Cern/ Dassault Electronique collaboration

A. DRAVET (Dassault Electronique) and JC. LEGRAND (Cern)

Technology requirements for nuclear detectors are among the most restricted for chip connections, multilayer boards fabrication and complete detector buildings.

ALICE TPC detector is a perfect illustration of all these requirements that have been globally industrially solved and that are common to a lot of other detectors and experiments like ATLAS and CMS.

Chip connection and packaging (bumpless TAB):

Requirements are:

- integration and testability due to the large number (>100) of active components on the same board. A packaging close to the chip size is required. For a good yield of the final detector full analog testability of each dies is very important,

- low cost and compatible with large series,

- compatibility with standard bare dies.

The use of resin encapsulated chips in bumpless TAB forms allows assembly on printed circuit boards with solder technologies. Repairability is also proved.

A complete fabrication flow is presented with picture of real pieces as well as test and yield results.

Motherboards support of detectors pads and of front end electronic:

Requirements of boards supporting detectors and electronics are planarity (parallelism), hermeticity to oxygen from one side to the other side.

A patented process to fill board holes has been used and is provided to be hermetic and industrial on large boards. An epoxy resin is used. Results are presented.

Complete 3D buildings: (different 3D views are presented)

Connections from boards to boards are made thanks to a TAB like technology that allows a good electrical and reliable connection and a 3D flexible assembly.

Other detectors of Atlas and CMS are on the way to use such technologies.

Other examples are presented with finer pitches (86 μm) on silicon and different buildings cases.
ALICE TPC
Functional Detector Module

PCB MOTHERBOARD
Support of shapers and cathodes
( design, fabrication, test )

Full tested 4 channels
TAB preamplifier ( shapers )

Planarity and Parallelism

Hermetcity

Surface mount assembly

High density TAB surface mount assembly
( 144 shapers per motherboard )

DAUGHTERBOARD ASSEMBLY
flex TAB motherboard

MOTHERBOARD and DAUGHTERBOARD
Connected together on their test tool

High density TAB FLEX
Connections

AT EACH

High density Output DATA

ALICE - TPC - INSTALLED READ OUT DETECTORS -
PRODUCTION TECHNOLOGIES FOR HIGH PERFORMANCE ELECTRONICS

Bo Wikstrom and Luciano Pasquariello E-mail: bo.wikstrom@xicon.se Xicon AB, Ideon Science Park, Malmö, Sweden

Abstract

Xicon is today involved in a couple of subatomic particle detector projects. Our focus is to develop new high performance assembly technologies for the electronic sector. We are also producing electronics for scientific, industrial and automotive applications. The improved performance, reliability, efficiency are improved by miniaturisation, fewer components and less material. The last two factors have been the most important reasons for us in the cooperation with the subatomic scientists. We have also a strong focus on solder free electronics which helps us to increase performance and the material have a less relative mass. This systems based on conductive adhesives includes everything from design rules, chemical solutions and new repair techniques. Chip assembly technologies as wire bonding and flip-chip are essential techniques in our activities. We are planning to present new integrated technologies for very high performance electronics assembly. This technology can achieve superior performance without printed circuit boards and substrates. This new technology also allows on board integrated components etc

FIELD ACTIVATED ANISOTROPIC WET CHEMICAL ETCHING AND ITS APPLICATIONS
Bert Junno, Stefan Alfredsson and Babak Heidari E-mail: bj@etchtech.com EtchTech Sweden AB, Box 60031, SE-21610 Malmö, Sweden

Abstract

A novel method for galvanic etching of micrometer and nanometer sized thin metal structures is presented in this paper. The main principle of this etching method is the activation and reduction of metal ions by electrons released from an electrode. This etching technique is both anisotropic and selective with results which are closer to dry etching techniques than wet etching. The different initial behaviour of metal etching is explained by the different ionic strengths of chemicals and the rate limiting factor is mass transport. The metal particle corrosion rate is related to the dissolution rate depending on pH and potential values of chemicals. The direction of the reaction depends on the field distribution and the chemical activation energy. Test substrates with 5 micron lines and spaces with a total thickness of 5 microns of copper were successfully etched. The undercut was less than 10%.

1. Background

Xicon AB (founded in 1989), in the EtchTech group, are developing and producing electronics for accelerators e.g. CERN, Brookhaven etc. The main focus is detectors for tracking systems, satellite electronics and fiber optical communication. Xicons development of electronics for scientific and measurement applications have led to new production technologies and to the collaboration with EtchTech Sweden AB on the development of new micro structuring techniques. EtchTech which was founded in 1998, develops new techniques in the field of lithography and etching of thin metal films and semiconductor microstructures. Some preliminary results from a novel etching technique will be briefly described in this paper.

2. Tracking system electronics

In 1992, Xicon started a cooperation with Ingvar Otterlund, Hans-Ake Gustavsson and Anders Oscarsson at the department of subatomic physics, Lund University. The development and production of some different tracking systems was the result of this work. Deliveries have, so far, been made to Europe, USA and Japan.

The most important aim was to create a large number of measurement channels. Today, up to 210,000 channels have been realised in one detector. Another important goal has been the ability to register small high velocity charged particles. The material content, in the pad registration electronics, is extremely low. The electronic assembly is made with naked chips. Passive components are connected with conductive adhesive. The printed circuit boards are of a thickness which is a fraction of a hair diameter. The production technologies developed for scientific applications have in a relatively short period of time also been transferred to industrial and medical applications.

The chips in the detectors consists of charge amplifiers and analog to digital converters for the readout of highly granular particle detectors. The chip assembly techniques are mainly wire bonding and flip-chip. The wire bonding process is a wedge-wedge aluminum or gold wire process. The gold wire process is a hot bonding process and the aluminum wire is a room temperature process. The flip-chip assembly techniques consist of two main
methods. The solder or gold bumped chips can be soldered on board. The polymeric or gold bumped chips can be connected with conductive adhesives.

The surface mounted components (SMD), are soldered or connected with conductive adhesive. The clear trend is towards solder free connection methods. The reasons for this are that these techniques yield a higher performance, better quality, reliability, improved efficiency and they are much less detrimental to the environment.

The carrier board material can be of different types due to the demands of the application. The most common materials used are glass fiber epoxy, polyimide (Capton), Teflon, glass, silicon and ceramics. The thickness of the carrier may vary from 25 microns to several millimetres. The lateral dimensions goes from a few millimetres to several 100 millimetres.

3. Fiber optics and satellite electronics

The production technologies above, give small dimensions and high performance connection methods. Fiber optical communication modules can the operate at high bit rates. The modules produced at Xicon are operating at multi Gigabit/s. The satellite electronic modules for scientific applications have a focus on high frequencies, e.g. spectrum analyzers operating at 500 Ghz. This applications have an extreme demand of small weight/volume and reliability.

4. Field activated anisotropic chemical etching (EFAACE)

We present a novel versatile nano and microstructure etching technology applicable to most electronic materials. Development of the technique for etching fine lines in Al, Cu, Au and Si plus alloys of these materials is our first concern, other materials will follow shortly. We will apply the technique to the production of printed circuit boards, flexible printed circuit boards and semiconductor chips. Because of the material friendly solutions and the high level of material selectivity in the process we will test high density naked chip and flip chip mounting with new soldering and packaging techniques including conductive glues and and isolating resins. These techniques will together allow for several layers of chips and metal lines mounted on top of each other and a higher packing density.

The etching technique builds on a set of patents which describe processes where materials are etched in a wet solution with an applied electric field. In contrast to other wet etching techniques it gives highly anisotropic results. We have demonstrated etching fine lines in copper, chromium, aluminum and nickel on different substrates. The line widths and pits have ranged from a 100 microns down to 50 nanometres. 10-50 microns wide etchpits have been demonstrated in 2-18 microns thick copper on laminate substrates. Finer pits and lines between 50-700 nm have been demonstrated on copper and nickel films on various substrates including Si substrates. The film thicknesses in these tests ranged from 100-500 nanometres.

The present status is that we have started activities for the development of the technique to be used for more materials and in a production environment. At present we focus on developing processes for the etching of copper and aluminum films with thicknesses ranging from 0.1 to 35 microns. The line widths and spacings in these tests are ranging from 20 nanometres to 100 microns.

5. Conclusion

We aim at reducing the cost of development and production in the electronics industry in general. This together with our collaboration projects with scientists in the fields of medicine, microelectronics and subatomic physics have led to novel production technologies to meet the demanding component specifications. One example, applied to the semiconductor industry, the EFFACE technique described above, will lead to new possibilities in the design of chips. The layer protecting the components from the damaging effects of plasma etching can be greatly reduced, enabling a further decrease of the component size and simplifying the process. This together with the possibility to define very fine lines allows for higher component densities.
CMOS and BiCMOS Transimpedance Preamplifiers for Silicon Drift Detectors Read-Out

N. Randazzo, L. Lo Nigro, G. V. Russo

Dipartimento di Fisica, Università di Catania and INFN, Sezione di Catania
Corso Italia 57, I 95125 Catania, Italy
E-Mail: randazzo@sunel.ct.infn.it, vrusso@sunel.ct.infn.it

1. INTRODUCTION.

The ALICE’s Inner Tracking System (ITS) consists of 5 planes of position sensitive detectors [a]. The 3rd and 4th plane are of Silicon Drift Detectors (SDDs) [b]. They are very large area detectors: 35 mm in the beam direction (Z); 87 mm in the direction one (X).

The charge collected by the anodes implanted at the edge of the detector has a Gaussian shape due to the diffusion process. The collection time depends strongly on the distance x of the impact point from the collecting anodes: a rise time up to 70 ns is expected.

The main features for fast front-end amplifiers imposed for LHC experiments are low power, low noise, low cost, high gain and good stability.

The folded cascade configuration shows two poles given by [d]:

\[ P_1 = -\frac{1}{R_L C_L} \]
\[ P_2 = -\frac{g_m}{C_{gd1} + C_1} \]

where \( R_L \) is the equivalent resistance as seen at node 1 and \( C_1 = C_{gd1} + C_{gd4} + C_{gb4} + C_{gb3} + C_{gb2} + C_{gb1} + C_{gb0} \).

In our design we have put these poles at 22 MHz and 234 MHz. One more pole is added by the input impedance of the amplifier coupled with the detector capacitance. With 500 fF of detector capacitance (including stray) this pole is at about 44 MHz.

This configuration shows a very good stability with 84 degree phase margin.

The impulse response of the amplifier has a rise time given by:

\[ t_r = 0.35/f_c = 16 \text{ ns} \]

that gives a good solution for processing this kind of signal. \( f_c \) is the 3dB cut-off frequency.

The amplifier must be able to treat all the signals coming from the detector.

Figure B shows the simulated output response vs. time of the amplifier for several input charge with different

![Figure A: TA Schematic Diagram](image)

![Figure B: Simulated output shape for x = 1 and 35 mm.](image)
over 25 MIP. Fig. C shows the output response versus input charge for different impact points. As you can see the TA is not a linear device.

3. EXPERIMENTAL RESULT.

The amplifier was implemented as a 16-channel chip with a pitch of 200 μm just to match the anode pads of the detector. The silicon chip is shown in the photo below.

4. THE SECOND PROTOTYPE

This preamplifier was designed in view of the defined schematic view of read-out [E] with the following characteristics:

<table>
<thead>
<tr>
<th>Characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAIN = 900 kΩ</td>
</tr>
<tr>
<td>BANDWIDTH &gt; 25 MHz</td>
</tr>
<tr>
<td>MARGIN PHASE &gt; 60°</td>
</tr>
<tr>
<td>NOISE &lt; 2 mV rms</td>
</tr>
<tr>
<td>DRIVING CAPABILITY = 7 pF</td>
</tr>
<tr>
<td>POWER DISSIPATION &lt; 2 mV/channel</td>
</tr>
</tbody>
</table>

The schematic circuit of the amplifier is shown in Fig. E

Both high gain and good stability were achieved using a feedback resistance $R_L = 300 \, \text{kΩ}$. The technology used is BiCMOS 0.8μ.

We chose a NMOS transistor as the input device, because it has input current zero. To eliminate offset of the amplifier, the blocking capacitance $C_B$ must be equal to 10 pF.

The transimpedence gain is given by
A R R R R c F E 33 900 Mhucc-e M al Q .

ac: Rclbblill 1u -an -as -Q-3l -an -71.1 -on -1 II In in -H u. * u

Fig. F
A Bode plot of the transimpedance gain is shown in Fig. F.
The transfer function in the frequency domain can be expressed by:

\[ T(s) = \frac{g m_1 R c_2}{(1 + sR_f C_D)(1 + sR_c C s)} \]

where:

\[ T_0 = g m_1 \cdot R c_2 = 30 \]

\[ P_D = -\frac{1}{R_f (C_1 + C_p + 2C_{gd1})} \equiv -5.4 M \text{ rad/s} \]

are open loop gain and dominant pole.
The value of the gain-bandwidth product is given by:

\[ GBW \equiv T_0 \cdot \frac{P_D}{2 \pi} \equiv 26 \text{ MHz} \]

The margin of phase is 74°.
A Bode plot of the transfer function in frequency domain is shown in Fig. G.

5. NOISE ANALYSIS
We have investigated two kinds of contribution of noise, thermal and flicker, due to the input transistor and the feedback resistance.
The density spectral noise considered are:

\[ S V_r = 4 \frac{K T R_f}{f} \]

\[ S V_1 = 4 \frac{K T}{3} \left( \frac{2}{3} \cdot g m \right) + k \frac{f^{0.5-2}}{f} \]

The density spectral noise output is given by:

\[ S_o \equiv S V_r \left( \frac{R c_2}{R e_3} \right)^2 + S V_1 \left( \frac{R c_2}{R e_3} \right)^2 \]

The voltage noise then is equal to:

\[ N = \sqrt{S_o \cdot \Delta f} \equiv 1.2 \text{ mV} \]

6. CONCLUSION
Two transimpedence amplifiers were well designed.
The second prototype give an especially good performance from point of view of the read-out described in [E].

REFERENCE
Novel Current Mode Feedback Loop - CERN EPC
95/10, May 1995

[E] N.Randazzo, G.V.Russo - Transimpedence amplifier
SIMULATION AND CHARACTERIZATION OF THE FRONT-END OF SDD IN ALICE ITS

C. Petta\(^{(1),(2)}\), U. Becciani\(^{(3),(2)}\), G. V. Russo\(^{(1),(2)}\)

1. Department of Physics - University of Catania
2. INFN Sezione di Catania
3. Astrophysical Observatory – Catania

email: Catia.Petta@ct.infn.it

Abstract

The front-end of a semiconductor detector usually requires a charge amplifier followed by a shaper and a voltage ADC. This typical solution is not suitable for Silicon Drift Detectors in ALICE. We have performed many realistic simulations concerning the ALICE event, the detector and the front-end electronics to optimise the structure and the parameters of the readout electronics. The solution we propose consists of a transimpedance amplifier followed by a switched capacitor array analog memory and an ADC.

1. INTRODUCTION

The constraints imposed by high-energy physics experiments to the front-end electronics are becoming more and more rigorous. The higher the number of channels, the smaller the size of the electronics, the quantity of matter through the particle tracks and the power consumption. At the same time, the noise has to be as low as possible to allow better resolutions and efficiency.

Clearly, the challenge is offered to technology, but a lot of work is possible designing appropriate solutions for a fixed technology. With the help of an accurate simulation relating to the whole generation chain, signal treatment and reconstruction of the transported information, the values to be assigned to the specific parameters of the electronics project, crucial for the precision and efficiency of the whole measurement, can be defined. This publication presents the preliminary results of our study of the most suitable electronics for the readout of the Silicon Drift Chambers used in the Inner Tracking System (ITS) of ALICE ((1)+[2]+[3]).

ALICE is a high-energy physics experiment that will be performed using LHC (Large Hadron Collider) to explore the ‘quark gluon plasma’. The six innermost cylindrical layers of high-resolution detectors constitute the Inner Tracker System (ITS), whose basic functions are low-momentum particle identification and tracking, and secondary vertex reconstructions. The third and the fourth layers will be arranged with SDDs (Silicon Drift Detectors).

2. SILICON DRIFT DETECTORS IN ALICE

The SDDs ([(4)+[5]+[6]]) for ALICE will be large-area planar detectors (8.7x7cm) (Fig.1) of a 300 μm high resistivity n-type silicon wafer. An external high voltage applied to an integrated on-board divider fully depletes the volume of the detector and generates a drift field inside the edge of the detector where 384x2 n+ anodes with a pitch of 210 μm are implanted.

A charged particle crossing the detector releases energy creating electron-hole pairs along its track. The holes are removed by the nearest electrodes, but the electrons, focused in the middle plane of the detector are collected by the anodes just in front of the impact point by the drift field. During its motion, the electronic cloud diffuses and its gaussian widening depends primarily on the distance of the impact point from the anodes (X - drift coordinate). The drift field foreseen is about 450 V/cm, with an electron velocity of 6 μm/nsec.

The information given by a SDD about an interacting particle, is a collection of signals, suitably sampled, on the anodes in front of the impact point. In ALICE the sampling frequency is 40 MHz.

A conservative proposal for the readout of the SDDs foresees the acquisition and the further analysis of all the signals over the threshold (zero-suppression). The two spatial coordinates will be reconstructed off-line by means of the centre-of-mass method, taking into account the influence of the amplifier response in the signal time developing. Both the resolutions vary with the localisation of the point of impact \([7]\). In Fig.2 the SDD resolutions in both directions vs. X, the distance of the point of impact from the anodes, are depicted for single tracks.
The current signal feeding the preamplifier is:

\[ I_j(t) = \frac{q_j}{\sqrt{2\pi\sigma_t}} \exp\left[-\frac{(t-t_0)^2}{2\sigma_t^2}\right] \]  

(1)

where \( D_e \) is the diffusion constant for electrons in silicon, \( \omega \) is the drift time, \( v \) is the drift speed and \( q_j \) the total charge collected by the j-anode.

3. EVENT, SDD AND READOUT SIMULATION

The physical event is the collision between two ions accelerated by the collider, which leads to a shower of charged particles impinging on the detector. These have a realistic distribution both in space and as far as energy loss is concerned. The our set of "generation data" comes from three events, i.e. central collisions Pb-Pb generated by the SHAKER code [10] with charged particle rapidity density of dN/dy = 8000 and a pseudo-rapidity region of -1.3 < \( \eta \) < 1.3 (30° < \( \theta \) < 150°). Besides, productions of \( \pi^0 \), \( \eta \) and their decays to two \( \gamma \) were included as well, leading to 38000 charged particles and \( \gamma \) per event. The generation data set consists of about 50,000 single charged particles with a uniform distribution in \( X \) (1000-35000 \( \mu \)m) and in \( Z \) (-105-105 \( \mu \)m). Their initial produced charge distribution is shown in Fig.4. In the detail inside the box, it is shown the same distribution up to 10 mips.

The following step of the simulation takes into account the interaction of the charged particle with the detector and the creation of hole-electron pairs along the particle path inside the SDD. All the tracks are supposed to be normal to the detector surface. So the generated electronic cloud has an initial \( \delta \)-distribution centred at the impact point \((X,Z)\) and focused by the field on the middle plane of the detector (half thickness). The detector is realistically biased, therefore the electronic cloud will migrate towards the anodes facing the impact point. At the same time, the cloud will spread in space, according to the diffusion laws for charge carriers in silicon.

The model chosen for the simulation of this device is the one relating to a linear transimpedance amplifier with semi-gaussian shaper \( RC-CR^* \). The delta response is shown in Eq.2 where \( \eta \) is the shaping time and \( \tau \) the time constant \( RC=CR \):
\[ V(t) = k \frac{r^n}{n!} e^{-\frac{t}{\tau}} \]  

(2)

For \( n=4 \), the correlation efficiency between a gaussian with a spread equal to \( \sigma_{\text{amp}} \) (half of the shaping time) and the CR-RC\( ^4 \) results in 98.7%. Therefore, in the course of the simulation gaussian output signals were considered, allowing shaping time to vary, so as to establish what effects this had on the resolution and on overall efficiency.

4. NOISE EFFECTS

Noise greatly affects the overall readout characteristics. To avoid ghost tracks, simulated by noise, a threshold must be set. This latter increases with noise decreasing efficiency too. Besides resolution, both for charge and position worsens. It is therefore reasonable to reduce noise as much as possible. Due to the power consumption increase, a more efficient cooling system would lead to an increased physical noise caused by the multiple scattering.

The source of noise is localised in: the detector itself, the preamplifier-shaper, the sampling system, and the ADC. The first one is negligible. We can decrease the preamplifier noise adding a suitable filter. In order to achieve a better noise the signal shapes are changed. This fact, in turn, affects both resolutions, efficiency and power consumption. The sampling system, that is the AM generates a noise too. Since it depends essentially on the matching of capacitors inside the system, we use a suitable value already obtained for a dedicated AM [9]. As regards digitalisation we will introduce it as already mentioned in the previous section. The quantization error will be introduced using three different values: 8, 9 and 10 bit.

The problem we want to solve is to find the best filter, and the minimum number of bits compatible with power dissipation.

Noise depends both on design and process parameters. We have chosen for this work a CMOS .8 \( \mu \)m, double-poly, double-metal process. We have investigated all the contributions of noise: flicker (ENC\( f \)), thermal (ENC\( t \)) and shot (ENC\( s \)). The total noise ENC\( \text{tot} \) is given by:

\[ \text{ENC} \text{tot} = \sqrt{\text{ENC}^2_f + \text{ENC}^2_t + \text{ENC}^2_s} \]  

(3)

The first transistor from which the noise essentially depends is a PMOS. The analysis has been performed as in previous papers ([11]) and [12]). We have assigned some parameters as, for instance, the leakage current ILk, the capacitance Cd of the detector and the number of integration. The number of integration \( n \) was chosen as 4 to have a gaussian response and a better noise.

The first attempt to optimise was made without any limitation for \( Ts (Ts = n \tau) \) and \( \tau \) (the time constant of the filter integrator), ID (the bias current of the first transistor and W (first transistor gate width) ranges. A minimum noise of 38 e\(^-\) was achieved. The results are quite paradoxical! Only \( W = 1218 \) \( \mu \)m and \( L = 1 \) \( \mu \)m are reasonable values. Nevertheless the shaping time of 3.2 ns and the ID current of 7.6A are values unrealistic!

A limitation for power reasons has to be introduced, so the ID has to be not more than 100 \( \mu \)A. It means that using 2.75 Vdc for its supply then about 300 \( \mu \)W is its power need.

A new optimisation has led to the results shown in Fig.5: \( W = 61 \) \( \mu \)m is almost independent of \( Ts \). With \( W = 60 \) \( \mu \)m it is possible to reach a minimum noise of about 115 e rms using \( Ts = 60 \) ns (Fig 6).

Taking into account that a filter CR-RC\( ^4 \) gives a quasi-gaussian response, the noise in volts can be calculated in a fixed dynamic range (in our case 2V) starting from the optimised ENC. Finally, a parallel code [13] has been developed to generate the noise in the time domain.

5. EFFICIENCY AND RESOLUTIONS

One of the problems when we try to analyse the simulated data is the cluster localisation inside a noise matrix. The chosen algorithm detects a cluster if two successive samplings of the same channel exceed an optimum threshold. The inefficiency is the number of 'lost' clusters (not identified) over the total number of simulated tracks.
The impact point and the charge released by the particle are reconstructed by means of centre-of-mass method and opportune integration of samplings.

We fixed the preamplifier input/output dynamics, the noise spectrum, the AM uncorrelated noise, and we varied the ADC bit number and the shaping time. Figs.8-11 show the obtained inefficiency and resolutions.

The results show that 9 or 10 bits give comparable performances, while 8 bits are not indicated. The best shaping time is a compromise between the two opposite behaviours of spatial resolutions with respect to the charge resolution. A shaping time of about 50 ns seems to be a good choice, both for inefficiency and for resolutions. A fast shaper response has to be excluded, because of the efficiency deterioration. With higher shaping times there is a light amelioration of efficiency, but there is a degraded charge resolution, especially in the first centimeter. Figs.12-13 show the X distribution of inefficiency and resolutions. A part from scale factors, spatial resolutions behave as shown in Fig.2.
We also performed a preliminary comparison between OLA performances [14] and other realised and/or designed preamplifiers (Gramegna [15], SUPERSBREX [8], PRELUD [16], ALIAS [17]). Table I resumes the characteristics and the obtained results.

6. CONCLUSIONS

We performed a simulation of the ALICE event, the SDD response and the front-end electronics, designing and coding a software to study the variation of efficiency and resolutions when some crucial parameters (ADC bit number, shaping time, etc... ) are modified. We introduced a noise optimisation taking into account the assigned constraint regarding power consumption. The results obtained show that a shaping time of 55 ns and a 9 bit resolution ADC can guarantee good performances, according to the technical proposal requirements.

REFERENCES


<table>
<thead>
<tr>
<th></th>
<th>Shaping time (ns)</th>
<th>ENC (electrons)</th>
<th>Q range (fC)</th>
<th>V range (V)</th>
<th>Inefficiency (%)</th>
<th>X resolution (µm)</th>
<th>Z resolution (µm)</th>
<th>Q resolution (fC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OLA 8bit</td>
<td>55</td>
<td>250</td>
<td>8</td>
<td>0.3</td>
<td>0.37</td>
<td>9.65</td>
<td>10.13</td>
<td>3.28</td>
</tr>
<tr>
<td>OLA 9bit</td>
<td>55</td>
<td>250</td>
<td>8</td>
<td>0.3</td>
<td>0.25</td>
<td>13.9</td>
<td>13.7</td>
<td>3.28</td>
</tr>
<tr>
<td>Gramegna</td>
<td>50</td>
<td>120</td>
<td>50</td>
<td>2</td>
<td>0.4</td>
<td>6.6</td>
<td>8.0</td>
<td>0.36</td>
</tr>
<tr>
<td>SUPERSBREX</td>
<td>20</td>
<td>240</td>
<td>100</td>
<td>0.4</td>
<td>8.85</td>
<td>98.6</td>
<td>98.3</td>
<td>1.42</td>
</tr>
<tr>
<td>PRELUD</td>
<td>15</td>
<td>40</td>
<td>28</td>
<td>2.6</td>
<td>0.4</td>
<td>6.5</td>
<td>8.4</td>
<td>0.92</td>
</tr>
<tr>
<td>ALIAS</td>
<td>55</td>
<td>140</td>
<td>28</td>
<td>1</td>
<td>0.6</td>
<td>6.8</td>
<td>9.7</td>
<td>0.56</td>
</tr>
</tbody>
</table>

TAB. I – Comparison between SDD preamplifiers (realised and/or designed)
FRONT-END ELECTRONICS FOR PARTICLE DETECTION AND DATA COMMUNICATION

F. Giannini, E. Limiti, G. Orengo
Department of Electronic Engineering – University of Roma “Tor Vergata”
email: giannini@elettra.eln.uniroma2.it

Abstract

A family of GaAs monolithic front-end amplifiers, to be used in a large number of applications in present and future radiation detection experimental apparatus, is described in this paper. Design, realization and measurements are presented for MMICs especially designed for front-end circuits in particle detectors as RPC or solid-state detectors, including discriminators, charge amplifiers and logarithmic amplifiers, or front-end receivers in high-speed data communication link as optical front-end amplifiers and cable equalizers.

1. INTRODUCTION

In the future experiments in the field of high energy physics, such as the planned experiments of the Large Hadron Collider (LHC) at CERN, the increasing flux of ionizing particles and the large number of detectors in a small volume will end up being a large flux of data to be processed. The detecting apparatus will require low power, high gain-bandwidth product front-end electronics, easy to serialize, possibly in a custom version, to keep the cost of a large number of channels very low. On the other hand, the communication network that will be handling high transmission rates coming from different sources will require large bandwidths in receiving subsystems. Moreover, this electronics should exhibit low sensitivity to radiation [1].

Beyond the fact that a monolithic approach is necessary to guarantee high yield and repeatability in a large scale production, these requirements are today not completely fulfilled by traditional silicon technology, both in terms of reception and transmission speed, gain performance and power budget [1,2].

In the next sections, different MMIC front-end amplifiers for particle physics readout electronics will be presented, and their design, realization and experimental tests will be described. The types of circuits investigated and realised can be grouped into two main categories: front-ends for particle detectors and optical or cable front-ends for data communications. The circuits have been designed by the Group operating at the University of Roma Tor Vergata and at the National Institute of Nuclear Physics (INFN).

2. PARTICLE DETECTOR FRONT-ENDS

2.2 An 8-Channels Discriminator Front-end

Both for RPC (resistive plate chamber) and solid-state detectors, the pick-up system can be treated as a delay line, when the collection charge time is lower than the propagation time in the pick-up system. A voltage amplifier must be adopted as front-end stage, possibly matched to the low source impedance of the system. As an example, an RPC operating in avalanche mode typically produces a single signal of 5 ns FWHM (Full Width Half Maximum) and 1.5 ns time jitter, while the pick-up propagation time is 15 ns, in a 25 Ω impedance environment [3].

An 8-ch front-end discriminators for application in readout electronics of RPC particle detectors, composed of a high-gain pulse amplifier integrated with a variable threshold comparator and an ECL buffer, have been designed. The chip turns out to be very stable, featuring high voltage gain (>1000), gain-bandwidth product (1011) and sensitivity (~50μV), fast rise time (1.5ns), high trigger time resolution (1ns), and 25mW per channel of power consumption.

The input stage of the front-end is a voltage amplifier; the good time performance of the RPC detectors, utilized for the bunch crossing identification, imposes an amplifier rise time of the order of the RPC jitter time (~1.5ns), because the large fluctuations in signal amplitude of the detector (100μV to 0.5 V) generate a jitter time at the threshold crossing of the order of the pulse rise time. The amplifier frequency response is optimized for typical time structure of the avalanche signal according to the following conditions: 1) same risetime for the amplifier and input signals, which is nearly 1.5 ns; 2) minimum return-to-zero time for the output signal. The resulting frequency response has a maximum at 100 MHz and a 3dB bandwidth of 160 MHz. The amplifier output shows a bipolar shape, as plotted in Fig.1, giving zero integrated charge, thus avoiding a possible dependance of steady output voltage on the counting rate.

The high input impedance $R_I$ of the amplifier has been matched to the low impedance $R_P$ of the pick-up strip teaming the amplifier with a transformer input coupling by means of coaxial air-coupled spiral inductances, since ferrite materials cannot be used in the high intensity magnetic fields of the high energy physics experimental apparatuses.
A comparator is cascaded to the amplifying section to generate a standard positive or negative squared pulse from a bipolar one, with less than 2 ns rise and fall time, as schematized in Fig.1. The threshold value can be regulated to give adequate immunity respect to the noise. The minimum comparator threshold combined with the amplifier gain fixes the minimum detectable signal amplitude. A block diagram of the whole front-end discriminator is shown in Fig.2.

![Fig.1. Front-end response to a triangular-shaped detector output.](image)

From the technological point of view, 20GHz cutoff frequency MESFETs have been chosen for their intrinsic high gain-bandwidth product. Moreover, the GaAs MESFET features the minimum serial-parallel noise at the given frequency band, which is above the 1/f corner. The chip size resulted 1.5x2.3 mm².  

A summary of channel characterization is presented in Figs 3-5. All measurements were performed on an 8-channels full-custom test board by means of a TEK TDS684B digital oscilloscope. Finally, the measured power consumption per channel is lower than 25mW.

![Fig.2. Block diagram of the 8-channel front-end.](image)

![Fig.3. Max. rate performance (100 MHz).](image)

![Fig.4. Output shaping for input pulse variation in width (6-20ns).](image)

![Fig.5. Output jitter time (on the fall) vs input pulse amplitude (0.5-7 mV).](image)

2.2 Charge Amplifying Front-ends

An 0.3μm HEMT-based charge amplifier is presented. The amplifier has been manufactured by the ALENIA Foundry. The function blocks of the amplifier are shown in Fig.6. The input charge preamplifier is followed by an RC-CR filter with two interstage buffers, which assure a better linearity with respect to the single transistor buffer version. Dry etching techniques have been adopted both to increase the feedback resistance of
the charge amplifier up to 100kΩ, so improving the thermal noise, and to change the front-end HEMT device gate length from 1 to 0.2 μm, in order to enable the amplifier to match the 1–10 pF input detector capacitance. Despite of the increased circuit complexity, the chip size is only 2.3x1.5mm², while the total expected power dissipation is less than 5mW. The simulated performances of the front-end are shown in Fig.7, where the frequency behaviour of the open loop voltage gain of the charge preamplifier is plotted, and in Fig.8, where are reported the responses to a voltage step, applied to an input capacitance simulating the detector, of the preamplifier and the RC-CR shaping buffer stages, respectively.

![Fig.6. Block diagram of the charge amp.+ RC-CR shaper](image)

![Fig.7. Simulated open loop voltage gain of the preamplifier.](image)

![Fig.8. Simulated response of the preamp. (CH2) and of the shaper (CH3) to an input voltage step (CH1) (Cdet=5pF).](image)

2.3 A High-Speed Logarithmic Amplifier

The design methodology is based on a parabolic approximation of the ideal logarithmic characteristic yielding a major reduction of the logarithmic error. The amplifier, realised in GaAs 0.5μm MESFET monolithic low-noise technology, features ultra-broadband performance from 0.3 GHz to 5 GHz. A three chips amplifier was assembled utilising a modular strategy, allowing the fulfillment of design goals simply increasing the number of cascaded stages [4].

The circuit has been fabricated entirely in monolithic 0.5 μm MESFET low-noise technology by ALENIA, on a 120μm-thick GaAs substrate. A photograph of the realised chip is reported in Fig.9. The chip dimensions are 2x2 mm².

![Fig.9. Photograph of the realised MMIC chip](image)

In Fig.10 the simulated and measured input-output voltage characteristic for a single stage, at two different frequencies (2 and 0.5 GHz), are reported. Finally, three stages were cascaded and measured. The resulting input/output voltage characteristic is plotted in Fig.11, demonstrating the very good behavior of the "parabolic shaped" true log-amp.

![Fig.10. Single-stage simulated (solid line) and measured input-output voltage characteristics at 0.5 GHz (triangles) and at 2 GHz (crosses)](image)
3. DATA LINK FRONT-ENDS

In a high energy physics experimental apparatus, such as the LHC (Large Hadron Collider) at the CERN of Ginevra, the communication system is characterized by start-stop transmission on a star link topology, connecting different sources, each transmitting at a speed between 0.5 Gbit/s and 1 Gbit/s. Data stream should be 1000 Gbit/s (1000 optical link at 1 Gbit/s). This communication system can be implemented both on fiber or cable links. Fibers show clear advantages for data transmission respect to electrical cables such as lower attenuation, larger distance-bandwidth product, combined with an intrinsic electromagnetic coupling immunity. Despite of the high fabrication, installation and maintenance costs, fibers seems to be the most suitable link for long distances (200 m at least). On the other hand, the possibility of digital data transmission on coaxial cables at high rates (1 Gbit/s) along distances beyond 100m has been successfully attempted, and suggested the development of an MMIC equaliser-amplifier chip, matching different needs with a simple unique technological solution.

3.1 A 1 Gbit/s Optical Front-end

This section reports a MMIC GaAs transimpedance amplifier for optical systems, carried out in collaboration with the Brazilian Telecomm (Telebrás). Operating bandwidth in excess of 2.2 GHz, without the input photodiode parasitic, and a transimpedance gain of 65 dB were achieved; a complete receiver module has been realised and tested with an optical signal in the STM-4 hierarchy at 622.08 MHz [5]. The receiver consists in a first stage for optoelectronic conversion, realised with a PIN diode, and a transimpedance amplifier to obtain a voltage signal from the current generated in the photodiode. After optoelectronic conversion, the signal is fed to a low-pass filter, to eliminate out-of-band thermal and shot noise, and to a limiting amplifier; the last one guarantees a constant output level, independently from the signal variation in the dynamic range of the transimpedance amplifier, drives the decision circuit and the clock recovery circuit. Both outputs are sent to a demultiplexer (1:4) to obtain the STM-1 signal (155 MHz). The block composition of the system is shown in Fig.12.

![Fig.11. Measured input-output characteristics of the cascade of three stages at 2 GHz](image1)

![Fig.12 : Block diagram of the receiver.](image2)

The clock recovery in high rate transmission systems can be realized using non linear circuit as PLL, or, as in our case, band-pass filters employing the SAW technology. The clock recovery block employs a transition detector, acting as a frequency doubler, and a SAW band-pass filter at 622 MHz, producing a sinusoidal signal at the same frequency at the output. The clock signal is introduced together with data signal in the decision circuit. Its topology is basically a D-type Flip-Flop Master/Slave, and its main function is to synchronize data and clock signals to be fed to the demultiplexer. This one can operate alternatively as 1:4 at 622 Mbit/s or 1:16 at 2.5 Gbit/s, compatible with SDH/STM-4 or SDH/STM-16 respectively, and providing 155 Mbit/s output channels.

The eye diagram at the output of the transimpedance amplifier (190 mVpp) is plotted in Fig.13, for an optical signal in the STM-4 hierarchy at 622 MHz NRZ, while Fig.14 shows the signal of an output channel of the demultiplexer at 155 Mb/s and 800 mVpp together with the eye diagram demonstrating a low bit error rate.

![Fig.13: (a) Eye diagram at the output of the optical preamplifier (622 MHz, 190 mVpp)](image3)
after the equaliser-amplifier. Plus 42 m of RG58 coaxial cables. C) Output waveform stream.

Fig. 14: An output channel of the demultiplexer and the corresponding eye diagram (155 Mb/s, 800 mVpp).

3.2 Cable Equalizers

The performance of a coaxial cable depends on its length, and for a distance larger than 10m the most used cables exhibit a disequalised attenuation, which could make the output digital pulses to be "misunderstood" by a threshold device. A simple equalising technique could be based on a receiving device with an opposite gain slope. To behave properly with different cables of different lengths, this solution is required to perform different equalisations.

In order to achieve this features, a new GaAs integrated equalizer-amplifier was designed to match different cable types and lengths by means of a voltage-controlled equalisation procedure [6]. The chip has been fabricated by the Alenia foundry and performs a maximum gain of 24 dB at 1 GHz, while the slope can be varied from 3 dB/dec to 16 dB/dec in the 100-1000 MHz band. The effect of the equaliser-amplifier insertion on a cable transmission link in the worst conditions has been reported in Fig. 15. The original bit sequence has been recovered, although inverted, and complementary bit recognition is still allowed.

Fig.15. A) Input waveform for a 500 Mb/s NRZ bit stream. B) Output waveform after 100m of C-0-12 SAT plus 42 m of RG58 coaxial cables. C) Output waveform after the equaliser-amplifier.

CONCLUSIONS

The reported results, extracted from the ones related to more than thirty different MMICs designed at the University of Roma Tor Vergata, demonstrated the effectiveness of the approach and the success of the particular effort, devoted to the establishment of a design and testing capability in the field of very high frequency integrated microelectronics.

Moreover, the feasibility of the GaAs monolithic integrated solution as an effective way to solve some of the many problems arising from the new high energy physics experiments, was also demonstrated.

REFERENCES

<table>
<thead>
<tr>
<th>PARTICIPANT</th>
<th>INSTITUTION</th>
<th>ADDRESS</th>
<th>EMAIL</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANTREASYAN Dikran</td>
<td>LeCroy</td>
<td>2, rue du Pré de la Fontaine CH-1217 Meyrin Switzerland</td>
<td><a href="mailto:antreasvan@lecroy.com">antreasvan@lecroy.com</a></td>
</tr>
<tr>
<td>ARTAMONOV Alexey</td>
<td>Specialized Electronic Systems</td>
<td>Kashirskoe Shosse, 31 RU-115 409 Moscow Russia</td>
<td><a href="mailto:Artusm@spels.msm.ru">Artusm@spels.msm.ru</a></td>
</tr>
<tr>
<td>ATKIN Eduard</td>
<td>Moscow Engineering Physics Institute</td>
<td>Department of Electronics Kashirskoe Shosse, 31 RU-115 409 Moscow Russia</td>
<td><a href="mailto:Atkin@eldep.mephi.ru">Atkin@eldep.mephi.ru</a></td>
</tr>
<tr>
<td>BACCHETTA Nicola</td>
<td>INFN Sezione di Padova</td>
<td>Via Marzolo, 8 I-35131 Padova Italy</td>
<td><a href="mailto:Nicola.Bacchetta@pd.infn.it">Nicola.Bacchetta@pd.infn.it</a></td>
</tr>
<tr>
<td>BAUR Roland</td>
<td>Paul Scherrer Institut</td>
<td>Würenlingen und Villigen CH-5232 Villingen Switzerland</td>
<td><a href="mailto:Roland.Baur@psi.ch">Roland.Baur@psi.ch</a></td>
</tr>
<tr>
<td>BEAUMONT Wim</td>
<td>Physics Department</td>
<td>Universitaire Instellin Antwerpen Universiteitsplein 1 B-2610 Wilrijk (Antwerpen) Belgium</td>
<td><a href="mailto:Wim.Beaumont@uia.ua.ac.be">Wim.Beaumont@uia.ua.ac.be</a></td>
</tr>
<tr>
<td>BERGLUND Svante</td>
<td>Physics Department</td>
<td>University of Stockholm Vanadisvägen 9 S-113 46 Stockholm Sweden</td>
<td><a href="mailto:svan@physito.se">svan@physito.se</a></td>
</tr>
<tr>
<td>BERTELSEN Henrick</td>
<td>Niels Bohr Institute</td>
<td>University of Copenhagen Blegdamsvej, 17 DK-2100 Copenhagen Denmark</td>
<td><a href="mailto:bertelsen@nbi.dk">bertelsen@nbi.dk</a></td>
</tr>
<tr>
<td>BERTUCCIO Giuseppe</td>
<td>Politecnico di Milano</td>
<td>Dipartimento di Elettronica Piazza L. da Vinci, 32 I-20133 Milano Italy</td>
<td><a href="mailto:Bertucci@elet.polimi.it">Bertucci@elet.polimi.it</a></td>
</tr>
<tr>
<td>BISOGNI M. Giuseppina</td>
<td>INFN Sezione di Pisa</td>
<td>Laboratorio di San Piero Via Livornese 1291 I-56010 San Piero a Grado (PI) Italy</td>
<td><a href="mailto:Bisogni@pisa.infn.it">Bisogni@pisa.infn.it</a></td>
</tr>
<tr>
<td>BLANQUART Laurent</td>
<td>Centre de Physique des Particules de Marseille - IN2P3</td>
<td>163, avenue de Luminy Case 907 F-13288 Marseille Cedex 09</td>
<td><a href="mailto:blanquart@crppm.in2p3.fr">blanquart@crppm.in2p3.fr</a></td>
</tr>
<tr>
<td>BOCCI Valerio</td>
<td>Dipartimento di Fisica - INFN</td>
<td>Università di Roma I &quot;La Sapienza&quot; Piazzale Aldo Moro, 2 I-00185 Roma Italy</td>
<td><a href="mailto:Valerio.Bocci@Roma1.infn.it">Valerio.Bocci@Roma1.infn.it</a></td>
</tr>
<tr>
<td>BOERMANN Christian</td>
<td>Physics Department</td>
<td>University of Stockholm Vanadisvägen 9 S-113 46 Stockholm Sweden</td>
<td><a href="mailto:bohm@physito.se">bohm@physito.se</a></td>
</tr>
<tr>
<td>BORGAUD Pierre</td>
<td>CEA/DSM/DAPNIA</td>
<td>Centre d'Etudes de Saclay F-91191 Gif-sur-Yvette Cedex France</td>
<td><a href="mailto:Borgaud@hep.saclay.cea.fr">Borgaud@hep.saclay.cea.fr</a></td>
</tr>
<tr>
<td>BORGIAPA Bruno</td>
<td>Dipartimento di Fisica</td>
<td>Università di Roma I &quot;La Sapienza&quot; Piazzale Aldo Moro, 2 I-00185 Roma Italy</td>
<td><a href="mailto:Bruno.Borgia@Roma1.infn.it">Bruno.Borgia@Roma1.infn.it</a></td>
</tr>
<tr>
<td>BOUCHERAT Gilles</td>
<td>Thomson-CSF</td>
<td>Semiconducteurs Spéciqques B.P. 123 F-38521 Saint-Egrève France</td>
<td><a href="mailto:Gilles.Boucherat@sc.thomson-csf.fr">Gilles.Boucherat@sc.thomson-csf.fr</a></td>
</tr>
<tr>
<td>BOUCHARLAT Gilles</td>
<td>INFN, Sezione di Catania</td>
<td>Dipartimento di Fisica dell'Università 57, Corso Italia I-95129 Catania Italy</td>
<td><a href="mailto:caponetto@sally.ct.infn.it">caponetto@sally.ct.infn.it</a></td>
</tr>
<tr>
<td>BOUROV Serguei</td>
<td>DESY</td>
<td>H1 Notkestrasse 85 D-22603 Hamburg Germany</td>
<td><a href="mailto:burov@mail.desy.de">burov@mail.desy.de</a></td>
</tr>
<tr>
<td>BOUVIER Stéphane</td>
<td>SUBATECH</td>
<td>La Chantrerie Rue A. Kastler B.P. 20722 F-44307 Nantes France</td>
<td><a href="mailto:Bouvier@subatech.in2p3.fr">Bouvier@subatech.in2p3.fr</a></td>
</tr>
<tr>
<td>BRETON Dominique</td>
<td>Laboratoire de l'Accelerateur Linéaire</td>
<td>F-91405 Orsay Cedex France</td>
<td><a href="mailto:breton@lalcls.in2p3.fr">breton@lalcls.in2p3.fr</a></td>
</tr>
<tr>
<td>BRETEL Horst</td>
<td>Max-Planck Institut Für Physik</td>
<td>Föhringer Ring 6 D-80805 München Germany</td>
<td><a href="mailto:bretel@mppmu.mpg.de">bretel@mppmu.mpg.de</a></td>
</tr>
<tr>
<td>BURCKHART Helfried</td>
<td>CERN</td>
<td>EP Division CH-1211 Geneva 23 Switzerland</td>
<td><a href="mailto:Helfried.Burckhart@cern.ch">Helfried.Burckhart@cern.ch</a></td>
</tr>
<tr>
<td>BUSSAT Jean-Marie</td>
<td>Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP) B.P. 110 Chemin de Bellevue F-74941 Annecy-le-Vieux Cedex France</td>
<td><a href="mailto:bussat@lapp.in2p3.fr">bussat@lapp.in2p3.fr</a></td>
<td></td>
</tr>
<tr>
<td>BUYTAERT Jan</td>
<td>CERN</td>
<td>EP Division CH-1211 Geneva 23 Switzerland</td>
<td><a href="mailto:Jan.Buytaert@cern.ch">Jan.Buytaert@cern.ch</a></td>
</tr>
<tr>
<td>CAPONETTO Luigi</td>
<td>INFN, Sezione di Catania</td>
<td>Dipartimento di Fisica dell'Università 57, Corso Italia I-95129 Catania Italy</td>
<td><a href="mailto:caponeto@sally.ct.infn.it">caponeto@sally.ct.infn.it</a></td>
</tr>
</tbody>
</table>
CESARONI Federico
Dipartimento di Fisica
Università di Lecce
Via per Monteroni
I-73100 Lecce
Italy
cesaroni@le.infn.it

CHUMAKOV Alexander
Specialized Electronic Systems
Kashirskoe Shosse 31
RU-115 409 Moscow
Russia
aichum@spets.msk.ru

CIRIO Roberto
INFN Sezione di Torino
Via Pietro Giuria, 1
I-10125 Torino
Italy
Cirio@to.infn.it

CITTOLIN Sergio
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Sergio.Cittolin@cern.ch

CORBIERE Thierry
TEMIC / MHS S.A.
La Chantrerie
B.P. 70602
F-44306 Nantes Cedex 03
France
Thierry.Corbiere@temic.fr

CORSI Francesco
Dipartimento di Elettronica
Politecnico di Bari
Via Orabona, 4
I-70125 Bari
Italy
corsi@ba.infn.it

CRANFIELD Robert
Physics Department
University College London
Gower Street
London WC1E 6BT
United Kingdom
rc@hep.ucl.ac.uk

CRETI Pietro
INFN Dipartimento di Fisica
Università di Lecce
Via per Arnesano
I-73100 Lecce
Italy
creti@le.infn.it

CROS Philippe
Laboratoire de l'Accélérateur Linéaire
F-91405 Orsay Cedex
France
cros@lal.in2p3.fr

CSATÓ Péter
KFKI - RMKI
Konkoly Thege Miklós út 29-33
P.O. Box 49
H-1525 Budapest 114
Hungary
p.csato@rmki.kfki.hu

DABROWSKI Wladyslaw
Faculty Physics & Nuclear Techniques
University of Mining & Metallurgy
Aleja Mickiewicza 30
PL-30 055 Kraków 30
Poland
W.Dabrowski@fti.agh.edu.pl

de la TAILLE Christophe
Laboratoire de l'Accélérateur Linéaire
B.P. 34
F-91898 Orsay Cedex
France
taille@lal.in2p3.fr

DE PEDIS Daniele
Dipartimento di Fisica - INFN
Università di Roma I "La Sapienza"
Piazzale Aldo Moro, 2
I-00185 Roma
Italy
Daniele.DePedis@Roma1.infn.it

DE VENUTO Daniela
Dipartimento Scienza dei Materiali
Facoltà di Ingegneria
Via per Monteroni
I-73100 Lecce
Italy
Daniela.Devenuto@poliba.it

DELL'ORSO Mauro
Dipartimento di Fisica
Università degli Studi di Pisa
Piazza Torricelli, 2
I-56100 Pisa
Italy
Mauro.Dell'orso@pi.infn.it

DÉNES Ervin
KFKI
Konkoly Thege Miklós út 29-33
P.O. Box 49
H-1525 Budapest 114
Hungary
Ervin.Denes@cern.ch

DENES Peter
Physics Department
Princeton University
Princeton, NJ 08544
United States of America
Peter.Denes@cern.ch

DENTAN Martin
CEA/DSM/DAFNA
Centre d'Etudes de Saclay
F-91191 Gif-sur-Yvette Cedex
France
dentan@hep.saclay.cea.fr

DEWULF Jean-Paul
Physics Department
University of Bruxelles ULB
Boulevard du Triomphe C.P. 230
B-1050 Bruxelles
Belgium
dewulf@hep.ihe.ac.be

DINKESPILER Bernard
Centre de Physique des Particules
de Marseille - IN2P3
163, avenue de Luminy Case 907
F-13288 Marseille Cedex 09
France
Dinkespiler@cppm.in2p3.fr

DOÇSATS Peter
KFKI - RMKI
Konkoly Thege Miklós út 29-33
P.O. Box 49
H-1525 Budapest 114
Hungary
p.csato@rmki.kfki.hu

DURIEZ Eric
Dassault Electronique
Quai Marcel Dassault 55
F-92214 St.-Cloud Cedex
France
Eric.Duriez@dassault-elec.fr

EGED Bertalan
Technical University of Budapest
Goldmann ter 3
H-1111 Budapest
Hungary
Bertalan.Eged@cti.hu

EISENHANDLER Eric
Physics Department
Queen Mary & Westfield College
Mile End Road
London E1 4NS
United Kingdom
e.eisenhandler@qmw.ac.uk

ELIAS John
Fermi National Accelerator Laboratory
P.O. Box 500
Wilson Road
Batavia, IL 60510
United States of America
Elias@fnal.gov

FACCIO Federico
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Federico.Faccio@cern.ch

FALCIANO Speranza
Dipartimento di Fisica - INFN
Università di Roma I "La Sapienza"
Piazzale Aldo Moro, 2
I-00185 Roma
Italy
Speranza.Falci@roma1.infn.it

FALCIANO Speranza
Dipartimento di Fisica - INFN
Università di Roma I "La Sapienza"
Piazzale Aldo Moro, 2
I-00185 Roma
Italy
Speranza.Falci@roma1.infn.it
FANTECHI Riccardo
INFN Sezione di Pisa
Laboratorio di San Piero
Via Livornese 1291
I-56010 San Piero a Grado (Pi)
Italy
Riccardo.Fantechi@cern.ch

FARTHOUAT Philippe
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Philippe.Farthouat@cern.ch

FELICI Giulietto
Laboratori Nazionali di Frascati
INFN
Via Enrico Fermi, 40
I-00044 Frascati
Italy
felici@lnf.infn.it

FEUERSTACK-RAIBLE Martin
Physics Department
Ruprecht-Karls University
Schödterstrasse 90
D-69120 Heidelberg
Germany
feuerstack@physi.uni-heidelberg.de

FISCHER Horst
Physics Department
University Freiburg FRG
Hermann-Heider-Strasse 3
D-79104 Freiburg
Germany
Horst.Fischer@cern.ch

FORMENTI Fabio
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Fabio.Formenti@cern.ch

FRENCH Marcus
Rutherford Appleton Laboratory
Chilton
Didcot OX11 0QX
United Kingdom
m.french@r1.ac.uk

GALLNO Per Gunnar
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Per.Gunnar.Gallno@cern.ch

GERENCSER István
Technical University of Budapest
Goldmann ter 3
H-1111 Budapest
Hungary
gelpisti@sirkan.sch.mne.hu

GEMMEKE Hartmut
Forschungszentrum Karlsruhe
Postfach 36 40
76021 Karlsruhe
Germany
Hartmut.Gemmeke@fzkarlsruhe.de

GENOLINI Bernard
Institut de Physique Nuclaire
Rue G. Clemenceau 15
F-91406 Orsay
France
Bernard.Genolini@ipno.in2p3.fr

GILL Karl
CERN
EP Division
CH-1211 Geneva 23
Switzerland
gill@mail.cern.ch

GIRALDO Andrea
INFN Sezione di Padova
Via Marzolo, 8
I-35131 Padova
Italy
Andrea.Giraldo@pd.infn.it

GOLDSHER Abram
State Scientific Research Institute
"Pulsar"
Okruzhnoy proezd 27
RU-105 187 Moscow
Russia
root@pulsar.msk.su

GOORENS Robert
Physics Department
Vrije Universiteit Brussels
B-1050 Bruxelles
Belgium
Goorens@hep.thc.ac.be

GRASSI Tulio
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Tulio.Grassi@cern.ch

GREEN Barry
Physics Department
Royal HollowayUniversity of London
Egham Hill
Egham TW20 0EX
United Kingdom
b.green@rhbc.ac.uk

GRIECO Giovanni
CAEN S.p.A.
Via Vetreria 11
I-50049 Viareggio
Italy
Grieco@caen.it

GRILLO Alexander
Santa Cruz Institute for Particle Physics (SCIPP)
1156 High Street
Santa Cruz, CA 95064
United States of America
grillo@scipp.ucsc.edu

HALL Geoff
Blackett Laboratory
Imperial College
Prince Consort Road
London SW7 2BZ
United Kingdom
g.hall@ic.ac.uk

HALLGREN Bjorn
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Bjorn.Hallgren@cern.ch

HAMEL Maurizio
LABEN S.p.A.
Strada statale padana superiore 290
I-20090 Vimodrone (MI)
Italy
m.hamele@laben.it

HANSEN Finn
Niels Bohr Institute
University of Copenhagen
Blegdamsvej, 17
DK-2100 Copenhagen
Denmark
fhansen@nbi.dk

HEINE Eric
NIKHEF
Kruislaan,409
P.O. Box 41882
NL-1009 DB Amsterdam
Netherlands
eriche@nikhef.nl

HENRARD Jean-Claude
ALCATEL SDM
P.O.Box 4205
B-6000 Charleroi
Belgium
henrard.jc@etca.alcatel.be

HOCHELWELLER Gerd
DESY
Notkestrasse 85
D-22603 Hamburg
Germany
Gerd.Hochweller@desy.de

HOFFMANN Hans Falk
CERN
EP Division
CH-1211 Geneva 23
Switzerland
Hans.Falk.Hoffmann@cern.ch
INDEX

A

Abbot, P. 79
Aguiar, C. 96, 344
AhKabay, B.A. 486
Alberici, G. 151
Alfredsson, S. 604
Ambrosini, G. 387
Amend, W. 165
Anderson, K. 239, 246
Andrieux, M.-L. 364, 470
Anelli, G. 175, 569
Aphanisi, F. 180
Antinori, F. 331
Arbet-Engels, V. 96, 344
Arnold, L. 170
Artamonov, A.S. 471, 480
Atkin, E. 550, 555
Augé, E. 207
Ayachi, M. 160
Azevedo, C. 96, 344

B

Bacc, C. 269
Bageott, W. 321
Baechler, J. 165
Bailey, D.S. 326
Bailly, P. 456
Ban, J. 207, 234
Bardi, A. 407
Batten, J. 96
Baudot, G. 170
Bauer, C. 538
Baumhauer, A. 250
Baur, R. 140
Becciani, U. 610
Bec, H.-P. 387
Beker, H. 331
Bellforte, S. 407
Benedetto, J.M. 533
Berglund, S. 239, 246
Beret, J.-C. 165
Berst, J.D. 160, 170, 180
Bertuccio, G. 581
Binkley, M. 250
Bisogni, M.G. 339
Blanc, J.P. 79
Blanchot, G. 239
Blankart, L. 133
Blondé, P. 160, 170
Bloodworth, I.J. 331
Bo, Z. 456
Bohn, C. 239, 246, 311, 316
Bonazzola, G.C. 151
Boorman, G. 397
Borgeaud, P. 79, 180
Boterenbrood, H. 397
Boucham, A. 170
Bouchart, G. 543
Bouvier, S. 160, 170, 511
Braun, G. 564
Breton, D. 207
Bretel, H. 234
Bright, Thomas, P. 311, 316
Brosch, O. 402
Burckhart, H.J. 19, 423
Burns, M. 114

C

Calin, T. 105
Calvet, D. 133
Campbell, D. 175
Campbell, M. 105, 114
Cancelo, G. 528
Cantatore, E. 114
Carcaud, M. 79
Cardarelli, R. 269
Carl, R. 538
Castiglia, N. 207
Caruso, S. 431
Castellani, L. 285
Cavagnino, D. 151
Cavalli-Sforza, M. 239
Ceradini, F. 269
Cervelli, G. 96, 344
Cetin, S. 387
Charlton, D.G. 349, 354, 359
Chaupet, J. 543
Chauveaux, J. 456
Chen, X.Y. 250
Chisari, M. 581
Christian, D. 528, 599
Christiansson, T. 165
Chumakov, A.I. 471, 476
Ciuperti, G. 269
Cistermino, A. 514
Clark, A. 175
Clauss, G. 160, 170
Coffin, J.P. 170
Cola, A. 339
Colas, J. 213
Collaged, C. 160, 170
Conka, T. 387
Connors, A. 311, 316
Conti, M. 339
Corbière, T. 79
Corre, A. 275
Corsi, F. 145
Couscoulia, J. 105
Coulon, J.P. 213
Cranfield, R. 397
Croix, J. 180
Crone, G. 397
Cros, P. 207
Crosetto, D. 517
Ctôô, P. 369, 508
Cunlitz, H. 207
Cwienk, W.D. 234

D

Dabrowski, W. 175, 569
Dachs, C. 431
Dallavalle, G.M. 291, 294
Dantez, A. 79
D’Antone, I. 291, 294
Dasu, S. 321
D’Aviria, L. 514
De Giorgi, M. 285
de La Taille, C. 213
De Pedis, D. 468
de Pontcharra, J. 79
de Remigis, P. 151
De Venuto, D. 145
Delagnes, E. 79, 207
Delevoe-Osiris, E. 79
Dell’Orso, M. 407
Delmasino, M. 105
Dénes, E. 369, 508
Denes, P. 223
Denta, M. 79
Deppe, H. 538
Deptuch, G. 160, 170, 180
Detcheverry, C. 119, 431
Di Ciaccio, A. 269
Dillinger, P. 402
Dinapoli, R. 114
Dinkespalier, B. 364, 470
Donati, P. 165
Doran, D. 175
Dowell, J.D. 349, 354, 359
Dravet, A. 602
Dubbs, T. 175
Dulinski, W. 160, 170
Dupanloup, M. 180

E

Edwards, J. 311, 316
Eged, B. 369, 503, 589
Egorov, A.N. 471
Einweiler, K. 131
Eisenhandler, E. 47, 311, 316
Elias, J.E. 250
Ellis, N. 275
Engst, C. 165
Engström, M. 311, 316
Errico, W. 407, 514
Estev Bosch, R. 165
Evans, D. 331
Evans, G. 364

F

Faccio, F. 105, 114, 119, 374
Fallot-Burghardt, W. 538
Fantacci, M.E. 339
Gachelin, O. 397
Galeotti, S. 407
Gallina, P. 581
Gallina-Martel, L. 364
Gannon, W. 175
Gara, A. 207
Gardien, S. 180
Garvey, J. 311, 316
Gee, C.N.P. 311, 316
Gelencsér, I. 369, 503, 589
Gemmeke, H. 560
Genat, J.-F. 456
Geweniger, C. 311
Giannessi, P. 407
Giannini, F. 615
Gill, K. 96, 344
Gillman, A.R. 311, 316
Gingrich, D. 207
Giovannetti, S. 584
Giraldo, A. 105
Giubellino, P. 151
Glass, B. 538
Goertler, U. 180
Goldshuer, A.I. 545
Gonella, F. 257
Grabit, R. 96, 344
Grasella, P. 569
Green, B. 397
Greco, G.M. 439
Grillo, A. 175
Grüneauier, A. 564
Guehrard, J.M. 79
Guillemette, G. 170
Guo, C. 180

Haller, B. 423
Hancock, P. 311, 316
Hansen, S. 250
Hatley, R. 311, 316
Hausmann, S. 538
Havet, C. 275
Hazen, E. 440
Heath, G.P. 326
Hébrard, L. 160, 170
Heering, A. 100
Heidari, B. 604
Heijne, E. 114
Heinsius, F.H. 564
Hellmann, S. 311, 316
Hernandez, R. 151
Hewlett, J. 207
Higuieret, S. 170
Hillier, S. 311, 316
Hoff, J. 528
Hoffmann, C. 180
Hoffmann, H.F. 61
Hoghe Nien, F. 387
Holmes-Seidel, A. 91
Holmgren, S-O. 239, 246
Homer, R.J. 349, 354, 359
Homl, L. 207
Homma, K. 280
Horisberger, R. 140
Hu, Y. 160, 170, 180, 452
Huettel, M. 397
Huhtinen, M. 119
Humphreys, J. 68
Huppert, J.-F. 456
Huth, J. 440

Ilyushchenko, I. 550

Jaeg, R. 180
Jakobs, K. 311, 316
Jansweijer, P. 397
Janvier, N. 543
Jarron, P. 7, 105, 114, 175, 431, 569
Jaworski, M. 321
Jensen, F. 96, 344
Jon-And, K. 239, 246
Jones, G.T. 331
Jones, L.L. 185, 190
Joos, M. 387
Joshi, A. 131
Jovanovic, P. 331, 359
Jundt, F. 170
Junno, B. 604
Jusko, A. 331

Kalashnikov, O.A. 484
Kano, H. 280

Kaplon, J. 175, 569
Karpinski, W. 86
Kenyon, I.R. 349, 354, 359
Kerwin, D.B. 533
Klopopov, P. 550
Kieft, G. 397
Kinson, J.B. 331
Kirk, A. 331
Kiryanin, A. 234
Kiss, T. 369, 498, 503
Kleinfielder, S. 131
Kleereborn, J. 246
Klinger, V. 560
Kloukinas, K. 105, 574
Kluge, E.E. 311, 316
Kluit, R. 201, 538
Knöpfle, K.-T. 538
Kooper, B. 331
Koehler, E. 165
Kolovutari, A. 331
Kondratenko, S. 550, 555
Königsmann, K. 564
Kormesser, K. 402
Kôtz, U. 538
Krälik, I. 331
Kucewicz, W. 160, 170
Kuchersky, V. 545
Kugel, A. 397, 402
Kuhn, C. 170
Kundu, N. 175
Kuprianov, E. 550
Kurchaninov, L. 234
Kwan, S. 599

La Marra, D. 165, 175
Lacasta, C. 175, 569
Lacava, F. 269
Lachartre, D. 79, 180
Lackey, J. 321
Lambin, J. 326
Landon, M. 311, 316
Lankford, A.J. 383
Lanza, A. 440
Lax, I. 291
Lay, R. 402
Le Du, P. 397
Le Mouelic, C. 79
Le, T.-D. 180
Lebolo, H. 456
Lechner, M. 140
Leger, A. 407
Legrand, J.-C. 165, 602
Lehmann, G. 387
Lenti, V. 331
Leonardi, S. 431
Leray, J.L. 79
Leroux, C. 79
Levinson, L. 280, 402
Lichard, P. 393
Limiti, E. 615
Ling, T.Y. 262
Lippi, I. 285
Lo Nigro, L. 606
<table>
<thead>
<tr>
<th>T</th>
<th>U</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tang,F.</td>
<td>Unel,G.</td>
</tr>
<tr>
<td>Tarchini,A.</td>
<td>Urban,H.J.</td>
</tr>
<tr>
<td>Tafján,D.</td>
<td>Urban,M.</td>
</tr>
<tr>
<td>Tarle,J.-C.</td>
<td></td>
</tr>
<tr>
<td>Tchermiakhovski,D.</td>
<td></td>
</tr>
<tr>
<td>Telegdy,A.</td>
<td></td>
</tr>
<tr>
<td>Thompson,M.</td>
<td></td>
</tr>
<tr>
<td>Tocut,V.</td>
<td></td>
</tr>
<tr>
<td>Tofil,T.</td>
<td></td>
</tr>
<tr>
<td>Tomasicchio,G.</td>
<td></td>
</tr>
<tr>
<td>Torrieri,G.D.</td>
<td></td>
</tr>
<tr>
<td>Torromeo,G.</td>
<td></td>
</tr>
<tr>
<td>Tosello,F.</td>
<td></td>
</tr>
<tr>
<td>Trembllet,L.</td>
<td></td>
</tr>
<tr>
<td>Tripicione,R.</td>
<td></td>
</tr>
<tr>
<td>Troksa,J.</td>
<td></td>
</tr>
<tr>
<td>Truche,R.</td>
<td></td>
</tr>
<tr>
<td>Trunk,U.</td>
<td></td>
</tr>
<tr>
<td>Tschirhart,R.</td>
<td></td>
</tr>
<tr>
<td>Turchetta,R.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>van den Brand,J.</td>
</tr>
<tr>
<td>van der Bij,E.</td>
</tr>
<tr>
<td>Vande Vyvre,P.</td>
</tr>
<tr>
<td>Varnari,R.</td>
</tr>
<tr>
<td>Vascootta,A.</td>
</tr>
<tr>
<td>Vasey,F.</td>
</tr>
<tr>
<td>Veillet,J.-J.</td>
</tr>
<tr>
<td>Velazco,R.</td>
</tr>
<tr>
<td>Veneziano,S.</td>
</tr>
<tr>
<td>Vermeulen,J.</td>
</tr>
<tr>
<td>Vesztergombi Jr.,G.</td>
</tr>
<tr>
<td>Vesztergombi,G.</td>
</tr>
<tr>
<td>Villalobos Baillie,O.</td>
</tr>
<tr>
<td>Vissi,B.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Walder,J.-P.</td>
</tr>
<tr>
<td>Wastie,R.L.</td>
</tr>
<tr>
<td>Watkins,P.</td>
</tr>
<tr>
<td>Watson,A.</td>
</tr>
<tr>
<td>Watts,S.J.</td>
</tr>
<tr>
<td>Weidberg,A.R.</td>
</tr>
<tr>
<td>Weilhammer,P.</td>
</tr>
<tr>
<td>White,D.J.</td>
</tr>
<tr>
<td>Wikstrom,B.</td>
</tr>
<tr>
<td>Wilmott,C.</td>
</tr>
<tr>
<td>Wilson,J.A.</td>
</tr>
<tr>
<td>Wingerter-Seez,I.</td>
</tr>
<tr>
<td>Witzmann,T.</td>
</tr>
<tr>
<td>Wolter,M.</td>
</tr>
<tr>
<td>Wrochna,G.</td>
</tr>
<tr>
<td>Wu,S.</td>
</tr>
<tr>
<td>Wu,X.</td>
</tr>
<tr>
<td>Wunsh,M.</td>
</tr>
<tr>
<td>Wyllie,K.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yanenko,A.V.</td>
</tr>
<tr>
<td>Yarema,R.</td>
</tr>
<tr>
<td>Ye,J.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zanello,L.</td>
</tr>
<tr>
<td>Zavada,P.</td>
</tr>
<tr>
<td>Zhukov,V.</td>
</tr>
<tr>
<td>Zimmermann,T.</td>
</tr>
<tr>
<td>Zimmermann,S.</td>
</tr>
<tr>
<td>Zotto,P.</td>
</tr>
<tr>
<td>Zsenei,A.</td>
</tr>
</tbody>
</table>