Large Hadron Collider Project

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Improved Turn-on Characteristics of Fast High Current Thyristors

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Abstract

The beam dumping system of CERN's Large Hadron Collider (LHC) is equipped with fast solid state closing switches, designed for a hold-off voltage of 30 kV and a quasi half sine wave current of 20 kA, with 3 μ s rise time, a maximum di/dt of 12 kA/ μ s and 2 μ s fall time. The design repetition rate is 20 s. The switch is composed of ten Fast High Current Thyristors (FHCT's), which are modified *symmetric* 4.5 kV GTO thyristors of WESTCODE.

Recent studies aiming at improving the turn-on delay, switching speed and at decreasing the switch losses, have led to test an *asymmetric* not fully optimised GTO thyristor of WESTCODE and an optimised device of GEC PLESSEY Semiconductor (GPS), GB. The GPS FHCT, which gave the best results, is a non irradiated device of 64 mm diameter with a hold-off voltage of 4.5 kV like the *symmetric* FHCT. Tests results of the GPS FHCT show a reduction in turn-on delay of 40 % and in switching losses of almost 50 % with respect to the *symmetric* FHCT of WESTCODE. The GPS device can sustain an important reverse current during a short period. This eliminates the need for an anti-parallel diode stack in the final switch. Extrapolation of the test results onto the final switch result in a turn-on delay of 600 ns and 6 J total conduction losses from turn-on to 20 kA peak current.

Further tests on the GPS FHCT at 4.4 kV, 60 kA peak current and a repetition rate of 10 s resulted in a di/dt of 50 kA/ μ s with a turn-on delay of 700 ns.

These encouraging results, obtained with a slightly modified standard device and based on several hundred thousand discharges, open a wide field of fast high current, high voltage applications where presently thyratrons and ignitrons are used.

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Abstract

The beam dumping system of CERN's Large Hadron Collider (LHC) is equipped with fast solid state closing switches [1], designed for a hold-off voltage of 30 kV and a quasi half sine wave current of 20 kA, with 3 μ s rise time, a maximum di/dt of 12 kA/ μ s and 2 μ s fall time. The design repetition rate is 20 s. The switch is composed of ten Fast High Current Thyristors (FHCT's), which are modified *symmetric* 4.5 kV GTO thyristors of WESTCODE.

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Introduction

Because of their extremely low self-firing hazard, no power consumption during the ready-to-go status, instantaneous availability, simple condition control, very low noise emission during soft turn-on switching and easy maintenance Fast High Current Thyristors (FHCT's) are used in the discharge switch of the extraction kicker pulse generator of CERN's Large Hadron Collider (LHC) [1]. The first prototype switch was made of 10 modified 4.5 kV, 66 mm *symmetric* GTO's, connected in series. It holds off a d.c. voltage of 30 kV and conducts a 5 μ s half-sine wave current of 20 kA with an initial di/dt of 12 kA/ μ s. This switch has been tested with 70×10^3 discharges at a peak current of 30 kA and with more than

100×10^3 discharges at a peak current of 20 kA at a repetition rate of 15 s.

The *symmetric* 4.5 kV FHCT has an action integral of $1300 \times 10^3 \text{ A}^2 \text{ s}$ for a 10 msec half sine wave pulse. The cathode n-layer of 20 μ m thickness, the gate p-layer and the p-base layer of 50 μ m are diffused on the main n-layer wafer, which has a thickness of 1.25 mm. The p-base layer is alloyed on a 4 mm thick molybdenum disk for high thermal capacity. Disadvantages of the thick silicon wafer are a long turn-on delay t_d and high switching losses. Conventional *asymmetric* 4.5 kV GTO's have a free-floating silicon wafer with thickness of about 800 μ m resulting in improved switching behaviour. This has led to test a *asymmetric* non optimised FHCT of WESTCODE and an optimised FHCT of GPS (GPS was recently acquired by MITEC Semiconductor, Canada).

The optimised fast hard gate driven GPS device of 64 mm diameter has a peak off-state voltage V_{DRM} of 4.5 kV and a peak reverse voltage V_{RRM} of 16 V. The 10 msec half sine wave pulse integral amounts to $1280 \times 10^3 \text{ A}^2 \text{ s}$. This device is well known for its high service reliability. The quoted wafer thickness is 730 μ m which is a 42 % reduction with respect to the silicon thickness of the *symmetric* FHCT and about 100 μ m thinner than conventional 4.5 kV GTO's. The total GPS gate-cathode boundary line is 7.4 m. The WESTCODE FHCT's use a ring gate-cathode structure while the GPS FHCT has a center gate contact.

Test circuit

Fig. 1 shows the test set-up for testing the *asymmetric* FHCT's and Fig. 2 the equivalent circuit. Principle test parameters are: peak gate current I_{GM} , rate of rise of gate current di_g/dt , peak anode current I_{AM} ,

Fig. 1 Test set-up rate of rise of anode current di_A/dt and the dynamic anode-cathode voltage V_A .

Fig. 2 Basic test circuit diagram

The FHCT is mounted on the central axis of the set-up. It is connected via a vertical rod to a metallic disk, onto which 4 discharge capacitors C are connected in parallel. A STANGENES current monitor is mounted over the center rod. The capacitors are units of $4\ \mu\text{F}$, type GT1853, NCL, GB and are charged from 2 to 4.4 kV. The circuit stray inductance L can be adjusted to $<100\text{nH}$ by changing the position of the metallic connection disk as shown in Fig. 1. The anti-parallel diode D consisted of 4 parallel 4.5 kV elements, type GPS, DF67545-5536A, mounted close to the FHCT with minimum loop inductance. It appeared quite quickly that the negative oscillating sine wave current was not transferred from the *asymmetric* devices to the anti-parallel diodes, but instead was conducted by the FHCT itself. For this reason these diodes were disconnected for the rest of the test.

For turn-on, an improved gate drive unit was employed producing at 200 V a gate current pulse amplitude of 300 A, with a leading edge of $400\text{ A}/\mu\text{s}$. The turn-on delay time is strongly determined by the amplitude and the rise time of the gate current. Fig. 3 shows the gate voltage and current during the tests.

Fig. 3 Gate voltage and gate current (Hor. scale 500 ns/div.)

The amplitude and the rate of rise of the gate current are chosen such that further increase does no longer improve the turn-on delay time. The loop inductance in the gate trigger circuit was kept to a minimum value of about 500 nH.

During the oscillating discharge current the gate current was maintained at a minimum level of 100 A to ensure that all the active areas of the FHCT remain in conduction for positive current passage.

Measurements

For the first series of tests the amplitude of the circuit discharge current was 20 kA. The waveform is a damped sine-wave of about 20 oscillations, with a quarter period of $2.2\ \mu\text{s}$ corresponding to the risetime of $3\ \mu\text{s}$ of the LHC beam dump generator measured from gate trigger instant onwards. The capacitor C was charged to about 2 kV. The discharge repetition rate was 6 seconds. Fig. 4 shows for comparison reasons the gate current and the anode current for the first $2.25\ \mu\text{s}$ of the WESTCODE *symmetric* device.

Fig. 4 Gate current and anode current at $I_{AM}=20\text{ kA}$ (Hor. scale 250 ns/div.)

The turn-on delay t_d is 1280 ns and the switching losses from trigger instant to 20 kA peak current are 12 J. This FHCT was tested with $50 \cdot 10^3$ discharges.

Fig. 5 shows the test results of the *asymmetric* WESTCODE FHCT. Gate current, anode voltage and anode current are shown for the first $4.5\ \mu\text{s}$. The turn-on delay t_d was 1090 ns and the switching losses from trigger instant to 20 kA peak current 7.8 J. The FHCT was tested for $40 \cdot 10^3$ discharges.

Fig. 6 shows the test results of the *asymmetric* FHCT of GPS, again displaying gate current, anode voltage and anode current for the first $4.5\ \mu\text{s}$. The turn-on delay t_d was 800 ns and the switching losses from trigger instant to 20 kA peak current 6.4 J. The FHCT was tested for $100 \cdot 10^3$ discharges.

Fig. 5 Gate current and anode voltage at $I_{AM}=20$ kA (Hor. scale 500 ns/div.)

Fig. 6 Gate current and anode voltage at $I_{AM}=20$ kA (Hor. scale 500 ns/div.)

Fig. 7 Gate current and anode voltage at $I_{AM}=20$ kA (Hor. scale 20 μs/div.)

Fig. 7 shows gate current, anode voltage and anode current for the full pulse duration of 180 μs. Because of the superior results further testing was carried out only with the GPS FHCT.

Fig. 8 and Fig. 9 show the tests performed at 3600 V to obtain a peak current of 40 kA. The turn-on delay t_d decreased from 800 ns at 1900 V to 700 ns. The adjusted circuit inductance of about 125 nH was not modified. The switching losses increased from 6.4 J to 16.5 J. The FHCT was tested at 40 kA for $100 \cdot 10^3$ discharges.

Fig. 8 Gate current and anode voltage at $I_{AM}=40$ kA (Hor. scale 500 ns/div.)

Fig.9 Gate current and anode voltage at $I_{AM}=40$ kA (Hor. scale 20 μs/div.)

Fig. 10 shows the test results at 4400 V with a peak current of 60 kA. The turn-on delay t_d remained at 700 ns. The circuit inductance was adjusted to about 100 nH in order to obtain at an anode current amplitude of 60 kA. The total number of discharges at 60 kA was about 2000.

Fig. 10 Gate current and anode voltage at $I_{AM}=60$ kA (Hor. scale 500 ns/div.)

Analysis of the results

Table 1 shows a summary of test results. The following conclusions can be drawn.

A peak gate current of 300 A with a rate of rise of 400 A/μs assures an optimal performance in this application with high peak anode current and di/dt values. Further increase of the amplitude and rate of rise of the gate current does not have much influence on the turn-on behaviour.

The measurements in Fig. 6, 8 and 10 show that after the initial anode voltage collapse, the anode voltage is constantly decreasing in spite of the increasing anode current. This means that the current density is decreasing during the dynamic turning-on phase and that the about 2000 individual thyristor elements are switching homogeneously at the same rate. In this hard drive mode the best rate of rise of the gate current pulse for a 20 kA anode peak current is 3% of the anode current di/dt. It should be noted that the anode voltage measurements have not been compensated with $L_{stray} \cdot FHCT \cdot di_A/dt$ ($L_{stray} \approx 11$ nH).

Westcode 4.5 kV symmetric	2.0 kV, 20 kA td=1280 ns
Westcode 4.5 kV asymmetric	1.92 kV, 20 kA td=1090 ns
GPS 4.5 kV asymmetric	1.9 kV, 20 kA td=800 ns
GPS 4.5 kV asymmetric	3.6 kV, 40 kA td=700 ns
GPS 4.5 kV asymmetric	4.4 kV, 60 kA td=700 ns

Table 1 Summary of test results

The asymmetric Fast High Current Thyristor has a lower turn-on delay and switching loss than the symmetric device. For asymmetric devices these

properties are slightly better for the non irradiated GPS version than for the not fully optimised Westcode device with a 70 μm thicker wafer thickness.

Conclusion

Construction of an improved semiconductor power switch for the LHC beam dumping system has started. The switch is composed of ten asymmetric thin wafer FHCT's. These 4.5 kV devices will improve the turn-on delay and the switching losses of the switch. Anti-parallel diodes will not be employed in the switch. In order to safely operate the FHCT's in series the devices have been matched for turn-on delay time. Important reductions in turn-on time can be achieved with gate currents of high amplitude and high rate of rise. Measurements on the previous 30 kV switch assembly showed a maximum spread in turn-on time of 100 ns. It is expected that the new switch will show a substantial smaller spread.

Protection of the FHCT's against over-voltages caused by differences in switching speed and turn-on delay, is realised by capacitors connected in parallel to the FHCT's. The value of these capacitors is kept to a minimum so that they not only protect against over-voltage but also improve slightly the turn-on time of the series operation switch by internal discharge over the FHCT's during turning on.

Outlook

Despite the substantial progress made with asymmetric GTO thyristors as closing switches there is still a potential for future improvements. We expect a further reduction in wafer thickness from 730 μm to 530 μm for a 4.5 kV device. This requires a novel concept of the anode structure. Instead of a conventional anode with high injection efficiency, a low efficiency (so-called transparent) anode with the combination of a buffer layer (ABB concept) will allow a massif reduction in wafer thickness.

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References

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