Fifth Workshop on Electronics for LHC Experiments

Snowmass
Colorado

University of Wisconsin, Madison, Wisconsin, USA
Snowmass, Colorado, September 20-24, 1999
Organized by University of Wisconsin, Madison, WI, USA
on behalf of the CERN LHCC Electronics Board

20-24
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# Table of Contents

## ORGANISATION

## OVERVIEW

_**PLENARY SESSIONS**_ .................................................................................................................. 2

_**ROUNDTABLE**_ .......................................................................................................................... 3

_**PARALLEL WORKING GROUPS**_ ............................................................................................... 3

_**POSTERS**_ ................................................................................................................................. 3

_**INDUSTRIAL EXHIBITION**_ ........................................................................................................ 3

## NEXT WORKSHOP

## PLENARY TALKS

**Raymond Rausch** (CERN, Geneva, Switzerland) **Electronics Components and Systems, Radiation Qualification for Use in the LHC Machine** .................................................................................................................. 7

**Krishna Shenai** (University of Illinois, Chicago, Illinois, USA) **Electronics for High-Energy Physics Experiments in the Giga-Scale Integration Era** .................................................................................................................. 14

**Andrew J. Laukford** (Department of Physics & Astronomy, University of California, Irvine, California, USA) **Developing and Commissioning BABAR Electronics** .................................................................................................................. 23

**Peter Alfke** (Xilinx, Inc., San Jose, California, USA) **The Future of Field-Programmable Gate Arrays** .................................................................................................................................................. 36

**Jorgen Christiansen** (CERN, Geneva, Switzerland) **Testing LHC Electronics** ..................... 41

**Birger Schneider** (microLEX Systems A/S, Hoersholm, Denmark) **Scalable Test Solutions: A Means of Improving ASIC Performance and Time-to-Market in Mixed-Signal Engineering Test** ........ 51

**Jim Kinnison** (The Johns Hopkins University, Applied Physics Laboratory, Laurel, Maryland, USA) **Using COTS at the LHC: Building on Space Experience** .................................................................................................................. 61

## ELECTRONICS FOR TRACKERS

**John Richardson** (Lawrence Berkeley National Laboratory, Berkeley, California, USA) **The ATLAS Pixel On-Detector Electronics** .................................................................................................................. 83

**Kenneth Wyllie** (CERN, Geneva, Switzerland) **A Pixel Readout Chip for Tracking at ALICE and Particle Identification at LHCb** .................................................................................................................. 93

**Abderrezak Mekkaoui** (Fermi National Accelerator Laboratory, Batavia, Illinois, USA) **FPIX1: an Advanced Pixel Readout Chip** .................................................................................................................. 98

**Waclaw Karpinski** (I.Physikalisches Institut RWTH, Aachen, Germany) **Performance Studies of Pixel Readout Electronics in RICMOS IV-SOI and DMILL Processes** .................................................................................. 103

**Ulrich Goerlach** (Institut de Recherches Subatomiques IReS, Strasbourg, France) **Recent Developments and Results on APV (DMILL) Circuits for Silicon and MSGC Detectors** .................................................................................................................. 108
Wladek Dabrowski (Faculty of Physics and Nuclear Techniques, UMM, Krakow, Poland) presented by Francis Anghinoletti (CERN, Geneva, Switzerland) Radiation Hardness of the ABCD Chip for the Binary Readout of Silicon Strip Detectors in the ATLAS Semiconductor Tracker .......................... 113

Francis Anghinoletti (CERN, Geneva, Switzerland) Performance of the Electrical Module Prototypes for the ATLAS Silicon Tracker ........................................................................................................... 118

Tim Dubbs (Institute For Particle Physics, University of California, Santa Cruz, California, USA) The Development of the CAFE-P/CAFE-M Bipolar Chips for the ATLAS Semiconductor Tracker ...... 123

Mitch Newcomer (Physics Department, University of Pennsylvania, Philadelphia, Pennsylvania, USA) Progress in Development of the ASDBLR ASIC for the ATLAS TRT ................................................. 128

Carlos Lacasta (Instituto de Física Corpuscular, Valencia, Spain) Wafer Screening of the Front-End ASICs for ATLAS SCT .......................................................................................................................... 133

Gianni Mazza (Istituto Nazionale di Fisica Nucleare, Tonnio, Italy) Recent Developments on the Silicon Drift Detector Readout Scheme for ALICE Inner Tracking System ........................................ 138

Arie de Haas (NIKHEF, Utrecht, The Netherlands) Very Low Mass Microcables for the ALICE Silicon Strip Detector .............................................................................................................................. 143

Jean Robert Lutz (Institut de Recherches Subatomiques IReS, Strasbourg, France) TAB Bonded SSD Module for the STAR and ALICE Trackers ................................................................................. 147

Markus French (Rutherford Appleton Laboratory, Didcot, UK) The Development of a Rad-Hard CMOS Chip for the Binary Readout of the ATLAS Semiconductor Tracker ................................................................. 152

Angelo Rivetti (CERN, Geneva, Switzerland and Politecnico, Torino, Italy) Analog Design in Deep Submicron CMOS Processes for LHC ........................................................................................................ 157

Lawrence Jones (Rutherford Appleton Laboratory, Didcot, UK) The APV25 Deep Submicron Readout Chip for CMS Detectors ........................................................................................................... 162

Edger Sexauer (Max-Planck-Institute for Nuclear Physics, Heidelberg, Germany) Design of a Prototype Frontend and Bias Generator for a new Readout Chip for LHCb .............................................. 167

Optoelectronics and data transfer systems .............................................................................................................. 173

Giovanni Cervelli (CERN, Geneva, Switzerland) Optical Links for the CMS Tracker ............................................ 175

Kukka Banzuzi (Helsinki Institute of Physics, Espoo, Finland) Optical Link Developments for the CMS RPC .............................................................................................................................................. 180

Gilles Mahout (School of Physics and Astronomy, University of Birmingham, Birmingham, UK) Radiation Hard Optical Links for the ATLAS SCT and Pixel Detectors ........................................ 185

Federico Faccio (CERN, Geneva, Switzerland) An Amplifier with AGC for the 80Mbit/s Optical Receiver of the CMS Digital Optical Link ...................................................................................... 189

Paulo Moreira (CERN, Geneva, Switzerland) A 1.25Gbit/s Serializer for LHC Data and Trigger Optics ................................................................................................................................. 194

Radiation and Magnetic Field Tolerant Electronics Systems .................................................................................. 199

Stephen Watts (Brunel University, Uxbridge, UK) Status of the RD48/ROSE Collaboration ................................ 201

Pratibha Vikas (University of Minnesota, Minneapolis, Minnesota, USA) Avalanche Photodiodes for the CMS Electromagnetic Calorimeter ........................................................................ 203

Giovanni Bonna (ST Microelectronics, Catania, Italy) A Radiation-Hardened Low-Dropout Voltage Regulator for LHC and Space Applications ........................................................................... 208
Electronics for Calorimeters

Jacques Colas (LAPP, Annecy-le-Vieux, France) Overview of the ATLAS LARG Electronics

Sergio Rescia (Brookhaven National Laboratory, Upton, New-York, USA) presented by Helio Takai (Brookhaven National Laboratory, Upton, New-York, USA) Characterization of the Coherent Noise, Electromagnetic Compatibility and Electromagnetic Interference of the ATLAS EM Calorimeter Front End Board

Horst Brettel (Max-Planck-Institute für Physik, München, Germany) Cold Electronics for the Liquid Argon Hadronic End-Cap Calorimeter of ATLAS

Bernhard Skaali (Department of Physics, University of Oslo, Oslo, Norway) Photodiode Read-Out of the ALICE Photon Spectrometer PbWO₄ Crystals

Mauro Citterio (Brookhaven National Laboratory, Upton, New-York, USA) The Atlas Calorimeter Preamplifier: Performance, Radiation Damage, Electrostatic Discharge Resistance, Reliability and Manufacturing Issues

Dominique Breton (Laboratoire de l'Accélérateur Linéaire, Orsay, France) The Front-End Electronics for LHCb Calorimeters

Teresa Monteiro (CERN, Geneva, Switzerland) Selective Readout in the CMS Electromagnetic Calorimeter

Bo Lofstedt (CERN, Geneva, Switzerland) The Digital Readout System for the CMS Electromagnetic Calorimeter

Magnus Engström (University of Stockholm, Stockholm, Sweden) presented by Jonas Klerborn (University of Stockholm, Stockholm, Sweden) The ATLAS Tile Calorimeter Digitizer

Alan E. Baumbaugh (Fermi National Accelerator Laboratory, Batavia, Illinois, USA) First Testbeam Results for the QIE-Demonstrator Readout for the CMS Hadronic Calorimeter

Guy Perrot (LAPP, Annecy-le-Vieux, France) The ATLAS Calorimeter Calibration Board: Tests of a First Set of Boards New Developments

Jürgen Fent (Max-Planck-Institut für Physik, Werner Heisenberg Institute, München, Germany) Jet Determination in LAr- Calorimeters using a Heavily Interconnected System of FPGA's

Gérard Bohner (Laboratoire de Physique Corpusculaire, Université Blaise Pascal, Aubière, France) A Mixed Analog/Digital Shaper for the LHCb Preshower

Trigger Electronics

Valerio Bacci (Istituto Nazionale di Fisica Nucleare, Roma, Italy) Trigger Implementation in the KLOE Experiment

Vito Lenti (Dipartimento di Fisica dell'Università and Istituto Nazionale di Fisica Nucleare, Bari, Italy) New Developments for the ALICE Trigger

Cornelius Schumacher (Institut für Höherenergiefysik der Universität, Heidelberg, Germany) The Readout Bas of the ATLAS Level-I Calorimeter Trigger Pre-Processor

Sridhara Dasu (University of Wisconsin, Madison, Wisconsin, USA) CMS Calorimeter Regional Trigger Prototypes

Viraj Perera (Rutherford Appleton Laboratory, Didcot, UK) The electron/photon and tau/hadron Cluster Processor for the ATLAS First-Level Trigger - a Flexible Test System

Jay Hauser (University of California, Los Angeles, California USA) Primitives for the CMS Cathode Strip Muon Trigger

János Erő (Institute for High Energy Physics HEPHY, Vienna, Austria and CERN, Geneva, Switzerland) New Approach for the CMS Muon Trigger Track Finder Processor
Data Acquisition & Detector Control and Real Time System

Attila Racz (CERN, Geneva, Switzerland) Generic Hardware for DAQ Applications ............................................. 343
Dominique Gigi (CERN, Geneva, Switzerland) Dual-Port Memory with Reconfigurable Structure.................. 348
Jose Toledo-Alcarcon (Politechnical University, Valencia, Spain) Readout Unit for the LHCb Experiment ................................................................. 352
John A. Coughlan (Rutherford Appleton Laboratory, Chilton, Didcot, Oxon, UK) presented by Steve Quinton (Rutherford Appleton Laboratory, Chilton, Didcot, Oxon, UK) A PMC Based ADC Card for CMS Tracker Readout ........................................... 357
Carlos Beltrán Almeida (Instituto de Engenharia de Sistemas e Computadores, Lisboa, Portugal) Testability Issues in the CMS ECAL Upper-Level Readout and Trigger System ........................................... 361
Wilfred. E. Cleland (University of Pittsburgh, Pittsburgh, Pennsylvania, USA) Readout Driver for the ATLAS Liquid Argon Calorimeters ........................................... 366
Detlef Swohoda (CERN, Geneva, Switzerland) The Detector Control System for ALICE - Architecture and Implementation ......................................................... 371
Alexander Kluge (CERN, Geneva, Switzerland) Study of the ALICE Time of Flight Readout System - AFRO ................................................................. 377
Horst Fischer (Fakultät für Physik, Universität Freiburg, Freiburg, Germany) FI - An Eight Channel Time-to-Digital Converter Chip for High Rate Experiments ............................................... 383

Grounding Shielding and Cooling

Fritz Szoncsó (CERN, Geneva, Switzerland) Assessment of EMC Parameters of LHC Front End Electronics ........................................................................................................... 391
Werner Lusternmann (ETH, Zürich, Switzerland) presented by Nedko Shivarov (Bulgarian Academy of Sciences, Central Lab. of Mechatronics & Instrumentation, Sofia, Bulgaria & ETH, Zürich, Switzerland) Low Voltage Supply System for the Very Front End Readout Electronics of the CMS Electromagnetic Calorimeter ......................................................... 397
Mauro Citterio (Brookhaven National Laboratory, Upton, New-York, USA) Are Switching Power Supplies Acceptable for the Liquid Argon Calorimeter Front-End Electronics? ........................................... 402
Warren H. Newman (Internat Corporation, Melbourne, Florida, USA) Radiation Hardened Power Electronics ........................................................................................................... 407
Juan A. Agapito (Universidad Complutense, Electronics Department, Madrid, Spain) Preliminary Test for Radiation Tolerant Electronic Components for the LHC Cryogenic System ........................................................................................................... 411
Michel Bosteels (CERN, Geneva, Switzerland) Liquid Cooling Systems (LCS2) for LHC Detectors ................................................................. 416

Greg Hallewell (Centre de Physique des Particules CPPM, Marseille, France and CERN, Geneva, Switzerland) Fluorocarbon Evaporative Cooling Developments for the ATLAS Pixel and Semiconductor Tracking Detectors ................................................. 421


Electronics for Muon Detectors 429

Jean-Claude Santlard (CERN, Geneva, Switzerland) The Gassiplex 0.7-2 Integrated Front-End Analog Processor for the HMPID and the Dimuon Spectrometer of ALICE .............................. 431

Werner Riegler (Harvard University, Cambridge, Massachusetts, USA) Development of an Octal CMOS 82D for the ATLAS Muon Detector ........................................................................................................ 436

Osumu Sasaki (High Energy Accelerator Research Organisation KEK, Tsukuba, Japan) ASD for the Thin Gap Chambers in the LHC ATLAS Experiment ................................................................. 443

John W. Chapman (University of Michigan, Ann Arbor, Michigan, USA) Data Flow Simulations through the ATLAS Muon Front-End Electronics ............................................................ 448

Paul O'Connor (Brookhaven National Laboratory, Upton, New-York, USA) Readout Electronics for a High-Rate CSC Detector ................................................................. 452

Flavio Loddo (Dipartimento Interateneo di Fisica and Istituto Nazionale di Fisica Nucleare, Bari, Italy) A Prototype Front End Chip for the CMS Resistive Plate Chambers ............................................ 457

Yasuo Arai (National High Energy Accelerator Research Organisation KEK, Tsukuba, Japan) Performance and Irradiation Tests of the 0.3 μm CMOS 7DC for the ATLAS MDT .................. 462

POSTERS 467

Pisana Placidi (CERN, Geneva, Switzerland and University and Istituto Nazionale di Fisica Nucleare, Perugia, Italy) A 40 MHz Clock and Trigger Recovery Circuit for the CMS Tracker Fabricated in a 0.25 μm CMOS Technology and Using a Self Calibration Technique ................................................................. 469

Thomas Meyer (Department of Physics and Astronomy, Iowa State University, Ames, Iowa, USA) CANbus and Microcontroller Use in the BaBar Detector at SLAC ........................................ 473

Cornelius Schumacher (Institut für Hochenergiephysik, Heidelberg, Germany) The ATLAS Level-1 Calorimeter Trigger Pre-Processor ................................................................. 478

Gastavo Cancello (Fermi National Accelerator Laboratory, Batavia, Illinois, USA) Optimization of a Readout Architecture for Pixel Detectors ................................................................. 483

Zoltán Meggyszi (CERN, Geneva, Switzerland) FPGA Design in the Presence of Single Event Upsets ..................................................................................................................... 489

György Rubin (CERN, Geneva, Switzerland) The ALICE Detector Data Link ................................................................. 493

Yury Volkov (Moscow Engineering Physics Institute, Moscow, Russia) Development of the Printed Circuit Units for Multiwire Chambers ........................................................................... 499

Eduard Atkin (Moscow Engineering Physics Institute, Moscow, Russia) Analog Signal Splitter ................................................................. 501

Cristoforo Marzocca (Istituto di Elettronica ed Elettronica, Politecnico, Bari, Italy) Relative Robustness Against Process Fluctuations of Basic Building Blocks for Analog Front-End of Particle Detectors .......................................................................................... 503

Ulrich Trunk (Max-Planck-Institut für Kernphysik, Heidelberg, Germany) Performance and Radiation Tolerance of the Helix128-2.2 and 3.0 Readout Chips for the HERA-B Microstrip Detectors ................................................................. 508
**Jonathan Fulcher** (Imperial College, London, UK) Single Event Upset Studies on the APV6 Front End Readout Chip .................................................................................................................. 513

**Nunzio Randazzo** (University of Catania and Istituto Nazionale di Fisica Nucleare, Catania, Italy) Charge Amplifier and Analog Memory for Silicon Drift Detectors in ALICE ........................................................................................................... 518

**Paul Mockett** (University of Washington, Seattle, Washington, USA) A Low Cost CAN Node for A/D Measurements in ATLAS ........................................................................................................................................ 521

**Magnus Hansen** (CERN, Geneva, Switzerland) FERMI - A Digital Front End Readout Micro-System for Calorimetric Detectors at LHC ............................................................................................................... 525

**Jean-Pierre Mendiburu** (LAPP, Annecy-le-Vieux, France) The Electronic Calibration of the ECAL-CMS ............................................................................................................................................... 531

**Christine Hu-Guo** (Institut de Recherches Subatomiques IReS, Strasbourg, France) Low Noise BiCMOS Front-End Amplifier in the DMILL Technology .............................................................................................................. 537

**Christine Hu-Guo** (Institut de Recherches Subatomiques IReS, Strasbourg, France) A 128 Channels Analog Readout Chip (APVD, DC) for DC-Coupled Silicon Detectors of the CMS Tracker .................................................................................................................... 542

**Peter Skorobogatov** (Specialized Electronic Systems, Moscow, Russia) Use of Diffused Laser Irradiation to Improve Dose Rate Simulation Adequacy .................................................................................................................. 547

**Christian Kiesling** (Max-Planck-Institut für Physik, München, Germany) Neural Network Triggers for Global Event Decision at the LHC .................................................................................................................... 551

**Vladimir Popov** (Institute for Theoretical and Experimental Physics, Moscow, Russia) The HERA-B high-\(P_T\) Level-0 Trigger Logic Electronics .................................................................................................................................................... 557

**Daniel Dzhahini** (ISN, Grenoble, France) An Automated Test Bench for the ATLAS Shapers and SCAs ......................................................................................................................................................... 561

**Hermann Kolanski** (DESY, Zeuthen, Germany) Large-System Experience with the ASD-8 Chip in the HERA-B Experiment ......................................................................................................................... 564

**PAPER ONLY** ........................................................................................................................................................................................................................................ 569

**Federico Facchio** (CERN, Geneva, Switzerland) SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 μm CMOS technology for applications in the LHC ................................................................................................................. 571

**Ekkehard Gerndt** (DESY, Hamburg, Germany) The HERA-B Level 1 Trigger ................................................................................................................................................................................................................ 576

**Michel Dupanloup** (Institut de Physique Nucléaire de Lyon, Villeurbanne, France Preliminary Irradiation Tests of the APVD Circuit for the CMS Tracker ..................................................................................................... 581

**Vitali V. Sushkov** (University of California, Riverside, California, USA) Noise Contribution to Timing with Fraction Discriminators ..................................................................................................................... 588

**LIST OF PARTICIPANTS** .............................................................................................................................................................................................................. 593

**INDEX** .............................................................................................................................................................................................................................................. 607
ORGANISATION

The fifth in this series of workshops on Electronics for LHC Experiments, was organised for the CERN LHCC Electronics Board by the University of Wisconsin, Madison, Wisconsin, USA.

The workshop was held on September 20-24, 1999 in the Snowmass Conference Center, Snowmass Colorado, USA.

Local Organisation Committee:

Wesley SMITH (Chairman)  University of Wisconsin
William BADCOTT  University of Wisconsin
Sridhara R. DASU  University of Wisconsin
John ELIASS  Fermi National Accelerator Laboratory
H.H. LANKFORD  University of California at Irvine
Aimee LEFKOW  University of Wisconsin
Veljko RADEKA  Brookhaven National Laboratory

The Program Review Committee was comprised of the members of the LEB, namely:

Peter SHARP (Chairman)  Rutherford Appleton Laboratory
Pierre BORGEAUD  CEA Saclay
Francesco CORSI  Politecnico di Bari
Jorgen CHRISTIANSEN  CERN
Philippe FARTHOUAT  CERN
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Geoff HALL  Imperial College
Michael LETHEREN  CERN
Emilio PETROLO  INFN Rome
Steve QUINTON  Rutherford Appleton Laboratory
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Michael SCHMELLING  Max Planck Institute Heidelberg
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Michal TURALA  CERN

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Aimee LEFKOW  University of Wisconsin
Renee LEFKOW  University of Wisconsin

Proceedings Editor:

Catherine DE COSSE  CERN
OVERVIEW

The purpose of the workshop was to review the electronics for LHC experiments and to identify areas and encourage common efforts for the development of electronics within and between the different LHC experiments and to promote cross fertilisation in the engineering and physics communities involved in the LHC activities.

The program of the workshop included both invited plenary talks and parallel working groups for contributed papers. The focus of the workshop was research and recent development in the following topics:

- Radiation and magnetic field tolerant electronics systems
- Optoelectronics and data transfer systems
- Detector control and real time systems
- Electronics production and test techniques
- Systems reliability, quality assurance and maintenance
- Electronics for trackers
- Electronics for calorimeters
- Electronics for muon detectors
- Trigger electronics
- Low voltage and high voltage distribution
- Grounding shielding and cooling

The welcome address was given by Peter Sharp, Chairman of the CERN LHCC Electronics Board and by Wesley Smith, Chairman of the local organising committee.

PLENARY SESSIONS

Chaired by Peter Sharp:
- The LEb and the LHC
  Peter Sharp (Rutherford Appleton Laboratory, Didcot, UK)
- Electronics Components and Systems, Radiation Qualification for Use in the LHC Machine
  Invited Raymond Rausch (CERN, Geneva, Switzerland)
- Project Management
  Invited Ed Temple (Fermi National Accelerator Laboratory, Batavia, Illinois, USA)
- Electronics for High Energy Physics Experiments in the Giga-Scale Integration Era
  Invited Krishna Shenai (University of Illinois, Chicago, Illinois, USA)

Chaired by Steve Quinton:
- Developing and Commissioning BABAR Electronics
  Invited Andrew Lankford (University of California, Irvine, California, USA)
- Development, Production and Installation of CDF Electronics
  invited Peter Wilson (Fermi National Accelerator Laboratory, Batavia, Illinois, USA)

Chaired by Michael Letheren:
- The Future of FPGAs
  Invited Peter Aifke (Xilinx Inc., San Jose, California, USA)

Chaired by Philippe Farthouat:
- Testing Electronics
  Invited Jorgen Christiansen (CERN, Geneva, Switzerland)
- Scalable Test Solutions: A Means of Improving ASIC Performance and Time-to-Market in Mixed-Signal Engineering Test
  Invited Birger Schneider (Micrel, Hoersholm, Denmark)

Chaired by Peter Sharp:
- Using COTS at the LHC: Building on Space Experience
  Invited Jim Kinnison (Johns Hopkins University, Laurel, Maryland, USA)
**ROUNDTABLE**
The roundtable on COTS was chaired by Peter Winokur (Sandia Laboratory, Albuquerque, New Mexico, USA).

**PARALLEL WORKING GROUPS**
The two parallel working groups focussed on the system design issues involved in the electronics for:

**WORKING GROUP A:**
- Electronics for Trackers (Chairmen: Michal Turala and Geoff Hall)
- Optoelectronics and Data Transfer Systems (Chairmen: Michal Turala and Michael Letheren)
- Radiation and Magnetic Field Tolerant Electronics Systems (Chairman: Veljko Radićka)
- Electronics for Calorimeters (Chairmen: Veljko Radićka and Pierre Borgeaud)

Panel Discussion chaired by Hugh H. Williams (University of Pennsylvania, Philadelphia, Pennsylvania, USA)

**WORKING GROUP B:**
- Trigger Electronics (Chairmen: Wesley Smith and Sridhara R. Dasu)
- Data Acquisition and Detector Control and Real Time System (Chairman: Michael Schnellinger)
- Grounding Shielding and Cooling (Chairmen: Fabio Formenti and Jorgen Christiansen)
- Electronics for Muon Detectors (Chairman: Jorgen Christiansen)

Panel Discussion chaired by John Elias (Fermi National Accelerator Laboratory, Batavia, Illinois, USA)

**POSTERS**
The poster session was chaired by Steve Quinton

**INDUSTRIAL EXHIBITION**
Company attending was CAEN SpA, Viareggio, Italy.

**NEXT WORKSHOP**
The sixth workshop is expected to take place in Krakow, Poland, in September 2000.

Further information will be made available in due course on the World Wide Web.
Abstract

Studies, taking into account the expected radiation doses for the different sections in the LHC accelerator tunnel, such as regular arcs and dispersion suppressors, show that electronic equipment can be considered for installation under the magnets [1,2,3,4]. An estimate based on work carried out for String 2, the LHC Magnet String Program [5], and extrapolated to the whole LHC machine gives a total of several thousands electronic crates to be housed under the magnets. This represents a substantial installation and a large expenditure.

In order to qualify electronic equipment for installation in the LHC tunnel, from its radiation hardness point of view at the dose levels considered, an on-line radiation test facility has been created and installed along a secondary beam line in the north experimental area of the SPS accelerator.

The object of this paper is to present the type of electronic equipment and systems planned to be installed in the tunnel of the LHC and to give some preliminary results on radiation tests made for this electronics.

1. THE REGULAR MACHINE LAYOUT

The complete machine layout is described in the Large Hadron Collider Conceptual Design document [6].

For the purpose of this paper and in order to simplify the presentation, we will only consider the regular arc and the Dispersion Suppressors (DS) regions; we will not discuss the Long Straight Sections (LSS), in the middle of which are installed the experiments at the Interaction Points (IP).

The LHC is made of eight arcs separated by insertions. Each of the eight arcs is composed of 23 arc cells, giving a total arc length of 2456 m. All arc cells are made of two identical half-cells.

The layout of an arc half-cell consists of a string of three 14.2 m twin-aperture dipoles and one 3.10 m quadrupole separated from the string by 2.42 m. The separation between the dipoles is 1.46 m.

The two dispersion suppressor cells consist of four quadrupoles interleaved with four strings of two dipoles each. There is a total of 16 dispersion suppressors in LHC and their dipoles have the same length as in the arcs.

2. SPACE FOR ELECTRONICS

The LHC proton beams will circulate at 950 mm above the floor of the tunnel. Taking into account the actual size of the dipoles, of the quadrupoles and of the tunnel floor construction tolerance a height of 380 mm and a depth of 800 mm is available for electronic crates. Under each dipole and quadrupole space has to be left free for access to the supporting jacks and to allow access for the magnet transport system. A standard 6U crate with a 2U fan is accounted for a height of 350 mm, for a width of 600 mm with its support structure and for a depth of 800 mm including rear or front connections.

Work, initially carried out for the String 2 [7] and extrapolated to the whole LHC machine, has shown that several thousands electronic crates, or equivalent assemblies, can be housed under the supra conducting magnets.

Space has been allocated to the various data acquisition and control systems, the beam instrumentation, the vacuum, the cryogenics, the corrector power converters, the magnet protection equipment and to the controls. For each of the eight arcs the current estimation of the needs is given in Table 1.

<table>
<thead>
<tr>
<th>Systems</th>
<th>Equipment Crates</th>
<th>Control Crates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnet Protection</td>
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<td>208</td>
</tr>
<tr>
<td>Vacuum</td>
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<td>27</td>
</tr>
<tr>
<td>Cryogenics</td>
<td>154</td>
<td></td>
</tr>
<tr>
<td>Beam Instrumentation</td>
<td>54 (F.E)</td>
<td>27</td>
</tr>
<tr>
<td>Controls</td>
<td>27</td>
<td></td>
</tr>
<tr>
<td><strong>Total per Arc</strong></td>
<td><strong>778</strong></td>
<td><strong>551</strong></td>
</tr>
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3. ELECTRONIC EQUIPMENT

3.1 Housing of Electronics

The housing of electronic equipment and systems in the tunnel will have to be designed in such a way that their installation and removal can be done easily either by the owner of the equipment or by installation teams to which the work may be subcontracted. Considering the large number of crates, or equivalent assemblies, the positioning, the connection, the powering and the test in-situ should be as simple as possible and not require special tools.

Equipment located under the magnets at the floor level will have to be protected from shocks, from dust and must adequately be ventilated.

3.2 Type of Crates

The natural choice would be 6U and 3U Euro-Crates, as specified for VME and G64 mechanical standards, with an adequate ventilation. The choice is not limited to this type of crate. For example, complete assemblies of 5 crates are being studied to house four corrector power converters with the network connections and the power distribution located in the middle of this assembly.

As more and more complete industrial systems will be used to control the LHC other shapes of crates will also have to be integrated. One example is the use of electronic modules mounted on standard DIN rail. Industry provides a large choice for this type of equipment.

3.3 Programmable Logic Controllers

Industry offers a vast choice of Programmable Logic Controllers (PLC). These PLCs can be used for process control for the vacuum system, the cryogenics, the power distribution, the machine access systems, the cooling and ventilation systems. Since several years PLCs are also used for typical accelerator systems such as beam transfer equipment, beam extraction systems, beam target electronics and radiofrequency power generators.

For the controls of the LHC it is anticipated that PLCs will be used extensively for most systems. VME crates and modules or ad-hoc assemblies will remain the best choice for fast beam instrumentation and for very special systems.

In order to limit the diversity of PLC equipment to be used in LHC a study of the industrial offer has been made by an ad-hoc working group and a CERN recommendation for their use has been published, [8].

3.4 Input/Output Modules

Here again industry offers a large diversity of input/output modules for analogue and digital acquisition and control, for steeping motor control and for sensor interfaces. In addition, some special modules may have to be designed if they are not available commercially.

The mounting of these I/O modules is usually done on rails, conforming to the DIN standard, which can be housed under the dipoles, as explained above, or even be fixed directly onto the magnet’s wessel, close to the sensors.

4. NETWORKS

4.1 High Speed Networks

As Beam Instrumentation (BI) electronics must be installed close to the Beam Position Monitors (BPM) and to the Beam Loss Monitors (BLM) to provide measurements with the required precision, high speed point to point links to these BI crates will be required.

It has been decided to use point to point Ethernet segments for the high speed links available in the tunnel. Ethernet interfaces exist for all types of electronic crates, VME, VXI, G64, PCI, CompactPCI, PCs and also for industrial PLCs. In addition, the bandwidth provided by an Ethernet connection is also adequate for BI crates. The layout of the LHC tunnel requires Ethernet segments, of up to 800 m long, to be drawn between the 16 underground alcoves and the most distant BI crates located in the mid-arcs. Up to 12 Ethernet segments drawn to the left and 14 segments to right of each alcove are needed.

For 800 m point to point Ethernet segments and half-duplex transmission a good quality coaxial cable will be used to avoid intermediate electronic repeaters.

In order to provide each BI crate with the full bandwidth of 10 MBit/s Ethernet each alcove will house an Ethernet switch, thus providing a total bandwidth capability of up to 260 MBit/s per alcove. Under the floor of the tunnel, mono-mode optical fibres, laid in a drain, will link the 16 alcoves to the 8 Intersection Points (IP) where the experiments are installed. Gigabit Ethernet, ATM or SDH (the final choice remains to be done) will connect the 8 LHC points to the Central Control Room located on the CERN Prévessin Site.

4.2 Fieldbuses

A large variety of fieldbuses are offered by industry. A CERN working group has made a study of available fieldbuses. Taking into account the application of fieldbuses at CERN this working group has selected three standard fieldbuses and has made a recommendation for their use for the construction of the LHC machine and for its experiments, [9].

The use of only three fieldbuses has been recommended. Profibus and WorldFIP are preferred for the control of the machine for reasons of long distance
transmission capability while CAN is the choice for the experiments.

Conceptually Profibus is a Command/Response fieldbus; like the MIL-1553-B which has been used extensively over the past 10 years for the control of CERN’s accelerators.

Profibus is an industrial fieldbus well supported by a large number of manufacturers. Many interfaces exist for analogue and digital input/output modules, for stepping motor controllers, for sensors and actuators. Industrial PLCs, of different performance levels are available and provide all the necessary Profibus drivers and the development software facilities needed.

WorldFIP implements a Producer/Consumer concept in which a single command can be recognised and executed simultaneously by a variable number of consumers. Such a concept allows WorldFIP to offer real-time control capabilities. WorldFIP will be used for the transmission of the universal time and for the precise synchronisation of accelerator equipment.

WorldFIP is also an industrial fieldbus well supported by manufacturers but to a less extent than Profibus. WorldFIP will be used for controls applications where the real-time performance, the universal time distribution or the machine event synchronisation are required.

CAN implements a Producer/Consumer concept similar to that of WorldFIP, with in addition a priority access mechanism to the medium to resolve the contention problem. The drawback of this feature is that, for a given operation frequency, this medium access mechanism limits inherently the bus length.

CAN has been adopted for LHC experiments as it offers a large choice for protocol and interface chips which can be incorporated into dedicated electronic designs.

4.3 Real-Time Communication

WorldFIP and ATM channels are planned to be used as the real-time communication networks, [10].

For the control of the orbit stability of the two counter rotating proton beams it is currently proposed to implement a global feedback system; the sensors being the 972 BPMs and the 964 Correction Power Converters (CPC) being the actuators. The current plan is to implement a real-time beam orbit correction using a sampling rate of ten times per second, [11,12].

The beam position information, generated by the BPMs, will be pre-processed in the 248 BI crates. These crates will be connected to each private Ethernet segment and to WorldFIP fieldbuses, dedicated to BI. Every 100 ms, this BPMs real-time information will be sent to the central control room via WorldFIP fieldbuses and ATM transmission channels for computation. The new current reference values will then be sent down via ATM channels to each of the CPCs. All CPCs are connected to and controlled via another set of dedicated WorldFIP fieldbuses.

4.4 Machine Timing

The LHC machine equipment requires precise timing information, [13].

The most important timing is a precise universal time reference (Universal Time Co-ordinates, UTC) to synchronise all CPU clocks to better than a millisecond. To this purpose each of the 8 LHC access points plus the central control room are equipped with GPS antennas and reception equipment. The universal time reference is received and conditioned in commercially available VME modules and is locally distributed to all systems which need this time reference.

From each intersection point the GPS time is propagated both sides to the adjacent alcoves, distant of 943 m, via the Inter-Range Instrumentation Group (IRIG-B) standard transmission cable. In alcoves the IRIG-B signal is regenerated and made available to time-stamp local data acquisition and controls.

The magnet quench protection system, for example, will generate over 4000 possible inputs to the beam dump trigger system. In order to perform meaningful post mortem analysis, all related systems actions will have to be time stamped. Due to the uniform distribution of the major systems throughout the LHC complex, it will be essential to use the GPS as the source of time reference.

4.5 Beam Synchronous Timing

A Beam Synchronous Timing (BST) distribution is required by BI equipment to identify particle bunches. This BST information will be derived from the 40 MHz bunch clock, from the 11 kHz turn clock and from the machine events. The BST information is created in 24 stations (16 alcoves and 8 IPs) and distributed to all the beam instrumentation crates installed in the tunnel.

5. RADIATION QUALIFICATION

Before installation in the LHC tunnel, electronic equipment and systems must be fully tested and qualified for standing the radiation levels to which they will be exposed, depending on their position along the collider.

The absorbed dose levels have been calculated to be of the order of 1 Gy per year under the middle dipole of a regular half-cell and of 12 Gy per year under the Short Straight Section (SSS) quadrupole at a distance of 700 mm from the proton beams [1,2,3,4]. At such dose levels, no major radiation-damage problems are to be expected, and designers plan to use Commercial Off The Shelf (COTS) electronic components and systems.
5.1 CERN On-Line Radiation Test Facility

In order to do systematic radiation tests on to qualify all electronic equipment to be installed in the LHC machine tunnel, CERN has decided in 1998 to create a radiation test zone in one of the Super Proton Synchrotron (SPS) north experimental areas. A test zone, was settled along a secondary beam line of the SPS accelerator, some 100m downstream of a particle-conversion target (T6).

This radiation test area, fully operational since the start-up of the SPS in March 1999, provides all the required facilities: high power electrical supply for the test of power converters, compressed air for the test of pneumatic electro-valves, radio communication, video observation, CAN, Profibus and WorldFIP fieldbuses, connections to the accelerator control network and to the office LAN. In addition, numerous coaxial and twisted pair cables for analogue and digital signals have been laid between the radiation test zone and the local control room distant of some 200 m. In the local control room experimenters have installed their PCs, workstations and measurement instruments for the monitoring and the remote control of their experiment, if necessary. Some systems have been connected from this local control room to the general CERN office LAN, thus providing the experimenter with all the facilities needed to monitor and control his experiment from his office.

5.2 Irradiation Conditions

A 400 GeV-proton beam hits a metallic target (T6), muons are collected downstream and guided toward physics experiments. The radiation field around such target is typical of a proton accelerator; it includes mainly gammas and neutrons, plus some high-energy particles. The gamma spectrum extends from a few hundred keV to several hundred MeV, but is mainly between 1 MeV and a few MeV. The neutron spectrum is about the same, but it also includes a large quantity of low-energy neutrons thermalized by concrete shielding. The presence of other particles is very low, but it is not excluded that some hadrons (protons, neutrons, pions) and muons of high energy create particular effects in digital electronics. The radiation field is characterised by means of passive solid-state dosimeters and active semi-conductor dosimeters [14]. Measurements show that the radiation field is not homogeneous, neither in intensity, nor in nature; the weekly absorbed doses vary between 10 to more than 50 Gy, depending on the location, while the neutron fluences (1 MeV eqv.-Si) vary from $10^{11}$ to $2.10^{12}$ n.cm$^{-2}$, moreover the neutron spectrum also changes.

CERN radiation experts recognise that these irradiation conditions are similar to those that will exist in the tunnel of the future LHC where the dose-rate and the neutron spectrum will also change from place to place.

5.3 Radiation Monitoring and Calibration

From 1999, on-line monitoring of the radiation doses, to which the equipment is exposed, is available in the local control room and on the Web. The test zone has a surface of some 8 square meters. The monitoring of the dose rate is done by four ionisation chambers (3 litres of air), located at each corner of the test zone at a height of 800 mm (= beam height). These monitors are connected to the CERN radiation monitoring system, “ARCON”. The radiation data is stored in the central ORACLE Database which can be consulted at leisure by the experimenters to retrieve historical data and to correlate it to the results obtained from his experiment. The doses are stored day after day, every hour and the data is kept at disposal for several years.

In addition, the absorbed doses are also integrated by passive solid-state dosimeters (polymer-alanine, radio-photo-luminescent glasses, and MOS dosimeters). The measurement of the neutron fluence uses the activation technique (radioactive isotopes are created in metals) and silicon PIN diodes. After exposure, these dosimeters are regularly exchanged and measured; the latter are measured in the laboratories of the French Atomic Energy Commission (CEA) in Valduc.

5.4 Tested Material

In 1998, passive radiation-tests have been done on some electronic components and systems during three distinct irradiation campaigns, where doses of 20 Gy, 50 Gy and 140 Gy have successively been reached. After each irradiation campaign all the material was taken out, let cool-down and tested to check its correct operation. If still operational the same samples where then exposed again for the next irradiation campaign. The total integrated dose has been close to 220 Gy and the neutron fluence was of the order of $2e12$ n.cm$^{-2}$ (eq.1MeV-Si). The tests included industrial Programmable Logic Controllers from various manufacturers, electronic modules conforming to the VME and G64 Bus Standards, Fieldbuses like Profibus, WorldFIP and CAN, Power Supply equipment and Components used for the LHC Cryogeny [15].

In 1999, new electronic components and systems have been included in the irradiation programme such as digital positioners, quench protection equipment, additional CAN, Profibus and WorldFIP interfaces, industrial PLCs, power converters, optical fibres and data-transmission equipment, fire and gas detectors, etc... [16].

5.5 Preliminary Results

In 1998, the lack of proper infrastructure in the area allowed only passive tests to be carried out. During the three campaigns of passive tests some components, mainly opto-couplers, analogue to digital converters and
some PLC input/output modules showed loss of functionality.

This year, the zone was fully equipped for on-line radiation tests and the irradiation campaign has started in May. The target doses are of the same order as last year but the material under test remains permanently under irradiation unless a failure appears. In this case the sample is taken out, let cool-down and then is analysed to identify the defective component(s).

In 1999, after a few weeks of irradiation, having reached dose levels between 20 and 200 Gy, and neutron fluence of the order of a few $10^{12}$ n.cm$^{-2}$ (1MeV equ.-Si), the measurements show disquieting results for some components and promising results for other ones.

Some type of opto-coupler degraded progressively right from the beginning of the irradiation; the CTR dropped to less than 20% at 20 Gy. Another opto-coupler model still continues to work properly after a dose of 100 Gy showing a CTR derating of only 5%, [17].

Within the framework of the protection system for supra conducting elements different kind of electronic devices have to be qualified with respect to radiation tolerance. The irradiation tests started with the main components of quench heater power supplies, aluminium electrolytic capacitors and phase control thyristors. The different type of thyristors passed the ongoing tests up to a received dose of about 55Gy ($=5.5 \times 10^{15}$ n.cm$^{-2}$) without any functional degradation, whereas some of the tested capacitors showed a significant increase of the leakage current. The measured DC capacitance remained constant for all tested specimens, [18].

For the cryogenic system, the high-precision resistors and the associated capacitors used in the construction of conditioners for thermometry have undergone successfully the radiation tests; only a tiny fraction of a percent deviation has been noticed, [20].

No errors have been detected in the Actel antifuse-based FPGAs, an error rate of 2 to 10 bit-error per day has been measured in the HP G-link, which makes both of these components suitable for use at the dose rate and fluences of the LHC, [21].

Tests on a 200 meter fibre cable, containing 12 mono-mode fibres and 12 multi-mode fibres, have been done. As expected, the multi-mode fibres showed an attenuation of some 50db per km while the mono-mode fibres only a loss of 8 dB per km at a dose of 80 Gy.

The CCD camera degraded progressively, the number of white spots increased continuously, at 25 Gy the picture was still visible but at 30 Gy the camera stopped working. This camera has been replaced by a new one.

The GSM repeater, used for mobile telephones, revealed a degraded operation at 20 Gy and went out of operation at 30 Gy.

The fire and gas detectors which have been exposed went faulty at 20 Gy and 25 Gy, respectively.

Analogue and digital telephone equipment went definitely faulty. An RNIS bus did not reply anymore after some 15 days operation having received a dose of some 30 Gy.

Memory tests have been done with different types of memory chips mounted on a VME PowerPC board. Continuous write/read/compare operation showed:

- DRAM 512 Kbytes, up to 25 Gy, no error,
- EEPROM 512 Kbytes, up to 25 Gy, no error,
- NVRAM 8 Kbytes, during 21 hours up to 10 Gy, 7 errors,
- SRAM 512 Kbytes, exposed during 61 hours up to 4.5 Gy, 652 errors and then during 143 hours up to 10 Gy, 1863 errors.

Three standard VME power supplies, well known and used in large quantities since many years at CERN, broke down very rapidly. The first after 250 hours with a dose of 14 Gy, the second after 126 hours with a dose of 10 Gy and the third after 6 hours with a dose of less than 0.3 Gy. All three showed the same fault: a power MOSFET transistor breakdown, probably due to single event failures.

Tests on a 200 meter fibre cable, containing 12 mono-mode fibres and 12 multi-mode fibres, have been done. As expected, the multi-mode fibres showed an attenuation of some 50db per km while the mono-mode fibres only a loss of 8 dB per km at a dose of 80 Gy.

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Analogue and digital telephone equipment went definitely faulty. An RNIS bus did not reply anymore after some 15 days operation having received a dose of some 30 Gy.
5.6 Improvement Plan for the On-Line Radiation Test Facility.

Following the first year of exploitation of this on-line radiation test facility experimenters have expressed their wish for some improvements.

In particular a radiation protected zone is needed to install the responder modules, power supplies and some measurement equipment. This will be possible in a gallery perpendicular to the present beam lines. Sample measurements have shown that a radiation dose ten times lower than in the active zone can be guaranteed in that place.

In order to better understand the tests results some experimenters would like to know the particle composition of the beam, the energy spectrum of the particles, the geographical in-homogeneity of the beam and the reliability of absolute calibration of the radiation measurements.

A study of these requirements is being done and an improvement plan of the on-line radiation test facility is being drawn-up and will be discussed with the experimenters. The implementation is planned to be done during the next winter shutdown of the SPS accelerator.

6. CONCLUSIONS

At the time of publication we have several preliminary radiation results on electronic components and systems to be installed in the tunnel of the LHC machine.

More statistic is needed but experimenters can already draw some conclusions for their particular application. Identification and replacement of sensitive components will improve the radiation hardness of this electronic equipment.

These preliminary results demonstrate clearly that testing and qualification of all COTS electronic equipment for the machine will be necessary, despite the low level of radiation expected in LHC tunnel.

7. ACKNOWLEDGEMENTS

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I am grateful to the members of the Working Groups on Tunnel Electronics (TEWG) and on Radiation (RADWG) for all the information they have provided.

The various electronic components and systems and their tests are under the responsibility of numerous users; I thank them all for their collaboration and for having communicated their results.

8. REFERENCES


ELECTRONICS FOR HIGH-ENERGY PHYSICS EXPERIMENTS IN THE GIGA-SCALE INTEGRATION ERA

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Abstract

VLSI technology is being driven to giga-scale levels of integration with IC minimum feature dimensions approaching atomic scales. System-level integration is now pursued as critical in major commercial applications including wireless communication, computing, and multimedia. On-chip signal integrity, noise, and electromagnetic compliance (EMC) are becoming “show-stoppers” in addition to escalating wafer costs. This paper will identify major technology developments and applications in the commercial market and discuss how the high-energy physics community can leverage these advances in years to come. The role of the university research will be discussed as well as new opportunities for collaborative efforts.

1. OVERVIEW AND INTRODUCTION

Functional integration is becoming the dominant industry driver, as systems realize the benefits of reduced IC count, shorter interconnect lengths, and lower power dissipation. System integration, which began with digital functions such as processors and memories, is now being extended to include analog signal processing (ADCs and DACs), RF telecommunications, power generation and conditioning, and pixel sensors. Table 1 lists some of the requirements of these integrated systems from the perspective of HEP experiments.

<table>
<thead>
<tr>
<th>Table 1: Performance Requirements</th>
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<tr>
<td>System</td>
</tr>
<tr>
<td>Computing bandwidth</td>
</tr>
<tr>
<td>Embedded memory</td>
</tr>
<tr>
<td>Signal processing sensitivity</td>
</tr>
<tr>
<td>Communications</td>
</tr>
<tr>
<td>Low bit error rate</td>
</tr>
<tr>
<td>Power conditioning</td>
</tr>
<tr>
<td>Power levels</td>
</tr>
<tr>
<td>Radiation hardness</td>
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<tr>
<td>Temperature ruggedness</td>
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1.1 Bulk and SOI CMOS

Two flavors of CMOS, bulk and SOI, are available for systems integration, each having specific advantages and limitations. Figure 1 compares the cross sections of a device implemented in bulk and SOI.

Bulk has typically better radiation-hardness considering it has no buried oxide with its associated interface traps. SOI, however, offers better isolation given that the buried oxide prevents device crosstalk. Within SOI, both partially and fully depleted implementations are possible. Although fully-depleted SOI provides better electrical performance, the top-gate threshold voltage is linked to the buried oxide potential and is therefore more susceptible to long-term irradiation than PD-SOI. SOI, despite somewhat poorer radiation tolerance, is an ideal candidate for systems integration. The dielectric isolation permits the co-fabrication of many different...
systems, in which the performance of each can be uniquely optimized. Samples are shown in Fig. 2 of SOI implementations of merged power and logic devices, pixel sensing, and combined mixed-signal and RF functions.

Delivering these integrated systems, however, requires the solution to many challenges in signal integrity, noise, EMI, technology optimization, and testability. These issues will be discussed throughout this paper.

Figure 2: SOI implementations of (a) merged power and logic devices, (b) pixel sensing, and (c) combined mixed-signal and RF functions.

1.2 Wide Bandgap Semiconductors

In addition to silicon technology, wide bandgap semiconductors such as SiC and GaN are attracting some commercial attention for harsh environments. Although they promise new levels of temperature and radiation robustness, each is immature with numerous material and device challenges remaining. Neither will compete with Si in functional integration applications until these fundamental limitations are overcome. Figure 3 compares the bandgap of three common semiconductors.

Figure 3: Comparison of wide bandgap semiconductors (Si, SiC, GaN).

1.3 Technology Observations

Despite the wealth of available technologies for commercial and research purposes, semiconductor technologies remain expensive and designs are becoming more sensitive to process variation. Figure 4 identifies some of the trends in IC manufacturing. Complexity has grown commensurately with lithography scaling. Unfortunately, the modeling of these devices has not progressed as effectively. Short-channel effects, gate oxide tunneling, and hot carriers already challenge accepted models. As devices progress below 0.1 µm additional quantum characteristics will demand further characterization and theory.

Apart from purely commercial applications in which power dissipation, form factor, and performance are the key criteria, many of the environmental factors present in HEP experiments are not modeled. For instance, radiation hardness and SEE behavior are not common traits tested by commercial manufacturers. This additional shortcoming is another roadblock to the widespread adoption by the HEP community of off-the-shelf components.

Functionally integrated systems are appearing in consumer markets to meet these demands for compact electronics. But, as device scaling continues to push the envelope toward low-voltage and low-power operation many second-order effects begin to dominate such as EMI, coupling, signal integrity, and non-uniform internal heating. Functionally integrated systems, however, demand additional attention to global signal coupling and isolation, architectural optimization, and power vs. performance tradeoffs.

In following sections the current state-of-the-art in several integrated systems is presented. They show the trend in performance and power metrics with an indication of the COTS suitability for HEP electronics. Many systems in HEP and commercial products have similar performance requirements. The comparison neglects the differences (primarily in reliability and environmental ruggedness) and focuses on performance and efficiency of the electronics.
1.4 HEP and Commercial System Similarities

As listed previously in Table 1, many electronics systems comprise the hardware for HEP experiments. Although no commercial application combines the same functional requirements, trends in industry toward functional integration are producing several single-chip solutions to electronics subsystems. A summary of these subsystems is shown in Fig. 5.

Each bubble represents a key market segment. To accommodate new products, particularly in wireless services and multimedia, crossover integration is appearing. For instance RF systems may incorporate digital circuits for baseband processing or a mixed-signal IC may include power management.

The systems selected for review are drawn from this figure: processor/memory, data bus, signal converters, RF, and power management and generation.

2. DIGITAL SYSTEMS

The performance of digital electronics is primarily determined by the processor to memory bandwidth. A typical system block diagram is shown in Fig. 6. It reveals that internal bandwidth far exceeds the capacity of external storage and I/O to supply data. Despite trends to integrate memory closer to the processor, as shown in Fig. 7, bandwidth still limits performance. Two solutions are under investigation for removing the bottleneck. The first involves placing a small set of logic gates into a full memory (DRAM) process: processor-in-memory. The second inserts a small DRAM macrocell into a microprocessor technology: embedded DRAM.

Figure 4: Trends in IC manufacturing complexity with a five-year projection (from Semiconductor Consulting Services, www.semiconsulting.com).

Figure 5: Common systems undergoing functional integration to single-chip products.

Figure 6: Typical digital system block diagram.

Figure 7: Trends in memory integration.
2.1 Processor-in-Memory

Processor-in-memory (PIM) systems currently integrate on the order of 100K to 500K gates as shown in Fig. 8. This architecture has been most successful for large parallel systems in which simple arithmetic, logical, or conditional operations are to be performed on mass data. Typical examples include image processing, search routines, and associative memories.

2.2 Embedded Memory

Embedded DRAM macros presently include up to 32Mb by combining smaller 8-Mb macros as shown in Fig. 9. This technology is more process sensitive than PIM since the DRAM is produced in a logic technology. It offers more support for general-purpose computing than PIM and is the likely format for future microprocessors and DSPs. Current applications include complex signal processing that requires high-speed memory intensive algorithms.

2.3 Memory Partitioning and Optimization

One result of the variety of memory integration approaches and the diversity of logic and memory technologies is a need for new techniques to optimize processor-memory architectures. Shown in Fig. 10 is the resulting performance of five architectures after scaling. We have shown that embedded memory alone does not guarantee best performance [1]. Architectural design remains important, and may scale non-uniformly.

3. ANALOG - DIGITAL CONVERSION

A critical circuit element of many commercial and research electronics systems is the analog-to-digital (ADC) or digital-to-analog (DAC) converter. Although digital electronics dominate high-speed computing and signal processing, the fundamental analog nature of real-time signals requires a translation between the domains. Specifications include power dissipation, sample rate, and bit resolution. These requirements are mutually exclusive, so application-specific designs typically sacrifice one characteristic for another.

Many topologies exist, usually with inherent advantages for either resolution or sample rate. The comparisons below do not distinguish between topology.
3.1 Digital to Analog Converters

Most recent systems favor 10-12 bit resolution to deliver high-quality audio modulation. A few high-resolution (>15 bit) cases exist, but they have considerably lower sampling rates. Typical applications include audio telecommunications and dynamic contrast or threshold control in pixel imagers.

3.2 Analog to Digital Converters

Figure 12 shows a nearly linear trend from low-res, high-rate to high-res, fast-sampling ADCs. The trend reflects the demand for digital signal processing and the need to provide an optimal balance of rate vs. resolution during digitization. Specific topologies yield high-rate (flash) or high-resolution (∑-∆) conversion. Multiple architectures such as parallel, pipelined, and folded exist to improve effective conversion rate or for error correction.

![Figure 12: Trends in ADCs (circle area is proportional to power dissipation).](image)

3.3 Wide Bandgap Semiconductors

In high-speed and high-rate converters such as flash ADCs, a significant component of overall power loss is introduced by the auto-zero operation. Another component is the DC current flow through differential amplifier pairs. Figure 13 shows two current waveforms in a flash ADC before and after power minimization.

![Figure 13: Current waveforms in a flash ADC before and after power-reduction techniques.](image)

We have designed a flash ADC based on dynamic power reduction techniques that achieves a rate of 30-MSa/sec of 500-µV with a per-comparator power loss of 6.25 mW. Alternatively, it can be tuned to deliver 5-MSa/sec of 50-µV with a per-comparator power loss of 5.75 mW. This design was implemented in 0.8-µm SOI CMOS [2-3].

For a 0.35-µm SOI CMOS we expect performance with >100-MSa/sec of <10-µV with a per-comparator power loss of 1 mW

4. RF WIRELESS TRANSCEIVERS

The importance of RF wireless communications to consumer electronics is well established. For the HEP community, wireless telecom promises to eliminate many of the cabling and harness infrastructure that complicates system design and maintenance. Two areas of research are actively pursued. The first is monolithic RF technology to produce compact, very energy efficient radios. The second is architectures with noise suppression and harmonic cancellation to facilitate multi-channel communications with low bit-error rate.

4.1 Transceiver Topologies

Two common topologies are shown in Fig. 14. The shading in the first indicates the chip level implementation of the design. Filters limit the density of the packaging. Technology specific circuits, like Si bipolar mixers and GaAs power amplifiers limit the density of integration.

In the second case, one mixer/filter stage is eliminated by applying frequency translation directly to/from baseband. This zero-IF (direct conversion) transceiver is more amenable to single-chip implementations. Baseband filtering is achieved with digital processing, which can be integrated with the baseband A/D, D/A translation.

Future architectures are looking at extremely high sample rate ADCs and DACs to elevate the baseband processing closer to the RF carrier frequency.

![Figure 14: RF transceiver topologies in (a) heterodyne and (b) zero-IF formats.](image)
4.2 Noise Suppression Architectures

Multi-channel communication, especially using new simultaneous access protocols like CDMA, requires broadband linearity with a tight signal envelope. The former is largely a device and packaging matter to ensure correct matching and output characteristics for a full range of power and frequency ratings. The latter requires active cancellation of harmonics (3rd, 5th, and 7th).

Two techniques are shown in Fig. 15 for harmonic cancellation. Both produce out-of-phase components of the high-order harmonics, which when subtracted eliminate the non-linear noise.

![Harmonic cancellation](image)

(a) (b)

Figure 15: Harmonic cancellation using (a) feedback and (b) bi-directional control.

5. POWER MANAGEMENT

In consumer electronics, power efficiency is often a critical design requirement since many products are battery-operated. On chip power management has several levels of granularity, ranging from global sleep modes to a power-down of specific idle circuits. An enabling technology of power management is on-chip voltage conversion. Many board systems still require 3.3-V or 5-V signaling, but internal IC electronics may prefer <2.5V rails. An on-chip converter can therefore scale the voltage for active operation or suppress the rail voltage for low off-state leakage.

The efficiency of on-chip power electronics is limited by two factors: topology and passives. Unlike high-power electronics, in low-voltage electronics switching and conduction losses through the control devices can quickly lower efficiency below acceptable levels. For example, a diode forward voltage drop of ~1 V represents a significant percentage of the total rail voltage.

Similarly, VLSI passives are generally inferior to discrete elements. Passives in VLSI suffer larger coupling losses and a lack of magnetic materials.

5.1 Converter Topologies

Several integrated converter topologies have been reported, but these typically limit the integration to the digital control electronics; passives are mounted as discrete components. We have developed two generations of fully monolithic DC-DC converter for buck or boost applications [4]. They deliver output voltages as low as 1 V from an input of 3-5 V. Efficiency is over 85% at 100-MHz switching using a VLSI inductor with Q < 5. Its block diagram is shown in Fig. 16.

![Converter block diagram](image)

Figure 16: Block diagram of a fully monolithic DC-DC converter.

5.2 Integrated Magnetics

The current manufacturing hurdle for monolithic power electronics is VLSI integrable magnetics. Inductors and transformers are essential elements of power electronics circuits. Their quality factor, Q, directly impacts overall conversion efficiency, as shown in Fig. 17.

The current state-of-the-art in monolithic inductors and transformers is listed in Table 2. Magnetic material strongly improves Q, but its acceptance has been limited because of process incompatibilities with standard CMOS technologies. SOI suspended inductors are an alternative with similarly high Q, although they have been characterized only for RF performance. Their limited current handling may prevent their use in power circuits.

![Efficiency vs Output Power](image)

Figure 17: Trends in converter efficiency as a function of inductor quality factor.
Table 2: Monolithic inductor and transformer status.

<table>
<thead>
<tr>
<th>Quality Factor</th>
<th>Inductance</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VLSI Inductors</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.5</td>
<td>9.0 nH</td>
<td>spiral</td>
</tr>
<tr>
<td>5.7</td>
<td>3.2 nH</td>
<td>hollow core</td>
</tr>
<tr>
<td>20.0</td>
<td>1.0 nH</td>
<td>suspended</td>
</tr>
<tr>
<td><strong>VLSI transformers</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.2</td>
<td>9.0 nH</td>
<td>planar interwound</td>
</tr>
<tr>
<td>3.7</td>
<td>1.4 nH</td>
<td>planar interwound</td>
</tr>
<tr>
<td><strong>Micromagnetics</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>transformers</td>
<td>12.0</td>
<td>1.0 pH</td>
</tr>
</tbody>
</table>

6. POWER GENERATION

Looking beyond on-chip voltage conditioning and level shifting, on-chip power generation promises a new approach for harvesting energy from ambient sources. The simplest system is illustrated by the turbine, which in spinning drives a DC motor. A cross section is shown in Fig. 18. The prime mover fluid can either be an environmental feature (e.g. air or water) or a supplied energy source.

For HEP applications the chief advantages of local power generation are 1) the elimination of magnetic materials, 2) a reduction in lengthy wiring harnesses, 3) the decoupling of noise transients between the load and the energy source, and 4) its compact dimensions. A microturbine implementation is expected to occupy less than 1 cm$^2$ of surface area.

Figure 19 shows the theoretical performance of a MEMS microturbine. At 7000 rad/sec the generator yields 12 V and 22 W of short circuit power. It can be fabricated with CMOS devices, and SOI offers further options for isolation of MEMS and active devices using the buried dielectric.

7. RELIABILITY ISSUES

The integration of functional units with widely different dynamic signal characteristics, noise susceptibilities, and activity rates can lead to a significant deterioration of overall signal integrity. Spurious coupling effects also increase the standby power dissipation. As signal rates rise and die sizes shrink, more networks will become sensitive to these transient effects.

Figure 20 illustrates the boundary of transmission line effects for several technologies and physical implementations. As CMOS rise times dip below 10 ps, the transmission-line behavior of digital networks will become common. As Fig. 21 shows, technologies at feature sizes under 0.25-μm with advanced metallization will offer rise times well under 10 ps.

It is therefore necessary to consider the deleterious effects of coupling and impedance mismatch during the entire design phase. This is accomplished through partitioned interconnect routing, the insertion of redundant ground nets, and the insertion of broad ground planes.
Universities, however, have the resources and collaborations to effectively cultivate the talent for deep submicron functionally integrated system design. Using several research groups at the University of Illinois at Chicago as an example, the argument is presented that universities are ideally suited to act as design and verification centers.

Among the requirements of giga-scale integration are access to a breadth of CAD tools to model systems from the process level to the package/behavioral level. Figure 23 shows the CAD infrastructure resident at UIC. It represents an investment of $50 million and includes software from all major vendors: Analogy, Ansoft, CADENCE, HP EEsof, Silvaco, and Synopsys. It has been integrated into a comprehensive environment for the design and modeling of mixed-signal and RF systems.

Hosting the software is an 8-workstation clustered linked to a multiprocessor server. To support multimillion gate IC design and 10K mesh point finite-element analyses, the network offers over 5 GB of RAM and over 120 GB of permanent storage. The combined computing investment is over $300,000.

Finally, an extensive characterization and instrumentation suite is necessary to extract experimental data. We have a networked mixed-signal/RF testbed. It contains complete digital, analog, and RF experimental instruments and is linked with the computing resource to perform automated measurements and rapid modeling.

These groups at UIC have numerous collaborators within industry and federal research organizations, shown in Fig. 24. As a research entity, they have absorbed the state-of-the-art in design and validation of giga-scale integrated systems. Since industry presently has only a limited interest in radiation-hard electronics for harsh environments, it is necessary to join into teams such as these to address common interests and objectives.

UIC also has access to a variety of commercial and research-oriented foundries, listed in Fig. 25. Deep submicron CMOS offers a contrast to SOI technologies for investigating radiation-tolerance in scaled low-voltage architectures.

9. CONCLUSIONS

Many key components of commercial and HEP-related systems have been investigated with trends outlined toward giga-scale integration. These systems have common performance requirements, except that HEP electronics must survive harsh environments. In addition to anticipated performance limits, deleterious integration effects were discussed. Technology complexity and the lack of industry support for HEP needs limits the application of COTS products. Instead, collaborative research groups led by universities will serve as central design and verification centers by combining multidisciplinary expertise.
REFERENCES


DEVELOPING AND COMMISSIONING BABAR ELECTRONICS

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for the BABAR Collaboration

Abstract

Many aspects of the architecture and performance requirements of the electronics system for the BABAR Experiment are similar to those for the much larger LHC experiments. We briefly describe the requirements and architecture of BABAR Electronics, focusing on aspects that are similar to the LHC. We then discuss the experience of developing the system from design to operation, including such topics as prototype and system tests, manufacturing, grounding and shielding, integration, and initial performance. We focus primarily on front-end electronics, including IC development; however, we also discuss data acquisition.

1. INTRODUCTION

This rather informal paper is a recollection of the experience of developing and commissioning the BABAR Electronics System. Hopefully, this account can serve as a reminder to LHC electronics developers of some of the issues, concerns, and pitfalls to remember during the development process. This paper is not intended as a description of the BABAR Electronics System. A brief introduction will point out how the BABAR Electronics System resembles electronics systems under construction for the LHC experiments, despite the fact that it differs in scale. However, neither the common aspects of the system nor the detector-specific electronics will be described. Summary descriptions of these aspects can be found in the paper that I presented at the 1998 LHC Electronics Board Workshop [1] and in the papers to which it refers, and in references [2-5].

Furthermore, this paper is by no means a complete guide to the "Do's" and "Don'ts" of electronics development. It is anecdotal, relating personal impressions and the comments of people involved in the BABAR project. It recounts some of the problems and setbacks encountered during development of BABAR Electronics; however, it does not recount all. It also includes lessons learned by the individuals during prior projects that were felt to have been successfully applied to BABAR.

Several of the other leaders of the BABAR electronics development contributed to the preparation of this paper. I have frequently included their comments verbatim in the text. In these cases, I have chosen to include their comments as quotations without identifying the specific contributor since these comments were often informal. The contributors of the quotations are identified in the Acknowledgements.

2. THE BABAR EXPERIMENT

The BABAR Experiment will study CP violation at the SLAC B-Factory. Its detector consists of five major systems: a silicon vertex tracker [6], a cylindrical drift chamber with dE/dx capability [7], a particle identification system (DIRC) based on imaging of Cerenkov rings [8,9], a cesium-iodide crystal calorimeter [10], and a muon identification system (IFR) based on resistive plate chambers [11]. The specialised requirements of each detector system are addressed by front-end electronics customised to the detector technology but integrated into a uniform data acquisition architecture.

3. BABAR ELECTRONICS OVERVIEW

In order to address the requirements of its detector and operating environment, BABAR has designed an electronics, trigger, and data acquisition architecture that is quite similar to architectures being designed for the LHC. For instance, the BABAR architecture is multilevel, pipelined, and nearly deadtime free. It employs detector-specific custom ICs to realise the full performance of detector systems. Front-end electronics is detector-mounted. It simultaneously digitises analogue signals, writes data to buffers, and is read out to the data acquisition system. Although analogue front-ends and
Digital readout circuits are located in close proximity, full analogue performance has been realised without digital noise. The trigger system has two levels, with the option for an additional intermediate level. The first level trigger is based on pipelined hardware processors and utilises tracking and calorimeter data. The higher level trigger is based on an online event-processing farm of commercial processors and is integrated with a network-based event builder into the data acquisition system. The online system also includes a prompt reconstruction phase that performs full “offline” processing of the data.

The BABAR design incorporates an unusual level of standardisation across detector-specific subsystems. Front-end electronics is customised to detector-specific needs; however, front-end buffer architecture and front-end links and protocols, for both readout and control, are standard. All off-detector electronics is standardised. The BABAR Readout Module provides standard interfaces to timing, data acquisition, and detector controls systems. It also provides a standard protocol and architecture for front-end-specific pre-processing and calibration code. Data acquisition crates, fast control and timing modules, and much detector controls hardware are also standard across BABAR systems.

All front-end electronics subsystems of BABAR share a common architecture. Each front-end chain consists of an amplifier, digitisation (discriminator or flash ADC), a circular buffer (to store data during level 1 latency), and a derandomizing buffer (to store data between the level 1 accept and transfer to a Readout Module). Analogue signal processing, digitisation, and data readout occur simultaneously. All front-end subsystems except the IFR provide data sparsification. All level 1 latency buffers are digital; hence, it is possible to store data longer than analogue buffers would allow. The buffers of all front-end systems are managed by a common protocol. All level 1 latency buffers function as pipelines of fixed length, and all derandomizing buffers function as FIFOs which are capable of storing a fixed number of events, regardless of the actual implementation of the buffers. For instance, in the readout IC of the vertex detector [7, 8], the derandomizing buffer holds four events in a series of a registers, two buffers, and the sparsification logic; whereas, in the drift chamber digitizer IC [9, 10], the derandomizing buffer is an SRAM that stores waveforms for four events.

Each front-end subsystem also shares standard BABAR interfaces to the detector-spanning, or common, electronics subsystems. In all cases, the front-end electronics is mounted directly on the detector for performance reasons. This solution also substantially reduces required cable plant. The design of each detector-specific subsystem balances its individual and common requirements in order to achieve a cost-effective, robust, and easy to maintain implementation. Custom integrated circuit solutions have been adopted for four of the five detector subsystems. Seven custom integrated circuits were developed.

### 3.1 Catalogue of BABAR custom ICs

For the silicon vertex detector, a 128-channel amplifier/discriminator IC (ATOM) [2,12-15] was developed by Pavia, LBNL, and Santa Cruz. It features a programmable shaping time and a 4-bit, time-over-threshold pulse height measurement. It contains a level 1 latency buffer, sparsification, derandomizing buffer, readout control logic, and a 60Mpbs serial output. It was fabricated in Honeywell rad-hard 0.8µm CMOS.

For the drift chamber electronics [3], a four-channel amplifier/shaper IC (DCAC) with analogue and discriminated outputs was developed by Santa Cruz in Maxim Cpi semi-custom bipolar. In addition, an 8-channel drift chamber digitizer chip (ELEFANT) [16-18] was developed by LBNL. It features a TDC with 1ns bins and a 15MHz, bilinear, 6-bit flash ADC for each channel. It also includes a level 1 latency buffer, sparsification, and derandomizing buffer. It was fabricated in Hewlett Packard triple-metal 0.8µm CMOS.

For the DIRC electronics [4], an eight-channel, low-noise, amplifier for phototube signals with zero-crossing discriminator and a multiplexed analogue output [19] was developed by Orsay in AMS 1.2µm CMOS. A 16-channel DIRC Digital Chip [20] containing TDCs with better than 250ps linearity was developed by LPNHE Paris 6-7. It also contains a programmable level 1 latency buffer, sparsification, and derandomizing buffer. It was fabricated in Atmel-ES2 double-metal 0.8µm CMOS.

For the calorimeter, a single-channel low-noise amplifier chip was developed by SLAC. It contains only one channel for reliability/redundancy reasons. It also provides a split-range output and a cable driver. A 4-channel Calorimeter Auto-Ranging & Encoding chip (CARE) [5] was also developed by SLAC. It provides a sample & hold on four amplitude scales and encodes the index of the scale of interest. Both calorimeter chips were fabricated in AMS 1.2µm CMOS.

### 4. ORGANIZATION

#### 4.1 Organisation of the Electronics System

The BABAR Electronics System incorporated all electronics related activities into a single comprehensive electronics working group. The Electronics System included front-end electronics, data acquisition, trigger, including the level 3 trigger, electronics for detector controls, and electronics infrastructure. The only electronics components that were not provided by this overall working group were the detector-mounted components (readout IC and hybrid) of the vertex detector, although the overall electronics organisation was involved in reviews of these components. In general,
the same working group also provided all software directly associated with electronics. For instance, the software of the data acquisition system, of the level 3 triggers, and for electronics initialisation, diagnostics, and maintenance was provided by the electronics working group. Of course, the overall working group included subgroups working on subprojects, such as drift chamber electronics, and these subgroups further split into smaller subgroups as appropriate.

The purpose of organising all the electronics in a single detector system working group was to facilitate co-ordination and to foster common solutions. As commented by a leader of one of the electronics subsystems, "The grouping at the design and realisation phase of all electronics in one electronics group proved very effective to assure commonality and uniformity. The caveat here is to maintain enough relationship with the subdetector here, but this is not very hard to achieve." We found that the bond between individual electronics subsystems and their respective detector systems was sufficiently strong that it was not necessary to explicitly place the electronics subsystem group within the detector system organisation. We found that our organisation bound together, in a closer way than would otherwise have been possible, all the electronics subsystems, including the trigger and data acquisition systems. This organisation worked quite well throughout the construction project. It contributed to a coherent overall system design, including shared design solutions among electronics subsystems. It contributed to the constructive attitude of design reviews performed by peers. It resulted in subsystems helping each other during design and during implementation. It also afforded the project leaders flexibility to redirect resources and effort when necessary.

4.2 Working with multiple institutions

When a working group consists of a large number of institutions, there is need for good communications and frequent contact. The \textit{BaBar} Electronics working group included about 28 institutions from five nations. One of the electronics subsystem leaders commented, "Developing electronics with the involvement of several labs on two continents requires very good communication between teams. Thanks to the Web and videoconferences, it is now easy to exchange quickly any kind of documents. However, at the very beginning and at the end obviously, nothing can replace meetings and work \textit{in situ}." Even with the Web and video conferencing, significant travel is needed as part of the communications. Participants must travel to meetings regularly, although not all participants from each institution need to travel to each meeting. During the design phase, \textit{BaBar} held meetings of the overall working group about six times per year, at four collaboration meetings and at two additional electronics workshops. These meetings were held both in the U.S. and in Europe, with at least two per year in Europe.

The electronics co-ordinators, particularly at the level of the "system manager" and "system engineer", must also perform site visits to demonstrate their interest, to foster close co-operation, and to meet the participants at institutions that they might not meet through meetings. Site visits of course also offer the opportunity to see first hand the facilities at participating institutions and to see the work being performed.

In multi-institutional projects, design reviews are even more important than they otherwise would be. This importance is because they help compensate for difficult communications. For instance, they provide a critical opportunity to carefully examine interface definitions and implementations of interfaces.

By paying attention to the need to communicate, that is by arranging frequent meetings and providing mechanisms for communications between meetings, it is possible to draw upon the strengths of many institutions without compromising the integrity of the electronics design. It is important to have at least one very qualified person at each institution in order to make certain that work is on track and compatible with the overall system design. The importance of communicating between meetings should be stressed. The timely completion of the project requires that questions and open issues not be left unanswered or unresolved until the next meeting. Email, telephone, or special meetings should be used to resolve issues promptly as they are identified and as resolution is needed.

5. REQUIREMENTS

Defining requirements at the outset of the project is essential. Requirements provide the yardstick against which performance of prototype and production systems is measured. Without this metric, the collaboration risks that the system under development will not meet the performance requirements of the experiment. There are also the risks that the design effort will not converge as the design team strives for unnecessary performance or that the design solution will be unnecessarily complex, causing undue technical risk.

Requirements should be realistic. Overly stringent requirements can cause the same risks relating to unnecessary performance and complexity mentioned above. Proper discourse between physicists and engineers during the definition of requirements, and ultimately throughout the design and prototyping phase, can help tremendously in achieving a set of requirements that are both adequate and practical.

Achieving appropriate design solutions requires a good knowledge of the problem being addressed, including an understanding of the context of the problem. This
knowledge and understanding can be more difficult to achieve in the multi-institutional efforts of large experiments. As observed by one of our electronics subsystem leaders, "With the growing size of the experiments, it is more and more important that people work with a sufficient knowledge of the context in the experiment, where a piece of circuitry is sitting, how it is intended to be used, which issues can be expected if some requirements are not met." An appropriate set of requirements properly defines the problem to be addressed. Documentation explaining the requirements can provide an understanding of the context.

When defining requirements, one should keep in mind that "Simple is beautiful!" Again, collaborative projects exacerbate the tendency to define requirements or design solutions that are unnecessarily complex. As observed by one of our electronics subsystem leaders, "Everyone can add features that delay and sometimes compromise the main goals. Unnecessary complexity is often the result of too many people interacting. This is a drawback of easy communication." The tendency towards complexity should be properly checked. Why take undue technical risk? That risk leads ultimately to cost risk, schedule risk, or both.

Requirements should be documented. Documentation is necessary in order that the requirements are not forgotten during the design process. It also makes the requirements available to newcomers on the project. In addition, the motivation or justification for each requirement should be documented. Documenting the justification enables designers to understand and recall the origin of any requirement, frequently enabling a designer to question a requirement that is proving difficult to satisfy. Documenting the justification for requirements also provides a method of checking that requirements are still valid as time passes and a project evolves, in case the underlying assumptions of some key requirement change.

6. SYSTEM DESIGN

A coherent system design is the central component of an adequate technical solution. The system design should be developed first, before developing detailed solutions to aspects of the overall problem. The system design should be developed from the "top down" from the requirements that should be addressed and from a clear vision of a solution that addresses the entire scope of the task. "Bottoms up" designs, which derive from a solution to only a part of the task or that originate in a desire to employ a particular technical solution, should be avoided. Although it seems obvious to say that the first step in design should be a top-down system design, in practice, design often does not happen that way.

For Babar, we felt that it was important to develop a system design with unified solutions for the mechanisms that control the front-end electronics, for data acquisition for all front-end electronics subsystems, for monitoring of electronics, and for slow control and monitoring of detector systems. Such common solutions simplify the overall design and greatly ease integration.

When establishing common solutions, it is important to gain acceptance of all electronics subsystems and to give subsystems flexibility in the detailed implementation of the solution. Acceptance is of course important to the completeness and success in the implementation of common solutions. In Babar we gained acceptance by involving the entire community, through the overall electronics working group, in the development of Babar protocols and standards. Flexibility in the detailed implementation of common solutions allows subsystems to tailor protocols and standards to the details of their system. Allowing subsystem-specific details in the implementation also helps subsystem designers to take "ownership" of the design of their subsystems.

Each design team should understand its requirements, and it should depart from convention when a departure simplifies system design or allows an important optimisation. For instance, although Babar adopted a "standard" deadtimeless, multilevel architecture, certain characteristics of Babar allow its architecture to incorporate some unusual features. For instance, all level 1 latency buffers in Babar are digital, i.e. there is no analogue storage during the level 1 latency. This characteristic allowed Babar to adopt an unusually long level 1 latency (12.5 µs) without impacting the cost of front-end electronics. The benefit of this long latency was a level 1 decision time significantly longer than usual values of two to five microseconds. The longer decision time simplifies trigger requirements and reduced the cost of level 1 trigger. Similarly, modest hit occupancies in Babar detector systems result in bandwidth requirements that fit comfortably within the capabilities of existing optical link technologies. The resulting headroom in bandwidth facilitated adoption of a "data-pull" architecture between the buffers in the front-end electronics and the data acquisition system, as opposed to a "data-driven" or "push" architecture, without a consequent increase in deadtime. This architecture avoids data loss, and it greatly simplifies buffer management and event synchronisation.

In order to result in a high performance system that is easy to bring into operation, the system design must include attention to power supplies and power distribution, grounding and shielding, cabling, and cooling. These are demanding areas that require attention during the design phase in order to avoid awkward remedies to problems discovered during commissioning. In Babar, we were fairly successful in achieving attention to detail; however, problems arose in some areas where we were not sufficiently attentive. For instance, one of our front-end subsystems required several retrofits
to the location and mounting of electronics on the detector.

Because system design demands insight into requirements, a broad view of possible technical solutions, and attention to detail, an experienced electronics engineer can contribute invaluably to the success of the system design.

6.1 Connectors and connections

With respect to reliability and signal integrity, connectors and connections are often the weakest link of the electronics chain. Furthermore, connection problems can be very difficult to diagnose. For instance, in BABAR, we had a problem with some of the backplanes in our data acquisition crates. These were custom backplanes that we fabricated separately from the crates. They were somewhat thicker than a standard backplane, and the pins did not always contact the pathways in the backplane. Contact would sometimes be lost when cards were plugged into the crate, resulting in unpredictable behaviour of the backplane that could not be diagnosed by interchanging modules and spares.

Because problems with connections can be difficult to diagnose, they should be avoided in advance by careful consideration during the design phase. Testing, both during the design phase and during production, can help avoid problems. As commented by the leader of one of our electronics subsystems, "Pay special attention to cables and connectors. Get the best quality you can afford. Cheap connectors in particular can lead to lots of headaches. Make sure the vendor does a thorough test of each cable (not just a random sampling of connections). Specify what resistance constitutes an open or a short. Get an early sample and give it a workout to see if any shorts or opens develop. We thought we had done this, but when we actually started working with the cables we wished we had spent even more on connectors."

Problems with connections often arise when the electrical connection also provides mechanical support. To avoid such problems, always provide mechanical support that is independent of the electrical connection. A simple example is to strain relieve cables where they connect to printed circuit boards. Electrical connections can also be broken due to mechanical stress in the connections between motherboards and daughterboards if adequate mechanical support is not provided. For instance, in BABAR we experienced problems between two detector-mounted boards on the calorimeter. Our calorimeter Input/Output Boards (IOBs) directly plugged into right-angle connectors on ADC Boards (ADBs). The electrical connection between the connector and the board on the ADBs was frequently broken during mounting or remounting of the IOBs. This type of problem is particularly insidious because a new problem (a broken connection on an ADB) can easily be created when trying to remedy an existing problem (a failure on an IOB).

6.2 Grounding and shielding

Details of grounding and shielding are critical to the performance of analogue front-end electronics. Each electronics subsystem needs to invest careful design in its grounding and shielding plan. In fact, one subsystem with poorly designed grounding or shielding can adversely affect other subsystems.

In BABAR, we had a fairly successful experience with grounding and shielding in our final installation. Detailed grounding and shielding plans were part of design and were included in design reviews. In summary, detector subsystems in BABAR are isolated from one another. Each has a single point ground. Extensive work was done on grounding and shielding during prototype and system tests. Consequently, relatively little further work was needed during final installation. The in situ performance exceeds requirements, and is as good as on the bench. The one exception is the calorimeter power supply problem discussed in Section 12, the whose remedy is presently being implemented.

7. PLANNING

Planning a project such that enough time is allocated to each stage of the project, for instance to design and prototyping, procurement and fabrication, and installation and commissioning, can be important to the timely success of the project. It is particularly important to budget adequate time for design. Adequate time on design can avoid later problems, as pointed out by one of the leaders of our electronics project, "Spending sufficient time to make sure the design (overall and detail) is right and that it communicates properly with other parts is very important, since making it later work by testing and debugging the hardware is much more time consuming and expensive."

In order to maximise the amount of time available for design of BABAR electronics, while budgeting adequate time for subsequent project phases, we drew up our project schedule by planning backwards from the earliest date that electronics could be used by each detector system. In reverse order, we conservatively scheduled time for commissioning, installation, testing, production, and prototyping. Then we added some schedule contingency to our estimates for those phases. Finally, we allocated all the remaining time for design. Fortunately, we performed this planning exercise sufficiently early that this approach led to ample allocations of design time.

7.1 Design iterations

For all board-level components, we scheduled three iterations: one full-functionality prototype, one preproduction model, and one production run. In some cases, the full-functionality prototype was preceded by partial prototypes. The preproduction model was intended to be identical to the production version and was intended to
validate the final design, although in some cases we allowed further small design changes between the preproduction model and the production version. In such cases, we generally assembled and tested first articles of the production design before assembling the entire production run. Likewise, for high volume items, we also generally assembled and tested first articles before completing the full system.

For custom integrated circuits, we planned for more prototyping rounds than were budgeted for board-level components. Our experience was that our custom ICs required between four and eight iterations in total from prototype through production. Our Drift Chamber Amplifier Chip (DCAC), of which we needed approximately two thousand chips manufactured in a Maxim CPi semi-custom bipolar process, required about five iterations (1 prototype run, 2 preproduction runs, and 2 production runs). This number of preproduction and production runs included mistakes made by the manufacturer which, although not really design iterations, nevertheless cost time in our schedule. Our Drift Chamber Digitizer Chip (ELEFANT) [16-18], of which we needed about one thousand chips in a Hewlett Packard triple-metal 0.8µm CMOS process, required about four iterations (preprototypes of key functional blocks, 1 full-functionality prototype run, 1 preproduction run, and 1 production run). Our DIRC Analogue Chip [19], of which we needed about 1500 chips in an AMS 1.2µm CMOS process, required about six iterations (3 prototype runs, 2 preproduction runs, and 1 production run). Our DIRC Digital Chip [20], of which we needed approximately 750 chips in an Atmel-ES2 double-metal 0.8µm CMOS process, required approximately five iterations (3 prototype runs, 1 preproduction run, and 1 production run). Our Calorimeter Amplifier Chip, of which we needed approximately thirteen thousand chips in an AMS 1.2µm BiCMOS process, required approximately eight iterations (1 semicustom preprototype run, 3 prototype runs, 1 preproduction run, and 3 production runs). In this case, the number of production runs included issues beyond our control at the manufacturer. Our Calorimeter Auto-Ranging & Encoding Chip (CARE) [5], of which we needed approximately two thousand chips in an AMS 1.2µm BiCMOS process, required approximately seven iterations (1 semicustom preprototype run, 3 prototype runs, 1 preproduction run, and 2 production runs). Again in this case, the number of production runs was increased by incidents beyond our control. Note that the above statistics are not exact, and do not count multiple prototyping and production runs in the same way from chip to chip.

7.2 Manpower

In BABAR, one of our biggest problems was the loss of engineers during the project. This problem was particularly significant at U.S. and U.K. laboratories. We suffered many delays from this problem. For example, on the vertex detector readout IC, as described by one of the project leaders, "We basically had 100% turnover of the U.S. engineers, which was a real nightmare. Luckily, the Pavia group stayed on the project and provided some continuity ...". Loss of engineers during the project was primarily caused by job opportunities in industry.

Engineers are still needed after the design and prototyping phase. They are needed through the debugging and commissioning phase as well. As observed by the leader of one of the BABAR electronics subsystems, "With the long time frame [of the project], we couldn't keep any engineer on board, and had no engineer available for debugging. This really hurt." Engineering work is not complete until the readout system is fully commissioned and operational.

The possibility of losing an engineer during a project, means that having a single engineer working on a complex, critical project is dangerous. As stated by the leader of one of BABAR's electronics subsystems, "I think the main lesson is to have few or no one-engineer sub-projects, since they become zero or minus one engineer projects with Poisson statistics." For instance, at one point, we lost the one engineer working on our Readout Module that serves all detector systems. Although we recovered in time to complete Readout Module production on schedule, this debacle delayed our data acquisition software development by many months, making it much more difficult to prepare detector-specific software for commissioning. The loss of this engineer was such a significant setback for BABAR that it is perhaps worthwhile to describe how we recovered, and, in this account, to sketch the design of the Readout Module as it was completed.

7.3 The BABAR Readout Module

When the lead engineer for the Readout Module (ROM) design left the project unexpectedly in late summer 1996, a prototype ROM had already been built, and the design of the preproduction model of the ROM was largely complete. Nevertheless, in order to complete the ROM project as rapidly as possible, we decided to start a new design that was quite different from the original. The new ROM conceptual design addressed the same requirements as the original; however, it had the added goal of not requiring the same high level of engineering, i.e. to require a level of engineering less sophisticated than the original design. The new design did benefit from some of the experience gained during the initial design. Being modular, it facilitated multiple engineers to participate in the design, and it also somewhat decreased the coupling between ROM hardware design and data acquisition software design. The production cost of the new solution was more costly than would have been the case with the original design, because the new design uses embedded commercial CPU
boards. Nonetheless, the additional production cost was offset by reductions in the number of ROMs required and by reduced engineering costs. The new design and first prototype of this complex module was completed in just over one year.

The implementation of the BABAR ROM consists of four printed circuit cards that assemble into a single-width 9U VME module. A commercial single board VME computer (Motorola MVME2306) running a real-time operating system (Wind River VxWorks) buffers and processes data and interfaces to VME. A custom controller board provides the interface to the fast control and timing system and manages front-end buffers and the transfer of data. A custom personality module interfaces to the controller card via a private bus and interfaces to the front-end electronics through BABAR-standard control and data links. There are two types of personality module. The first type is used by all detector systems for control and by all systems except the calorimeter for data transfer. The second type is used only by the calorimeter for data transfer. Finally, a custom PCI mezzanine card (PMC) interfaces between the CPU and controller boards and provides the DMA engine (Intel i960) for data transfer from event data buffers on the personality card to CPU memory via a PCI/i960-bus bridge.

8. REVIEWS

Reviews played an important role in the development of BABAR Electronics. We instituted a series of three design reviews for each component or subsystem. The general scheme of our reviews followed a plan proposed by R. Jared of LBNL for the SDC Experiment. Our system of reviews was fairly similar to those of the quality assurance plan of the Rutherford Laboratory. Each electronics subsystem and each electronics component, either IC or board, underwent a series of three reviews. The three reviews were:  

**PDRR+CDR:** This review was the Preliminary Design Requirements Review and Conceptual Design Review. It was held when requirements definition and conceptual design were complete and before detailed design began. It reviewed the appropriateness of the requirements that had been defined, and it reviewed whether the proposed conceptual design addressed requirements.

**PDR:** This review was the Preliminary Design Review. It was held following completion of detailed design and before fabricating the first full-functionality prototype. It was a detailed review of interface specifications and schematics. It also reviewed results of partial prototypes.

**FDR:** This review was the Final Design Review. It was held following completion of prototyping and of system tests and before production fabrication was started. It focused on completeness of the detailed design and on results of prototype and systems tests, where test results were measured against the requirements that had been defined at the first review. The Final Design Review also reviewed plans for acceptance testing of production units.

For integrated circuits, there were often additional design reviews before each submission.  

Note that BABAR electronics reviews were tied to milestones in each subproject. Consequently, each review was held when there was a definite purpose to the review. BABAR did not perform periodic reviews of the electronics. We felt that reviews tied to milestones were more effective than periodic reviews. Because the development of BABAR Electronics was rather rapid, the period between reviews for any subsystem or component was never longer than about nine months. Note that in addition to these reviews, each subsystem reported progress at collaboration meetings and electronics workshops.

In BABAR, most reviews were tied to the submission of fabrication runs. This timing avoids the unnecessary expense of fabricating something that will not work because it is designed to the wrong functional or interface specification. A leader of one of BABAR’s subsystems suggests, "Have a sign-off procedure so that no component can be submitted for production (prototype or final) until the people responsible for the components connected to it in any way (mechanical or electrical) have reviewed and signed off on the design. System manager should also sign. … [This procedure] caught many problems before it was too late."

Our review procedure was well accepted within the electronics leadership and community. As commented by one of the subsystem leaders, "The concept of regular reviews at fixed intervals in the project was a very good thing. Our own experience … was the first [PDRR+CDR] and final [FDR] one were very useful." Another comment was "Do reviews early on."

A qualified and appropriate review committee is essential to an effective review. In BABAR, each review committee included a physicist from the appropriate detector system who was familiar with its requirements and performance. The largest part of the review committee consisted of engineers and physicists from other electronics subsystems. These members were familiar with the architecture of BABAR Electronics and with the issues of concern in developing electronics. Each committee also included engineers and physicists from systems that interface to the system under review and who were familiar with interface requirements. Finally, each committee included one or two outside reviewers, who provided their experience and wisdom to the review.

Each BABAR electronics review required formal documentation. Electronics management provided the list of required documentation. Most of the required documentation was documentation that should be developed during the normal course of design; consequently, very little additional documentation was
required. For instance, the following documentation was required for the Final Design Review:

Updated materials from the PDR:
- Requirements Document
- Hierarchical set of block diagrams
- System Description (at level of block diagrams)
- Interface Specifications Document
- Grounding and Shielding Plan
- List of deliverables
- Cost estimate
- Production schedule

New materials for the FDR:
- Summary of design changes since PDR
- Detailed schematics of production components
- Mechanical drawings of production components
- Reliability analysis of components and of system
- Results of tests of individual preproduction units
- Results of system tests of preproduction units
- Quality Assurance Plan, including:
  - Production plans
  - Burn-in plans
  - Acceptance test plan
  - Maintenance plan
- Cooling and Access Plan
- Cable specifications (including safety ratings)

Documentation was circulated, usually by posting on the Web, approximately one week in advance of each review. We found that the review was generally not effective when documentation was not available well in advance.

For each review, the committee provided a written report. Before finalisation, draft committee reports were sent to the group being reviewed in order that factual errors in the report could be corrected. These reports served as recommendations to the Electronics System leaders. Written responses to committee reports were not requested. After consultation between the leaders of the Electronics System and the group under review, it was agreed which recommendations would be implemented. Generally all recommendations were implemented; however, there were cases when it was agreed that some particular committee recommendation should not be implemented, either because the recommendation was not practical or not in the experiment's best overall interests.

In order to allow the fullest participation of the group whose work was under review, and to foster the collaborative aspects of the review process, design reviews were usually held at the home institution of one of collaborating design teams.

In order to perform an adequate review, a design review must be sufficiently long to allow the committee to understand the design and to allow ample time for questions and discussion. In Babar, we felt that it was particularly important that the review committee be left with no outstanding questions or misunderstandings during their deliberations. Consequently, we also scheduled discussion following committee deliberations. Our electronics reviews were generally two to three days in length, although reviews of individual components were frequently performed in a single day.

Peer reviews can have a positive impact on the collaborative spirit and effectiveness of electronics development. As commented by one of the participants, "Reviews offer opportunities to exchange ideas, stay on (or leave a bad) track, get out of your computer screen."

9. MANAGEMENT

One purpose of project management is to help avoid setbacks and mistakes. The following comments are related to this purpose.

- Everyone involved in electronics development and management should appreciate that "If it can go wrong, it will go wrong." Fortunately, this statement is not completely true, but plan for setbacks.
- Problems don't go away on their own. If left unattended, problems only grow worse. Be proactive, focus on priorities, keep everything moving forward.
- There is no problem that cannot be solved, in a system that is well-designed and well-planned. Nonetheless, solutions often require time and/or money.
- Good system engineering helps avoid many mistakes and setbacks.

10. COST CONSIDERATIONS

Clearly, cost must be a consideration during design. Nevertheless, one must avoid undue technical risk when trying to reduce costs. In particular, systems should be designed to meet requirements in their first production iteration, even if more expensive. The cost and schedule impact of failing usually overshadows any small cost savings. As pointed out by one of the leaders of Babar Electronics, "Cutting cost in order to save money will cost a lot more later to fix the problem."

Cost considerations during parts selection can often lead to costly retrofits or long term problems. For example, Babar experienced a significant problem with reliability of the optoelectronics used to transmit data from the calorimeter to its Readout Modules. This subsystem used approximately 300 G-links and was experiencing about one failure of the optotransmitters per week until all transmitters were replaced. Failures caused loss of data, and required frequent resynchronisation of the troubled links. The problematic transmitters were not the same unit used during prototyping. Prototypes and other Babar subsystems used a transmitter from Finisar. The problematic transmitters were purchased because of lower cost. The units purchased were manufactured by Methode under license from Finisar. At the time of
purchase, we were not aware of the fact that the Methode parts we purchased used CD lasers; whereas, the Finisar units available at that time used VCSELs. Short lifetime of the CD lasers caused the problematic failure rate. In fact, Methode no longer fabricates the model that Babar used, and Methode Gigabit Ethernet transmitters use VCSELs. Until replacement, these transmitters were our largest reliability problem.

11. SYSTEM TESTS

System tests can avoid integration problems and problems of scale. A system test is a test of the complete readout chain, from front-end to data acquisition. It includes an actual or prototype detector, enough channels to detect large scale system problems, and actual power supplies, grounding, shielding, etc. The purpose of a system test is to validate that system performance is consistent with requirements. In Babar, we required a system test for each subsystem before full scale production. Although our tests did not reveal any serious problems, they did help us refine grounding and shielding plans in some of our subsystems. They also gave us the confidence to enter production without worry of significant setbacks that would be costly in terms of money or valuable schedule time. In the case of one Babar electronics subsystem, if the system test had involved a larger number of channels, two problems found later might have been avoided. As that subsystem leader commented regarding the "Importance of pre-testing a reasonably large sample of pre-production parts before going into production. We had two failures, which really were components. One was in manufacturing (solder-on surface-mount connectors), and the other was the bad transmitter problem [described above]. If we had made a larger preproduction and had a longer time to break it in, we might have spotted it."

12. VENDOR QUALITY

Inexperienced vendors will often take longer to complete projects within specifications than experienced vendors. Moreover, there is some risk that an inexperienced vendor will never be able to manufacture production units that consistently meet specifications. Babar experienced two important problems with manufacturers of electronics components, one in the calorimeter subsystem and one in the vertex detector subsystem.

The problem in the calorimeter electronics subsystem was with power supplies for the front-end electronics. As described by one of the subsystem leaders, "In open European bidding, we got much lower bids from companies with no experience in building the sort of product we wanted. Our power supplies would no doubt have been well made by" experienced companies "but the company that made ours learned on the job." The consequence was that the supplies were delivered at the last moment and were out of specification. They contributed common-mode coherent noise at about two times design value until additional external filters were installed on all supplies.

The problem in the vertex detector subsystem involved hybrids for the detector-mounted electronics, and ultimately led to changing vendors. The experience led one of the subsystem leaders to comment, "The key was to identify a good vendor, and not to waste a lot of time working with vendors who could not quite meet specifications. Once we found the right vendor it turned out very well." The original vendor, who produced toys and consumer electronics, was not familiar with hybrids of the quality needed for the vertex detector. The consequence was a huge delay in our ability to test the vertex detector readout chip in large numbers with detectors. Such key components "should be on a fast-track with a very experienced and responsible group in charge." It is often a delicate issue to change vendors; however, a timely change can often save time or even rescue a project.

13. CUSTOM INTEGRATED CIRCUITS

Custom integrated circuits have profoundly changed the way front-end electronics systems are designed. Indeed, there is no other way to build most present high energy physics experiments. However, the use of custom integrated circuits implies years of development, and the development period is almost always underestimated. As pointed out by one of the Babar designers of integrated circuits, one of the reasons for underestimating development time, among others, is that there is essentially no room for even the smallest error during the multi-step development process. "If simulated, a chip may work; if not, it never works." The same is true for IC evaluation testing. Furthermore, throughout the development process, "One relies strongly on industry, academic design centres, and students. One single failure is able to compromise months of efforts, and due to the size of projects, it is impossible to cross-check everything." The demanding task of developing a full-performance IC can be further complicated by unnecessary complexity. Consequently, as pointed out by one of the subsystem leaders, "You can never start custom IC design too early in the project, it is usually the pacing item. Always budget time and money for additional prototype runs to fix the mistakes you didn't know you would make." And as remarked by an IC designer, "This is the price to pay for getting both quantity and quality."

13.1 Unexpected IC setbacks

Development of custom integrated circuits can also be delayed by unforeseen circumstances beyond the control of the design team. Babar experienced several such
delays. Because an engineering change order twice was not transmitted properly between foundry and packaging house, two consecutive fabrication runs of our Drift Chamber Amplifier Chip (DCAC) were incorrectly bonded and were useless. In another incident, the complete order of our Calorimeter Auto-Ranging & Encoding (CARE) chip disappeared in U.S. Customs. In the case of our Calorimeter Amplifier Chip, we ended up with three slightly different shaping times that required amplifiers to be sorted and grouped for trigger reasons. The second shaping time arose because the foundry fully processed only a portion of the production run until receiving our evaluation of its performance, and then processed the remainder of the run. The third shaping time arose because the manufacturer overestimated the yield, and did not produce enough working chips in the first production run. One can draw separate lessons from each incident; however, the general conclusion is that one should plan for setbacks and delays. In Babar, we experienced delays beyond our control on three of our seven custom ICs.

13.2 Radiation-hard ICs

Radiation-hard integrated circuits pose additional challenges to IC development. In the case of the Babar vertex detector readout chip (ATOM), one of the subsystem leaders drew the following conclusions, some of which are general and some of which are particularly relevant to development of a radiation-hard IC. In fact, the ATOM development followed most of these suggestions.

- "If the project is distributed across more than one institution, try to use a common set of design and layout tools (seems obvious, but we had two different sets.)"
- "If you are prototyping in a rad-soft process for a rad-hard design, adopt a set of layout rules combining the most conservative rules of both processes so that the layout does not need to be modified in going from prototype in the rad-soft process to pre-production in the rad-hard process. We prototyped in HP 0.8µm CMOS and fabricated in Honeywell 0.8µm CMOS (both processes had 3 metal layers)."
- "Submit any analogue circuit elements to the rad-hard process as early as possible in the design process."
- "If the rad-hard process is not well-characterised by the vendor, plan to invest in the tools and the effort to characterise it yourself and to understand what process variations you can expect."
- "Develop your own test structures to be inserted in the reticle along with the one used by the vendor to qualify the run so you can figure out why a run failed when the vendor says it passed QA and wants payment. We did this after problems with the first production run. The test structure we submitted was a full channel with a lot of probe points, and it was very useful for debugging the prototype. (Unfortunately we didn't include it in the pre-production!)"

13.3 Vendor IC testing

Production testing of several of the custom integrated circuits developed for Babar was performed by the manufacturers. We were definitely pleased with the results of doing the testing this way. It was fast, effective at eliminating bad chips, and cost-effective. The calorimeter amplifier IC was tested at AMS. Babar supplied the test jig. After some initial difficulties of getting the test jig to work properly, testing proceeded very quickly. We did not retest the chips until after they were mounted in pairs on the amplifier boards. The Calorimeter Auto-Ranging & Encoding (CARE) IC was also tested at AMS. For this chip, we supplied the test sequence and the limits of acceptance. The test vectors and the circuitry were developed at the test house. We did not retest the chips prior to assembly on the ADC boards. Less than about 0.5% of the chips failed upon retest after assembly. The vertex readout IC (ATOM) was tested as die at Honeywell. In this case, we supplied the probe card and test vectors. Honeywell supplied the tester. The test set-up was difficult to debug at the foundry, but it gave a very rapid turn-around once the wafers were out of fabrication. The DIRC Digital IC was tested by Atmel-ES2. The test vectors used at the factory covered about 60% of the chip. The delivered yield was very good.

14. PRODUCTION TESTING

Acceptance testing of production units before installation in the experiment is an important step in the development process. Adequate production testing can be a very time consuming process. Developing a test stand suitable for production testing can also be very time consuming. Acceptance testing should be planned in advance of receiving the production run. In order to ensure that acceptance test procedures were adequate in Babar, we reviewed Acceptance Test Plans for each component before production as part of the Final Design Review. One of the Babar subsystem leaders suggests, "Agree on a set of testing specifications and procedures for every component, to be followed by the responsible institution(s) and documented (on the Web if possible). In this way the history of every part is available on the Web and problems later on can be tracked down. Also you can be sure that each part really meets the specs."

Easy-to-operate test fixtures are often needed for acceptance testing components in large numbers. Such fixtures often require extensive software suites for tests. Babar found that multiple test set-ups and stations were sometimes needed. More set-ups can be needed than expected or planned. A detector system leader suggests,
"Don't forget to build enough prototypes to provide a complete electronics readout chain to every institution that will be building detector modules or testing front-end components. ... Budget enough spares to provide a similar final test set-up wherever it will be needed to carry out any maintenance or repairs."

14.1 Industrial board production and testing

Our French colleagues working on the BABAR DIRC subsystem had a very satisfactory experience manufacturing and testing their principal component, the DIRC Front-end Board (DFB), in industry. As described by the subsystem leader, "We have been lucky enough to interest a big company [Thomson CSF] for which cost was not so much an issue but that wanted to learn our techniques. Besides the (usual I guess) very high requirements on quality and control for the fabrication process, the key action was to implement OUR test bench in the factory to fully validate the fabrication and to train THEM to use it." The tests at the factory included complete point-to-point coverage of the card, burn-in, and testing with a test bench provided by BABAR. Fifty percent of the DFBs passed the tests the first time at the factory. When the cards were received in Orsay, further tests were made. One hundred percent of the cards passed the same tests in Orsay as they did in the factory. Five percent did not pass a set of more stringent final tests used in Orsay. The screening provided by these tests was quite successful. Since installation, we have had only one or two minor problems on 168 cards. As an additional benefit of manufacture in industry, the manufacturer as part of the bid process computed the MTBF of the DFBs (for free). Note that BABAR required MTBF calculations before production of all major components as part of the Final Design Review.

15. INSTALLATION AND CHECKOUT

BABAR generally installed and checked out each front-end electronics subsystem on its respective detector system before the detector system was installed in the experiment. Installation and checkout in this way greatly facilitates and accelerates final commissioning in situ. It also provides a better, more peaceful environment for commissioning. For instance, for the particle identification system (DIRC), front-end electronics was assembled and tested on DIRC sectors in France before shipment to SLAC. They were then remounted and retested on the DIRC sectors in a staging area at SLAC before installation of the DIRC. Meanwhile, off-detector electronics was installed in the counting house prior to DIRC installation. Only final cabling and checkout occurred after installation.

We also found that system tests are a useful prelude to installation and checkout. Initial checkout is also greatly facilitated by existence of a subsystem of the final data acquisition system or, in the absence of final data acquisition components, by suitable test modules that could perform the essential data acquisition functionality. We were not as successful in BABAR at having full subsystems of the final data acquisition system available for early checkout as we would have liked, primarily due to our problem with turnover of engineers. This situation made the leader of one of the electronics subsystems remark that "The lack of a readout platform before production was complete really made debugging system problems extremely difficult." We did however have test modules and prototype data acquisition modules available for early checkout, and partial subsystems of data acquisition for final installation. The full data acquisition framework was only available at the last moment. Finally, we found that cosmic ray tests can provide an excellent opportunity to perform final checkout with the detector.

Installation and checkout are a manpower intensive effort, and teams of ample strength should be assembled. We did not have enough effort available during this phase in some of our subsystems. These were larger subsystems that had less capability of being checked out outside the experiment prior to installation. The consequence was a protracted commissioning period for these subsystems, and lower quality initial performance.

Installation and checkout require a team of physicists that is larger than needed during design and production phases. However, it is often difficult to identify teams to commission a subsystem that did not have a role in design and production of some component of the system. Consequently, the teams that will eventually do the commissioning should be included in the project near the beginning of the development process.

Commissioning requires appropriate software suites of diagnostics. These can be the basis of final in situ diagnostic programs, if they are based upon (or compatible with) the APIs of the data acquisition system. In situ diagnostics should be capable of validating proper operation of the entire electronics chain, including connections to the detector and of localising failures to the replaceable component (board, cable, etc.). More refined diagnostics for board repair can be reserved for the test bench. Developing the needed diagnostic suites is another major software effort associated with electronics development.

16. DATA ACQUISITION

16.1 Partitioning

Partitioning refers to the simultaneous and autonomous operation of portions of the data acquisition system with full functionality. For example, the drift chamber and particle ID system can use the cosmic trigger, while the vertex detector does threshold scans, while the level 1 electromagnetic energy trigger uses the calorimeter for checkout, while the calorimeter diagnoses failures in one crate, etc. Partitioning is important for efficient
integration of detectors into the central data acquisition system, for efficient checkout and commissioning of detector subsystems, and for efficient calibration and maintenance of detector subsystems. Partitioning is pervasive. It must be implemented in all systems that control and initialise electronics subsystems, that distribute fast timing and trigger signals, that acquire data from electronics subsystems, and that control the detector (e.g. high voltage).

*Babar* implemented a system that allows partitions with any combination of crates, utilising any combination of triggers. It also allows trigger crates to participate in partitions with detector-specific crates. This architecture was facilitated by our compact data acquisition system (~25 crates), which allows fully flexible interconnections between "partition masters" and data acquisition crates.

### 16.2. Synchronisation

Because the flow of data is largely asynchronous from each front-end element in pipelined readout architectures, synchronisation of the flow of data into the data acquisition system is of central importance. This issue is often further complicated when flow control does not extend all the way to the source of data. That is, there is often no mechanism to throttle triggers when front-end buffers fill. Data flow synchronisation is a central design issue. The system should be robust against lack or loss of synchronisation; i.e., the system should not crash. Otherwise, it can be very difficult to commission the system or to debug synchronisation problems.

*Babar* has approximately one thousand independent front-end sections. Although its readout architecture is pipelined, *Babar* implemented a "data-pull" operation between the front-end electronics and the Readout Modules in order to simplify the synchronisation problem. In *Babar*, the difference in deadtime for a data-pull connection vs. a data-driven connection between front ends and Readout Modules was very small, even at a 10KHz level 1 trigger rate vs. the nominal 2KHz rate. Deadtime is minimised by the multiple event buffer in the front-end preceding the readout link (D-link), and by the ample bandwidth of the D-links. Data-pull simplifies synchronisation by eliminating potential data loss between the front-end electronics and the Readout Modules. This is accomplished by allowing backpressure at the level of the Readout Module to throttle the level 1 trigger, and by creating added event coherency in the Readout Module.

In *Babar*, despite our best intentions, thorough documentation, and design meetings, some subsystems implemented slightly different interpretations of our standard protocol, thus causing synchronisation problems. Fortunately, all of the differences were capable of remedy by reprogramming logic.

Once running in synchronisation, the *Babar* system remains synchronised in the absence of link problems that "damage" data. The system was more difficult to get running in the first place, than to keep running. Integrating each front-end subsystem into the data acquisition system required a very big investment of effort by the data acquisition group. Standard buffers, protocol, and readout module facilitated integration.

The most complex synchronisation issues during *Babar* commissioning were in subsystems that require synchronisation between their front-end electronics and the trigger as well as between their front-end electronics and data acquisition. We experienced some sequencing problems in these systems.

### 16.3. Software

During the planning phase, software effort is frequently, or even usually, underestimated. Software is needed throughout the development cycle. It is needed to test and evaluate prototypes, to perform system tests, and to perform production acceptance testing. It is needed to check out and commission the system. It is needed to diagnose and monitor the system during operation and to maintain and repair failed components. As pointed out by the system engineer of one of electronics subsystems, "Last but not least, hardware and software have never been so closely mixed in electronics design. The time it takes to get a chip working, optimise the implementation of an algorithm, is 90% writing code: C, VHDL/Verilog, assembly, tests vectors. Even pure analogue design requires programming for the hardware test set-up."

### 17. CONCLUSION

A long and tortuous path, with many potential obstacles, winds between conceptual design and operation. Nevertheless, it is a path that can be navigated successfully. The development of the *Babar* Electronics System was completed in about four years. The *Babar* Experiment was approved in spring 1995. At that time, the conceptual design of the Electronics System was not yet complete. Electronics installation on detector systems started in Early 1998. Detector assembly, without the vertex detector, was completed in October 1998. A cosmic ray run was performed from November 1998 to January 1999. The detector, with the vertex detector, was completed in October 1998. A cosmic ray run was performed from November 1998 to January 1999. The detector, with the vertex detector, was rolled on beam line in spring 1999. Physics running started in May 1999. *Babar* was able to record physics data within weeks, without an engineering run. Although some wrinkles in the Electronics System are still being ironed out, with few exceptions, the electronics has performed as designed since the start of data taking.

### 18. ACKNOWLEDGEMENTS

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Genova, Milano, Napoli, Padova, Pavia, Pisa, Torino), the United Kingdom (Bristol, Edinburgh, Imperial College, Royal Holloway, RAL), and the United States (UC Irvine, UC Santa Cruz, Caltech, Colorado, Colorado State, Iowa, Iowa State, LBNL, Maryland, Pennsylvania, Princeton, SLAC, Stanford). This group deserves credit for the outstanding work described here. Dr. G. Haller of SLAC led the technical development.

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19. REFERENCES
Field-programmable logic is ideal for customized digital designs. Like microprocessors and memories, it offers the well-known advantages of very high integration: high complexity and density, small size, low power consumption and cost, and high reliability. On the other hand, programmable logic avoids the problems of ASICs: high Non-Recurring Engineering (NRE) costs, long delays, complex testing issues and the increasingly difficult electrical issues of deep sub-micron ASICs.

1. TYPES OF PROGRAMMABLE LOGIC

Simple Programmable Logic (SPLDs or PALs) were introduced >20 years ago, and are now an insignificant, rapidly shrinking part of the $2B market for programmable logic.

Complex Programmable Logic (CPLD) devices make up 35% of the market. These devices inherited the AND-OR structure from PALs, but offer more inputs and outputs and better sharing of product terms. Pin-to-pin delays are very short, making CPLDs best suited for wide decoding, synchronous state machines, and counters. The design software is simple, easy to use, and it compiles very fast.

CPLDs are inherently limited in size, and offer relatively few flip-flops. The architecture cannot be expanded to large arrays. CPLDs have a fairly high static power consumption, caused by their wired-OR interconnect structure with many read amplifiers. Only the CoolRunner family (formerly Philips, now Xilinx) offers ultra-low static power consumption.

FPGAs, 53% of the market, have a more ASIC-like architecture with many flip-flops and distributed routing.

A small subgroup of FPGAs uses antifuses to control their interconnect structure. Consequently, these devices maintain their configuration when powered down, they power-on instantly, and they require no external configuration memory. Their internal flip-flops are as sensitive to radiation-induced single-event upsets as any other CMOS storage element, but the logic is fairly immune to radiation problems.

Antifuse FPGAs serve a niche market and are only offered by two small manufacturers.

The most successful and fastest-growing programmable device families are the so-called SRAM-based FPGAs. These devices store their configuration (program) in on-chip latches that in turn control pass transistors. Logic tends to be implemented in 4-input look-up-tables (16-bit ROMs). SRAM-based FPGAs offer the highest logic capacity and the highest flip-flop count. The devices can be configured in milliseconds, and may be reconfigured an unlimited number of times. Since they use a standard CMOS logic process, they migrate quickly and easily to the most advanced technology pioneered by the microprocessor industry. The configuration must be reloaded whenever Vcc is being reapplied. This is, however, a major strength of the architecture, since the devices can easily be reconfigured with a new and different program, even after installation.

2. SYSTEM DESIGN OPTIONS

- Microprocessors offer greatest flexibility and high functional versatility, but they are too slow for many tasks.
- Gates, MSI, and PALs are inefficient, inflexible and really outdated.
- Dedicated devices and chip sets are powerful and often inexpensive, but offer no design flexibility.
- ASICs (gate arrays and standard cells) offer highest complexity and speed, but suffer from high NRE cost, design effort and risk.
- FPGAs offer flexibility, fast-time-to-market.
- Dynamic reconfigurability is a unique advantage. Their speed, size, and cost are now approaching those of ASICs.

3. ASIC PROBLEMS

As ASICs are migrating to deep sub-micron technology, they are getting less attractive. NRE cost is driven up by the larger number and increased complexity of their masks. The larger wafer size and smaller die size forces the manufacturer to increase the minimum order quantity. The high-end mainstream ASIC suppliers prefer to deal only with a few, very high-volume users. Low-tech ASICs find themselves in direct competition with advanced FPGAs. In mixed-signal (analog/digital) applications, ASICs have an unchallenged advantage.
FPGA History (XC4000)

- > 20x Bigger
- > 5x Faster
- > 50x Cheaper

Figure 1

Process Technology Evolution

Figure 2
4. FPGA EVOLUTION

The following pages describe the present state and the future of SRAM-based FPGAs. The user community expects a wide choice of device sizes, from 5,000 to several million gates, at speeds up to 100 MHz and above. Design time and effort must be reasonable, and the FPGA supplier must offer and support a wide choice of advanced cores with guaranteed functionality and performance, and must provide powerful synthesis and simulation tools.

Looking back in time, the industry’s most successful FPGA family (XC4000) has made tremendous progress between 1991 and 1998 (see figure 1):

The devices got five times faster, the largest available device increased in complexity (gate count) by a factor 20, and for a constant complexity of 10,000 gates, the price dropped by a factor 50.

These historical trends will continue in the future. The coming years will see larger devices, from the present 1 million gates to 2 million gates in late 1999, to 4 million in 2000, 10 million in 2002, an even larger ones in the following years.

The present speed capability can be characterized by >200 MHz on-chip RAM, 200 MHz interface to external RAM, 155 MHz SONET and also 311 MHz bit-serial interfaces, and 66-MHz PCI compliance. The present performance will double by 2002.

5. FPGA PROGRESS

FPGA progress is driven by three independent forces:

- IC technology provides smaller geometries and thus faster transistors and lower cost per function. Better defect density on the wafer makes it possible to manufacture larger chips with acceptable yield.

- FPGA architecture is improved by incorporating system features and by providing a better hierarchical interconnect structure.

- Design methodology is improved with more and better cores, more capable and user-friendly design tools, and faster compile times. The new tools allow a modular, team-based design, and even a distributed design effort via the internet.

5.1. Technology

IC technology has advanced very rapidly during the past 5 years, from 0.5µ minimum feature size to 0.18µ today. This offers faster speed and lower cost, but it also means that the 30-year reign of 5V as the only supply voltage is over. Vcc must now be reduced for every new step in the process evolution. Purely by accident, the Volt number is and will be exactly ten times the micron number. (see figure 2)

FPGA technology is essentially identical with microprocessor technology, and thus benefits directly from the fast evolution in that very competitive industry. We use 0.18µ technology in production today, have 0.15µ circuits in development, and see a clear road to 0.13 and even 0.10µ in the future.

Copper interconnect will be introduced in the year 2000, and will be combined with low-k dielectric in 2001, providing lower resistance and lower capacitance for the interconnects, and avoiding metallization issues.

FPGA packages have evolved from PLC and PQFP packages with connections confined to the periphery, to ball-grid array packages with increasingly finer pitch. Presently, we offer up to 1156 connections to the chip. The future will see an increasing use of flip-chip packaging technology.

5.2. Architecture

High-end FPGAs must offer more than lots of gates. They must offer a system solution with on-chip memory, a wide choice of interface standards, and must provide sophisticated and robust timing (clock) management.

The Virtex and Virtex-E families offer a 3-level memory hierarchy:

Many (up to 38,000) distributed 16-bit single or dual-port RAMs with sub-nanosecond access time.

Up to 160 versatile 4k-bit dual-port RAM blocks with 3 ns access time and configurable aspect ratio, from 4k x 1 all the way to 256 x 16.

A configurable, fast interface to essentially unlimited external RAM with less than 10 ns access time.

Clock management uses up to eight on-chip digitally-controlled Delay-Locked Loops (DLLs), that can eliminate the on-chip clock distribution delay, de-skew clocks on the board, double or divide the clock frequency, and restore a 50% duty cycle.

As the FPGA implements complete subsystems, it can no longer rely on external level translators. Virtex implements 17 different I/O standards, and the new Virtex-E adds differential LVDS and 3.3 V PECL.

On-chip, Virtex provides a hierarchy of interconnect resources. There are four high-drive, ultra-low-skew global clock nets, each with its own optional DLL, and each capable of driving all flip-flops and registers on the chip. There are 24 additional low-skew global nets for more clocks or other critical nets. All Xilinx FPGAs have bi-directional horizontal Longlines, ideal for on-chip bussing. The many remaining interconnects are segmented, which reduces clock capacitance and thus delay and power consumption.
Moore Meets Einstein

Speed Doubles Every 5 Years…
...But the speed of light never changes

Figure 3

Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>1965</th>
<th>1980</th>
<th>1995</th>
<th>2010(?)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Clock Rate (MHz)</td>
<td>1</td>
<td>10</td>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>Min IC Geometries (µ)</td>
<td>-</td>
<td>5</td>
<td>0.5</td>
<td>0.05</td>
</tr>
<tr>
<td># of IC Metal Layers</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>PC Board Trace Width (µ)</td>
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<td>500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td># of PC-Board Layers</td>
<td>1-2</td>
<td>2-4</td>
<td>4-8</td>
<td>8-16</td>
</tr>
</tbody>
</table>

- Every 5 years: System speed doubles, IC geometry shrinks 50%
- Every 7-8 years: PC-board minimum trace width shrinks 50%

Figure 4
5.3. Design Methodology

Users demand a more efficient design methodology, driven by high-level languages, and compatible with a variety of industry-standard synthesis and simulation tools. The design effort must be modular, so that several, even geographically dispersed designers can work together on one design.

The internet can be used in several ways. WebFitter allows anybody with internet access to implement a CPLD design on a Xilinx-resident computer. Internet Team Design lets groups of designers share their work over the internet. Internet Reconfigurable Logic (IRL) means that a working FPGA design can be modified, upgraded, tested, or repaired by downloading a new configuration via the internet.

6. RECONFIGURABLE FPGAS

In-system reconfigurability is a unique FPGA advantage with many exciting possibilities. In the design phase, it encourages unlimited experimentation, since mistakes are easily fixed. In production, the system can be customized at the last minute “on the loading dock,” or even after it is in operation at its final destination, where the end-user can upgrade a working system. The user can also choose between multiple implementations, and in some cases the system may even reconfigure itself automatically, in a matter of milliseconds, or even microseconds.

Think of an instrument built with FPGAs. Functionality can be changed in milliseconds. One box can serve different purposes at different times. A storage scope can change into a spectrum analyzer, using the same A/D and memory circuits, controlled by a reconfigurable FPGA. The user can also upgrade or repair the instrument, and thus extend its lifetime, effectively reducing the cost of ownership.

7. CHALLENGES FOR THE USER

Moore’s law states that IC complexity doubles every 18 months. A corollary claims that average system speed doubles every 5 years, from 1 MHz in 1965 to >100 MHz in 2000. Unfortunately, the signal propagation speed on a PC-board remains constant at 15 cm/ns. If we postulate that interconnect lines should not waste more than 25% of a clock period, we can calculate a max interconnect length, which shrinks from many meters in the ’70s to 30 cm in the year 2000 and 7 cm in the year 2010, when system clock rates exceed 500 MHz. And there is no remedy in sight... (see figure 3)

Higher clock rates demand shorter output rise- and fall-times, about 1 ns today. Interconnect lines longer than 7 cm can no longer be considered lumped capacitive loads, but must be treated as transmission lines, terminated either at the destination or - if there is only one destination -- at the source. Those 7 cm will change to 4 cm in a few years.

Here is a look at the evolution of digital systems over the 45 year span from 1965 to the future in 2010. It highlights the tremendous progress in the past, but also points at future challenges. (see figure 4)

The rapid increase in the number of metal layers on the IC after 1995 is due to the introduction of Chemical-Mechanical Planarization (CMP) which eliminates the accumulation of surface “bumpiness.” Adding a further metal layer now means just a slight increase in wafer cost and a small yield loss.

Power consumption and the resulting rise in chip temperature are a serious concern. Although CMOS consumes practically no static power, the dynamic power is fCV². As the clock rate increases and the chips get bigger, the increasing power consumption is only partly mitigated by a reduction in Vcc. Big chips running at high clock rates dissipate >10W and require heat sinks and forced air to keep the junction temperature below 125°C, preferably below 85°C.

8. RADIATION TOLERANCE

The new XQR and XQVR series of Xilinx FPGAs avoid latch-up even at 120 MeV cm²/mg and tolerate >50 krads of total ionizing dose. Single Event Upsets (SEUs) have been investigated and reported, with a primary emphasis on the use in high-altitude flight and Low Earth Orbiting Satellites (LEOS). (See: http://www.xilinx.com/products/hirelqml.htm#RadiationHardened)

SEUs in the configuration latches can be detected by reading back the configuration (which does not interfere with the normal operation of the chip) and comparing it against the original configuration bitstream. SEUs can be corrected by using on-chip triple-redundancy.

9. CONCLUSION

- SRAM-based FPGAs are the fastest-growing segment of the semiconductor industry, sharing technology with microprocessors.
- As standard off-the-shelf components, FPGAs offer fast time-to-market and reduced design effort and risk.
- Density, speed, and cost start to rival ASICs, while avoiding the problems facing the designer of deep-submicron ASICs.
- And finally, only SRAM-based FPGAs can implement reconfigurable systems.

This is the Dawning of the Age of Programmable Logic.
Testing LHC electronics

J. Christiansen, CERN, Geneva, Switzerland (email: jorgen.christiansen@cern.ch)

Abstract

The special testing requirements of LHC electronics are analysed and compared with standard testing techniques used in industry. General testing problems at the IC, MCM, board and system level are analysed and related to the construction of the large and complicated electronics systems required in an experiment.

1. INTRODUCTION

Testing aspects of the construction of the large and complex electronics systems, required for LHC experiments, receive more and more attention as the LHC electronics community is moving from a conceptual and design phase to a real production phase. During the conceptual and early design phase of the electronics systems, testing problems have to a large extent been ignored. The main focus has been assigned to the construction of small demonstration systems, required to prove the correct function of a proposed architecture and its implementation. The construction of these demonstration systems, and their related components, has in many cases been performed in a competitive environment and under a significant time pressure. Testing aspects have received little attention, as it was not a major problem in the construction of small demonstration systems.

Many LHC sub-detectors are now in a situation where it has been proven that electronic systems can be built with the required physics performance. It is now required to prove that the final systems, many orders of magnitude larger and more complicated, can be built from the components used in the demonstration systems. Many integrated circuits have been designed and shown to work in small systems. These integrated circuits have though in many cases not been optimised for being produced and tested in large quantities. Some components used in demonstration systems even have serious design flaws, which could be handled in the demonstration systems, but can not be tolerated in the final system.

In the electronics industry it is known from the start of a project that no profit can be gained from a product before the design has been qualified to be of sufficient quality and that it can be produced in large quantities. The market time window of commercial products in the electronics domain is so short that a few additional months, used to solve qualification and testing problems, can reduce the final profit significantly. It is therefore common that testing and qualification aspects are dealt with from the start of a project. A part of a design team is made responsible for insuring that the final design can be transferred to a production phase as quickly as possible. A whole set of design approaches, design tools and internal design reviews are used to minimise the problems of transferring the design into production.

2. MOTIVATION FOR TESTING

The main motivation to spend significant amounts of resources and time on testing is to be capable of making reliable systems at minimum total cost. One of the main testing philosophies is sketched in figure 1. Testing is divided into two significantly different domains. Design verification consists of qualifying a design before it is released for production. Production testing consists of testing each individual component to remove devices with failures coming from the production process.

![Figure 1. Cost of finding and repairing a failing design/chip.](image)

The design process has been divided into a specification, a design and finally a prototype verification phase. A missing feature is very expensive to discover when the first prototype chip is tested (\(\sim 100K\$\) for a commercial prototype run) but could have been added at much reduce cost at the design or specification phase. The critical part of design verification testing is if an imperfect design is released for production. In the best case a complete production lot is lost. In the worst case scenario the chips will be used in the final system, which will not function correctly or will encounter frequent breakdowns.

Production testing of integrated circuits can also be performed at different levels as shown in the figure. The higher level a failing device is detected, the higher the cost. The cost of detecting a failing chip at wafer level testing could be of the order of 1$ per chip. At the next level, when the chip has been packaged, the detection of a chip failure means that the additional costs of packaging will also be lost (if packaging is cheap and the yield is high, it may though be cheaper to skip wafer testing and only perform testing of packaged
ICs). If a failing component makes it all the way to the final system installation, it may become very expensive to diagnose the cause of a system failure and perform the required repair. In LHC experiments a system repair may be further complicated by the fact that the electronics may be inaccessible for extended periods of time.

3. ELECTRONICS FOR LHC EXPERIMENTS

Electronics for LHC experiments are often technically characterised by the fact that they must be capable of handling very small detector signals. These signals must be buffered, during one or several levels of triggers in the front-end electronics, before finally being transferred to the data acquisition system in a digital form. It is for the front-end systems that a large set of different types of electronics has been developed. This spans from analogue low noise amplifiers to special purpose digital processors (trigger systems) over highly integrated and complex mixed signal devices. For the DAQ systems a high level of standardisation is possible, and commercial modules are used to a large extent.

A large set of different integrated circuits is required to deal with the different kinds of signals from the detector technologies used in each sub-detector. An estimated number of one hundred different ASICs (Application Specific Integrated Circuit) has been developed for the four major LHC experiments. The total production volume of ASICs for the same four experiments is estimated to be of the order of 1 to 2 million. Hundreds of new modules and MCMs (Multi Chip Modules) must be developed and a total volume of hundreds of thousands must be tested after production.

A large majority of these ASICs and modules are developed within the university environment by a large number of small design groups spread over the large world-wide High-Energy Physics (HEP) community. These kinds of groups have in most cases shown them selves capable of designing the required integrated circuits, but they only have limited experience in producing large quantities of high reliability circuits. High reliability is in many cases required from the front-end electronics, as a large part will be mounted inside the detectors where it can only be serviced on a yearly (or a few years) basis. In addition, it is required that the components maintain high reliability in a very hostile environment with high levels of radiation, magnetic fields and high voltages.

A significant part of the front-end systems must be built using MCM technology, to comply with the limited space available inside the detectors. An important question concerning MCMs is the possibility of performing repairs if one of its components is found to be faulty. If MCMs can not be repaired it requires a very high quality of its components to get sufficient yields. A typical front-end MCM with 12 integrated circuits will only have 50% chance to be fully working if each integrated circuit has a 5% risk of being malfunctioning ($0.95^{12}=50\%$ yield). This is even under the assumption that additional failure mechanisms (MCM substrate faults, bonding faults, etc.) are ignored. It is therefore critical for these applications to perform very exhaustive tests at the component level. Testing of the MCM itself is also problematic, as normal testing schemes used for PCBs can not easily be used for MCM testing.

For a significant part of the front-end systems special radiation hard or tolerant IC technologies must be used. These kinds of technologies are only produced in low quantities and may therefore suffer from significant lower yields than mainstream commercial technologies.

4. DESIGN VERIFICATION TESTING

Design verification testing consists of proving that a designed circuit behaves in a way that is compatible with its required role in the final system. A design is normally started from a written textual specification. From this a behavioural model using Verilog or VHDL for the digital functions can (should) be built to optimise and verify the performance of a given architecture. Analogue behavioural modelling can potentially be performed to verify the architecture of the analogue functions. Based on this, the design is mapped into a chosen technology using a given design methodology (full custom, standard cell, gate array). Detailed gate level or transistor level simulations are then used to verify the correct function of the designed circuits. It is here important to take into account all parameter variations which may result from variations in the fabrication process and in the environment (temperature, supply voltage, radiation, etc) the component has to work in. When finally a prototype chip is produced it must be verified if it complies with the original specification.

Statistics from ASIC designs in industry show that 50% of new designs are found to be working correctly during the design verification testing. The circuits are then plugged into the system, where they have to be used, and it has been found that only 25 % of the designs are found to work correctly within the system. The remaining 25 % fail in the system because the original design specification did not cover in sufficient details the functions required. This gives a clear indication of the importance of system level simulations, to verify the correct function of the behavioural model of the integrated circuit, before detailed design at the gate/transistor level is started. In HEP it is though often seen that bugs in IC designs are
circumvented, by running the system in a restricted manner.

Figure 2. Design verification testing.

When a prototype has been shown to work correctly it must be verified if it is ready to be transferred into production. Before this can be done it must be insured that the design has sufficient margins to variations in process parameters. It is also important that the design can be sufficiently tested within an acceptable testing time. It must in many cases also be verified that the circuit has sufficient resistance to radiation.

For design verification testing it is important to have access to a complete set of flexible test equipment, where the circuit can be exercised with a large set of tests. To be capable of tracing the cause of possible malfunctions it is important that the designers are actively involved in the design verification testing. The total test time per circuit is not an important issue for this kind of test. The flexibility and ease of use of the test system must be considered first priority.

Design verification will in most cases be a significant part of the design time and development costs of an integrated circuit. For complicated mixed signal integrated circuits the design verification testing can be up to half of the total development costs.

5. PRODUCTION TESTING

Production testing consists of testing each produced unit to insure its correct function, before it is used in the final application. To reach a sufficient quality level the produced circuits must pass a whole set of tests. A typical production test of a digital IC consists of the following steps: functional test, internal speed test, external speed test, and finally test of IO signal levels. Mixed signal ICs must in addition pass a set of extensive analogue tests. All these tests must be performed with sufficient margins, to take into account the precision of the test equipment used and the environment in which the IC must be guaranteed to work. Testing at worst case temperature poses a particular practical problem, as the ICs must be preheated before testing is performed.

For production test systems it is important that a sufficient throughput (tested ICs/boards per time unit) can be obtained. For large scale productions the time needed to test each circuit must be minimised through at set of optimisations, still keeping a sufficient level of fault coverage. The ease of generating tests is less important as the time invested is amortised over the complete production volume.

As previously mentioned, IC’s can be tested at different levels: wafer level, bare die or packaged. For large-scale productions it is often cost effective to perform test both at the wafer level and when packaged. Performing test at the wafer level can not be used to skip the testing of packaged devices as new failure mechanisms are introduced during bonding and packaging.

Obtaining sufficiently tested circuits at the bare die level poses a specific problem, as they are very difficult to handle mechanically. Wafer level testing is no guarantee that the devices have not been damaged during cutting and the related handling. As previously mentioned, sufficient quality of components are vital to the final yield of MCMs. In addition it may be required to perform burn-in to ensure sufficient reliability (requiring an additional test after burn-in).

The development of efficient production test procedures can be a significant part of the total development budget. The cost of testing each component can be up to 50% of the final component cost in case of complex mixed signal circuits. An additional complication in the testing of HEP circuits is the monitoring of radiation resistance, which requires destructive tests to be performed on a representative sample of the production lot.

6. TEST OF INTEGRATED CIRCUITS

The resources needed to perform effective tests of integrated circuits are often largely underestimated (not only in HEP). The major driving force behind the required high level of testing of integrated circuits is the problem of yield, related to the critical and very sensitive processing steps needed for the production of modern IC’s. The expected yield of a given chip area,
assuming a constant defect density, can be seen in figure 4. High volume commercial processes, used for components where yield optimisations of the design has been performed, has significantly better yield than low volume technologies used for specialised ASICs (radiation hard technologies). Some types of components can significantly improve production yield by having redundant sub-circuits (e.g. memories). In HEP circuits a failing front-end channel can in some cases be accepted, thereby significantly reduce the number of chips to reject. It must though be kept in mind, that accepting chips with certain failures may have an influence on their long-term reliability. A good overview of manufacturing yield and reliability of semiconductors can be found in [1].

![Figure 4. Yield of different IC technologies.](image)

**Reliability**

Reliability of integrated circuits is a special worry for applications where repairs are difficult to perform. It is known that integrated circuits have a rather high failure rate during their first few months up to a full year. After this time period it has been found that ICs have very low failure rates for tens of years. The circuits failing during the initial time interval are normally termed infant mortalities and can in some cases be of the order of one to a few percent.

![Figure 5. Reliability of integrated circuits.](image)

A one percent failure rate of the integrated circuits of the previously mentioned MCM with 12 ICs translates into a MCM failure rate of 12 %, which in most cases is unacceptable. These weak components can be screened by means of a burn-in procedure, where the circuits are heated to 100 – 125 degrees, resulting in an acceleration factor of the order of 30 – 40. A few days at this temperature is the equivalent of several months at normal working conditions. For this burn-in scheme to be efficient to sort out the weak population it is also required to power the devices during this period (static burn-in) and if possible continuously stimulate them to keep their internal logic working (dynamic burn-in).

The reliability of components can in certain cases be reduced significantly. Badly designed components may have problems with electromigration, if the power distribution network on-chip has not been sufficiently sized. Circuits working at elevated temperatures because of insufficient cooling will also have reduced lifetimes. Contamination problems related to improper packaging or passivation may be a problem in certain working environments. Careless handling of CMOS circuits have also been seen to provoke small ESD (Electro Static Discharge) damages that may not be seen immediately. The mounting of bare die ICs on a mechanical substrate may introduce stress-based failures to occur if the thermal expansion coefficients of the IC and the substrate are incompatible. Failures from this mechanical stress are a specific problem for direct flip-chip mounting. Radiation effects are one of the major worries when it comes to the reliability and lifetime of the electronics located inside the detectors or in the caverns of LHC experiments.

**Basic IC testing problems**

To be capable of making effective tests of integrated circuits it is important to understand some of the basic problems in IC testing. A simple combinatorial circuit with N inputs requires $2^N$ test patterns to perform an exhaustive functional test. If the circuit is of sequential nature, containing M storage elements, an exhaustive test will require $2^{(N+M)}$ test patterns. It is evident that modern integrated circuits with many thousand storage elements can not be tested with this kind of brute force approach. The topology of the circuit must be used to reduce the number of test patterns to a level that can be generated by available test equipment.

The topology of the circuit can be looked at from different abstraction levels: Transistor level (layout), Gate level (netlist) or functional level of macros. A defined set of fault mechanisms must also be taken into account to limit the length of the test: shorts to ground, shorts to Vdd, broken lines, bridges between lines, etc.. Faults in simple basic components (gates) used in all digital designs poses surprisingly large problems in testing. Two examples have been chosen to illustrate this.

A simple inverter as shown in figure 6 is normally tested by asserting a logic one and a zero at the input, and then verify that the inverse values are present at the output. In case the PMOS transistor of a CMOS inverter is constantly conducting (stuck on) the failing
circuit will resemble an old fashioned NMOS logic inverter with a pull up. If the NMOS transistor used in the inverter is sufficiently strong, it will still be capable of driving the output voltage below the threshold voltage of the following gates in a logic circuit. In this case it is impossible to detect the PMOS transistor being stuck on with a simple functional test. The failure may though have serious consequences for the correct function of the circuit. The noise margins of the generated “digital” signal is seriously deteriorated and small levels of noise may result in functional failures. The propagation delay through the inverter will also be significantly changed in the described failure mode.

Figure 6. Failing inverter can not be detected.

The power consumption of the gate will be significantly increased when both transistors are in a conductive state. For a large IC this will just give a slight increase in power consumption, but may at long-term overload the internal power supply distribution network locally and cause electromigration effects. The increase in power consumption can actually be used to detect this kind of failure by measuring the steady state power supply current for a given set of test patterns. When a state is reached where both transistors are conducting a significant increase in steady state current consumption can be seen in CMOS logic circuits (called Iddq testing).

An even more worrisome problem in CMOS circuits is the fact that simple logic gates can start to function as sequential elements if one of their transistors is stuck open. This is illustrated in figure 7 where one on the PMOS transistors in a two input nand gate is stuck open. When the output is supposed to be driven by the faulty transistor the parasitic capacitance on the output node will “remember” the previous output value and thereby appear as a storage element. A set of basic test patterns for a nand gate is shown and it can be seen that in a give sequence the fault will be detected, but an alternative sequence of the same patterns will leave the fault unnoticed.

Figure 7. Failing nand gate becomes sequential.

Fault coverage

Fault coverage is normally used as a measure of the efficiency of a certain set of test patterns. Fault coverage is obtained by a fault simulation of the given design, to determine the faults detectable by a given test. Fault simulation requires large computing resources to determine if all faults are detectable by a given set of patterns. It is necessary to limit the number of fault types taken into account to limit the computing resources necessary. The most commonly used fault model for large digital circuits is the “stuck at zero”/“stuck at one” model. This only considers the effects of any node in the gate netlist being tied to logic one or logic zero. Bridging faults and open faults are in this case simply ignored. Based on the fault simulation the fault coverage is calculated as the ratio of detected faults to the total number of possible single stuck at faults.

As previously demonstrated the stuck at zero/one fault model does not take into account even simple failure mechanisms in CMOS logic at the transistor level. The conclusion from this is that a chip, which has passed a test with a 100% fault coverage, can in fact not be guaranteed to be fully functional !. The percentage of failing ICs passing such a test is very hard to estimate.
**Testability**

To arrive at designs that can be efficiently tested during both design verification testing and production testing, it is very important that the design has been made with testability in mind. A design made with testability features can obtain very good fault coverage with a limited number of test vectors as illustrated in figure 8. Designs made without any support for testing may require order of magnitude longer test patterns, if it is possible at all to reach the required quality level. What is seen in normal designs is that the first part of a set of test patterns obtains a quick increase in fault coverage. It is the coverage of potential faults in "hidden" parts of the design which makes it very hard to obtain the final few percent of fault coverage (even assuming the simple stuck at 0/1 fault model).

![Figure 8. Testability of different designs.](image)

![Figure 9. Decreasing testability with increased integration.](image)

Testability in integrated circuits has continuously decreased because the number of gates per pin typically increases an order of magnitude for each new technology generation as shown in figure 9. This has meant that resources needed, to obtain sufficiently testable designs, has been steadily increasing. For mixed signal ICs this tendency has been even more pronounced. A whole set of design methodologies and design tools has been developed in the CAE industry, to optimise and automate the process of obtaining sufficient testability.

**Use of scan-path and JTAG**

The use of scan paths in digital designs is one of the main schemes used to obtain sufficient testability. If all storage nodes can be accessed (read and write), in a special test mode, the testing can be performed efficiently using these virtual signal pins. The testing can in fact be so simplified that test patterns with 100% fault coverage (assuming stuck at 0/1 fault model) can be generated with Automatic Test Pattern Generation tools (ATPG). IBM has for decades obliged all in-house designs to have complete scan paths, using a scheme called level sensitive scan design (LSSD).

The IEEE 1149.1 standard has been defined to enable internal test features in integrated circuits to be accessed in a standardised manner using a minimum of pins (4). This standard, also known under the name of JTAG (Joint Test Action Group), has a large set of features improving testability at the component and board level. A simple serial protocol allows direct access to internal scan paths and Built In Self Test (BIST) features. An additional scan path gives direct access to all physical pins of the device to enable efficient tests of the connections between chips at the board level. Most commercial ICs, above a certain complexity level, supports JTAG boundary scan for board testing. These chips have in most (all) cases also extensive internal test features to insure the required fault coverage during production testing. These internal test features are though never publicly documented, as they are of no practical use to the normal user.

![Figure 10. JTAG scan path architecture.](image)
attention during the specification and design phase of the projects.

7. IC TEST EQUIPMENT

Test equipment for high performance integrated circuits is very expensive with a price range from $500K up to $10M. VLSI testers are very complicated machines with very stringent requirements. They must be capable of testing ICs with millions of test patterns at several hundred MHz on hundreds of channels (pins), with very accurate time resolution (tens of Pico seconds). Production testers must in addition have a very high throughput to be cost effective.

Figure 11. Commercial high-end VLSI tester.

Digital testers can be bought as standard commercial systems. Mixed signal test systems are though not available as standardised systems as each individual mixed signal IC has special testing requirements. Mixed signal test systems for certain types of mixed signal ICs are though now appearing (DAC/ADC, Telecom, etc.).

CERN IC test installation

The CERN microelectronics group, consisting of the order of 10 IC designers finalising several new IC designs per year, has during several years had a significant testing problem. ICs have been tested with custom-made test set-ups for each new design. The design of these dedicated test systems requires a significant effort. In many cases more time was spent debugging the test system than the time used on testing the integrated circuit itself. This kind of home-made test systems only has limited flexibility and testing performance. A significant set of parameters is limited by the system (test frequency, timing on signals, logic voltage levels, etc.). There is neither any kind of calibration available to guarantee the quality of the tested components.

It was considered to use testing facilities available in industry (manufactures or specialised testing houses). This kind of service is though very hard to use for design verification of complicated mixed signal integrated circuits. In many cases the required mixed signal testing features are not available in these facilities. Detailed design verification of mixed signal ICs requires access to test equipment for several months and needs a close interaction with the designers. External industrial test facilities are appropriate for production testing of large quantities (high throughput, Automated handling equipment), when well defined tests are available, but were not found appropriate for detailed design verification.

Because of financial constraints it was not possible to buy a flexible high-end IC tester with sufficient mixed signal capabilities. It was therefore investigated what kind of test equipment could be purchased for a total value below a million Swiss francs. The total test system should have digital and mixed signal capabilities and also include a wafer prober in a clean room. The clocking speed of the digital part should be 100 MHz or more, to cover the 40MHz LHC bunch clocking rate with sufficient margins, and also cover ICs using double sampling. Timing resolution of the order of 100ps was considered acceptable. For mixed signal tests high speed and high-resolution arbitrary waveform generators and digitizers were required.

Figure 12. CERN mixed signal IC test system.

A system based on a “low-cost” digital design verification tester and a VXI system with the required analogue instruments was found to be an appropriate solution with a high level of flexibility. The microelectronics group was though not in a position to assemble the system and write all the required software (this part is always underestimated). A commercial company specialised in this kind of test equipment was identified to do the system integration and deliver a set of their software tools to obtain a fully integrated system (from point of view of hardware and software). This system has now been used over a period of two years and a large set of digital and mixed signal ICs has successfully been tested. This test system is available to the LHC electronics community to the extent that sufficient tester time is available. Detailed information
During the use of this test system experience in IC testing has been gained and set of lessons learnt:

- Testing is always underestimated
- Testing requirements are often badly defined in specifications.
- Test developments must be performed by designers or in close collaboration with designers.
- You can never put to many testing facilities in your chip.
- IC testing in some cases gets delayed because of urgent beam tests. These beam tests will though often be of limited use, as function of ICs not fully understood.
- Mixed signal testing can be quite slow:
  A: Lacking test facilities in IC.
  B: Slow transfer and processing of large amounts of acquired data per IC.
- Synchronisation between instruments important.
- Do not have write only registers.
- Scan path and BIST test facilities extremely useful.
- Redundancy or self-checking features can be hard (impossible) to test.
- ICs with PLLs requires special attention to initialisation and synchronisation.

8. RADIATION TESTING

Verification of sufficient radiation hardness of integrated circuits is an additional complication of the testing problems in HEP. Radiation testing has no equivalence in the normal commercial electronics industry. Only highly specialised domains like space and military applications have similar problems. In these domains, only a very limited quantity of devices is needed and they can therefore better accept the high costs related to this (the launch of a satellite is already very expensive). Space industry can not accept any major component failures as repair is excluded. In LHC experiments repairs can in principle be performed, but only at infrequent intervals.

Radiation testing requires significant time and is expensive as many different effects must be investigated:

- Total dose effect
- Dose rate effects (bipolar)
- Single event latch-up
- Single event upsets
- Gate rupture (high power MOS devices).

In addition the radiation environment in the experiments is not know with a high certitude. For the radiation tests it is basically impossible to generate a realistic environment comparable to the final application. A whole set of tests with different kinds of particles with different energies must be performed to get some kind of confidence that the components can survive. Certain technologies are “guaranteed” radiation hard or radiation tolerant, but this must still be verified both in the design verification phase and also during production.

The use of Commercial Of The Shelf (COTS) components for radiation tolerant applications has for obvious reasons received a lot of attention. This is though by no means trivial as commercial IC’s often have significant variations in their tolerance to radiation. This can be explained by the fact that the manufacturer may have several different process lines producing the same component. The detailed processing steps may also be changed by the manufacturer, without any notice to the customers. It has even been seen that a specific component type from a manufacturer in some cases comes from a processing line of an other manufacturer (hidden second sourcing). Even in the case of a special agreement with a manufacturer, that chips will come from the same process line with exactly the same processing, there is still no guarantee that the produced chips will be as radiation resistant as the chips previously tested.

For components and systems located in places with low radiation dose levels it is very hard to determine a safe limit that a standard electronics module may accept. Normal (especially modern sub-micron) CMOS IC technologies in most cases works correctly above a total dose of 10 Krad. Some very sensitive components may though start to fail at a dose level below 1Krad. Single event upsets can also be a serious problem for complicated electronic modules (with processors, memories, FPGA’s, etc.) even in a low dose rate environment.

9. MCM AND BOARD TESTING.

When performing MCM or board testing, it is normally assumed that the individual components are correctly working. It must though be taken into account that components may have been damaged during the mounting process (Soldering, ESD or incorrect handling of bare dies). MCM and board testing is to a large extent concentrated on identifying missing or wrong components and verifying the correct connections between components. It is not only important to detect if the module works or not. It must also be identified why it does not work to enable quick and effective repair.

Traditional board testing is performed using in-circuit tests and/or functional tests. In-circuit testing probes all nets on a board via a bed of nails fixture. This enables all connections on the board to be tested and allows all components to be verified with a simple set of tests. Failing or missing components can be identified directly insuring an easy repair procedure. In-circuit test has been a very popular test procedure in
industry for many years. It is unfortunately encountering significant problems on modern high-density modules using surface mount technology. It is not any more possible to probe directly all nets on the board.

The electronic systems for HEP experiments are very large and complicated systems which in addition must work in a hostile environment. Test procedures must be available to test all parts of the system in-situ. To insure this level of testing capabilities, the required functions must be in the specifications of the sub-systems, boards and components of the total system. Many electronic sub-systems, in the front-ends of experiments, are very hard to access. It must therefore be possible to identify the exact cause of a failure to perform repairs as effectively as possible.

Electronic systems for HEP experiments use large quantities of data links to transport data. These links must also have testing procedures to identify if they are the cause of a system failure.

To perform efficient system testing it must be possible to access the different parts of the system even in case of a major system failure. This data path will in HEP experiments normally consists of the DCS control path (in fact not considered a part of DCS in some LHC experiments) to the different sub-systems. In case only one combined data path (combined readout and control) is available it becomes very difficult (impossible) to identify why the system has failed. It should also be insured that all registers in the electronics can both be written and read, to have a means to verify that data has actually arrived at the intended destination.

As previously mentioned the systems have to work in a hostile environment. System failures should be expected to happen, caused by single event upsets, glitches and alike. This makes it important that the system is to a large extent self-testing during normal running, to identify if errors have occurred.

11. CONCLUSIONS

It must be considered a significant challenge to produce the required electronics for LHC experiments with sufficient quality. The size and complexity of the electronics needed are an order of magnitude larger and more complicated than what have been used in previous generations of high-energy physics experiments. To be capable of building these systems it is of vital importance that testing and qualification procedures are defined for all levels of the complete system: components, modules and sub-systems. The heavy use of custom-made integrated circuits poses a new challenge for the community. Integrated circuits can not be “repaired” once produced. In previous generations of HEP experiments, based on electronics with standard commercial components, small bugs could often be repaired at the module level. With the introduction of new technologies (IC, MCM) this will not any more be possible. It is therefore of outmost importance that all designs have been properly qualified and that all components have been extensively tested after
production. The problems of accessibility and radiation damage to large parts of the electronics is an additional complication, which has newer before been faced at this scale within high energy physics (nor anywhere else).

References

Scalable Test Solutions: A Means of Improving ASIC Performance and Time-to-Market in Mixed-Signal Engineering Test

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Abstract

In a quest for shorter time-to-market and higher test quality of complex mixed-signal ICs, a novel approach for Mixed-Signal Engineering Test and Low Volume Production Test is devised. The approach builds upon making available to designers a scalable approach for engineering test of mixed-signal ASICs where the low cost entry starts at using standard off-the-shelves low-cost PC-plugin instrumentation and scales upwards to VXI based instrumentation, when performance demands increase in terms of test instrumentation fidelity and/or volume throughput requirements. The high end of the solution approach meets the demands of medium size production volume.

For the entire scalable range of test solutions there is a high level of portability to ensure that an optimum of test program efforts spent at one level can be ported to the next higher level at a minimum cost.

The software environment seen from the user’s point of view offers the same look-and-feel for the scalable solutions, and a high level of generic instrumentation secures portability. The software tools available with the approach offer ease-of-use and fast test generation even for complex tasks. Furthermore, the tools lend themselves well for use by designers to promote a natural extension of ASIC design verification. Examples are given on the use of mixed-signal simulation results as the basis for test generation, and a comparison is shown for A/D converter performance based upon SPICE level simulation, VHDL-A level simulation and actual performance of a device under test.

1 Introduction

Mixed-signal ICs, and particularly the analog subcircuits of such ICs, have become challenging bottlenecks in testing of many of today’s high growth application domains such as mobile phones, telecommunications, automotive, datacoms, etc. Faced with demands for shorter design and manufacturing cycles, higher quality and an ever-increasing chip complexity and functionality, existing methods for mixed-signal engineering test have proven insufficient and cumbersome for most design and test engineers.

Over the last two decades many efforts have been employed to improve the general situation of time-to-market in the design and test domains. The world has seen several advances during this period, not least in the field of complex digital chip design. However, the progress in the analog design methodologies have progressed at a much lower degree.

The eightieths were the decade where test problems were solved as an afterthought by involving massive test engineering to compensate for chip designers’ lack of knowledge in how to handle the test and quality issues of a given chip function. The design process itself typically was handled in a sequential manner where hardware design basically had to be completed before software design started, and then eventually test engineering started.

In the industry, a general consensus existed since the beginning of the ninetieth that the existing approaches of isolated hardware and software design paths were less than optimal. To bridge this, new approaches in digital design engineering like hardware-software co-design/co-verification, design reuse have emerged over the decade.
This has made it possible for the design community to meet the rapid escalating complexity of chips and still keep design resource employment almost constant or even reducing the total design time.

However, the mixed-signal EDA domain has not seen a similar development as that of the digital domain. Neither has the area of mixed-signal testing. Prototype validation and test in general of mixed-signal ICs are still to a large degree left as activities to be handled by test engineers as rather isolated approaches after completion of the chip design. Customers report that as much as 25-35% of the time and cost for getting an integrated circuit to the market is test related, with test of design and debugging taking a substantial share of this. Some advanced users estimate that verification and simulation problems take an even larger share. In general, the relative balance in designing a state-of-the-art mixed-signal ASIC is changing towards more verification/validation while the design process itself occupies a declining part of the entire cost of obtaining a mixed-signal ASIC.

Simulation of the functional performance plays an important role during a design of a mixed-signal ASIC. However, the simulation process remains a major challenge, and mixed-signal simulation is lagging the performance of digital counterparts. Many simulators for mixed-signal design are still based upon transistor level analog descriptions, e.g. SPICE based simulators that cannot handle more complex circuitry. For this reason, simulators are often applied to isolated problems only, where an analog simulator is employed to a limited domain of the circuitry in an “island-solution” approach, while a digital simulator is used for other domains of the design. However, such isolated approaches suffer from general applicability, and many problems remain in the interfaces between domains that are not covered by the simulators, hence left to show up in first silicon.

Assembling the results of simulations typically prove a substantial problem. Add to this that analog simulations normally take a significant amount of time. Mixed-signal simulators are available, but normally only for limited functionality. Recently, new behaviour level simulators have started to emerge, and simulators such as HDL-A (Mentor Graphics), AHDL (Analogy) or VHDL-AMS promise well for the application of mixed-signal simulation to larger functional elements. While HDL-A suffers from lack of hierarchy, the most recent developments like VHDL-AMS seem to offer an improved performance, also for use in conjunction with mixed-signal test generation.

Simulation results are of growing importance for use as test stimuli in mixed-signal testing. Due to the increasing complexity of mixed-signal blocks, it is getting more and more cumbersome to generate functional tests using a black-box concept. To obtain an efficient test generation in a minimum of time, a mixed-signal test ought to be based upon a maximum knowledge of the ASIC block functionality itself. This means that the designer must take a lead role in the prototype evaluation process, utilising the knowledge available for the design already at the design level. Mixed-signal modelling based upon functional simulators like PowerMill ACE (Cadence), or the previously mentioned behavioural level simulators seem to promise a way forward. Such techniques are still in their infancy, but results from European R&D projects under the ESPRIT programme such as ESPRIT 24.268 “TACTIC” [Ref. 1], ESPRIT 26.877 “OPTIMISTIC” [Ref. 2], and ESPRIT 27.943 “SUPREME” [Ref. 3] have shown encouraging results in using such approaches. Later on in this paper, we will address some of the results obtained in these projects.

2 Technological Challenges

A highly real problem to anyone who plans a test strategy, let that be in digital testing, in analog testing or in mixed-signal testing, is what tomorrow’s ASICs will bring of performance. Obviously, no one can answer such questions, but guidance can be found from several sources. One important source is “The National Technology Roadmap for Semiconductors” made by the US Semiconductor Industry Association (SIA). Key participants in this exercise are the Semiconductor Research Corporation (SRC) and SEMATEC. This roadmap, the most recent one is from 1997, estimates the trend in semiconductors up to 15 years ahead. Usually these roadmaps are rather realistic.

According to the 1997 roadmap, we should by year 2012 expect chips to have up to 100 M transistors/cm², the chip feature size will shrink to 50 nm, chips may comprise up to 13 cm² of real estate, and the power supply will drop to the vicinity 0,5-0,6 V of supply. ASICs are envisaged to grow also in number of pins from max 1.100 pins in 1997 to about 5.500 pins in 2012. Likewise, the analog performance is expected to grow from 25 GHz in 1997 to 120 GHz.

Although the number of transistors/chip will increase about 58%/year, the design productivity is only seen to grow 21%/year, thus creating a gap of 30%/year, which may prove critical.

A major element in future design will be increasingly adaptation of a reuse of designs made by others. System-on-a-chip will require employing large, pre-designed blocks, often made by third parties. Chips will predominantly be designed by teams. The EDA tool makers (electronic design automation) are making major efforts in providing tools that allow analysis already before silicon exists, but in mixed-signal the tools are lagging those of the digital domain, and mixed-signal designs keep demanding substantial human interaction.
The materials used on chip are gradually changing, and mixed-material structures will be more dominant. New dielectrics will be applied, and recent advances in copper metal layers combined with aluminium will see a more widespread use.

Fig. 1: The performance of CMOS analog is closing in on bipolar performance up to year 2012.

Interconnect delays on a chip are beginning to approach the delays of gates, hence requiring a change in the modelling strategy. In very deep sub-micron, the modelling of interconnect delays and capacitive coupling is insufficient using present day static wireload modelling, and even digital is becoming analog at the frequencies in question.

3 Trends in Design Technology

As stated above, reuse is becoming a time and performance critical parameter for many designs. Verification will become a mixture of verifying internally designed blocks with externally designed blocks. As a result, a major emphasis will be on handling the interfaces between blocks. It is envisaged by several that simulation/verification problems may soon comprise 30-65% of the cost and time for a complex mixed-signal design. We also see a clear trend in the change of the relative balance in design and verification with increasing activity in verification and a relative decrease in the design effort itself.

We envisage that the future designer will rely even more on the existence of capable and accurate simulation models. However, despite these the first-time correlation between theoretical performance and actual silicon will remain rare – especially in mixed-signal.

The process of back-end verification, as we know it today, will change. It will have to start concurrently with chip designs to support finding bugs early, since time-to-market is becoming even more mission critical. For this reason, we believe that it is imperative that the designer takes a lead role in back-end verification and characterisation process (engineering test). In the Ref. 1 and Ref. 2 project activities, such techniques are already successfully being applied to some of today’s most advanced ASIC designs in mobile telephony applications.

Although the EDA tools are undergoing many improvements, we envisage that mixed-signal designs will continue to be a major challenge. Also in the next few years to come, we expect 1-2 redesigns on average for a typical mixed-signal application. Today, mixed-signal designs take considerably longer to complete than digital designs, because tools are lagging or are less mature than in the digital domain.

In today’s applications we see that simulation tools are mostly applied to isolated domains, digital or analog. This creates a problem just to assemble the various simulation results. We expect that the advent of VHDL-AMS and similar simulation environments will ease the situation somewhat, but several challenges will remain to exist. In current activities, we are involved in the applications of such improved simulation approaches, or rather their application in test generation activities, and the results obtained up to now look encouraging.

4 The Problems of Non-Testable Mixed-signal ASICs

As a consequence of the growing complexity of mixed-signal circuits, testing becomes almost impossible, if the chip designers do not take a lead role in a test generation process. It no longer seems feasible to maintain yesterday’s philosophy of test generation, where a test engineer solves all testing issues of an ASIC as an afterthought.

If a test generation is to be achieved in a minimum of time, at a moderate cost, yielding a high test coverage, and at the same time preferably offering high throughput in testing, the mixed-signal test must be planned early in the design process. If not, an ASIC may prove difficult or even impossible to test. The latter can be disastrous to an otherwise good design. Most test engineers have come across such problems, and many have faced situations where a mixed-signal circuit may take minutes to test, which alternatively could have been done in few seconds, if a well planned test strategy had been adopted already in the design process. We typically refer to such
As a result of this definition, test solutions may exist for “non-testable” parts, but the cost of testing can be high, e.g. exceeding the price of the silicon itself or more, and hence is unacceptable to most companies.

5 High Costs of Mixed-Signal-Testing

Another dilemma in mixed-signal testing is the high costs often associated with test equipment and test program generation in this area. Many automatic test equipment production testers (ATEs) like the Teradyne’s, Credence’s, HP’s and others exceed investments of 1 million US$. Such systems have optimised characteristics for high volume testing, and do a good job in that, but may not offer measurement characteristics that exceed what can be obtained using good standard instrumentation like GPIB based rack-&-stack test system solutions or, even better, VXI-based instrumentation.

In mixed-signal engineering testing, the expensive ATE systems, with all their “bells and whistles”, are usually prohibitive for use in engineering testing because of their high costs. As a result, many design engineers end up making their own mixed-signal test set-up, typically a lab instrument set-up, often based upon GPIB instruments or PC-plug-in instruments. However, modern mixed-signal ASICs are typically systems-on-a-chip, and the embedded system testing required is difficult or even impossible to obtain based upon discrete instrument solutions, although such instruments are physically present in a rack-and-stack instrument solution. A system solution requires a good deal more. For example, mixed-signal testing often demands coherent testing [Ref. 4], which is difficult to achieve, unless a system approach is made for this. A number of other requirements are obvious, including a system software environment that supports the system-like testing required in mixed-signal testing. A simple request of being able to perform reproducible tests, for example after a redesign, may be difficult to honour, if the instruments used are disassembled between test events.

Most professional approaches for mixed-signal testing usually end up being relatively complex simply to meet the requirements, since a simple rack-&-stack solution does not suffice. In conclusion, a mixed-signal test, e.g. engineering test performed by designers, may call upon a solution somewhere in-between a high-cost ATE solution and a simple rack-&-stack instrument cluster solution. This simplified picture is obviously often blurred by a number of other facts in a given mixed-signal test situation. A chip may for example offer a number of built-in-self-test features (BIST) and/or good testability approaches that changes the scope of the test strategy. But by and large, most users need professional solutions for mixed-signal testing, and solutions at affordable costs.

6 A Scalable Mixed-Signal Test System Solution

One set of solutions to modern mixed-signal ASIC testing is described in the following.

As a result of European Commission funded projects under the ESPRIT programme, a scalable mixed-signal test system architecture is emerging. The first systems have been installed for engineering test, i.e. two models of test stations, one of which is a line of low cost personal test stations and the other is a line of high performance test stations. These two lines of solutions have proven very efficient and competitive.

A third line of systems, a medium volume production test system is soon to be marketed as well.

The scalable set of system solutions have been developed with the following in mind:

- Low cost
- Openness in concepts (software and hardware)
- Ease-of-use
- Modularity, preferable standard off-the-shelf instrument hardware modules

Fig. 2: The 3 lines of mixed-signal test system categories in the scalable solution. The software architecture offers the same look-and-feel at all three levels.
Software instrumentation to meet the needs of the user applications
- Efficient test execution
- Minimum test times
- Minimum program development time

for the test itself. Bridging of design and test is a major prerequisite for future mixed-signal ASIC designs.

7 System Architecture

To manage optimally the access of designers to mixed-signal testing as well as offering a volume test capability for mixed-signal, once the ASICs go into production, a range of solutions are available in the scalable range of mixed-signal test stations.

The scalable test system architecture builds upon a three-tiered architecture having the following distinct types of test hardware platforms:

- The Personal Mixed-Signal Engineering Test Station, the ALPHA Test Station.
- The High Performance Mixed-Signal Engineering Test Station, the BRAVO Test Station.
- The Mixed-Signal Engineering Production Test Station, the CHARLIE Test Station.

The Alpha Test Station is a low cost engineering test solution based upon standard PCI instrument platforms running under WinNT, and having some supporting GPIB-controlled instruments like relays switches and Power supplies. The analog input and output functions are obtained using a MIO module offering 8 differential analog inputs or 16 single ended inputs, and 2 analog outputs. A 16-bit resolution is achieved at sampling rates up to 100 kSa/s or 12 bits to 1.25 MSa/s. Counter functions are available. If for example higher speed analog digitisers are needed, this can be added as well. Digital channels are available as static functional high speed digital I/O channels in steps of 32. The speed is up to 20 Mwords/s in handshaking I/O.

The high Performance Bravo Test station offers similar functionality (and more), and the software has the same look-and-feel as that of the mixed-signal Personal Test Station. Here a variety of analog capabilities are available. Selecting the generic drivers in the system yields portability of application test programs for the low-cost personal test station. Analog test features may offer digitising up to 5 GSa/s at 8 bits, and 18-19 bits in the audio range is featured as well. For analog stimuli, 19-bits of linearity is achievable in the audio range, and up to 500 MSa/s can be achieved at 8-10 bits. Digital test can be offered up to data rates of either 25 MHz or 50 MHz, dynamic digital testing, offering full control over timing edges, trailing as well as leading edges. Positioning of edges to within a few ns is featured. A vector memory depth of 256 k is available at e.g. 96 channels or more in steps of 32 channels, and loop based testing can be obtained without any cycle steel. Switching of signals through high speed switching systems improves the versatility of the system, allowing the user to route signals under software control.
Volume testing is featured using a Charlie mixed-signal production test station. This test station has almost identical characteristics as the high performance Bravo engineering test station. However, in addition a separate test head holds pin electronics and parallel precision measurements features (PMUs) and programmable loads. This allows parallel measurements of DC parameters like leakage measurements and other DC characteristics that typical have to be verified at all pins of a DUT, hence reducing the overall test time significantly. Ironically enough, DC measurements often comprise a substantial part of the total test time for a device under test. To reduce this part of the test time and to avoid that costly functional test resources are idle for long sequences, the system is equipped with 4 source meters for every 32 test channels.

The test head of the production test system features easy access to component handlers and wafer probers, and offers a short signal path from test system I/Os like the programmable drivers and receivers to the DUT.

8 Software support for Ease-of-Use

The scalable solutions build upon an optimum system architecture as well as a flexible software, not least very efficient solutions for signal manipulations of mixed-signal and versatile software instrumentation (elaborate software instruments for the given type of test applications). Emphasis has been put on providing the same look-and-feel of the software for the various platforms of testers. Hence, a design engineer, who normally performs mixed-signal testing at his personal test station will be familiar with how to operate the more advanced systems, should he or she have a need to use such systems.

The system software builds upon a proven, advanced, software architecture and its related test tools for test and validation systems. This is tailored to meet the needs of especially mixed-signal applications. Since test optimisation is a major issue, dedicated software instruments constitute an important part of the adaptation. Test programs are generated in the test sequencer environment, SequenTEST. In this environment, the user can easily overview all conditions associated with making a test. Most programming is done using a menu-style fill-in of parameters. If dedicated changes are called upon, this is facilitated through the availability of graphics based programming (LabVIEW). From the test sequencer, basically most other software tools can be
controlled. This applies to limiter functions, InstruWARE software, the test database HandyBASE, etc.

Under the test sequencer, different categories of mixed-signal testing are facilitated like parametric test (analog), vector based test (analog waveforms), boolean (digital test, etc.), and strings.

The LimiTEST software tool makes it possible for a user in an easy manner, and at a minimum of time, to set up even complex types of limiter templates for tunnel based limiters, window limiters, point limiters etc. Limiters for analog signals can be programmed, or imported from e.g. a design environment or learned from a known good device. The LimiTEST subsystem also features test and logging of key parameters. These are user definable and may include finding the peak coordinates of an analog signal (amplitude, frequency), the frequencies at which the curve is 3 dB down, as well as a variety of other key parameters, where basically only human imagination sets a limit. Use of limiter templates is essential in mixed-signal testing.

The test sequencer tool also has features for controlling production test environments like providing control over handlers, wafer probers, and other external equipment as well as facilitating statistical tools for averaging, read out of Cp and Cpk values and many others. A list of the 10 most frequent failure in production testing is continuously updated.

In engineering testing as well as in production testing, large amounts of test data often needs to be manipulated and analysed. To ease this job of the user, a test database, HandyBASE, is available. This is a Web-based data management, analysis, and reporting solution for data acquired during test and characterisation. The test database utilises a MsAccess or SQL Server database for its operation. Through an easy-to-use, internet browser-based interface, the user can get access to the data stored in the database. A variety of analysis tools exists for making this task easier. For the user, a clear advantage is that no special software needs to be installed at the individual user platforms, only at the database server. Hence, the updating of new features is easily handled for even a large group of users. The test database can be accessed over internet, intranets, through modem lines, etc. provided that the user is given access through the security system.

The mixed-signal waveform editor and viewer, WaveMAKE, is a pivot of mixed signal editing and interfacing to design tools. This tool offers a true mixed-signal environment, where all signals, input stimuli as well as output response, can be visualised in one viewing window. Signals may be analog, digital or arbitrary.
signals including a mix of combinations. Separate editors are available for the analogue signals, the arbitrary signals and the digital signals. They allow for easy and fast creation of signals, using an intuitive programming style. In addition to signal editors, the tool includes analysis functions such as fast fourier analysis (FFT) and signal characterisation features such as rise time measurements. A double cursor system allows for selective FFT of a given signal or may be used for parameter estimation like rise/fall times, signal levels, etc.

The WaveMAKE tool can export/import signals to and from e.g. a mixed-signal simulation environment. In this manner the tool serves as the natural bridge between the design environment and the physical test environment. Using WaveMAKE, simulation results can be downloaded from a simulator to the test hardware for generation of actual electrical signals. Similarly applies to the actual response to be captured from a device under test (DUT). The tool allows large amounts of data to be transferred to be handled, and a number of conversion features allows easy conversions between domains, e.g. analog-to-PDM, PDM-to analog, FFT of digitised waveforms, etc.

From the WaveMAKE tool, waveforms can be downloaded into the actual test hardware, i.e. analog waveform generators, digital test subsystem, etc. Transfer times are of high importance in this process. Below is shown an example of transfer times for digital signals from WaveMAKE to a VXI-based digital test hardware subsystem (Interface Technology SR2500).

<table>
<thead>
<tr>
<th>Data transferred</th>
<th>Transfer type</th>
<th>Time [sec.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>256k x 1 bit</td>
<td>Export</td>
<td>2.3</td>
</tr>
<tr>
<td>256k x 1 bit</td>
<td>Import</td>
<td>5.2</td>
</tr>
<tr>
<td>25 waveforms x 256k x 1 bit</td>
<td>Export</td>
<td>57</td>
</tr>
<tr>
<td>25 waveforms x 256k x 1 bit</td>
<td>Import</td>
<td>130</td>
</tr>
<tr>
<td>65k x 16 bits</td>
<td>Export</td>
<td>7.1</td>
</tr>
<tr>
<td>65k x 16 bits</td>
<td>Import</td>
<td>5.8</td>
</tr>
<tr>
<td>256k x 16 bits</td>
<td>Local disk</td>
<td>&lt; 2</td>
</tr>
</tbody>
</table>

9 Reuse of Results

A major element in the scalable approach is that it allows a maximum of reuse of results. Basically 4 important elements of reuse have been identified for the solutions.

Reuse of design elements (1) offers a means of providing faster and more efficient generation of tests.
results from the bridging of the design tools and the test environment. This is primarily the transfer of signals, analog and digital from the mixed-signal simulation environment.

Reuse of important parts of the engineering test in production testing (2) helps avoid re-doing many software elements again, once an ASIC chip goes into production. Several elements can be reused here. However, one should also note that some elements have to be reprogrammed due to the simple fact that production testing aims at verifying flaws in the ASIC manufacturing process whereas engineering test aims at disclosing design errors. Hence, some testing will by nature be different.

Reuse of vital, well-proven test macros (3) that have been used in previous design/test solutions of similar chip block functionality. This may for example be test macros for given A/D or D/A converters, or other types of digitised analog signals.

Finally, the reuse of major test program elements in an optimal way (4) is essential for several applications. If for example several devices types, almost identical, but having small variations, are to be tested in a production environment, the test sequencer should offer a efficient way of handling diversities.

The scalable solutions support above.

10 Concurrent Test Generation for Mixed-Signal

A general problem in many ASIC engineering test environments is that debugging of the test program cannot really start until first silicon is available. This major problem does not fit with an improved time-to-market strategy.

One strategy to improve on this has been pursued in the TACTIC project [Ref. 1]. Here, simulated electrical response signals from a chip design, that has been finalised but not yet processed, are used in conjunction with arbitrary function generators in a test system. In this way, it is possible to generate some complex electrical signals similar to the ones that the chip will eventually generate, once the first prototypes exist. In this manner, the user generating the actual test program has a means of generating the electrical signals for debugging the test program itself. Using the WaveMAKE environment of the engineering test solutions described earlier on in conjunction with the test hardware itself, it is possible to debug the actual test program before actual silicon exists, See Fig 10.

The approach, we refer to it as VirtualSTIMULI, is convenient for the class of very complex mixed-signal chips that is designed at a leading mobile phone manufacturer. For such chips, only relatively few ports have to be verified for rather complex signal. Using the approach at this company means cutting about 1-2 months off the design time, which is important in a market segment, where the market window of opportunity may only be 6-9 months. The optimisation is shown in Fig. 10.

Fig. 11: Illustration of principles in VirtualSTIMULI. In the upper picture, simulated signals are used to generate electrical stimuli for verifying the test setup. In the lower picture, the actual chip is being tested using the hardware modules that were earlier used for test program
11 A Case Study for Concurrent Test Generation in Mixed-Signal

To illustrate some of the achievements obtained using the design links and the general tool environments of the scalable test system approaches described, some examples of signal generation are shown below.

The signal is valid for a 1 kHz sine. Simulations of the signal and its digitised version at the chip level took about 95 hours using a Sun Ultra 450 Processor (4 internal CPUs). This simulates a duration of about 15 ms. If a single CPU processor architecture like the older HP735/200 is employed, the simulation time is about 340 hours.

Three different results were analysed. First a simulation was done for the given converter block using Accusim SPICE. Following that, a functional simulation of the same block was carried out using Cadence PowerMill ACE. Finally the actual silicon was analysed, Macro Verification. As can be seen from Fig. 12, the results are in good harmony with one another at least down to -60 dB, and for the Spice simulation and Macro Verification the results even showed good results to -80 dB. As can be expected, the DC conditions differ. A number of similar results were obtained supporting the importance of the VirtualSTIMULI approach. Ongoing work is in process bringing in also simulation results based upon behavioural level simulation like HDL-A and VHDL-AMS.

![Converter Block](image)

Fig. 12: Verification of simulated results for an advanced mixed-signal macro block (Spice and functional simulation) versus actual macro verification of the silicon.

12 Conclusions

A scalable engineering test and production test approach for mixed-signal is shown. The set of solutions presented aims at bringing the cost of the testing solutions down and at the same promoting tools that will allow ASIC designers to take a lead in the ASIC test generation process.

A technique for performing concurrent test generation of complex mixed-signal circuits is discussed, and some results are shown.

The general mixed-signal tool environment presented seems to have an appeal to a number of the organisations that participate in the CERN experiments, since it will ease the task of mixed-signal test. At the same time, it provides the users with more powerful tools than normally available for the designers of mixed-signal.

13 Acknowledgement

The author would like to thank Tapio Koivukangs, Esko Kurttila, Veikko Loukusa, Yrjö Mäkelä, Veli-Matti Karpinnen, Kalle Lipping, Pekka Rytky, Arto Suopanki and Thomas Burger for valuable and inspiring discussions concerning the test approaches reported for the mixed-signal testing.

We would also like to thank the Commission of the European Union for its contribution to the R&D activities laying the foundations for the system approaches mentioned as well as to several of the tool developments facilitating the scalable mixed-signal approach. This has been funded through projects under the ESPRIT Programme, more specifically ESPRIT 24.268 “TACTIC”, ESPRIT 26.877 “OPTIMISTIC”, and ESPRIT 27.943 “SUPREME”.

14 References

Using COTS at the LHC: Building on Space Experience

James D. Kinnison
David R. Roth
The Johns Hopkins University
Applied Physics Laboratory

Presentation Outline

- Introductory Remarks
- Environment Comparison
- Basic Effects in COTS
- COTS Issues
- Hardness Assurance
- Mitigation Strategies
What is COTS?

Competing Definitions
- Anything you can buy from a catalog
  - If it has a part number and a data sheet, it’s COTS
  - No special requirements or added specifications
- Systems and components not specifically designed for mil/aero applications
  - Emphasizes high volume manufacturing and commercial electronics or automotive use
  - COTS are those things we couldn’t use before

COTS In This Talk
COTS are:
- Standard items available from a manufacturer
- Not designed for radiation environment, but may have some specified tolerance
- Usually “black boxes” to the user
- Not tweaked or modified for the user

Space Experience
Marketplace Changes
- Spacecraft are becoming commodities
- Emphasis is reducing cost
  - More science
  - Stimulate space business ventures
- Cost savings from:
  - Cheaper vehicles
  - Smaller, more capable systems
  - Simpler operations
Space Experience

Dilemma:
- Demand for spacecraft components is flat
- Consumer electronics market offers higher profit per man-year of labor
- Result is fewer devices available which are designed for the space market

Yet the need for high performance systems in space is higher than ever!

Space Experience

COTS Cases
- Choice between hard part and related unhardened commercial device
  - Survivability vs. performance
- COTS sometimes provide mission-enabling performance
  - Usually no radiation tolerant alternative
- COTS vs. equivalent mil/aero part
  - Traditional hard military part often cheaper when qualification costs are considered

Space Experience

Example: Microprocessors in space
- COTS processors usually 3 generations or so ahead of “rad-hard” mil-aero technology
  - Clones of existing commercial processors usually aren’t exact copies
- Advanced commercial tools usually not available for hardened technology
- SEE mitigation for COTS is complex
  - EDAC, watchdog circuits, triple voting, etc.
Space Experience

Risk Elimination
- “No risk is acceptable”
- Usually managed at the lowest level
  - Example: environmental risk in ICs
- Often driven to proven technology
  - Demands technology demonstration flights
- Can be mission or capability limiting
  - Upside - systems generally work

Risk Management
- “Mission must not fail - all else is negotiable”
- Low levels may be risky, but risks are mitigated at next higher level
- Often provides mission enabling technology
- Reality: not a new idea
  - We can never eliminate risk, and so these ideas have been used in every piece of engineering

Risk Management Methodology
- State the problem and proposed solutions
- Quantify the risk, if possible
- Know the impact of the risk
- Decide if the risk is acceptable
  - Mitigate?
  - Eliminate?
- Implement the optimum solution
LHC Experience

COTS Use
- Many of the same problems
  - Small market
  - Specialized needs, especially radiation
  - Need for high performance
- Unique Issues:
  - Many different independent groups
  - Wide variety of parts and subsystems
  - No equivalent of a prime contractor?

Environment Comparison

<table>
<thead>
<tr>
<th>Space</th>
<th>Aircraft</th>
<th>LHC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation</td>
<td>Radiation</td>
<td>Radiation</td>
</tr>
<tr>
<td>Charged particles</td>
<td>Neutrons</td>
<td>Neutrons, gamma</td>
</tr>
<tr>
<td>TID, SEE, Displacement</td>
<td>Neutron SEE</td>
<td>TID, Neutron SEE, Displacement</td>
</tr>
<tr>
<td>Physical Char.</td>
<td>Physical Char.</td>
<td>Physical Char.</td>
</tr>
<tr>
<td>-55 to 125 C</td>
<td>Controlled, 0-70C</td>
<td>Controlled, 0 - 70 C</td>
</tr>
<tr>
<td>Launch vibration</td>
<td>Some vibration</td>
<td>No Vibration</td>
</tr>
<tr>
<td>Repair/Upgrade</td>
<td>Repair/Upgrade</td>
<td>Repair/Upgrade</td>
</tr>
<tr>
<td>Usually, none</td>
<td>Cost driven</td>
<td>Undesirable</td>
</tr>
</tbody>
</table>

LHC Radiation

Total Ionizing Dose
- 10 krad - 10 Mrad, depending on location
- Mostly gamma dose

Neutron Exposure
- $10^{11} - 10^{12}$ n/cm$^2$
- Single event effects
- Displacement damage
Basic Mechanisms and Macroscopic Effects

Total Dose in COTS

ELDRS Effect
- Hardness is dose rate dependent
  - Lateral PNP transistors are more sensitive than others at low dose rate
  - At space rates, lateral PNPs are softer than at test chamber rates
  - Temperature confounds the effect
- Serious implications for test fidelity in space applications
Total Dose in COTS

Microscopic Effects
- Slower gate switching speeds
- Increased leakage currents
- Threshold voltage shifts

Macroscopic Effects
- Analog and Mixed-Signal Parts
  - Supply current, leakage currents increase
  - Offset voltage increases
  - Gain decreases
  - Converter non-linearity increases
  - PSRR, CMRR increases
  - Reference voltages change
Total Dose in COTS

Macroscopic Effects
- Digital Parts
  - Supply currents, input leakage increase
  - Timing slows down
  - DRAM data retention time decreases
  - Charge pumps fail
  - Transistor threshold voltages shift, so logic gates get stuck in one state
- Digital CMOS
  - Typically 1 - 50 krad
- Analog MOS
  - 1- 30 krad (depending on application)
- Bipolar
  - 10 - 100 krad
  - ELDRS effect may not be an LHC issue
- Boards and Systems
  - Strongly dependent on board design
  - Often observe increased supply current
  - In many cases, board works until it just quits
  - May be possible to find reduced operation that continues to work at higher doses.
Displacement in COTS

Microscopic Effects
- Neutron interacts with silicon nucleus
- Dislocates atom
- Formation of a Frenkel Pair which can be thought of as a recombination center
- Vacancy and interstitial cause unwanted quantum states in band gap
- Changes carrier flow

Macroscopic Effects
- Mostly an issue for photonic or optoelectronics
  - Lasers, LEDs
  - Opto-isolators, including DC-DC converters
  - CCDs, similar detectors
  - Bipolar electronics
- Decreases output power of light sources
- Reduces charge collection in receivers
- Increases leakage (or “dark”) current
Displacement in COTS

Damage Equivalence
- Test data usually taken with mono-energetic, unidirectional beams
- We need a way to convert a spectrum into a single equivalent fluence of a “standard” particle

\[ \Psi_e = \int K(E) \Psi(E) \, dE \]

Displacement in COTS

Damage Equivalence Factors in Si
Omnidirectional Proton to Unidirectional 10 MeV Proton

Displacement in COTS
Neutron Irradiation of LEDs

[Graphs and plots showing data and calculations are present but not transcribed.]
SEE in COTS

Microscopic Effects
- Neutron interacts with silicon nucleus
- Charged secondaries deposit charge
- Collected charge pulse causes effect
- Fundamentally a statistical process

SEE in COTS

Macroscopic Effects
- Destructive Effects
  - Latchup, gate rupture, burnout
  - Neutrons do not generally cause these
- Non-Destructive Effects
  - Upset, functional interrupt, transient
  - Most likely neutron effects

SEE in COTS

Single Event Upset
- Change in state of a memory element
- System-level manifestations depend on application

Single Event Functional Interrupt
- Upset places device in an ill-defined condition
- Sometimes requires power cycle to clear
SEE in COTS

Example: DRAM
- Upset Modes
  - Cell upset
  - Address error
  - Data latch error
- Functional Interrupt Modes
  - Spare memory area
  - Built-in test mode

Example: Microprocessor
- Upset Modes
  - Data error
  - Program error
- Functional Interrupt Modes
  - Built-in self test
  - Invalid instruction
  - Bad memory fetch

Example: Field Programmable Gate Array
- Non-SRAM Device
  - Dielectric rupture
  - Data errors
- SRAM-Based Device
  - Data errors
  - Inadvertent reprogramming
  - Functional interrupt in state machine
SEE in COTS

Boards and Systems
- Several (sometimes many) devices may be sensitive to effects
- Unpredictable results
  - Depends on type of error and system design
  - Very little visibility to diagnose problems
  - Can't depend on a system to completely police itself

COTS-Specific Issues

COTS Issues

Lot-to-lot Variation
- Parameters which determine total dose hardness aren’t closely controlled by manufacturers
- Hardness can vary widely across wafers and manufacturing runs
- Example: LM108 OpAmp - tested devices hard to as little as 5 krads and as hard as 80 krads
- SEE sensitivity determined by architecture, and so less variable across lots
COTS Issues

Architecture Changes
- SEE susceptibility determined by architecture
- Manufacturers revise die without warning
- Usually invalidates past SEE testing
- Related issue - product obsolescence
  - By the time you find a product you can use, the manufacturer has replaced it with something you can’t use!

COTS Issues

Boards and Systems
- Manufacturers change components frequently
  - Cheaper product
  - Performance improvement
  - Obsolescence
- Especially difficult with hybrids
  - No part numbers to check!

Testing and Procurement
Hardness Assurance

Steps To Hardness Assurance
- Determine requirements
  - Mostly determined by position
- Test components of interest
- Mitigate or circumvent damage effects
- Manage the supply of chosen parts

Total Dose Effects

Total Dose Test Methodology

ELDRS Effect

ELDRS Effect Test Methodology
SEE Effects

Event Rate Requirements
- From performance requirements
  - Highly application dependent
- Determination process is iterative
  - Requirements are given at system level
  - More sensitive devices can be used with mitigation if overall rate meets requirement

SEE Effects

Testing Issues
- Purpose: to measure the event cross-section and study external effects
  - Characterization of what happens to a device is necessary for mitigation design
- Quality of test impacts uncertainty
  - Dead time, beam measurement, etc.
  - Number of events detected
  - Fidelity of test

Displacement Effects

Testing Issues
- Data similar to TID Testing
  - Cumulative changes in device behavior as a function of fluence
- Execution similar to SEE testing
  - Beam issues of primary concern
  - Should simulate application as closely as possible
Procurement Issues

Common Buys
- “Frequently Used Parts”
  - Saves on qualification costs
  - Requires high degree of co-ordination
  - Need a centralized distribution system
  - May not help for systems

Procurement Issues

Data Sharing
- Database entries are often incomplete, making it difficult to apply results
  - Record as much info about the test as possible
  - Agree beforehand on how to do tests
- TID
  - Bias circuit, dose rate, anneal times
- SEE
  - Circuit, full cross-section curve, external effects

Mitigation Strategies
Total Dose Mitigation

Three Schemes
- Reduce the dose
  - External shielding
  - Advanced packaging
- Reduce the damage
  - Cold sparing
  - Intentional annealing
- Accommodate the effects
  - Design for end-of-life behavior

Displacement Mitigation

Two Schemes
- Reduce the fluence
  - Shielding
  - Advanced packaging
- Accommodate the effects
  - Design for end-of-life behavior

Displacement in COTS

Example: DC-DC Converters
- Often use optocouplers for isolation
- Mitigation
  - Use least sensitive components
  - Shielding or advanced packaging to reduce fluence
  - Accommodate power MOSFET threshold voltage shifts in design
### SEE Mitigation

<table>
<thead>
<tr>
<th>EDAC Method</th>
<th>Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parity</td>
<td>Single bit detect</td>
</tr>
<tr>
<td>CRC</td>
<td>Any errors in given structure</td>
</tr>
<tr>
<td>Hamming Code</td>
<td>Single bit correct, double bit detect</td>
</tr>
<tr>
<td>Reed-Solomon</td>
<td>Errors within symbol</td>
</tr>
<tr>
<td>Convolutional Encoding</td>
<td>Burst noise in data stream</td>
</tr>
<tr>
<td>Overlying Protocol</td>
<td>System designed to correct errors (i.e., data packet retransmission)</td>
</tr>
</tbody>
</table>

### SEE Mitigation

<table>
<thead>
<tr>
<th>Method</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog Timer</td>
<td>If not reset within some time interval, reset system</td>
</tr>
<tr>
<td>Redundancy</td>
<td>Equivalent systems operate on data.</td>
</tr>
<tr>
<td>Lockstep</td>
<td>Two devices are clocked simultaneously.</td>
</tr>
<tr>
<td>Voting</td>
<td>Three or more device provide function, which must agree</td>
</tr>
<tr>
<td>Repetition</td>
<td>System provides same data more than once</td>
</tr>
<tr>
<td>Scrubbing</td>
<td>Rewrite critical memory locations at regular intervals</td>
</tr>
</tbody>
</table>

### Resources
### Device Data

<table>
<thead>
<tr>
<th>Agency</th>
<th>Website</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>JPL</td>
<td>nppp.jpl.nasa.gov</td>
<td>TID/SEE</td>
</tr>
<tr>
<td>GSFC</td>
<td>flick.gsfc.nasa.gov</td>
<td>SEE</td>
</tr>
<tr>
<td>ERRIC</td>
<td>erric.dasiac.com</td>
<td>Variety</td>
</tr>
<tr>
<td>ESA</td>
<td><a href="http://www.spurelec.demon.co.uk">www.spurelec.demon.co.uk</a></td>
<td>TID/SEE</td>
</tr>
<tr>
<td>NRL</td>
<td>redex.nrl.navy.mil</td>
<td>TID/SEE</td>
</tr>
<tr>
<td>Data Workshop</td>
<td>IEEE NSREC</td>
<td>Variety</td>
</tr>
</tbody>
</table>

### General Info
- IEEE Transactions on Nuclear Science
- Journal of Spacecraft and Rockets
- Conferences/Seminars
  - NSREC
  - NSS
  - RADECS
- Space Parts Working Group
- GOMAC/HEART
THE ATLAS PIXEL ON-DETECTOR ELECTRONICS

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Representing the ATLAS Pixel Collaboration

Abstract

Large advances have been made over the last two years in the development of the front-end readout electronics for the ATLAS [1] Pixel Tracker [2]. I describe here the first phase of the Pixel Demonstrator programme which involved the production of two realistic ATLAS prototype readout-chips in radiation-soft technologies, along with the first Module Controller Chip. I will also describe the design of the first fully-functional FE-chip to be submitted to a radiation-hard foundry (Temic), which is currently being fabricated.

1. THE ATLAS PIXEL TRACKER

The Inner Detector of ATLAS will be composed of semiconductor-based discrete tracking elements with both strip and pixel geometries. The volume closest to the pp interaction region will be occupied by the Pixel Sub-system since the degree of granularity given by two-dimensional segmentation is most suited to the track densities and radiation levels encountered therein.

In Figure 1 the positioning of modules within the Pixel Tracker is depicted. There are three concentric barrel layers at 4.15, 9.7 and 12.7cm in r, along with 5 disc structures in each of the forward regions. Each module, of which there are a total of 2228, comprises a single 16.4 X 60.8mm active-area sensor tile. A tile incorporates 46080 pixel implants with pitches of 50µm in r and 400µm in the z-direction. The innermost barrel layer or B-layer, differs from the rest of the system in that the z pitch is 300µm with 61440 pixels per module.

Every individual pixel is DC-coupled to a preamplifier on one of the 16 front-end readout chips via a bump-bond. Each module is also instrumented with one Module Controller Chip (MCC), the primary purpose of which is to collect the hit data from the FE chips through 16 input FIFOs and to build up local ‘events’ for subsequent serial transmission. The modules also have the optical transmission devices, local termination resistors, decoupling capacitors and a temperature-sensor integrated onto them.

2. MODULE INTEGRATION

There are two hybridization strategies incorporated in the ATLAS Pixel system. The flex-kapton approach is the baseline choice everywhere except for within the B-layer where a technique known as MCMD is preferred. Modules constructed in both ways have been parameterised in laboratory and testbeam environments

2.1 Flex-Kapton Hybridization

Figure 2 shows schematically a flex-hybrid module. The lowest layer is formed from the 16 FE-chips which have their backplanes facing down and in thermal contact with the support structure. These are bump-bonded to the sensor tile which in turn has a single kapton bussing piece glued on to its backplane.

Along the long edges of the module the 16 FE chips (8 each side) protrude such that they may be connected up to the top surface of the hybrid using conventional wire bonds. These connections provide the necessary power, clock and control signals along with the output data link towards the MCC which is located in the centre of the hybrid. Connections between the MCC and bussing on the hybrid are also made with wire bonds.

2.2 MCMD Hybridization

In the MCMD (Multi-Chip-Module-Direct) scheme the necessary bussing is directly fabricated on the active side
of the detector surface. This is a post-production lithographic process providing up to 5 layers of copper with BCB dielectric. An individual via is crafted for each pixel to connect it electrically to the top surface of the sensor where solder or Indium bumps form the bond to the readout electronics. This enables the pixel connections to fan-in hence all pixels may have the same geometry whilst providing complete coverage in the inter-chip gaps. In the flex-hybrid scheme these gaps are covered by stretching the outer column implants by 50% and including eight extra rows of pixels which are ganged with other pixel rows. Avoidance of the extra channel occupancy and hit ambiguities implied by this approach is particularly beneficial in the B-layer.

3. THE DEMONSTRATOR PROGRAMME

The aim of the Demonstrator Programme was to develop on-detector readout-electronics designs which addressed all of the requirements of ATLAS. The initial phase of the programme resulted the development of two separate front-end chips and an MCC, which although conceived for radiation hard processes, were realised at non-radiation hard foundries.

The first of the front-end chips, FE-A, was designed at CPPM and Universität Bonn and fabricated using the BiCMOS process of AMS. The front-end of FE-A was based upon bipolar transistors although a 100% CMOS version (called FE-C) was later produced. The design of the other chip, FE-B, was developed at the Lawrence Berkeley Laboratory and this was manufactured by HP. The group at INFN, Genova were mostly responsible for the synthesis of the MCC design which was also fabricated at AMS.

To date more than 60 single-chip assemblies and 10 electrically-functional modules have been constructed using this first wave of electronics chips. These have been studied extensively in the laboratories of several collaborating institutes and during seven testbeam periods at CERN’s SPS facility. All of the ATLAS specification issues (which are applicable to radiation-soft electronics) have been addressed with highly encouraging results. A number of the single-chip devices were equipped with irradiated sensors in order to study the effects of worst-case leakage-current for example on aspects of the front-end performance.

The two front-end design efforts later joined forces to combine all of the experience gained with radiation-soft chips into a common layout which is currently being realised in Temic’s radiation-hard DMILL process, with the first wafers expected in the middle of October ‘99.

4. MODULE CONTROLLER CHIP (MCC)

Figure 3 shows the basic block diagram of the MCC. A Front-End Port consists of the drivers for all of the digital signals which configure and operate the FE chips along with sixteen receivers for the returning data streams.

For each FE chip there is a 25-bit-wide FIFO which buffers up to 32 hit words at a time. The event builder samples these FIFOs, one level-1 trigger at a time and builds up a score-board of hits for the whole module. All of the data for the trigger is then serialised off the chip as an integrated `event’. The other blocks shown in the diagram are the register array which stores the configuration information for the MCC and the command decoder which samples the input data line and distinguishes fast commands such as triggers from slow configuration-type commands. The chip is also designed to seek certain errors associated with the FE data and transmit the information as part of the general output-data protocol. The current MCC incarnation also operates in a transparent mode which enables individual FE chips to be read-out in direct stand-alone mode, i.e. not relying on the MCC event-building machinery.
5 DEMONSTRATOR FRONT-END CHIPS

5.1 Requirements

Potential sources of hit-inefficiencies in the Pixel System include bump-bond defects, timewalk, deadtime, charge loss through sharing and crosstalk, along with general electronics channel failures etc. Taking all of these into account, an overall hit-efficiency of better than 97% is specified. The false-occupancy is not to exceed $10^{-5}$ per channel ‘trigger’.

Following 10-years of operation, it is anticipated that the Inner Layer will have been subjected to a hadronic fluence which, in terms of NIEL, is equivalent to $10^{15}$ 1MeV neutrons cm$^{-2}$. The consequence of this for the sensors is that at the design operation-bias-voltage of 600V, the expected energy-deposition for 1MIP will be significantly reduced compared with the non-irradiated case. The electronics chips, themselves compromised by an ionising-radiation dose of 250kGy, must maintain sensitivity to these smaller signals whilst being immune to increases in leakage currents of up to 30nA per pixel implant. The spatial resolution in $\rho \phi$ is to be as high as possible given the constraints arising from bump-bonding and electronics-layout issues. The power consumption is not to exceed 40µW per pixel.

5.2 Design Features

In each FE-chip, 2880 channels are arranged into 18 column by 160 rows. The input receivers and output drivers are LVDS for all of the digital signals. Serial 5MHz-configuration-command and 40MHz output-data protocols are implemented in order to minimise the number of required connections.

The chips have integrated DACs providing the necessary biases for the analogue front-end circuitry. Each channel is equipped with its own 3-bit DAC for channel-to-channel threshold adjustments, thus a means of overall dispersion reduction is provided. All of the demonstrator chips have 7-bit charge measurement capability using time-over-threshold (TOT), taking advantage of the available deadtime per pixel (~2µs excepting the B-layer). Also featured is a global hit-OR (hitbus) which provides for a means of self-triggering operation. This is particularly useful when using $\gamma$-sources for absolute calibration determination.

A 2880-bit pixel register plus one corresponding latch per channel enable individual pixels to be masked-off for (independently) calibration-strobing and readout.

The charge-sensitive preamplifiers of both FE-A/C and FE-B feature a DC feedback scheme with a tuneable current providing control over the shaping-time for a given input charge.

The front-end of FE-B differs from FE-A/C in that it features a dual-threshold discriminator. In operation the thresholds are set such that the faster of the two, (the time-discriminator), is lowest and is used to define the timestamps for the leading and trailing pulse-edges. For a hit to be tagged, the pulse must cross through the upper level-threshold, (which is optimised for noise occupancy and efficiency), before registering a trailing edge through the time-threshold. This scheme also provides improved crosstalk performance since the level-discriminator may be operated more slowly than in a single-discriminator design.

The readout-architecture implementations are also markedly different for the two designs. In FE-A/C each column-pair is served by an 80-bit 40MHz shift register to clock leading-edge (LE) and trailing-edge (TE) hit-information towards the end-of-column (EOC) circuitry. There the timestamps of the hits are determined from the row-number information along with the time-of-arrival at the EOC. Since the length of the shift registers is 80-bits only one LE or TE from a 4-pixel cell may be introduced for a given BCO. If extra hits are registered in a particular crossing then their information is held until the next available crossing and a 2-bit late-field is used to indicate the required correction to the hit age at the EOC.

In FE-B the global time information is distributed throughout the array to every pixel as 7-bit Gray-code. When a hit is tagged in a pixel cell the timestamps for the LE and TE are stored locally. Meanwhile a continuous vertical-sparse-scan operates along the column pairs seeking tagged hits. As soon as such a hit is seen, the geographical and timing information is sent directly to the 20 buffer-sets at the end of each column-pair.

In the EOC buffers any hits which match the present latency-corrected timestamp are deleted unless a corresponding trigger has been received. Received level-1 triggers are buffered in a 16-deep trigger FIFO. The presence of a record at the top of this FIFO initiates a two-dimensional horizontal-sparse-scan which looks through the EOC buffers for hits which are then serially transmitted from the chip at 40MHz. The TOT is calculated for each hit as the TE-LE time-difference prior to this, resulting in a 7-bit charge field in each 26-bit hitword.
6: LABORATORY STUDIES

6.1 Threshold-Dispersion and Noise

A standard assembly test procedure is to perform a scan of calibration-pulse amplitudes for all channels. Error-function fits to the derived s-curve histograms of efficiency versus charge yield estimates of the threshold and equivalent noise charge (ENC) when combined with the magnitude of the calibration capacitance.

In Figure 6 distributions of thresholds are shown before and after the 3-bit trim-DACs (TDACs) for each channel have been tuned in order to minimise the dispersion. An initial dispersion of 296e- for this single-chip assembly is reduced to 105e-. The mean threshold is around 3ke- which is a standard operating point for most of the laboratory and testbeam operations. Typically the initial dispersion for the demonstrator chips is in the range 250e- to 450e- when bump-bonded to the prototype sensors [3]. The leftmost plot in Figure 7 shows the distribution of ENC for an assembly incorporating the base-line sensor design. A mean value of 176e- is recorded. The other plot shows the same distribution for a FE-chip bonded to a sensor which has been irradiated to 1.0X10^{15} 1MeV neutrons per cm^2 NIEL-equivalent dose (i.e. 10-years inner-layer hadronic fluence). The ENC, now dominated by the sensor leakage current, is measured to be 291e-.

6.2 Timing-Dispersion and Timewalk

Many studies of the timing performance of the demonstrator chips have been performed in the laboratory. The lower plot in figure 8 shows three distributions of time for all channels of a single-chip assembly for injected charges of 5,000, 10,000 and 100,000e-. The width of the distribution at 10ke- is 1.1ns whilst that at 5ke- is 2.2ns. The relative position of the distributions on the x-axis illustrates the degree of timewalk over this range of input charge. The upper three plots show the timewalk curves (time vs. charge) for three individual channels. Overall the charge for which the timewalk is measured to be 20ns relative to 50,000e- is around 7ke- at 3ke- threshold.

6.3 Crosstalk

The crosstalk between neighbouring channels within a column is measured by injecting a very large range of charge into a particular channel whilst reading out only its two neighbours. An error function is fit to the resulting hit-count vs. charge histogram and the median value is used along with the known threshold of the particular channel to estimate the percentage charge loss. In figure 9 the crosstalk for a single-chip assembly incorporating the baseline sensor design is shown to be 2.0% which compares well with the 5% ATLAS specification.
7. TESTBEAM EVALUATION

Detailed evaluation of demonstrator assemblies with irradiated and non-irradiated sensors [3] has been carried out during 7 running periods of the H8 testbeam at CERN’s SPS facility. Efficiencies of 99% are typically recorded for the non-irradiated cases whilst a device with a sensor irradiated to the maximum 10-year fluence (for the inner layer) yielded 98.2% at a threshold of 330e-.

The charge measurement capability has enabled comparative studies of charge-collection efficiency (CCE) vs. position within a pixel cell to be performed for 2 generations of prototype sensor layouts. Figure 10 shows such a map of CCE for the baseline sensor design. The uniformity is excellent with only a very slight dip at the inter-pixel position corresponding to the location of the reach-through bias grid structure.

8. 16-CHIP MODULE EXPERIENCE

Figure 11 shows distributions of threshold and noise for a 16-chip module assembled using a first-prototype flex-kapton hybrid. The sensor design is from the first-prototype design series and is expected to have better noise performance than the baseline design. A threshold dispersion of 171e- is recorded, the ENC peaks at 136e-.

In figure 12 the efficiency for the 16-chips superimposed is plotted as a function of time. An overall efficiency of 99% is extracted from this.

9. RADIATION HARD FE DESIGNS

The first radiation-hard design (FE-D) maintains the spirit of the demonstrator programme (i.e. pin-compatibility, same pitches etc.) and combines features of both FE-A/C and FE-B. The front-end design is based on that of FE-C. Constraints in pixel-cell space introduced by the DMILL process ruled out the possibility of the BiCMOS FE-A front-end being used along with that of FE-B. The digital readout architecture is derived from FE-B with some refinements, e.g. low-voltage swing signals for the column-pair readout bus’ sense amps at the EOC, (for reduced digital cross-coupling). The DACs are now formed from a 2D array of current mirrors for radiation tolerance. Plans are underway for a new system which will enable testing of digital operation at speeds of up to 100MHz in anticipation of the expected slowing of the logic arising from radiation exposure.

A design for the Honeywell SOI process (called FE-H) is also in preparation.

10. REFERENCES

A pixel readout chip for tracking at ALICE and particle identification at LHCb


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2) INFN Rome, Italy
3) University and INFN Bari, Italy
4) University of Glasgow, Glasgow, UK
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Abstract

The ALICE1 chip is a mixed-mode integrated circuit to read out silicon pixel detectors used for particle tracking in the ALICE Silicon Pixel Detector or particle identification in the LHCb Ring Imaging Cherenkov detector. The chip will be fabricated in a commercial 0.25µm technology and transistors are designed with a radiation-tolerant geometry. It consists of 256 x 32 pixel cells, each of 50µm x 400µm, and can be operated in one of two modes. In tracking mode, all cells are read out. In particle identification mode, 8 cells are grouped together, reducing the effective granularity to 32 x 32 cells of 400µm x 400µm. The cell architecture is described in detail, together with the two operational modes and issues of system integration.

1. INTRODUCTION

Pixel detectors will form an integral part of the detector systems of the Large Hadron Collider (LHC) at CERN. Using a hybrid structure of sensor and readout chip, they offer several advantages over other detector technologies in the severe environment of the LHC. The low noise and low power consumption per channel obtainable with such devices will allow the construction and operation of systems with high channel densities, low mass, and tolerance to radiation. The ALICE experiment [1] will use pixel detectors as part of its Inner Tracking System (ITS) [2]. Here, the pixel system will have to track particles in a high multiplicity environment close to the interaction point. The LHCb experiment [3] is investigating three different technologies for photon detectors in its Ring Imaging Cherenkov detector (RICH), one of which uses pixel sensors and readout chips to detect photoelectrons produced by Cherenkov photons. Although the requirements of the two detectors are quite different, an architecture for a pixel readout chip has been designed which, by means of a selectable mode of operation, can satisfy the needs of both systems. This paper describes the architecture of the chip, known as ALICE1, and its application in ALICE and LHCb.

2. PIXELS FOR TRACKING IN ALICE

2.1 Requirements

The silicon pixel detector in ALICE will form the two layers of the ITS closest to the interaction point. Thus a major requirement is that the mass of the system be minimised to reduce the chance of multiple scattering. Tracking precision is required in the r-φ direction with a resolution of 12µm. The nature of the heavy ion collisions will generate events of high multiplicity, and the system must be able to cope with a hit occupancy of 1%.

Any hits detected by the readout chip must be delayed until the arrival of the Level-1 trigger, which has a maximum latency of 10µs and a rate of a few kHz depending on the types of particles being collided in ALICE. The duration of the trigger signal is one clock period of the 10MHz system clock, so the delay of hits must be accurate to 100ns across this 10µs. The readout of the pixel chips is initiated by a Level-2 trigger, which has a maximum latency of 100µs and a rate of a few kHz.

To keep the deadtime under the specified 10%, the readout of an entire event from the pixel detector system must be completed within 400µs. The final requirement is that the system be tolerant to an ionising radiation dose of 500krad, integrated across 10 years of LHC operation.

2.2 Implementation

To minimise the mass of the detector, the silicon sensors will be thinned to 150µm. This implies that the most probable signal produced by a minimum ionising particle will be about 12,000 electrons. Hits detected by
the front end will be time-stamped according to the system clock and then precisely delayed by means of digital circuitry. All events accepted by the Level-1 trigger will be buffered inside the chip, which allows a number of chips to be readout sequentially using the 10MHz clock within the required 400µs.

The detector system will be constructed from a number of components. The basic ‘building block’ is a ladder, which consists of 8 readout chips bump-bonded to a single silicon sensor. 4 ladders are aligned in Z to form a stave, and the entire system consists of 60 staves arranged in two barrels around the interaction point.

A readout unit is formed by a half-stave of 16 chips, read out sequentially in 400µs. A half-stave is shown schematically in Figure 1. The 120 half-staves of the system are read out in parallel.

![Figure 1: Schematic of an ALICE half-stave, showing the 16 front-end chips and 2 silicon sensors, readout electronics and connector. The length of a half-stave will be about 20cm and the width 17mm.](image1.png)

3. PIXELS FOR PARTICLE ID IN LHCb

The concept of encapsulating a pixel sensor and readout chip within a vacuum tube to form a hybrid photon detector (HPD) has been demonstrated with a number of prototypes [4],[5]. This has led to the development of larger area pixel HPDs in the framework of LHCb [3]. Figure 2 shows schematically the concept of the pixel HPD. Photons incident on an optical input window release a photo-electron from a photo-sensitive cathode layer deposited on the inner surface. These photo-electrons are accelerated within the vacuum by a high potential and electrostatically focussed onto an anode which in this case is the pixel sensor and chip. The data from the chip is transmitted out of the device by means of vacuum-tight feed-throughs.

![Figure 2: Schematic of a pixel HPD.](image2.png)

3.1 Requirements

The demands on such a device are dictated by the sensitivity requirements and the need to maximise the data produced for physics analysis. The HPDs must be sensitive to single photoelectrons. They must also provide a very clean signal, since a high proportion of noise hits will deteriorate the pattern recognition. The requirements on spatial resolution can be met with a 2.5mm × 2.5mm channel size, but this also implies an occupancy of up to 8% in some regions of the RICH detector.

3.2 Implementation

The accelerating voltage applied to the HPDs will be 20kV, which generates a signal of around 5000 electrons in the pixel sensor. The encapsulation of the electronics within the vacuum envelope means that the chip and its packaging must be compatible with all the steps in the manufacturing process of the HPD. Additionally, since the vacuum will present difficulties to the removal of heat, the chip must consume minimal power.

The electrostatic focussing demagnifies an image on the input window by a factor of 5, so the 2.5mm × 2.5mm channel size maps to a 500µm × 500µm granularity on the pixel sensor.

Triggered events are de-randomised by buffering on the chip, and a 40MHz clock is then applied for the readout. A complete detector system for the RICH of LHCb would consist of 500 HPDs.

4. THE ALICE1 CHIP

The complementary requirements of these two detectors can be met by the architecture of the ALICE1 chip, described in this and the following sections.

4.1 Chip description

The chip will be fabricated in a commercial 0.25µm CMOS process. This offers two major advantages, namely a high component density and an intrinsic radiation tolerance due to the thin gate oxide of the transistors which will undergo only small changes in threshold voltage after irradiation [6],[7]. The radiation
tolerance is further enhanced by the use of enclosed gates for the NMOS transistors to minimise drain-to-source leakage, and guard rings to prevent inter-component leakage and reduce the risk of electrically- or radiation-induced latch-up [8]. A test chip designed in the same technology and with the same transistor layout geometry remained fully functional with up to 30Mrad of X-ray irradiation [9]. All digital storage elements in the chip have been designed to be immune to single-event-upset, a phenomenon which can alter the configuration of a chip during operation. They use a special latch design which recovers its original state following an upset [10].

Both the analog and digital circuitry has been designed to operate with a 1.6V power supply, and the total static power consumption will be 400mW. The chip will contain around 9 million transistors.

Figure 3 shows a schematic floorplan of the chip. The sensitive area measures $12.8 \text{mm} \times 12.8 \text{mm}$, and is divided into 8192 pixel cells of $50 \mu m \times 400 \mu m$. These pixels are arranged in 256 rows and 32 columns. The remainder of the chip consists of peripheral control logic, biasing circuitry, a JTAG serial interface and the input/output blocks, which will be described in Section 6.

### 4.2 Pixel Cell

The pixel cell is divided into an analog and a digital part, as shown in the schematic of Figure 4.

The analog front-end consists of a pre-amplifier followed by a shaper stage with a peaking time of 25ns. Both of these blocks are differential, with one input carrying the detector signal and the other tied to a clean reference. This has been done to improve the common-mode rejection of the circuitry and to minimise the sensitivity to digital switching noise injected into the front-end through the substrate. A test input can be given to the pre-amplifier using a voltage step applied across a capacitor. The size of the step is controlled on the chip and is triggered by a logic pulse generated externally. This scheme avoids having to send an analog test pulse to the chip, which would be sensitive to any external noise in the system.

A discriminator compares the output of the shaper with a threshold fixed globally across the chip. In addition, each pixel contains three logic bits which can be used to finely adjust the thresholds on a pixel-to-pixel basis. The outputs of the discriminators in the pixel matrix provide a fast-OR signal which is foreseen for diagnostic purposes during testing and for self-triggering. The static consumption of the front-end of each cell is 50µW.

![Figure 4: A schematic of the circuitry within one pixel cell](image)

The discriminator output is fed into the digital part of the cell. The first stage consists of two digital delay units, whose purpose is to store a hit for the duration of the trigger latency. Each delay unit consists of an 8-bit latch which, on receipt of a hit from the discriminator, latches the bit-pattern present on an 8-bit bus. This pattern is the Gray-encoded contents of an up-down counter whose state changes synchronously with the clock and has an adjustable modulo $n$. Gray-coding was chosen to minimise the digital switching in each clock cycle, and thus reduce the risk of noise coupling into the analog circuitry. The time structure of the pattern is shown in Figure 5.

![Figure 5: The time structure of the pattern used to timestamp hits in the delay units.](image)

The contents of each latch are compared with the pattern on the bus and, on each positive comparison, a 2-bit counter is incremented. The third positive comparison occurs $2n+2$ clock ticks after the hit, and a logic one is
then presented to the coincidence logic. This state also resets the delay unit. In this case, 2\(n+2\) clock ticks represent the trigger latency and this can be adjusted to meet the requirements of the experiment.

The result of the trigger coincidence is loaded into the next-available cell of a 4-event FIFO, which acts as the multi-event buffer and de-randomiser. This FIFO is read/write addressable by means of two 4-bit busses which again carry Gray-encoded patterns. The contents of the FIFO cells waiting to be read out are loaded into a flip-flop by the Level-2 trigger in ALICE and a NEXT-EVENT-READ signal in LHCb. The flip-flops of each column form a shift register, and the data is shifted out using the system clock.

Finally, there are five latches inside the cell whose contents switch on or off the test input to the front-end, mask or activate a pixel, and provide the three bits of threshold adjustment. These latches have been designed to be resistant to single-event upset.

Much attention has been paid to reducing the risk of noise injection via the substrate. In addition to the Gray-encoding of the busses and the differential front-end, the logic cells used in the pixels are current-starved, to minimise any bounce induced in the power supplies during switching.

5. OPERATIONAL MODES

With the addition of some extra logic, this architecture can be used for both applications. The mode of operation is selected by an external control signal.

5.1 ALICE mode

In this mode, each pixel cell acts as an individual channel and the full matrix of 256 \(\times\) 32 cells is read out.

Using the two delay units, each cell has the capability of simultaneously storing two hits for the trigger latency.

The 32 columns are read out in parallel. Using the 10MHz clock, a complete event is read out from the chip in 25.6\(\mu\)s. Figure 6 shows the configuration of the pixel cells in ALICE mode.

5.2 LHCb mode

In LHCb mode, eight pixels in the vertical direction are configured as a ‘super-pixel’ of 400\(\mu\)m \(\times\) 400\(\mu\)m, which is close to the LHCb requirements of 500\(\mu\)m \(\times\) 500\(\mu\)m.

The discriminator outputs of the super-pixel are OR-ed together and the sixteen delay units of these eight cells are configured as an array. Four of the 4-event FIFOs are connected together to form a 16-event FIFO, which can be written to by any of the sixteen delay units. This meets the required de-randomiser depth for LHCb. The FIFO output is loaded into the flip-flop of the top pixel in the group, which bypasses the other seven during readout. This scheme reduces the matrix to 32 \(\times\) 32 cells and allows a complete event to be read out within 800ns using a 40MHz clock. Figure 7 shows the configuration of the pixel cells in LHCb mode.

The sixteen delay units are necessary for storing the large number of hits which will occur in the high occupancy regions of the RICH. Additionally, the use of the eight separate analog blocks reduces the effective occupancy seen by the front-end. If the occupancy
remained high, then there would be a risk of pulse pile-up and a subsequent loss of hits. Thus, the segmentation of the front-end relaxes the requirements on the return-to-zero time of the pre-amplifier and shaper.

6. PERIPHERY, CONFIGURATION AND I/O INTERFACE

The peripheral logic of the chip contains the counters to address the delay units and the FIFOs. Additionally, there are a number of 8-bit digital-to-analog converters to provide voltage and current references for the analog front-ends and the current-starved logic. Any memory on the periphery is again constructed from un-upsettable cells. At the top of the chip will be a number of test cells connected to analog output buffers which will allow the observation of the pre-amplifier and shaper outputs during chip testing.

The configuration of both the peripheral logic and the matrix of pixel cells is done by means of a serial interface following the IEEE JTAG standard [11]. This has a number of advantages. It allows both the write and read of the configuration settings in the chip, including the test, mask and threshold-adjust states of each pixel. It also allows the reading back of the analog levels generated by the digital-to-analog converters via an additional output line. Connectivity tests of chips mounted on a stave can be done using the boundary-scan feature of JTAG. Additionally, the JTAG test feature has been adapted to detect bad chips in the serial chain and indicate their location.

The width of the ALICE stave restricts the number of lines available for signalling, and for this reason a single-ended standard has been adopted. Gunning Transceiver Logic (GTL) [12] will be used for all the digital signals to and from the chip. This has the advantage of a low signal swing (~800mV) which again reduces the risk of noise injection. Additionally, the output buffers on the chip have an adjustable slew-rate control which can be controlled to match the system requirements. These buffers are powered with a supply separate from that of the rest of the chip. Finally, multiple bonding pads have been provided for the supply lines to minimise the inductance of the connection and limit the supply bounce during switching.

7. CONCLUSIONS

The ALICE1 chip has been designed with an architecture which provides the functionality required by both the ALICE tracker and the LHCb RICH. The choice of a deep sub-micron technology has allowed the inclusion of a large amount of functionality within each pixel to meet the demands of both experiments.

Careful consideration has been given to a number of factors. Firstly, the risk of switching noise has been minimised by design features. Furthermore, the power consumed by the front-end has been kept to a minimum. Questions of testability have been addressed, and the chip contains features which are foreseen to ease its integration into a system. Finally, the circuitry has been designed to be tolerant to radiation, both total dose and single event effects.

The final stages of the chip layout are underway. Chip testing is planned to begin in 2000 and will be followed by first system tests.

8. ACKNOWLEDGMENTS

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9. REFERENCES

FPIX1: an Advanced Pixel Readout Chip
A. Mekkaoui, J.A. Appel, G. Cancelo, D. Christian, J. Hoff, S. Kwan,
R.J. Yarema, S. Zimmermann.
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1. INTRODUCTION

At Fermilab, a pixel detector for BTeV is proposed for installation a few millimeters from the beam. Its information will be used in on-line track finding for the lowest level trigger system. This requires a high-speed readout and immediate data transfer from the pixel chip to the trigger processor. It is also believed that a 2-4 bits of analog information is required to achieve the targeted spatial resolution [1] with 50µm wide pixels.

Our first prototype, FPIX0 [2], is now being used in a beam test to confirm physics simulations and to determine the required resolution of the analog “information”.

Our 2nd prototype, FPIX1, is a 160X18 pixel readout chip compatible with the ATLAS family of detectors. We have build and tested 4 FPIX1-detector assemblies. FPIX1 is realized in the HP 0.5µm process. The main features of FPIX1 are:
- 2bit flash ADC on each cell for maximum speed.
- Triggered or stand alone operation.
- High speed sparse and time ordered Readout.

2. THE FPIX1 CHIP

The FPIX1 is a column based pixel chip with 50×400 µm pixel cells arranged in an array of 160 rows by 18 columns. FPIX1 stores hit information awaiting readout in the pixel unit cells, and uses an indirect addressing scheme to reference the hits to BCO numbers held in registers at the end of each column. Instead of using pointers to accomplish the indirect addressing, as in [3], FPIX1 uses a command driven design, which is described below. The chip can be divided into three mutually dependent pieces: the Pixel Cell, the End-Of-Column (EOC) Logic and the Chip Command Logic (Figure 1).

The responsibility of the Chip Control Logic is to control and maintain all features that are common to the chip such as the clocks, the “current” and “requested” BCO numbers, and the status of off-chip communication. Each one of the eighteen EOC Logic cells controls one column.

The EOC Logic responds to information from the Chip Logic, and from the 160 pixels in a column by broadcasting commands to the Pixel Cells, and by arbitrating with the other EOC Logic cells for control of the on-chip data bus. Finally, each Pixel Cell connects to one sensor pixel and responds to commands from the EOC Logic. The commands used in this architecture are the following: the “input” command instructs a Pixel Cell to accept hits from its sensor pixel and to respond to a hit by alerting the EOC. In the absence of an input command, the hit is ignored. The “output” command instructs the Pixel Cell to prepare to write its information onto the bus. The “reset” command instructs the Pixel Cell to reset its contents. Finally, the “idle” command instructs the Pixel Cell to do nothing.

To buffer for 4 hits and decrease the column dead time, each EOC Logic cell consists of four EOC command Sets, each one capable of generating its own commands. When a Pixel Cell receives a hit, it immediately associates itself with whatever EOC Set is broadcasting the “input” command. From that point until it is reset or output, the Pixel Cell only responds to commands from its associated EOC Set. Meanwhile, the EOC Set holds the timestamp. The EOC Set can then issue the “output” or the “reset” command. The hit information is stored inside the Pixel Cell until readout.

The Chip Command Logic supports two readout modes. The first one, the “continuous” readout mode, requires no external trigger. This mode is expected to be used in the BTeV experiment. The other readout mode is the external trigger mode, in which an external system must provide the timestamp of the hits that should be read out. This mode is applicable for pixel detectors with external trigger, and for diagnostic purposes.

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2.1 Pixel Cells

The pixel cells hold the front-end electronics and the digital interface with the EOC Logic. The FPIX1 front-end is based on a design implemented in the FPIX0 and Pre-FPIX1 test chips. References [2,4] report in detail on measurements of FPIX0, both unbonded and bonded to an ATLAS test sensor. The front-end (Figure 2) contains a charge sensitive amplifier (CSA) and a second amplification stage. The DC feedback used in the CSA is similar to the one described in [5]. The average recovery time of the CSA can be adjusted from 50 ns to 1 ms by an external current source without requiring any reset signals to be transmitted across the sensitive analog region. The output of the second stage connects to a 2 bit flash ADC and a discriminator.

The digital interface of the pixel cell is depicted in Figure 3. It has two major components: the Command Interpreter, and the Pixel Token and Bus Controller. The Command Interpreter has four inputs, corresponding to the four EOC command Sets. Commands are presented by the EOC Logic simultaneously to all pixel cell Interpreters in a column. When an Interpreter is executing the input command and the Hit output from the discriminator is asserted, the Interpreter associates itself with the particular EOC Set that is issuing the input command. Simultaneously, it alerts the EOC Logic to the presence of a hit via the wire-ored HFastOR signal. After the association to a particular EOC Set has been made, the Interpreter ignores commands from all other EOC Sets. The pixel hit information is stored in the cell until the associated EOC Set issues an output or reset command.

When the associated EOC Set issues the output command, the Interpreter issues a bus request and asserts the wire or-ed HFastOR signal. This operation is executed independent of the master readout clock (Rdclk). The balance of the readout proceeds synchronous with the Rdclk. The EOC Logic provides a column token on the bottom of the column as a means to regulate bus access. The token quickly skips pixel cells with no information until it reaches a cell that is requesting the bus. This propagation to a hit pixel is done in less than one clock cycle, even if the pixel is the last in the chain. At the next rising edge of the Rdclk, the hit pixel with the column token loads its data onto the bus and drives it to the EOC logic for one clock cycle. In parallel, the column token is transmitted to the next hit pixel, pipelining the output of the Pixel Cell with the token passing. This allows the readout of one Pixel Cell per clock cycle, without any wasted Rdclk cycles. The data is composed of the ADC count Bits[3:1] and the row address Read[7:0]. As the hit pixel is read out, it automatically resets itself and withdraws its assertion of the RFastOR. The RFastOR returns to its inactive state while the last of the hit pixels is being read out. This way, the EOC Logic is able to detect when the last hit pixel in the column is being output. At the next rising edge of the Rdclk, control of the on-chip bus is transferred to the next column with hit data.

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1 Rdclk is referred to as MClk in figure 4.
At any given time, only one EOC Set is permitted to broadcast the input command. This ensures that hit pixel cells are associated with only one EOC Set. Pixel cells that have not been hit continue to monitor all four EOC Sets, waiting for a coincidence of hit and input commands.

2.2 End of Column Logic

Figure 4 shows a block diagram of the EOC Logic. It consists of a Priority Encoder and four EOC command Sets. The EOC Sets themselves consist of a timestamp register, a state machine for generating the appropriate EOC commands, and two comparators.

The Priority Encoder selects one EOC Set to issue the input command. When there is a hit somewhere in the column, the HFastOR signal is asserted, and the state machine inside the assigned EOC Set responds by latching the Current BCO (CBCO) in its EOC timestamp register and by issuing the idle command at the next rising edge of the BCO clock. This ensures that all pixels in a particular column hit in the same clock period are associated with a single EOC Set. The Priority Encoder assigns the next EOC Set to issue the input command to the column (at the rising edge of the BCO clock). Since the EOC Logic has four EOC Sets, pixel cells in the column can be hit without loss of data in four different crossings before any data is read out.

A “hit” EOC Set waits for matches with its stored timestamp BCO (SBCO). If the match is between the Requested BCO (RBCO) and the SBCO, the EOC Set broadcasts the output command, and if the match is between the Current BCO (CBCO) and the SBCO, it broadcasts the reset command. Any of the bits in the comparison between CBCO and SBCO can be programmed to be ignored. This allows for a user defined reset delay. This feature is designed primarily for the externally triggered readout mode.

3. RESULTS

We have thoroughly tested the FPIX1 chip both with and without a detector. In this paper we will focus on chips bump bonded to detectors. We have bonded several chips to different types of detectors (All from the same wafer form Seiko) that were provided by the ATLAS collaboration. Figure 9 shows a chip-detector assembly on the test PCB.

The readout was found to work as expected, despite a minor bug. A typical output sequence of the FPIX1 RO is shown in figure 11 as captured from a logic analyzer. The data valid bit (DV) indicates the presence of a valid data, which should be strobed at each negative edge of the readout clock. First the chip outputs the chip ID and the time stamp then the addresses and the ADC values of all pixels hit during that time stamp.
result was the same for p-spray and p-stop detectors.

performed at different locations across the chip. The test was the same for p-spray and p-stop detectors.

similar results were obtained with the other type of detectors.

An important design criterion is threshold and noise dispersion within one chip. Without a detector, we consistently measured across several chips threshold dispersion of about 250e-, at low threshold setup. The noise averages about 40e- rms, with a standard deviation of less than 3e-. After bump bonding to a detector the threshold dispersion was about 300e- rms and the noise reached about 70e- rms. After bonding the detectors we had to disable some extremely noisy pixels (about 25 in the bottom left corner of the detector as shown in figure 10) to perform adequate measurements. The excess noise is believed to be due to some bumps, being shorted together and/or to the guard ring.

Figure 9 and 6 depicts the threshold and noise distributions of an FPIX1 bumped to a p-spray detector. Similar results were obtained with the other type of detectors.

We were unable to detect any cell to cell cross-talk at a 2000e- threshold with the maximum input charge of 80000e-. The test was done by injecting only one cell and looking for any of its neighbors to fires. The test was performed at different locations across the chip. The result was the same for p-spray and p-stop detectors.

4. CONCLUSION

As summarized in table 1, most of the obtained results meet or exceed the preliminary specifications suggested by the BTeV collaboration. Our immediate plan is to beam test the described system and have a confirmation regarding the required resolution in the analog information. We are also planning to design a radiation tolerant quasi final chip next year. A small prototype front-end circuit has been already submitted for fabrication in a 0.25µ CMOS process.

5. REFERENCES


Table 1 Summary of the main results.

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<td>Cell to Cell Xtalk</td>
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</table>

Figure 11 A typical FPIX1 output sequence (6 pixels hit)
Performance Studies of Pixel Readout Electronics in RICMOS IV-SOI and DMILL processes

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Abstract

The CMS Pixel Collaboration investigates two radiation hard processes, DMILL and RICMOS IV-SOI Honeywell, for the production of the front-end electronics. To evaluate the applicability of the two technologies for this project a readout chip for a 22x30 pixel detector array has been developed. Chips were fabricated first in DMILL process (PSI30) [1], and then we translated this architecture to RICMOS IV technology. For both implementations, detailed measurements are presented before and following irradiation up to 30 Mrad.

1. INTRODUCTION

Experiments at the forthcoming LHC will place stringent requirements on electronics used in the tracking of charged particles, especially for those components which will be installed close to the beamline. The devices will be exposed to irradiation levels around 50 Mrad and 10^14 particles/cm^2 over their life time. Nevertheless, low noise operation is to be preserved, timing resolution must remain adequate and power consumption per channel has to be kept at a tolerable level. The technology used determines the quality of the whole readout system. To make the best choice and to prepare alternatives for mass production, the CMS Pixel Collaboration has been investigating two radiation hard processes: DMILL [2] and RICMOS IV [3].

We have previously tested the applicability of enhanced RICMOS IV (0.65 µm SOI CMOS) technology for pixel detector front-end electronics by measuring DC, AC and noise parameters of NMOS and PMOS transistors before and after irradiation with gammas from Co^{60} up to a total dose of 50 Mrad [4]. All devices remained functional after irradiation with no anomalous behaviour. The threshold voltage of the top channel shifted less than 140 mV for PMOS and 200 mV for NMOS transistors. The transconductance decreased only by 10% for PMOS and 20% for NMOS transistors. No radiation induced leakage current was observed over the entire duration of the tests. The devices exhibited low noise characteristics. After 30 Mrad the white serial noise increased by 10% for PMOS and 30% for NMOS.

2. READOUT CHIPS

2.1 Chip overview

The main purpose of the chips discussed here is to implement fully the analogue block and evaluate it with all the realistic difficulties of an electronic system, like power surges, crosstalk and device variations in larger pixel arrays. Therefore the analogue block has all functions implemented, but the readout block has a reduced circuit architecture and has been changed in subsequent versions of the chip. Each pixel cell contains a preamplifier, shaper, comparator, flag register and a shift register directing the readout. The gain of the preamplifier as well as the time constant of the shaper are controlled by feedback resistors. The shaper output is connected to a capacitor, which acts as an analogue store, and to the input of the comparator. A common threshold for all pixels can be set. For pixel to pixel variations a threshold trim mechanism is implemented using a 3-bit SRAM. One trim state is reserved to switch the comparator off. This pixel masking capability allows the removal of noisy pixels. In the data taking mode the same mechanism can be used to inject a calibration test charge into selected pixels. The readout is organized in double columns of pixels. The double column periphery is equipped with control logic that recognizes a hit in a pixel, provides a twelve-bit buffer for time stamping and organizes the data transfer from the pixels to the periphery.

All bias voltages and bias currents have to be set externally. This allows the control of parameter shifts before and after irradiation. In the final pixel chips biasing will be realized by an I2C programmable control register, DACs and current sources.

2.2 Physical Implementation

The architecture and the circuit schematics of both chip implementations are widely identical, but there are also some differences.

- The layout of the Honeywell chip has been changed to benefit from the advantages of the RICMOS IV process: higher transistor density and three metal layers for the interconnections.
- The DMILL chip consists of 660 pixels organized in 22 columns with 30 pixels per column. The RICMOS IV chip contains 704 pixels at 32 pixels a column.
- On a RICMOS IV chip a pixel covers an area of 125µm x 125µm. In the measured version of the DMILL chip (PSI34) the size of the pixels has been changed to 150µm x 150µm to accommodate the optimized size of the detector cell.
- The analogue output stage in this DMILL version
3. EXPERIMENTAL RESULTS

3.1 Test set-up

The chips were mounted and wire-bonded on a fine line PCB. The board was interconnected to a peripheral PCB carrying the additional components necessary for power supply, bias generation, input and output buffers. The analogue and digital outputs were unity gain buffered. The drive system was based on the Tektronix pattern generator DG2020 used to program the trim bits of each pixel cell and to set the calibration mechanism and for generate the repetitive readout sequences. A programmable pulse generator of the HP8110A series served to inject a test charge into the pixel cells. A LeCroy scope displayed and digitized the output data, and finally the programmable Racal-Dana 1992 counter recorded the detected hits. The whole system was controlled by a PC running LabView software.

3.2 Measuring conditions

The chips were characterized electrically using the analogue test input. A variable X-ray source enabled us to calibrate the test capacitance. This amounts to 1.73 fF and 1.68 fF for DMILL and RICMOS IV respectively. The DMILL and RICMOS IV chips were set up with the bias currents and voltages optimized for correct operation in each case. However the total power dissipation for both designs was kept the same and equal to 40 µW per pixel. The measurements were performed before and after irradiation with photons from a Co^{60} source. The following quantities were examined: shaper response, analogue output, noise, timewalk and threshold behaviour.

3.3 Measurements before irradiation

Fig. 1 shows shaper pulses of DMILL and RICMOS IV chips corresponding to an input charge of 10000 e\(^{-}\).

Fig. 1 Signal pulse at the shaper output

Obviously the RICMOS IV type is faster and produces higher amplitudes. This can be explained by the fact that transistors in RICMOS IV technology have lower drain capacitance. Fig. 2 presents the gain of the preamplifier-shaper chain for both versions. In both cases we observe a good linearity in the range below 15000 e\(^{-}\). In this region the gain amounts to 30 mV/1000 e\(^{-}\} and 35 mV/1000 e\(^{-}\} for DMILL and RICMOS IV, respectively. Above 15000 e\(^{-}\} the response becomes non-linear. Due to the planned charge sharing between adjacent pixels, we have adjusted the chips to have a large gain for relatively small pulseheights at the expense of some non-linearity for the relatively unlikely large pulses. Fig 3 illustrates the signal at the analogue output of the chip for the two implementations. Both curves show approximately the same characteristics as the corresponding shaper output (Fig. 2), but the gain of the DMILL circuitry is larger. This is due to the improved output stage in the measured version of DMILL chips (PSI34). This improvement is not yet implemented in the RICMOS IV chips.

The noise of the amplifier in each design is determined by a threshold scan as shown in Fig. 4. For this measurement the discriminator threshold is set to a fixed value (2200 e\(^{-}\)). Test charges with increasing amplitudes are then injected into a pixel. The fraction of hits detected by the discriminator is modulated by the noise of the amplifier. The slope of the curve is thus proportional to the noise. The rms width \(\sigma\) of the Gaussian noise distribution is given by the increase of signal charge needed to raise the detection efficiency from 50% to 84%.
Typical values are 160 e⁻ and 80 e⁻ for DMILL and RICMOS IV respectively.

Another parameter important to the operation of the pixel arrays at LHC is the timing performance of the complete system. Pixel hits must be correctly associated with the proper LHC bunch crossing. However, precise determination of the hit time is often limited by pulse-height-dependent delay effects (timewalk). This has been studied by measuring the timewalk as a function of the input charge. The threshold used for this study is 2500 electrons. The time is measured relative to the response time for very large signals (30000 e⁻). It is clear that for charges close to the threshold, timewalk becomes very significant and the discriminator is not fast enough to meet LHC requirements. For RICMOS IV input charges of more than 420 e⁻ above threshold are needed to have a delay of less than 25 ns, whereas the DMILL version requires an input charge of more than 1190 e⁻ over threshold for a delay of less than 25 ns (Fig. 5).

We have measured the variations of the pixel thresholds before and after trimming. For this measurement the chip was run in its regular mode using the time stamp mechanism. The distribution of the thresholds in a complete chip before and after adjustment is shown in Figs. 6 and 7 for DMILL and RICMOS IV, respectively. There is no systematic dependence of the threshold on the position of the pixel within the chip. The plots illustrate that after trimming the width of the threshold distribution has significantly decreased to roughly 120 e⁻ in both cases. The minimal threshold which could be achieved amounts to 2200 e⁻ and 1500 e⁻ for chips realized in DMILL and RICMOS IV technology respectively. This difference can be explained by the fact that the power distribution in the RICMOS IV implementation is better since we use two metal layers for power arrangement. Also the crosstalk between the analogue part and the digital part is reduced (due to the higher transistor density in RICMOS IV technology, the size of these two blocks is smaller and the distance between them can be made larger).

3.4 Measurements after irradiation

To investigate the radiation hardness of the chips a Co⁹⁰ source was used. The chips were irradiated to 10 Mrad and 30 Mrad at a dose rate of 150 rad/s, measured with an accuracy of 10%. The chips were tested directly after irradiation and after annealing for one week at 100°C. In both cases the bias voltages were set to achieve as much as possible the same pulse shape as for the unirradiated case, and the settings for the bias currents were adjusted to give the same supply currents as prior to irradiation.

After the 10 Mrad irradiation chips were operational (except that for the DMILL chip the pixel masking feature was not functional any more). After 30 Mrad the RICMOS IV chip was operational, but the DMILL chip was not (its pixel analogue electronics and the readout part were operational, but its calibration mechanism and
the programming mechanism were out of order). This made testing of the chip impossible. Since only a single chip was irradiated to 30 Mrad, conclusions should be drawn only after more samples have been irradiated and measured.

Fig. 8 illustrates for both the DMILL and RICMOS IV implementations the change of the bias voltages for the preamplifier stage, its feedback transistor and the source follower as a function of the total irradiation dose. It is seen that the shift of the bias voltages in DMILL (approx. 400 mV) is by a factor of two higher than in RICMOS IV (approx. 200 mV).

As shown in Figs. 9a and 9b for both technologies we observe no change of the shaper pulse. The noise measured as described before does not increase significantly (from 160 e before irradiation to 170 e after 10 Mrad for DMILL and from 80 e before irradiation to 90 e after 10 Mrad and to 100 e after 30 Mrad for RICMOS IV).

Figs. 10a and 10b illustrate the linearity of the analogue output for both versions of the chip before and after irradiation. We observe that the gain of the analogue output of the DMILL chip decreases slightly for large pulses after irradiation to 10 Mrad. The gain characteristic of the analogue output remains stable for the RICMOS IV chips even after irradiation up to 30 Mrad.

In Figs. 11a and 11b we plot the timewalk measurements performed on a single pixel. The Figures display no change of the timewalk for pixels in DMILL technology after 10 Mrad. The same measurements for pixels in the RICMOS IV chip show a that the charge over threshold corresponding to a timewalk of 25 ns has a small increase from 420 e before irradiation to 490 e after 30 Mrad. The threshold scan for the complete chip after irradiation and annealing shows that in the DMILL case the average threshold and the threshold dispersion remain the same, but we observe a kind of “edge effect” for RICMOS IV technology. As illustrated in Fig. 12a irradiation alone does not cause a significant change of the threshold behaviour, if one neglects a slight shift of the distribution.
However, as shown in Fig. 12b, after annealing pixels in the outer columns, #1 and #22 at the border of the chip, show a remarkably higher threshold: The threshold value is nearly twice as large as before. We do not see such problems for any other pixel within the pixel array. Such behaviour has not been observed for annealed chips not exposed to $\gamma$ irradiation. Thus it seems that the combination of radiation and heat deteriorates the behaviour of those pixels sitting close to the chip border.

We have not yet been able to determine the cause of the problem.

4. CONCLUSIONS

The prototype readout chip for the CMS pixel detector has been manufactured first in DMILL technology. This full mixed-mode circuit has then been successfully implemented in Honeywell RICMOS IV technology. The RICMOS IV run achieved a very good yield of 85%. We have made a comparative study of both designs. The measurements show that both prototypes are fully functional before as well as after irradiation to 10 Mrad. The results presented demonstrate that the RICMOS IV implementation has a better performance than the DMILL one in shaper response, noise, timewalk and threshold behaviour before as well as after irradiation. Following irradiation the shift of the bias voltages in the RICMOS IV version is smaller than for DMILL. Apart from “edge effects”, which we have observed in the RICMOS IV implementation after irradiation and subsequent annealing, measurements established that the RICMOS IV circuit tolerated a total gamma dose of 30 Mrad, while maintaining full functionality with only minor degradation of parameters. The high transistor density and the availability of four metal layers in the RICMOS IV technology are very advantageous because of better power distribution and lower area consumption. Our experience shows that to implement the same functions one needs an active area smaller by a factor of two in the RICMOS IV technology than in the DMILL case.

5. REFERENCES

RECENT DEVELOPMENTS AND RESULTS ON APV(DMILL) CIRCUITS FOR SILICON AND MSGC DETECTORS

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Abstract

For the analogue read-out of the CMS tracking system several variants of the APV design have been developed in DMILL technology: the APV\textsubscript{D}\textsubscript{A}C and APV\textsubscript{D}\textsubscript{C} for AC and DC-coupled silicon detectors, respectively, and a rapid front-end amplifier with 25 ns peaking time based on a bipolar transistor for the possible use of MSGC or silicon detectors. This paper introduces these circuits developed in the DMILL technology and focuses then on experimental results obtained with prototypes on silicon and MSGC detectors in a 200 GeV pion beam.

1. INTRODUCTION

Based on experience with the APV6 circuit\cite{1} developed in the HARRIS AVLSIRA bulk CMOS technology and on a circuit of similar architecture FILTRES\cite{2} in the radiation hard technology DMILL\cite{3}, the work on the APV\textsubscript{D}\textsubscript{C} circuit for the CMS tracker was started in the beginning of 1998 by a Franco-British collaboration. The architecture and the schematics of the APV\textsubscript{D}\textsubscript{C} are essentially identical to the APV6 and consist of 128 analogue channels, each composed of a low noise preamplifier, a CR-RC shaper with 50 ns shaping time, a 160 cell deep analogue pipeline operated at 40 MHz and an analogue signal processing stage (a deconvolution filter) which recuperates the initial fast response of a silicon detector and confines it to one LHC bunch crossing. One amplitude per trigger of each of the 128 channels is read-out serially via a high-speed 20 MHz multiplexer. Slow control is implemented on the chip using an I2C serial bus which allows to configure and to run the internal calibration system. For the most technology dependant part, the preamplifier and shaper, a design was adapted and modified from the schematics of the FILTRES amplifier. We have reported at previous conferences on the design and on measurements of this circuit\cite{4,5,6}.

2. THE APV\textsubscript{D}\textsubscript{C} CIRCUIT

2.1 Translation of APV circuit

The APV\textsubscript{D}\textsubscript{C} represents the first experience of translating a complete large mixed analogue-digital chip from one technology to another. Its immediate complete functionality can be regarded as a success of this translation. However, we also had to report on an instability problem of the analogue base line which was observed in all versions of the circuit up to now and which limits partially its use for detector tests. Numerous investigations of the circuit using various simulation tools and micro interventions on the chip itself revealed that these instabilities or oscillations are a collective phenomenon which only occurs if a minimum number of channels are active, the critical parameter being the total current drawn in the bias lines. Under these conditions the unavoidable common resistances in the ground and bias lines will establish various loops which couple in particular the source follower which drives the capacitive load of the pipeline, back to the preamplifier input. The phase shifts in the amplifier structure are crucially influenced by the parasitic capacitances which are specific in each technology. Eventually a resonance pole can appear within the bandwidth of the amplifier.

Consequently, the schematic and the layout of the amplifier have been revised rigorously to eliminate all possibly occurring couplings. In contrast to other circuit designs in DMILL technology which reported also stability problems in the past\cite{7}, and who use bi-polar input transistors, we have found only very weak evidence for capacitive feedback problems related to the back-plane of the SOI substrate in our circuit. However, precautions were taken in the last submission to avoid capacitive feedback. For more details see reference\cite{8} in these proceedings.

2.2 APV\textsubscript{D}\textsubscript{C} circuit

DC-coupled silicon microstrip detectors have significant advantages compared to AC-coupled devices due to their less complex fabrication process and
The preamplifier feedback loop provides already a NPN transistor embedded in a folded cascode topology. Achieved good but not quite the anticipated values. Tests of the fabricated circuit power of the input transistor to obtain the required speed one using only CMOS elements, increasing size and low noise performance. Problems occurred during these tests due to the instability of the APVD baseline discussed above. Although a large part of these oscillations could be corrected for by a common mode baseline correction, the remaining electronic noise was by about a factor of two higher than the values observed on our electronics test bench. This high level of noise affected the efficiency measurement as well the measurement of the delay curve in regions where the amplitude is very small. Nevertheless encouraging results were obtained.

### 3. OPTIONS FOR MSGCS

MSGC detectors will contribute to about one half of the over 10 million analogue read-out channels of the CMS tracker. Although not dissimilar to silicon microstrip detectors with respect to the total charge collected, a number of significant differences have to be accounted for. In particular, the signal formation time is determined by the ca. 60 ns long drift time and by statistical event-to-event fluctuations of the primary ionisation charge along the particles path in the sensitive gas volume of the detector. They lead to important variations of the signal peaking time and amplitude. This prevents the unique association of the measured amplitude to the bunch crossing (bco) in which the event was generated. The precision cannot be much better than 2-3 bco.

#### 3.2 Simulations

Numerous filtering algorithms employing different weights and different samples of the pipeline spaced by 25 or 50 ns have been evaluated in rather detailed simulations of the MSGC and the associated electronics[9]. Although significant differences between various signal processing methods occur, in general algorithms which optimise the amplitude or the detector efficiency lead to an analogue response spread over several bunch crossings. On the other hand the signal can be confined to a narrower time interval at the cost of some amplitude. In the end an optimum has to be found which will also depend on the precise operation parameters at which the MSGC will eventually be run.

In these studies the possible use of a faster shaping of the order of 25 ns at the input stage of the circuit has been proposed to improve the timing precision.

#### 3.2 Bipolar Amplifier

Two test circuits have been designed and submitted. One using only CMOS elements, increasing size and power of the input transistor to obtain the required speed and low noise performance. Tests of the fabricated circuit achieved good but not quite the anticipated values.

A second circuit was designed on the base of a bipolar NPN transistor embedded in a folded cascode topology. The preamplifier feedback loop provides already a sufficient short time constant, so no further shaping is required. A second stage is used as an active filter to eliminate noise outside the useful bandwidth. At a power consumption of 1.4 mW/channel a peaking time of 25 ns and a gain of 90 mV/mIP with a non-linearity of less than 5% over ±6 MIPs dynamical range was measured. Its noise performance of 1000 electrons ENC was obtained for a detector capacity of 12 pF. For further details see reference[10] in these proceedings.

### 4. OPERATION OF THE APVD_AC ON MICRO-STRIP DETECTORS

In September 1998 APVD_AC circuits where mounted on small 6 cm long silicon micro-strip detectors with 64 active read-out strips at 50 µm pitch. One circuit was connected to a MSGC detector of ca 230 µm pitch via 400 Ohm serial resistors implemented on the pitch-adapter in order to better protect the circuit against discharges. Both types of detectors were installed at CERN in a 200 GeV pion beam of the SPS accelerator. A high precision silicon telescope of 1-2 micron spatial resolution allowed precise track reconstruction to evaluate detector efficiencies and resolutions.

Problems occurred during these tests due to the instability of the APVD baseline discussed above. Although a large part of these oscillations could be corrected for by a common mode baseline correction, the remaining electronic noise was by about a factor of two higher than the values observed on our electronics test bench. This high level of noise affected the efficiency measurement as well the measurement of the delay curve in regions where the amplitude is very small. Nevertheless encouraging results were obtained.

#### 4.1 Results from Silicon Detectors

In Fig. 1ab we present the delay curve measuring the analogue response of the circuit and the track reconstruction efficiency as a function of time and in Fig. 1c the obtained spatial resolution on the peak. The results are shown for peak- and deconvolution-mode operation of the circuit on the left and right hand side of the figure, respectively. Operating the circuit in peak-mode we obtain an excellent efficiency of 99% and resolution of 7 µm despite a signal to noise ratio of only 12 due to increased noise. The timing curve does not coincide with a ideal CR-RC shaper, however is being reproduced by the in the laboratory measured response function with the actual bias settings during the beam-test, in particular the shaper feedback transistor.

In deconvolution mode the efficiency is reduced to 93% by the decreased signal to noise ratio of only 7 at the peak of the timing curve, but the measured spatial resolution of 11 µm is still good. We note that the delay scan in this mode is not being reproduced by the electronic response to an injected very short test pulse. The profile observed with particles in the beam is wider. This could be caused
by tails in the charge collection of the silicon detectors; however, a remaining effect from the large base-line oscillations cannot be ruled out.

4.2 Results with a MSGC Detector

Operating the MSGC at a moderate cathode bias of 520-530 Volts and a drift field of 2900 Volt per 3 mm gap in a 60/40 DME/Ne gas mixture a peak efficiency of 97% was obtained for tracks traversing the chamber perpendicularly with a signal to cluster-noise ratio of 17.

In Fig. 2 we show a delay-scan of the MSGC signals operating the circuit in peak-mode. The measurements are compared with two simulations, one using an ideal CR-RC amplifier response which falls faster than our data, and one folding the measured transfer function of the chip at the actual bias settings with the MSGC signal simulation. The latter curve reproduces very well the timing curve over the measured range. This agreement supports confidence in the use of simulations to optimize the signal processing algorithms.

The number of reconstructed clusters per single incoming track as a function of angle compared to simulations with equivalent cuts.

Fig. 3: Number of reconstructed clusters per incoming track as a function of angle compared to simulations with equivalent cuts.

by tails in the charge collection of the silicon detectors; however, a remaining effect from the large base-line oscillations cannot be ruled out.

Fig. 1abc: Results for silicon detectors: Delay scan of signal shape (a) and reconstruction efficiency (b) together with the obtained spatial resolution (c) in peak and deconvolution mode on the left and right hand side, respectively.

Fig. 2: Pulse shape of a MSGC detector signal obtained by a delay scan with the APVD compared to a detector and electronics simulation using an ideal CR-RC and the real shaper transfer function.

Fig. 3: Number of reconstructed clusters per incoming track as a function of angle compared to simulations with equivalent cuts.

The number of reconstructed clusters per single incoming track is compared in Fig. 3 to simulations as a function of the incident angle of the particle. As expected, the number of clusters increases as the track inside the MSGC is spread over several strips. The low average number of primary ionization clusters of about 12 and their fluctuations will lead occasionally to cluster
splitting and thus increase their average number per track. Choosing appropriate cuts in analysis and simulation the trend of the data is very well reproduced.

Similarly we observe an increase of the cluster width at larger incident angles. Also the spatial resolution changes from 40 µm to 1 mm for incident angles between 0° and 45°. respectively.

5. PRELIMINARY RESULTS OF IRRADIATION STUDIES

5.1 X-Ray Irradiation of the APVD_AC Chip

A separate paper[11] in these proceedings describes first irradiation results of a complete APV6 circuit. A 10 keV X-ray beam available at CERN was used to irradiate a circuit at a dose-rate of 15 krad/minute up to 20 Mrad. Important effects were observed concerning the linearity of the DAC converters in the bias generator block. As described in the paper, a modified layout has been implemented in the last submission of the APVD chip to correct for this.

The pulse shape changes slightly (-25% in amplitude and +10 ns in peaking time) if measured during irradiation at the nominal I2C bias settings. This change is partially due to the simultaneous changes of the bias settings. A good fraction of the pulse shape distortions are recovered some hours after irradiation. Running the CMS experiment, the shape could be retuned continuously.

During irradiation the noise increases at a rate of about 30-40 ENC/Mrad and recovers after 24h to a level about 250 ENC above its initial value.

5.2 High Intensity Pion Irradiation of the BiCMOS Front-End Amplifier

As the radiation hardness of DMILL bipolar transistors has been a crucial issue in the past we irradiated our BiCMOS amplifier in an intensive pion beam of PSI with an integrated flux of 10^{14} particles/cm², corresponding to about 10 years of LHC operation. Small changes in gain and speed were measured several days after irradiation. A change of beta from initially 200 down to 30 can be deduced from these changes. Nevertheless the circuit demonstrates full satisfactory functionality after irradiation.

6. PERSPECTIVES AND CONCLUSIONS

The APVD circuits provide the first LHC-radiation hard front-end chip to the CMS tracker. After the circuit had been translated into the DMILL process, the development has been severely delayed by the unforeseen occurrence of subtle feed-back loops within the amplifier architecture. We are confident that the modifications implemented for the last submission will overcome this problem.

In addition, a specific adaptation to DC coupled silicon detectors has been developed which will work up to leakage currents of at least 10 µA per channel. This option will allow more flexibility in the choice of detectors.

In the context of optimising the bunch identification capability of the MSGC detectors a fast 25 ns shaping front-end amplifier was designed and tested which may find also applications for other detectors.

Several evolutions in CMS have taken place during the last 10 month and will possibly modify the input for our further work: the CMS Tracker detector technology is under review to overcome possible weaknesses at high particle fluxes. The introduction of a GEM gas amplification plane in the MSGC detectors could affect the time development of the signal if the chamber is not operated at identical drift fields. Alternatively a “silicon only” tracker is being considered. - Certainly, optimisation of efficiency at relatively low gain operation has taken priority over timing precision. A possible submission of a DMILL MSGC circuit by the end of 1999 based on a 50 ns shaping time and containing also other important adaptations to MSGCs similar to the APV6_M[12] will be prepared. However its execution will depend on decisions taken by CMS during the next months.

Secondly, a further translation of the APV design into a 0.25 µm process is being attempted[13]. Although this technology is not qualified for a high irradiation environment, possibly it is proven to be so if certain precautions are respected in the layout[14].

Therefore, on the long term the further development of the APVD family will depend on the choice of detectors for the CMS tracker and also, much more important on the choice of technology for the tracker front-end electronics.

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8. REFERENCES

3 DMILL, A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics,


7 F. Anghinolfi et al.: ABCD, these proceedings;
M. Newcomer et al.: ASDBLR, these proceedings;

8 C. Hu-Guo et al.: APVD_AC and APVD_DC, these proceedings;

9 F. G. Sciacca, CMS note 1997/022 and 1997/105; -
J. F. Clergeau: thèse de doctorat IPNL Lyon 1997; -
J. Croix: thèse de doctorat IReS Strasbourg 1999; -
and references therein;

10 C. Hu-Guo et al.: Low Noise BiCMOS preamplifier..., these proceedings;

11 M. Dupanloup et al.: Irradiation ..., these proceedings;


13 L. L. Jones et al.: APV25, these proceedings;

RADIATION HARDNESS OF THE ABCD CHIP FOR THE BINARY READOUT OF SILICON STRIP DETECTORS IN THE ATLAS SEMICONDUCTOR TRACKER

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Abstract

The radiation hardness requirements of the ABCD chip are driven by the radiation levels expected in the ATLAS SCT after 10 years of LHC operation, which are 10 Mrad of total ionising dose and $2 \times 10^{14}$ n/cm$^2$ of 1 MeV eq neutron fluence for the displacement damages.

The ABCD chip, comprising both analogue and digital circuitry and realised in a BiCMOS technology, is sensitive to ionisation effects as well as to displacement damages. The recent prototype of the ABCD chip, which meets all SCT requirements, has been irradiated separately with X-ray, neutrons from a nuclear reactor, and with 24 GeV protons. In the paper we present and discuss the radiation effects observed in the ABCD chip.

1. INTRODUCTION

The development of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker [1] has been completed recently. The architecture of the ABCD design is reminded here very shortly since it has been presented and described before [2]. The block diagram of the chip is shown in figure 1. It comprises all blocks of the binary readout architecture, the front-end circuits, discriminators, binary pipeline, derandomizing buffer, data compression logic, and the readout control logic.

The first ABCD prototype chip met most of specification, however, the spread of the discriminator threshold in the front-end was not satisfactory. Analysis of the problem led us to a conclusion that given the matching performance of the DMILL technology, in which the chip was realised, we could not guarantee the required performance, following the original circuit concept. In addition, the performed irradiation tests indicated that matching performance degraded significantly after irradiation. Therefore, we upgraded the design by implementing a threshold correction using a digital-to-analogue converter (TrimDAC) per channel.
The prototypes, ABCD2T and a slightly tuned version of the original design (ABCD2NT - without TrimDACs), have been manufactured successfully. Both versions are fully functional and meet the specifications. The performance and parameters of the two versions are presented and discussed in another paper [3].

In this paper we focus on the radiation hardness issues of the ABCD2T chip since this option has been chosen as a preferred one for the SCT. There are two important aspects to be taken into account when considering the radiation hardness of the ABCD2T chip:

(a) the chip is realised in a BiCMOS technology so one has to pay attention to the ionisation effects as well as to the displacement damages,

(b) there is a number of specific effects related to the ABCD2T architecture and particular circuit implementations.

The DMILL technology is qualified as a radiation resistant one. However, the radiation levels expected for the SCT detector in the ATLAS experiments are at the upper limits of those specified for the DMILL process, i.e. 10 Mrad of the ionising dose and $1 \times 10^{17}$ n/cm$^2$. 1 MeV eq. neutron fluence. In addition, if one takes into account very advanced requirements regarding the noise, speed and power consumption of the ABCD2T chip, it becomes obvious that radiation effects in the basic devices, although limited, can not be ignored.

2. RADIATION HARDNESS ISSUES

On top of a general requirement that the chip should be fully functional after irradiation up to the maximum specified levels, there are some particularly critical issues of the ABCD design, which should be considered carefully with respect to radiation effects. The most critical aspects are: noise of the front-end, matching in the front-end circuit, in particular the offset spread of the discriminator, and the speed of the digital CMOS part.

2.1 Noise

The front-end circuit of the ABCD2T chip is built as a transimpedance amplifier using a bipolar input transistor. One of the noise sources, which contribute to the equivalent input noise charge is the shot noise of the base current of the input transistor. Due to a short shaping time of 25 ns, as required for the SCT readout, and a large detector capacitance, the relative contribution of this noise is acceptable as long as the base current does not exceed a level about 2 μA. For given detector capacitance, shaping time and current gain factor $\beta$ of the input transistor, one can find an optimum value for the collector current which yields a minimum value of ENC.

In modern bipolar transistors the current gain factor $\beta$ is degraded by the ionisation effects as well as by the displacement damage. Both types of radiation effects, ionisation and displacement damage, lead to reduction of the lifetime of minority carriers in the transistor base. Thus, a significant degradation of $\beta$ has to be anticipated, which implies that first of all the circuit design has to be insensitive to variation of $\beta$, regarding DC bias conditions as well as AC characteristics. With respect to noise there are two aspects to be taken into account, namely the size of the transistor and the collector current in the input transistor.

The degradation of $\beta$ depends on the actual current density in the transistor, therefore from that standpoint of view one would prefer to use a minimum geometry transistor in the input stage. On the other hand, in order to minimise the series noise contribution from the base spread resistance, one would rather use a large area input transistor. These two requirements are contradictory and an optimum size of the input transistors can be defined provided we know how the $\beta$ degrades after irradiation for a given technology. The radiation effects in the bipolar transistors in the DMILL technology have been studied and based on these results [4] we chose the emitter area of the input transistor to be $1.2 \times 10^3 \mu m^2$.

From the radiation tests performed up to now we expect that $\beta$ of the input transistor will change significantly, by a factor of about 4, during the lifetime of the ATLAS experiment. With the $\beta$ value decreasing during the lifetime of the experiment the optimum value of the collector current in the input transistor will also decrease. Therefore we have implemented a 5-bit DAC to be able to adjust the current and optimise the noise performance according to the actual value of $\beta$ in the input transistor. In addition, the bias current in the following stages of the front-end amplifier is also controlled by another 5-bit DAC, which allows to adjust DC biasing of the circuit and compensate the drifts due to decrease of $\beta$ in the bipolar transistors, shifts of the threshold voltages in MOS transistors and increase of resistor values.

![Fig. 1. Block diagram of the ABCD chip.](image-url)
2.2 Matching

One of the most critical issues of the binary architecture, as implemented in the ABCD design, is the matching of parameters of the front-end circuit since a common threshold for 128 channels in one chip is used. The effective threshold of the discriminator is determined by the offset of the discriminator and by the gain of the amplifying stages preceding the discriminator. The preamplifier stage has to be implemented in a single-ended configuration and the gain of the circuit is sensitive to variation of resistors which are used in the feedback loops. Thus, channel-to-channel matching of the gain is limited by the resistor matching across the whole chip. The discriminator circuit is based on a fully differential structure so that the offset of the discriminator is determined by the local matching of resistors and transistors.

From the tests performed for the previous ABCD prototype we have drawn the following conclusions:
(a) matching of resistors is a limiting factor for the offset spread in the discriminator,
(b) matching performance of resistors, which are available in the DMILL technology, is not sufficient to guarantee that the SCT requirements regarding the threshold spread can be met using the original scheme of the discriminator,
(c) matching of resistors degrades significantly after irradiation.

Taking these aspects into account we have proposed and implemented a scheme with individual threshold correction per channel. This is realised by 128 4-bit DACs (TrimDACs) implemented in ABCD2T design.

2.3 Speed of digital CMOS blocks

The digital part of the ABCD chip comprises a number of various blocks, including static and dynamic logic, synchronous and asynchronous circuits. The chip is required to work at a clock frequency of 40 MHz for any set of corner parameters as specified by the vendor, including the changes after irradiation up to 10 Mrad. In addition, the ABCD chip is designed for a digital power supply of 4 V, which is below the nominal supply voltage of 5 V specified for the DMILL technology. In order to cover possible variation of the process parameters, temperature, supply voltage and post-irradiation changes, the digital part of the ABCD chip was designed to work at least at a clock frequency of 80 MHz for the typical process parameters before irradiation and for supply voltage of 4 V.

3. IRRADIATION TESTS

The ABCD2T chips have been irradiated in three different experiments:
(a) with 24 GeV proton beam using the T7 irradiation facility at CERN PS accelerator,
(b) with neutrons from the nuclear reactor at Ljubljana,
(c) with X-ray of 10 keV using a standard X-ray facility at CERN.

The proton and the neutron irradiation have been performed for the chips mounted on the ceramic hybrids of the same type as foreseen for the final SCT modules. On each hybrid there was 6 chips, 3 ABCD2T chips and 3 ABCD2NT chips. In this paper we discuss only the results obtained for the ABCD2T chips with the TrimDACs since this option has been chosen for further evaluation. During irradiation the chips were biased and clocked at nominal conditions and the trigger signal was sent in order to exercise all readout blocks in the chips in a similar way like they will work in the experiment.

During proton irradiation the hybrid with the chips was kept inside a cold box filled with nitrogen at temperature about 2°C, while the measured temperature of the hybrid was higher, about 10°C. The proton beam of the size about 1×2 cm² was scanned across the hybrid. The chips were irradiated up to a fluence of 3×10¹⁴ p/cm² during a period of 10 days. The measurements were taken every one or two days, depending on the beam intensity. All basic parameters and characteristics were measured, including the noise and threshold spread, for various bias currents in the input transistor.

During the neutron irradiation the chips were biased and clocked in the same way as during the proton irradiation, however, the thermal conditions were different. The chips were not cooled and the temperature of chips was about 40°C.

The X-ray irradiation was performed for single chips mounted on an evaluation board. The bias and clocking conditions were similar to those used in the proton and neutron irradiation. In the X-ray test we focused on performance of the CMOS digital part of the chip.

In the radiation tests performed so far no particular annealing procedure was applied. The measurements were taken during irradiation or immediately after irradiation. This represents a worst case for the CMOS part since the radiation induced effects in CMOS components exhibit some annealing, which naturally will take place during irradiation with a low dose rate. For the bipolar components the performed tests represent an optimistic scenario due to the dose rate effect, which for bipolar devices means that an irradiation with a high dose rate is less damaging compared to an irradiation up to the same total dose but with a lower dose rate.

4. TEST RESULTS

The radiation test results regarding the chip performance and parameters are discussed in this section. It is important to note that all the results presented were obtained from standard test procedures in which the signal passes the whole data chain, from the internal calibration circuitry through the front-end, pipeline, and the readout circuitry.
4.1 Basic functionality

Given extreme radiation levels, which we used in our tests, a first question was whether there were no catastrophic failures in the chips which would prevent us from detailed measurements of chip parameters. For all performed irradiation we did not observe any of such a failure in the ABCD2T chips, i.e. the analogue parts remained biased correctly and the digital parts worked at least at 40 MHz.

The gain of the front-end circuit as a function of the current in the input transistor after X-ray, proton and neutron irradiation is shown in figure 2. The average gain of 128 channels in one chip is shown for each case. One can notice that after all irradiation tests the circuit still works for a wide range of the preamplifier current. A significant degradation of gain is observed after extreme neutron irradiation up to a fluence of $2 \times 10^{14}$ n/cm$^2$.

4.2 Noise

The irradiated chips have been measured with open inputs so that the capacitance at the preamplifier input can be neglected in a first approximation. Thus, the equivalent noise charge is determined by the parallel noise sources, i.e. thermal noise of the feedback resistor and the shot noise of the base current. Assuming that the changes of the feedback resistor after irradiation are negligible, one can associate the increase of noise with a higher base current due to degradation of $\beta$ in the input transistor. Figure 3 shows the noise as a function of the current in the input transistors after X-ray, proton, and neutron irradiation.

4.3 Matching

The irradiation tests were supposed to provide answers for two questions regarding influence of irradiation on the matching of device parameters:

(a) does the matching degrade after irradiation and,
(b) if so, is the range of the TrimDACs sufficient to cover the post radiation offset spread.

Figure 4 shows the distributions of discriminator threshold for 128 channels in one chip before irradiation (without correction), after proton irradiation up to a fluence of $3 \times 10^{14}$ p/cm$^2$ (without correction), and after irradiation and threshold correlation using the TrimDACs. One can notice a very significant degradation of threshold spread, by a factor of 3.5, after proton irradiation. After irradiation the TrimDACs work correctly and for majority of channels the offset can be corrected, however, some channels remain outside the range of the TrimDACs. These channels appear as flat tails in the distribution shown in figure 4c.

A similar behaviour of threshold spread was observed after neutron irradiation, however, the effect was smaller. After a fluence of $2 \times 10^{14}$ n/cm$^2$ the threshold spread increased by a factor of 2 and in this case the range of the TrimDACs was sufficient for effective correction of the threshold in all channels in the chip.
4.4 Performance of digital circuits

Regarding the radiation effects in the digital CMOS circuitry of the ABCD2T chip, a main concern is the speed, i.e. the maximum clock frequency at which the chip performs correctly all operations. Since the speed of the CMOS circuits depends on the power supply there are two parameters which provide information about the speed margins of the ABCD2T chip:

- (a) maximum speed measured at the nominal supply voltage of 4 V,
- (b) minimum supply voltage at which the chip works correctly at 40 MHz.

Figure 5 shows the degradation of speed of the ABCD2T chip after X-ray irradiation up to a total dose of 10 Mrad.

The results are shown for the following digital tests: TEST 1 - L1/BC counters check, TEST 2 - configuration check, TEST 3 - L1 overflow check, TEST 4 - data taking. We observe a degradation of speed almost by a factor of 2, nevertheless, after 10 Mrad the chip still meets the requirement of 40 MHz at the nominal supply voltage. It is worth to note that the results shown in figure 5 do not include any annealing so that they represent worst case post-radiation conditions.

5. CONCLUSIONS

Extensive irradiation tests of the ABCD2T prototype chips confirmed satisfactory radiation hardness of the design and the DMILL technology, in which the chip has been realised. The individual threshold adjustment per channel implemented in the ABCD2T design has been proved to work satisfactory after irradiation.

REFERENCES

PERFORMANCE OF THE ELECTRICAL MODULE PROTOTYPES FOR THE ATLAS SILICON TRACKER

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ABSTRACT

Electrical modules for the ATLAS Silicon Tracker (SCT) have been fabricated and tested. The modules consist of 6 ABCD front-end chips connected to silicon strip detectors, with the electronics hybrid and detector geometry as specified for the barrel and forward parts of the tracker. Tests were done with the second batch of the ABCD chip (ABCD2), connected to 6cm or 12cm long strip detectors. The functionality of the modules is demonstrated. The performance of modules depends on the signal gain in ABCD2 chips and on the grounding scheme. The design of the chip has been improved according to these observations. Recent results obtained with the new release of the chip (ABCD2T/NT) mounted on modules with 12cm strip detectors show the expected noise level of less than 1500 e\textsuperscript{+}, intrinsic stability and channel matching performance within 5\%.

1. INTRODUCTION

The ABCD design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker. The DMILL\textsuperscript{1} technology, in which ABCD is fabricated, is one of the possible choices for building the radiation hard front-end electronics. The functionality is fully compatible with another option developed for the SCT with two chips: CAFÉ-M, a front-end chip in MAXIM bipolar process, and ABC, a binary readout chip in rad-hard HONEYWELL CMOS process.

Initial results with single chips of the second run received last year (ABCD2) have been reported [1]. Modules have been built with 6 ABCD2 chips and the associated number of silicon strip detectors. Excessive mismatch of channel-to-channel threshold (already known at the chip level) and a large noise increase, observed only when all chips were mounted to the biased detectors, caused the analysis of the parasitic effects affecting the system stability and of the matching properties of some components. A new design (ABCD2T/NT) with protection against noise pick-up and the selection of new components from the technology has been done and chips were fabricated. The very recent results obtained with electrical module prototypes demonstrate the effectiveness of the new design.

2. CONSTRUCTION OF ELECTRICAL MODULES

The module prototypes are built according to the geometry of either the barrel part of the detector or the forward disks.

\textsuperscript{1} TEMIC Semiconductors, La Chantrerie, F-44306 Nantes
A typical geometry for the barrel is shown on Figure 1.

The electrical module has three main components: the silicon strip detector is made of two daisy-chained 6cm long p-on-n silicon strip detectors. There are 768 strips at a pitch of 80um. The hybrid is the support component for the electronics and provides the connectivity between detector, electronics and cables. The readout chips (ABCD) are glued and bonded directly to the hybrid. A realization of the hybrid for double-sided modules is shown in Figure 2 [2].

Figure 2: Kapton Hybrid for the barrel SCT detector (electrical prototype).

The geometry for the forward region uses an end-tap configuration and the hybrid has a “butterfly” shape. The typical layout for the forward hybrid and a preliminary drawing of the forward module are shown on Figure 3.

Figure 3: Kapton hybrid (a) and module (b) for the forward SCT detector (electrical prototype).

### 3. ELECTRICAL MODULE WITH ABCD2

The detailed evaluation of ABCD2 chip demonstrated complete functionality, a channel gain of 120mV/FC, a channel noise of 760e before detector mounting, but an excessive spread of threshold setting from channel to channel [1]. The construction of complete modules with 6 daisy-chained ABCD2 chips bonded to detectors exhibited a large increase in noise with 12cm strips, although with 6cm strips the noise remained acceptable. This is demonstrated on Figure 4.

Figure 4: S-curve 50% point distribution (upper curve) and noise distribution (lower curve) for one module with 2 ABCD2 chips with 12cm strips and 4 with 6cm strips

The upper graph on Figure 4 is the plot of the injected signal amplitude per channel (arbitrary units are on the vertical scale) to get the channel output being statistically 50% of the time 0 or 1 (the so-called 50% S-curve point) when threshold for all channels was set to 60mV. The horizontal axis shows the channel number, ranging from 1 to 128 for the first ABCD2 chip, 129 to 256 for the second chip, up to 768 for the last channel of the last chip. The two first chips (channel range from 1 to 256) were mounted with channels alternatively bonded to 6cm and 12cm strips. The last four chips (channel range from 257 to 768) were always bonded to 6cm strips. The lower plot of figure 4 shows the large increase in noise as soon as there are channels connected to 12 cm strips, affecting even the channels interleaved with 6cm strips.
Another demonstration of the excess noise with 12cm detectors is shown on Figure 5: the S-curve is plotted for all 128 channels for each of the 6 chips on one module. When all 6 chips are bonded to 6cm strip detectors only, the shapes of the curves are correct (except for the last chip in this figure) (plain lines on Figure 5). When one of the chips is bonded to 12cm strips instead of 6cm, the S-curves for all the chips are degraded (dotted lines on Figure 5).

![Figure 5: S-curve for each of the 6 chips on one module. Plain lines: all channels connected to 6cm strips. Dotted lines: one chip is bonded to 12cm strips (all others with 6cm).](image)

It was possible to deduce from these measurements the following conclusions [2,3,4,5]:

- The excess noise was unavoidable on modules with more than a few tenths of channels connected to 12 cm strips at nominal operating conditions
- It could be removed by reducing the signal gain per channel (60mV/fC instead of 120mV/fC)

Different combinations in hybrid ground plane geometry and different grounding schemes used to connect the detector bias to the analog ground of the chip were tested but without gaining any substantial improvement.

4. ABCD2T/NT DESIGN

4.1. Excess Threshold Spread Correction

Both new technology choice and design change were made to reduce the threshold spread observed on ABCD2 chips. The new ABCD2NT version keeps a high gain (140mV/fC) in signal amplification, but large size analog components are used to improve the matching properties. Also new high value resistors were used (extrinsic base resistor), instead of low implant resistor.

The ABCD2T version is using a more drastic option to reduce offset mismatch: there is a 4 bit linear DAC (trim DAC) included in each channel to correct for individual mismatch of the threshold in the range of 150mV. The 128 trim DAC are loaded with a new instruction set developed for this version of the chip.

4.2. Excess Noise Protection

The main correction concerns the pad layout of the channel inputs. DMILL is an SOI technology with an oxide buried layer framed inside the silicon volume below the active parts of the components. The silicon volume below the oxide (backside) can be left floating (no connection to any potential) or be connected to a potential as ground. The buried oxide layer acts as adding capacitance coupling between the nodes of some components (mainly the collector of bipolar transistors, the bottom of capacitors, the metal of I/O pads) toward the backside. In the case of modules with ABCD2, a very strong effect is observed depending on the connection of the backside to the ground. No stable operating condition was found (even without detector) if the backside was left floating. Simulation of the front-end (128 channels) with models of the couplings to the backside, with a full strip detector electrical model could confirm this observation. A possibility of the technology is to add a conductive implant layer below the pad metal [6]. The cross-section is shown in Figure 6. The buried implant layer is connected to a dedicated “ground” pad with no connection to other components of the chip, in order to minimize the risk of coupling the input pads to other nodes.

![Figure 6 : Cross-section of a modified input pad with shielding between pad metal and backside.](image)
5. ELECTRICAL MODULE WITH ABCD2T/NT

Electrical module prototypes with ABCD2T (low gain, trim DAC version) and ABCD2NT (high gain, no trim DAC) with 12cm strip detectors were found operating without excess noise in the full range of possible biasing of amplifiers.

5.1. Module with ABCD2NT

Figure 7 and 8 show the gain and the noise measured on a module with 6 chips and strip detector. Chip number 3 (channel range 256 to 383) is mounted with 1/3 channels to 12cm strips, 1/3 to 6cm strips, and 1/3 are not connected to detector. All other chips are connected to 12cm strips.

The noise amounts to 1400 (resp. 770, 430) electrons with 12cm strips (resp. 6cm and no detector bonded). The gain is as expected in the range of 140mV/fC.

Figure 9 represents the histogram of the S-curve 50% point along one module (the chip number 3 with different input loads has been removed from analysis). The spread of threshold is 7.8mV rms, which translates to 5.5% rms spread at 1fC threshold.

5.2. Module with ABCD2T

Figure 10 and 11 show the gain and the noise distribution measured on a module with 6 chips and strip detector. All chips are connected to 12cm strips. The noise amounts to 1375 electrons with the 12cm strips. The gain is in the range of 65mV/fC.
Figure 11: Noise distribution along one module (6 ABCD2T chips). Horizontal axis is mV. Vertical axis is mV.

Figure 12: Histogram of the S-curve 50% points for the 128 channels of chip 1 on module with ABCD2T chips, after trimming the threshold for each channel. Horizontal axis is in mV. Injected charge is 1.5fC.

Figure 13: Histogram of the S-curve 50% points for the 128 channels of chip 1 on module with ABCD2T chips, before trimming the threshold for each channel. Horizontal axis is in mV. Injected charge is 1.5fC.

Figure 12 represents the histogram of the S-curve 50% point along one module. The spread of threshold is 3.3mV rms, which translates to 5.1% rms spread at 1fC threshold. This value is obtained after the individual trimming of threshold for each channel. Before trimming the spread is 11.6mVrms (18.3% at 1fC threshold) as seen on figure 13.

6. CONCLUSIONS

We have built working electrical prototypes of the SCT modules designed for the barrel and forward parts of the detector. Results obtained with the last version of the ABCD readout chips (ABDC2T/NT) show a gain uniformity of less than 3%, noise level below 1500 electrons with 12cm silicon strip detectors, channel-to-channel uniformity of threshold of 5.5% at 1fC (ABDC2NT) or 5.1% at 1fC (ABCD2T, after trimming). Power consumption is 4V, 45mA for the digital part at 40MHz clock frequency, and 3.5V, 60mA for the analog part of the chip.

REFERENCES

3. ATLAS note ATL-INDET-99-006
5. http://hepwww.rl.ac.uk/atlas/tracking/ET/modtest.html
6. DMILL Design Guidelines, Spec No RDER2402
THE DEVELOPMENT OF THE CAFE-P/CAFE-M BIPOLAR CHIPS FOR THE ATLAS SEMICONDUCTOR TRACKER

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Abstract

A bipolar chip has been developed to provide the front-end functions of the binary readout architecture used for the silicon strip detectors in the ATLAS Semiconductor Tracker (SCT). This chip consists of 128 channels of low noise amplification and discrimination and provides an interface to a suitable CMOS data processing chip. The chip was successfully fabricated on the Maxim CB-2 process. Preliminary results including channel-to-channel matching, stability, noise, gain, and irradiation tolerance are presented. These results are compared to the previous CAFE-M chip and the ATLAS requirements.

1. INTRODUCTION

One solution for the baseline ATLAS SCT front-end electronics[1] is the bipolar – CMOS combination of the CAFE-P/ABC ASICs [2,3]. The CAFE-P is the most recent in the CAFE (Comparator Amplifier Front End) series of chips developed at UC Santa Cruz and Lawrence Berkeley National Laboratory. We discuss below the evolution of the CAFE design to meet the challenges of the ATLAS requirements, and the need for radiation tolerance in the hostile LHC environment. Preliminary data from the Cafe-M and Cafe-P are presented.

2. GENERAL CAFE ARCHITECTURE

The chips consist of 128 parallel channels of four stage amplifiers. Each channel has a single ended input to a charge sensing pre-amplifier, followed by a shaping stage (15 ns), a second stage amplifier, and finally a differential comparator. A common threshold is applied to the comparator of all channels via either a dc current input from the ABC chip, or an externally applied differential voltage pair. Each comparator then yields a current
output of approximately 130μA for all signals above the applied threshold (‘hit’) and 1μA for those below threshold (‘no hit’). Reference currents for the ‘hit’/‘no hit’ conditions are output for use by the ABC chip.

To simplify testing, a calibration circuit is provided by which test pulses may be injected into each channel of the pre-amplifiers. Four inputs are available from which these pulses may be provided externally, each to one forth the channels. In addition, an on chip chopper circuit is available which can be strobed from the ABC and will generate an internal test pulse in the CAFE. The magnitude of the internal pulse is set via a dc current from the ABC, and the channel selection by two voltage controlled inputs set by the ABC.

A constant current reference source (IDAR), has been provided to produce a stable current input to the ABC chip. Scaled portions of this current are then fed back to the CAFE chip to provide the threshold, and calibration pulse amplitude as mentioned above, as well as a third current which provides an adjustment for the pre-amplifier bias.

The layout consists of two rows of input pads on a 96um pitch, and three output rows to match the ABC. Power and servicing pads are redundant on both sides of the chip and routed through to the center of the chip before being supplied to the individual channels. This minimizes voltage drops across the chip and adds reliability in the event of bonding failures.

The 23 mm$^2$ die (Fig 1.) were manufactured with the MAXIM bipolar CB-2 process on 6” wafers. While this process has not been explicitly qualified as radiation resistant, it is inherently tolerant. Care was taken to design and simulate circuits that are tolerant with resistor increases of up to 90%, and β’s down to 20 while still biasing correctly.

### Figure 1. The ATLAS SCT CAFE-P.

The ‘M’/‘P’ versions of the CAFE chip primarily refer to the polarity of the input charge collected from the silicon detectors. The general layout and functionality is the same for both chips. The ‘M’ version was produced one year prior to the ‘P’ variety using the same process. Data presented below includes results from both versions of the CAFE.

### 3. PERFORMANCE & RESULTS

We have tested a large sample of CAFE-M and CAFE-P chips, both on wafer and mounted on a selection of hybrids and modules, to characterize their performance. Irradiations were performed on chips using the LBL 88” cyclotron providing 55 MeV protons, as well as with γ’s at UC Santa Cruz. Results for an equiv. 17 Mrad ionizing dose are presented below.

#### 3.1 ATLAS Requirements

Specifications have been set on the performance of the ATLAS SCT front end electronics which include:

- Low noise (<1500e with irrad detector)
- Excellent Threshold Uniformity. (<4% at 1fC)
- Low Power (<2mW/ch)
- Radiation Tolerant (10 LHC years)

The radiation hardness requirements of the CAFE chips are set by the levels expected in the SCT after 10 years of LHC operation. The chips are expected to function after levels which are projected to reach 10 Mrad of total ionising dose and 2x10$^{14}$ n/cm$^2$ of 1 MeV equivalent neutron fluence for the displacement damage.

#### 3.2 Support Circuitry Results

- IDAR Stability

The current source IDAR is fundamental to the operation of the CAFE chips, as it provides the scalable current for the threshold, pre-amp bias, and calibration amplitude. We find that IDAR is extremely stable with respect to bias voltage variation (Fig. 2), supply voltage (< 0.3 %), temperature and irradiation (Fig.3)

![Figure 2. Pre and Post irradiation variation of IDAR current with respect to bias voltage. Showing 3% drop in output current.](image-url)
Figure 3. IDAR temperature dependence. IDAR output is coupled directly to Ith input.

- Ith, Cali Linearity

The post irradiation linearity of the Ith generated threshold and Cali generated calibration amplitude are shown below in figures 4 and 5. An allowable threshold range of 0-700 mV is obtained and a maximum deviation of 0.6 mV over the 0.5 – 3.0 fC range of interest. The Cali circuit shows a 0 – 9 fC range and a maximum deviation from linearity of 0.03 fC over the region of 0-3 fC. In both cases we find excellent post irradiation functionality and < 0.5% change from the pre irradiation slopes, and thus the combined IDAR/Ith and IDAR/Cali circuits should prove radiation tolerant.

- Other Support Circuitry and Power Draw.

We observe a 15% drop in the output current of the ‘hit’ state of the comparator after irradiation. This should not be a problem as it is within the spec of the ABC input tolerance. No other problems in any of the other support circuitry have been identified, however, many of these functions (such as the internally generated calibration strobe) require the addition of the full ABC to test. This work is in progress.

Figure 6 shows the total current draw on Icc as a function of the supply voltage and the pre-amp bias current. For nominal settings of Vcc=3.5 and Viset = 200uA the total power draw is 1.5 mW/ch which is within the ATLAS specification.
3.3 Response and Uniformity

The ABC chip was not available at the time of this testing. All the following results were obtained with the CDP chip developed previously for SSC applications, and should not adversely affect the measurements. Calibration pulses and thresholds were set externally.

Prior to irradiation, the CAFE-M exhibited excellent amplifier performance [4]. However after irradiation a dramatic degradation in channel to channel matching, from 4% (1 σ variation across a single chip) to 25% was observed. This unacceptable uniformity was evident in the dispersion of the channel offsets in a typical response curve (Fig. 7), while the differential gain remained unaffected. Further measurements revealed the problem arose from large resistor increases, and decreases in β (>50%) of the pre-amplifier circuit, which caused the base current to change. This manifested itself in dc voltage variations at the input to the comparator.

To improve the post irradiation uniformity, the CAFE-P chip included a compensation circuit which corrected for the large resistor changes. In addition, the dynamic response was increased (~180 mV at 1fC) which gives a greater sensitivity to the threshold setting. The CAFE-P post irradiation response and uniformity are shown in figures 8 and 9. We see better than 4% uniformity at the nominal ATLAS threshold (1fC) after irradiation.

3.4 Noise and Module Stability

There was no observed difference in the noise and stability performance of the CAFE-M and CAFE-P. Figure 9 shows the noise for an irradiated Cafe-P chip with unloaded inputs. We measure ~750e noise, which is only slightly greater than the 700e found pre-irradiation.

With a single die on a hybrid, and no load on the input channel we find that the CAFE-P exhibits no sign of oscillation above a threshold setting of ~0.2 fC. A 6 chip set module (CAFE-P-CDP) with typical ATLAS P-type detectors was then constructed to study the stability and noise performance of a more complex system.

Figures 10 and 11 show the response and noise at 1fC threshold for the module. Chip 6 (channels 640-768) is the same CAFE-P for which the previous irradiated measurements in this paper were obtained. All other CAFE-Ps are not irradiated. Chips 5 and 6 were also connected to the 12cm detector. Again we observe excellent uniformity at 1fC across individual chips, less than 2% for the non-irradiated CAFE-Ps and approximately 4% for the irradiated chip. We also see good response uniformity across the entire module with the exception of chip 1 which has a small (15mV) threshold offset. For
this module, a single threshold was applied for the entire module. With the ABCs we will have individual threshold control for each chip so this threshold shift will not appear.

The noise performance for the CAFE-Ps not connected to detector channels is in agreement with previous measurements. The two chips connected to a detector show 13000 and 14000e noise for the unirradiated and irradiated chips respectively. This is well within the ATLAS required noise performance with 12cm detector.

The module was stable down to a threshold of approximately 0.3 fC which is slightly greater than observed with a single chip, but well within the acceptable performance range.

4. CONCLUSIONS
We have presented preliminary results that show the CAFE-M chip functionality meets the major requirements requirements of power, uniformity, noise and stability, but failed to be radiation tolerant. An adjustment to the circuit was made, and the CAFE-P appears more radiation tolerant while preserving excellent functionality within the ATLAS specifications.

Work continues on the same detailed characterization of the CAFE-P which was completed for the CAFE-M and presented at the SCT week. To date, we have found no significant problems. Further studies with the recently completed ABC [4] are underway, and full prototype module construction are planned. Preliminary wafer sorting shows we are obtaining yields of perfect chips near the 75% level.

REFERENCES
2. N. Spencer et al., Project Specification-CAFE-P V4.01.
3. A. Grillo et al., Project Specification-ABC V5.01
Progress in development of the ASDBLR ASIC for the ATLAS TRT

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Abstract

The ATLAS TRT straw tracker will consist of more than 420K straw tubes filled with a Xenon based fast gas located in a magnetic field of 2T. Some tubes will operate at rates up to 15 MHz. Stringent signal processing goals include: the ability to detect energetic Transition Radiation photons as well as the earliest clusters from ionizing tracks without baseline shifts have been determined using both simulation tools and measurement standards set by hand tuned discrete component prototypes. High channel count and restrictions on cable plant led to the development of custom ASICs to house the detector mounted前端 electronics and digitized readout. The ASDBLR is a custom analog bipolar ASIC that provides the full signal processing chain from straw input to the output logic pulse.

A. Introduction

The straw-tube Transition Radiation Tracker (TRT) in the ATLAS detector at LHC [1] is being designed to operate at extremely high radiation levels. Some elements of the 425,000 straw tube detector are expected to operate at rates approaching 20MHz each straw has a cathode diameter of 4mm, anode wire diameter of 30µm and will be filled with a gas mixture of 70%Xe+20%CF4+10%CO2 and operated at a gain of ≈ 2 x 10^4. Xenon gas improves the efficiency for stopping TR photons, but lengthens the ion tail of the current pulse significantly compared to more conventional Argon based mixtures. In order to achieve the required 150µm track resolution, at high rates, the baseline will need to be stable so that the avalanche signal from the primary electrons can be accurately detected. Ionizing tracks will deposit an average of 2KeV resulting in a charge of approximately 20fC at the input to the amplifier during the 7.5ns peaking time. Due to the circular cathode geometry and the relatively low velocity of the primary ions there is significant variation in the signal shape and total charge. For high efficiency it is necessary to operate at thresholds of 2fC or 200eV equivalent energy loss. Signals of 20-50 times threshold will occur frequently making it important that the signal at the input to the comparator be adjusted to reliably return to baseline as soon as possible after the last of the drift electrons from a track have arrived at the wire. Radiation and breakdown issues place relatively strict requirements on the gas gain, making it necessary to employ low noise design techniques. Finally, the large number of detector mounted electronics channels make it important to keep the power dissipation as low as feasible.

B. ASDBLR ASIC BLOCKS

The eight channel ASDBLR wire chamber ASIC, currently in its third generation, has been developed to meet the tracking and particle identification objectives of the ATLAS TRT using inherently radiation tolerant analog bipolar processes.

A block diagram of the first version of the circuit is shown in Figure 1. A more detailed description of each block may be found in reference [2]. Good common mode rejection, both on and off chip is achieved by providing package leads to both 150MHz preamplifiers on each channel. All remaining stages are fully differential. The shaper provides ion tail cancellation for either Xenon or Argon based gas selected by an externally controlled logic level. Ion tail cancellation is designed to operate linearly over a 600fC range with a soft saturation characteristic so that lingering ion current from large depositions does not severely inhibit double pulse resolution. Ion tail cancellation is followed by a multi-pole shaping block to provide noise filtering without compromising double pulse resolution. The signal at the output of the shaper is limited to about 120fC of equivalent input charge, the largest allowable threshold setting. A baseline restorer BLR is included to eliminate effects of pileup, reduce sensitivity to mismatch in the ion tail compensation and decouple the DC offsets in the preamplifier and shaper from the comparator section.

A low and high level comparator on each channel allows the ASIC to trigger on the earliest arriving clusters from tracks for optimal position resolution and to detect energetic TR photons with high efficiency. The peaking time of the signal into the low level or tracking comparator is 7.5ns, chosen to optimize tradeoffs between signal to noise and tracking resolution. The high level, TR photon discriminator, has a longer, 10ns, peaking time to allow the prompt and reflected signal from the
terminated straw to be integrated. This reduces the amplitude dependence on the position of the charge deposition along the wire, increasing the threshold dead band between ionized track depositions and TR photons. The output of the two comparators is summed as a differential current that forms a ternary output level of 0, 200 or 400 µA. A more detailed description of each block may be found in reference [2].

C. Measurements

Measurement of the first version of the ASDBLR pointed to the need for an increased gain (40%) in the BLR and a reduced shaping time. This was due to the realized gain of the straw and fabricated amplifier, combined with a minimum signal size requirement in the BLR for low signal attenuation. Taking advantage of provisions made for metal layer revision, we were able to use wafers held at pre-metalization from the first run to fabricate parts with the revised design parameters. This revised design has been measured extensively and meets all basic design requirements.

High rate operation has been measured with Argon and Xenon based gas mixtures. Figure 2 shows a scope plot of the first high rate operation of the ASDBLR attached to a straw module. The upper trace in the scope plot shows the analog monitor of the BLR output and the lower trace shows the ternary comparator output from the same channel. The straw was irradiated by several Sr90 sources achieving an effective rate of 10MHz. No baseline shift was observed. The operation of the ternary output is demonstrated in the last time division where the a discriminator trigger of twice the standard amplitude signals detection of an input pulse above the low and the high threshold levels.

Test beam measurements (Summer 1998) were taken at the CERN HI8 beam line using a silicon-strip detector telescope sandwiched around a straw module to measure track position. Radioactive sources were added to study rate dependence. Track resolution and efficiency were measured at rates up to 20MHz using both the ASDBLR and a carefully tuned, DC coupled, single channel of discrete electronics. A comparison of the measurements is shown in Figure 3. With the gas gain set to its nominal value, the lowest operational threshold was 266eV. At this value, the ASDBLR offered slightly poorer track resolution than the hand tuned electronics channel. Raising the gain by 50% improved the performance to better than that of the hand tuned channel suggesting that a higher internal gain before the BLR might help improve track resolution.

As the size and complexity of high energy physics detectors has grown there has been an increasing reliance on simulation tools to predict the detailed performance of high rate detectors. In Figure 4 the predictions of a montecarlo tool developed specifically for the TRT that includes the effects of the baseline restorer overshoot are compared with data measured in the test beam using the fabricated ASDBLR.

D. ASDBLR in Rad Hard BiCMOS

Significant overhead in the power and connections between the analog front end and the digital time measurement chip could be eliminated by the use of a radiation hardened BiCMOS process. We are evaluating the risks and benefits of using a relatively new SOI process, DMILL.

1) Prototype Version

In June 1997 we submitted a prototype six channel ASDBLR with three channels of Xenon and three channels of Argon tail compensation in this process.

A key part of this submission was the implementation of a new baseline restorer circuit. In this design, the shaper output is capacitively coupled to the BLR as before, but the simple diode shunt across the coupling capacitors is replaced by a four diode bridge. The impedance between the outputs is regulated by a differential pair that controls the current in the bridge. When the signal is of the desired polarity, the current is
Figure 4: Triggering Efficiency for hits within $2\sigma$ of the reconstructed track (The raw hit efficiency at 0 MHz is 97%). Good agreement is shown between test beam data and a simulation tool that predicts tracking efficiency for straw tubes based on characteristics of the tube and shape of the ASIC signal at the on chip comparator input. This tool will be employed in Monte-Carlo predictions of detector performance.

Figure 5: The above traces show the Shaper and BLR response as calculated by HSPICE for a $2\text{fC} (200\text{eV}$ equivalent deposition) parameterized TRT pulse into an ASD with bridge type BLR.

the shunt BLR is demonstrated over a large part of the expected operational range. SPICE calculations of gain and maximum overshoot are plotted for each BLR type over a range of input charge from 200eV to 8Kev. The bridge BLR gain is nearly uniform down to the 200eV, threshold level, inputs. Fabricated parts demonstrated high yield and good uniformity, but also indicated that the process was not yet mature. The resistors measured 25% higher than nominal and we observed a tendency for harmonic oscillation. Nonetheless, the fabricated ASIC provided useful measurements for all aspects of operation.

Figure 6: Comparison of overshoot and gain of the bridge and shunt type Baseline Restorer as a function of input charge.
Figure 7: The figure above depicts the model used for SPICE calculations of the effects of charge coupled to the uncommitted substrate below the insulator layer for the ASDBLR preamplifier fabricated in the DMILL SOI process. An important element is the capacitor between the emitters of the differential pair. A pulse applied to the unused preamp input generates a signal on the top side of the capacitor and does not produce additional harmonics in the output. A pulse applied to the active input does.

Figure 8: The upper trace is the recorded signal from a pulser designed to mimic the shape of point ionizations in a TRT straw filled with a Xenon based fast gas. As can be seen in the plot, there is still appreciable current flowing 180ns after the pulse. The response of the prototype DMILL ASDBLR after tail cancellation is shown in the lower trace. Considering the fact that the process resistors were 25% above their nominal value, the circuit for shortening the ion tail appears to be quite robust.

back substrate and carries the amplified signal from the active input. The other side faces away from the substrate and carries the amplified signal from the unused input. In the DMILL SOI process, the relatively low resistance back substrate can not be directly contacted through the 450nm insulator layer and is floating. We found that the harmonics observed in the prototype are consistent with capacitive coupling from the tail cancellation circuit to the inputs through the back substrate (see Figure 7). Pulser studies showed that when the hook up capacitance at the inputs is unbalanced, as will be the case when attaching to a TRT straw, harmonics are observed at the analog monitor output when a signal is applied to the active input, but not when an inverted polarity input is applied to the unused input.

The left plot in Figure 9 shows two measurements taken with a digital oscilloscope. In the upper trace, a positive pulse is injected into the unused input and in the lower trace a negative signal was injected into the active input. Similar behavior is demonstrated in the plot on the right side of Figure 9 using the simple SPICE model shown in Figure 7. The external capacitance at the inputs is unbalanced (5pF and 17pF) and a 100fF capacitance couples each input to the uncommitted substrate node. One plate of the tail cancellation capacitor couples to the back substrate with 300fF.

2) Engineering Version

We recently submitted an extensively revised and optimized version of the ASDBLR in the DMILL process that should meet or exceed the signal processing goals of the TRT readout. Each channel has approximately six hundred hand sized and placed components. SPICE based performance calculations were aided by the use of substantially more sophisticated models of the DMILL process revised to include the predictable parasitic
The signal at the shaper monitor point of the DMILL ASDBLR exhibits an input and load-dependent harmonic pickup. In the upper trace a positive pulse is injected into the unused input, in the lower trace a negative pulse (straw polarity) is injected into the active input.

Right Figure: The results of a SPICE calculation with 100fF feedback from a global substrate node to the inputs. The plots show the calculated response at the shaper output with a positive signal into the unused input in the top plot and a negative signal into the active input in the lower plot.

The capacitive load on the unused input is much lower than on the active input in all cases above.

capacitance to the back substrate. The calculated power dissipation is 36mW/channel and the RMS equivalent input noise is 200e. Several changes to the prototype design were employed to reduce the susceptibility to pickup from the back substrate. These include: 1) the installation of a grounded guard ring around input devices, 2) connection of unused silicon on the top side of the insulator to a fixed potential 3) the addition of a low gain differential stage to symmetrize the preamp signal before tail cancellation, 4) splitting of the tail cancellation capacitor into two half size capacitors cross coupled, 5) the use of two terminal pad structures that provide contact to a conductive buried layer just above the insulator to shield the signal on the pad from the substrate below the insulator. Important features of this submission are:

• Dual inputs with negative Input Protection using NPN transistors for fast response.

• Bridge type baseline restorer

• Two level discrimination: Low level 7.5ns peaking time, 0-10fC range. High Level 10ns peaking time, 15-20fC range.

• Programmable current ternary output 0 - 3mA steps (200uA design)

• Analog monitor of the input and output to the baseline restorer on channel 1 and 8.

This chip was designed for use with a partner chip, the DTmROC, which will decode the ASDBLR ternary output, register the time of leading and trailing edges of low level triggers as well as indicate the presence of a high level trigger (suggesting the presence of a TR photon).

I. REFERENCES
Abstract

The continuous increase in volume of silicon trackers in the coming experiments poses a number of new issues to unravel. Among them, the high number of detector readout modules to be built in a relatively quick time will require the use of preselected ASICs. In the particular case of the ATLAS SCT, where about 6 million channels have to be read out with little chance for replacement of the electronics, that becomes a considerable challenge. Specific architecture features of the front-end chips will call for very specific and dedicated electronic testers to provide a full and efficient characterization. This paper describes the system built for the preselection and characterization of the ABCD front-end chip to be used in the readout of the ATLAS SCT microstrip silicon sensors. The system has been used successfully during the last year to tag the 6000 ABCD chips that have been built up to now and has been upgraded to cope with the new features of the last version of the chip.

1. THE ABCD CHIP.

The Atlas Binary Chip DMILL (ABCD [3]) design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker [1]. The Radiation Hard DMILL technology [2], in which the ABCD chip is fabricated, offers the unique possibility of combining a bipolar front-end amplifier/comparator with the CMOS logic in a single chip.

A major issue in the binary architecture implemented in the ABCD chip is the matching between the channels. Two versions of the chip, presenting different solutions of this problem, are currently under development. The ABCD2T version has a gain of 80 mV/fC and a 4-bit DAC for the threshold correction implemented in each channel, together with a common threshold, controlled by a 8-bit DAC, for all the channels, allowing to tune the matching between them. The second version, the ABCD2NT chip, with only the common threshold for its 128 channels, has twice higher gain before the comparator and a layout optimized for better matching.

The block diagram of the chip is shown in Fig. 1. The preamplifier–shaper circuit provides signals with a peaking time of 25 ns, sufficient to keep the time walk of the discriminator in the range of 12 ns and a double peak resolution of 50 ns. This circuit is followed by a comparator whose threshold is applied channel by channel as explained above. The binary data from the discriminator are latched in the input register in either level or edge sensing mode –with a time resolution of 25 ns– and clocked into a 132-cell deep pipeline. For each trigger, the data are transferred from the pipeline to the second level buffer, 128 bits wide and 24 locations deep, that serves as a derandomizing buffer which removes the fluctuations from the L1 trigger distribution. It will store three bits of data per channel, corresponding to the three beam crossings centered on the L1 trigger time, and are set if the input was above threshold during the corresponding crossings. The data compression logic will take these data and suppress the empty channels making the chip output only the hits which match the pattern programmed in the configuration register. The readout logic will be responsible for the capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives and on its arrival it outputs the data of the chip. If the chip is in the middle of the chain, sends a token to the next chip. If the chip is configured in send–id mode, it will output the contents of the configuration register instead of the data from the channels.

Fig. 1. Block diagram of the ABCD chip.

In addition to the basic functional blocks described above, the ABCD comprises a calibration circuitry for internal generation of calibration pulses whose amplitude is set by a 8–bit DAC and their delay relative to the clock phase is controlled by a delay buffer of 6–bit resolution.

2. THE SETUP

The setup, as sketched in Fig. 2, is based on a Karl SUSS PA200–II probe station with a fully motorized chuck stage whose movement is controlled through the
GPIB interface. The functions implemented in the ABCD chip for internal testability, like internal calibration circuitry or pulsing input register function, allowed to build a simple and robust system where all the communication to the chip is done via digital serial interface. Since the goal is to test the chip with a high frequency clock -up to 50 Mhz-, all signals delivered to and received from the chip had to be buffered on the PCB close to the needles. To this end, a custom designed probe card (PCB) has been made with standard technology and 64 needles with the standard pitch of 200 µm.

![Schematic diagram of the wafer test system.](image)

The chip control and data acquisition is based on two VME modules: a sequencer (SEQSI [4]) which provides the clock and control signals to the chip, and a data receiver and decoder (DRAFT [5]).

For measurements of the characteristics of the digital–to–analogue converters on the chip, a HP voltmeter with an analogue multiplexer is used, and it is connected to the system through the GPIB bus. The same device is used to control the vacuum to fix the wafer onto the prober chuck. A Tektronics power supply is used to provide the chip with the digital and analogue bias and also to measure the power consumption of those lines.

All the system is controlled by a dedicated program written in C++ and running in a PC under Windows 95. The program controls the VME and the GPIB buses. It programs the sequencer to set the phase between the clock and the command line of the chip, builds the commands to carry out the tests and reads out the DRAFT. On the GPIB side, it controls all the movements of the wafer prober, sets up the voltmeters and power supplies and reads from them all the data. Probe movements are programmed very cautiously and all the system stops whenever any disagreement is found between programmed and monitored coordinates or the vacuum fails. Concerning the tests, it allows to independently select and configure any of them to be done and also takes care of the data acquisition and storage using standard packages to compress the data in order to save as much space as possible. In total, the system takes between 300 and 200 seconds to perform the complete set of tests in a chip, depending on whether the chip is a trim dac version or not.

On a second stage, the data collected by the acquisition program is analyzed using a separate software in order to effectively classify the chips. It also produces a sort of data summary file and provides the information needed to feed a chip database to help in the control of chip quality and distribution.

3. TEST PROCEDURE.

The ABCD chips will be assembled on the hybrids as unpacked devices and, in consequence, the chip preselection and characterization process has to be carried out at the level of wafer screening. The characterization process needs to be complete, accurate and as fast as possible since about 50000 chips need to be preselected. Inasmuch as the ABCD chip follows the binary architecture, a considerable amount of measurements are needed to obtain any information on the analogue performance of the front–end. Also a complete set of digital tests proving the readout protocol, different modes of operation and functionality of the whole logic, together with the characterization of the on–chip digital to analogue converters (DAC), need to be designed and carried out.

3.1. Digital tests.

A number of tests are made to check all the digital functionalities of the chip. The main characteristics to peruse are related to chip control, inter–chip communication and data compression. Additionally, some functionalities like channel masking and redundancy mechanisms should be proven. All the tests make an extensive use of some of the testing tools provided by the chip, like pulsing the input register or generating output patterns through the mask register. To evaluate the performance of the chip in the different tests, four different patterns with a length of 128 bits are usually injected:

- a sequence of 128 ones,
- a sequence of 010101...01,
- a sequence of 101010...10 and
- a sequence with 30% of the channels set to one randomly.

In order to evaluate the performance of the chip under the different tests, a fixed number of events were triggered for each of the patterns and the resulting efficiency studied.

Another key issue concerning the performance of the digital part is to determine the maximum speed of the selected chips. Since the maximum frequency clock attainable in the setup -50 Mhz- is lower than the maximum speed of the ABCD chip for nominal bias conditions1, the chip performance degradation was

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1 Results from IMS tester performed on diced chips show functionality up to 70 Mhz.
simulated by lowering the power supply. For that reason, all the tests were repeated for two different clock frequencies—nominal 40 MHz and 50 MHz—and for several values of the digital power supply (Vdd): from 3.3 V up to 4.2 V. The minimum Vdd for which a chip still shows full efficiency at 50 MHz was used to classify them according to their speed performance and in the yield calculation. This is shown in Fig. 3. The histogram has as X–Y coordinates the cells in the wafer and on the Z axis how far from the nominal Vdd −4 V− the chip still shows full functionality at 50 MHz.

The next paragraphs describe the digital tests performed:

- **Configuration register input/output:**
  This is one of the most determinant tests because it proves that the chip can be configured. The configuration register is written with random values, keeping the chip always as master and end chip. The values are then compared with the data returned by the chip in the send identification mode. Since addressing is not meant to be test here, the universal address is used.

- **Addressing:**
  The ABCD is supposed to be mounted in a module populated with 12 chips. In order to configure each of the ABCDs independently an addressing mechanism has been implemented which is tested here. The chip is given a random address and it is configured using that address. The value is compared with the one returned in the chip data. An extra test is done at this level: The L1 counter is followed and its value stored. It should start at 0 and increase in steps of 1.

- **Input Register:**
  To check the functionality of the mask register, the four patterns are loaded in the mask register and the input register is pulsed. Pulsing the input register sets to one the 128 channels. At the output, only the channels allowed in the mask register should be at one.

- **Input Lines:**
  The functionality of both input lines for the chip clock and commands is tested by injecting the four patterns through the mask register and sending the clock and the commands through both lines. The output is contrasted with the patterns.

- **Fake slave:**
  The chip is set as master and middle chip. In the first part of the test the token transmission through both lines is checked. In a second stage, a sequence simulating the data of a slave chip is injected through both input lines of the chip and contrasted with its output. The chip is also provided with a pattern programed in the mask register in order to check that it merges properly its data with that of the slave.

- **Slave:**
  The chip is set as slave and end chip. The four patterns are injected through the mask register and the token sent, after each trigger, through both input lines. The chip output is also searched on those lines.

![Fig. 3. Wafer map of the maximum distance in volts down the nominal Vdd −4 V− at which the chips, operated at 50 Mhz, still show full digital functionality. The X–Y plane represents the cells in the wafer.](image)

### 3.2 Power Consumption.

The setup measures the power consumption both of the digital part and the analogue part. To simulate the nominal requirements for the ATLAS SCT occupancy and L1 trigger rate, the measurement was done applying a 100 kHz trigger with an occupancy of 3% of the channels selected randomly. Fig. 5 shows the average values obtained for all the chips passing the digital tests in one of the wafers. Although the distributions are quite narrow, still some chips are far away from the peak. Those chips, with such a high power consumption, are rejected during the selection process due to possible weaknesses of some parts of the digital logic.

![Fig. 4. Current measured for the digital (upper plot) and analog (lower plot) voltages of the chip.](image)
3.3 Digital to Analogue Converters.

The ABCD has 3 main DACs whose performance have to be carefully tested:
- Threshold DAC (8 bits),
- input transistor current DAC (5 bit) and
- shaper current DAC (5 bit)

The chip incorporates one additional 8 bit DAC for the calibration pulse height which is not directly tested and its failure will translate in a deficient analogue performance. The trim dac version of the chip incorporates an additional DAC per channel to individually trim the value of the threshold. The test performed on this DAC are described in 3.4.1.

In order to prove the behavior of the three DACs, a full scan on the DAC bits is done and the DC levels provided by the chip in its test pads are read with the HP voltmeter. This will allow to measure their linearity, as shown in Fig. 5, where the relative deviation from linearity relative to the range of the DAC. Its scale is shown on the right axis.

3.4 Analogue performance.

The goal of these tests is to determine the basic analogue parameters of the front-end: gain, noise and discriminator offset spread. To this end, a threshold scan for three different input charges is done for each channel in every chip, as described in [6]. The input transistor current and the shaper bias are set to the nominal values and the chip is driven by a 40 Mhz clock. Three s-curve per channel are fitted to a complementary error function. From the 50% points the gain curve is built and fitted to a straight line. The gain and the offset are taken as the slope and the offset, respectively, of the linear fit. The electronic noise information is also obtained, for each pulse, from the s-curve fit.

Fig. 6 shows the distributions of the gain and noise of all the no trim dac chips in a wafer.

4. YIELD CALCULATION.

To calculate the yield, a selection criteria has been defined based on the results on the digital and analogue tests, together with the power consumption measurement and the DAC studies. Results from the analogue tests are correlated with the digital tests done at different clock frequencies and Vdd. At any of those points a chip will be considered as non-functional whenever a single failure is found in any digital test, the power consumption both in the analogue and the digital parts exceeds 20% the mean value from the wafer, the DAC non linearity is out of range or it has one or more dead channels. A channel is said to be dead when it does not respond to the calibration pulse –or its efficiency is smaller than 95%–, its gain is 20% lower than the mean value of the wafer or the noise is higher than 1500 e^-ENC.
Concerning the DAC linearity, although there is no strong constrain from the specifications, a selection criteria has been defined so that chips will be rejected whenever the spread of the non linearity distribution exceeds 1% in the threshold DAC and 10% in the bias DACs.

![Fig. 7. The lines labeled as Digital show the yield of the digital part of the chip obtained under different test conditions. The line labeled as no dead, shows the final yield after applying the criteria of the analogue tests, power consumption and DAC linearity. Also the yield values obtained when relaxing the requirement on the number of dead channels allowed in the chip are shown.](image)

Fig. 7 shows the digital yield for different digital biases and clock frequencies. The final value of the yield after applying the restrictions on the analogue performance, power consumption and DACs tests is also shown. Typical values of about 30% have been obtained from the wafers of the last process if no dead channels is allowed in any of the chips.

As for the analogue performance, a quality factor is defined as the ratio between the gain and the matching, defined as the spread of the 50% points. This factor is not directly used in the yield calculation although it is widely used during the selection of the chips. The distribution of the quality factor is shown in Fig. 8 for both versions of the chip. For the trim dac version, the quality factor is computed without trimming the channels. On diced chips, and after trimming, a quality factor of 20 has also been obtained.

![Fig. 8. Quality factor distribution for all the chips in a wafer.](image)

5. CONCLUDING REMARKS

A system has been built which is able to test all the functionalities of the ABCD chip on the wafer. It has proven to perform fast and accurately, providing all the information needed to tag the chips and build a general database for control and distribution of the chips. The system has been successfully used to test all the ABCD wafers supplied up to now and has been upgraded to cope with the new features of the last versions of the chip.

REFERENCES

Abstract

Recent developments of the Silicon Drift Detector (~SDD~) readout system for the ALICE experiment are presented. The foreseen readout scheme is based on 2 main units. The first unit consists of a low noise preamplifier, an analog memory which continuously samples the amplifier output, an A/D converter and a digital memory. When the trigger signal validates the analog data, the ADCs convert the samples into a digital form and store them into the digital memory. The second unit performs the zero suppression/data compression operations. In this paper the status of the design is presented, together with the test results of the A/D converter, the multi–event buffer and the compression unit prototype.
1. INTRODUCTION

The Silicon Drift Detectors are expected to provide high detection efficiency over the whole detector surface, a spatial precision of the order of 30 μm, a two-track separation down to O(600) μm. In addition the detector should provide a charge resolution such that the dE/dx resolution is dominated by Landau fluctuation, from which the truncated mean of the four ITS dE/dx samples is around 10% for M.I.P.

A M.I.P. releases about 4 fC in the SDD. For hits far from the anode pads the charge collected by one is typically one-third to one-half of the 4 fC; thus the tails of the hit signal, essential for the position determination, will consist of less than 1 fC. The range of useful signals is limited between the noise level (250 e⁻) and 28−32 fC, but higher signals (up to 160 fC) are possible.

The charge generated by a particle crossing the detector, depending on the crossing point and therefore on the drift time, can be collected by one anode as a fast gaussian signal ($\sigma = 5$ ns) or by several anodes (up to five) as a slower gaussian signal ($\sigma = 30$ ns), due to the diffusion during the charge drift through the detector.

In order to obtain the required precision the signal has to be sampled at quite high frequency (around 40 MHz); the dynamic range is 10 bits while an 8 bit resolution is sufficient if a non linear readout is adopted.

Due to the high sensitivity of the SDD to temperature variations and the very stringent requirement on the material budget which does not allow a very massive cooling system, the allowed power consumption for the electronic readout is very low (below 5 mW/channel).

2. SYSTEM ARCHITECTURE

In order to minimize the power consumption, the signals coming from the detector are not immediately digitized after the low noise preamplifier. Instead, they are continuously stored into an analog memory; only when the trigger signal is received the memory content is frozen and the data are converted and sent to a digital event buffer. In this way the most power demanding components work for a reduced percentage of the time (below 10%) greatly reducing the power consumption. After a local digital storage, which de–randomizes data for a lower transmission speed, the data have to be transferred to the acquisition system. Since the amount of data is very large (around 32.5 MBytes/event) and more than 95% of these data are zero, a data reduction is performed. In order to minimize information losses an Huffman encoder has been used, togheter with tunable filter functions which allow to reach the required compression factor in the presence of noise.

Figure 1 shows the full readout architecture.

3. THE FRONT END READOUT SYSTEM

In the Inner Tracking System of the ALICE experiment the SDDs are placed on linear support structures called ladders. The front–end modules are placed on the ladders, near the detectors, and are based on two functional modules, named PASCAL and AMBRA architectures.

3.1 The PASCAL architecture

The PASCAL architecture performs the low noise preamplification, analog storage and A/D conversion. A fully CMOS, low noise transimpedance amplifier continuously write the SDD signals into a switched capacitor analog memory at 40 MHz. When the trigger signal is received, the memory cells contents are converted in digital through a charge redistribution successive approximation A/D converter.

Current prototypes of the PASCAL architecture are designed as separate ASICs in standard technologies.
(0.7–0.8 μm); the A/D prototype fulfils the specifications while the preamplifier, which has been successfully tested in beam tests, has to be improved in term of dynamic range. Promising results has been obtained also with the analog memory.

The final goal is to design the full architecture as a single chip using the new deep submicron technologies (0.25–0.35 μm).

3.2 The AMBRA architecture

In order to decrease the number of transmission wires from the detectors to the end ladder to a manageable number an event buffer strategy has been adopted. The events are temporarily stored in local digital buffers near the detectors; in this way the analog memory can restart the write mode faster thus reducing the dead time. It has been shown [1] that with only two event buffer the dead time due to event buffer overflow is around 0.1%.

The current prototype of the AMBRA architecture is a single ASIC designed in 0.35 μm technology.

3.3 Front-end prototype results

The non linear preamplifier prototype. In order to study the feasibility of a signal compression at the preamplifier level, a prototype of a non linear transimpedance amplifier has been developed and tested [4].

The chip was designed to meet the following requirements:

- Maximum input signal: 32 fC
- Equivalent input noise charge: <500 e−
- Total input current noise: <2 nA r.m.s.
- Power consumption: <1 mW.

The developed prototype is a two stage system in which a non linear transimpedance amplifier is followed by a voltage differential amplifier.

The non linear input–output relationship is obtained using a MOS device as the feedback element around a cascode stage, as proposed in [7].

This architecture has two interesting features:

- It implements in a very small area a second order small signal transfer function already at the preamplifier level
- The non linear large signal behaviour relies on the I–V characteristics of a MOS device, which is mathematically very well modeled.

In the present design, the properties of the feedback branch have been adjusted so that the equivalent small signal gain is of the order of 500 kΩ.

This value has been chosen as a trade–off between noise, speed and power consumption. The peaking time of the preamplifier is 25 ns.

A voltage differential amplifier has been used as second stage, in order to have a total gain of 2 MΩ when the output is read–out in a single ended configuration and 4 MΩ when the output is read–out in a differential manner. Since the aim was to study the basic properties of the non linear signal processing performed by the preamplifier, the second stage has a wide bandwidth in order to avoid any additional shaping.

The amplifier has been designed to work with power supply down to 3.3 V and a power consumption (excluding the output drivers) of 0.6 mW.

The lab measurements show the amplifier is within the specification for both power consumption and noise. In fact, the measured power consumption is 0.66 mW with a 3.3 V power supply and the noise is less than 2 nA r.m.s, which is an upper limit dictated by the experimental setup.

The large signal transfer function was fitted with a parabola \( y=ax^2 + bx + c \), where \( y \) is the input current and \( x \) is the output voltage). The result are summarized in figure 2 and 3.

![Figure 2](image1.png)

![Figure 3](image2.png)

From these plots, it can be seen that the parabola is a very good approximation for input current up to 700 nA, which in the case of ALICE SDD corresponds to a maximum input charge of about 20 fC.
For higher input signal the input–output relationship is best fitted by a third order curve. This is due to a distortion in the voltage amplifier.

In the beam test conditions, only minimum ionizing particles were present (pions of momentum of 375 GeV/c). This means that with the beam test data, the lower region of the dynamic range could be studied. Drift detector equipped with this prototype preamplifier was successfully tested with particles.

The A/D converter prototypes. The analog to digital converter foreseen in the front–end module has to perform a complete conversion in 500 ns, with a average power consumption of 1 mW/anode. Since the A/D is used for less than 10% of the time, the the power consumption during conversion should be less than 10 mW/anode. When moderate speed and low power are required, successive approximation converters based on charge redistribution DACs are a very attractive approach, because with this technique resolution of 8–10 bits can be implemented in a silicon area small enough for multi–channel integration.

In a charge redistribution converter, an array of binary weighted capacitors is used to generate fractions of a reference voltage, $V_{\text{ref}}$, which are compared with the input voltage to be converted.

A prototype chip has been developed in order to meet the following goals:

- Identify an architecture that can satisfy the SDD requirements in term of power budget, speed and resolution.
- Study the problems arising from the parallel operation on the same chip of several ADCs (cross talk, loading on the reference voltage, etc.)
- Test the digital circuitry which controls the operation of the converters

The prototype chip containing sixteen A/D converters of the charge redistribution type has been fabricated in a 0.7 µm commercial CMOS technology. The architecture of the converters is the same that was used in the CRIAD ADC [8] and consists of a 8 bit DAC and a very sensitive offset compensated comparator.

The chip also contains a digital buffer and multiplexer and a digital control unit.

In figure 5 the FFT test shows a THD (Total Harmonic Distortion) below 55 dB, while the histogram tests gives a DNL (Differential Non–Linearity) between $-0.4/+0.4$ LSBs and no missing codes, and a INL (Integral Non–Linearity) between $-0.2/+0.5$ LSBs.

DNL and INL are shown in figure 4. FFT, DNL and INL has been measured on a 1 $V_{pp}$ sinewave at 5.5 kHz. For FFT 4075 samples has been used while DNL and INL are calculated with 20375 samples.

The AMBRA_01 chip. The first version of the AMBRA chip has been designed and sent to the foundry. Table 1 summarize its characteristics.

The AMBRA_01 is designed for an 8 bit ADC but it can be easily redesigned for 10 bit with some area penalty.
The main sources of power consumption are the event memories and the output buffers. Table 1 reports the power consumption of the circuit during operations, while the idle consumption is negligible; therefore the average power consumption is much less. The memory buffer peak consumption of 2.15 mW/channel decreases to an average of less than 0.2 mW/channel, since the memories are used less than 10% of the time and the output drivers consumption of 1.9 mW/channel decreases to a negligible 32 µW/channel since the output buffers are used only around 1.6% of the time.

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</table>

Table 1

The main sources of power consumption are the event memories and the output buffers. Table 1 reports the power consumption of the circuit during operations, while the idle consumption is negligible; therefore the average power consumption is much less. The memory buffer peak consumption of 2.15 mW/channel decreases to an average of less than 0.2 mW/channel, since the memories are used less than 10% of the time and the output drivers consumption of 1.9 mW/channel decreases to a negligible 32 µW/channel since the output buffers are used only around 1.6% of the time.

4. THE END LADDER READOUT UNIT

The end ladder modules are placed at both ends of the ladders, and contains the compression circuit, the optical interface to the data acquisition system and the control system.

The most important functional module is the CARLOS architecture. Its purpose is to compress the signals coming from the front−end readout units to a size compatible with the requirements by the ALICE data acquisition system.

4.1 Data compression

The amount of data generated by the SDDs is 32.5 MBytes/event. Most of these data are zeroes, therefore a data compression is required in order to save space on tape. Since a simple zero suppression leads to an unacceptable information loss, several compression algorithms have been studied:

- Zero sequence encoding : sequences of zeroes are transmitted as a zero code followed by the number of consecutive zeroes. Since the occupancy is quite low, long zero sequences are highly probable.
- Simple threshold zero suppression : the data below a certain threshold, which takes into account noise and pedestal, are set to zero. This technique is very easy to implement and increases the number of zeroes by cutting non zero values due to the noise. Unfortunately this results in information loss.
- Differential encoding : instead of the samples, the difference between consecutive samples is transmitted. In this way any channel baseline value is translated into a zero sequence. On the other hand a differential encoding scheme is more sensitive on sample errors during transmission.
- Simple threshold tolerance : it is a simple threshold zero suppression applied after the differential encoding. It reduces the noise variations over a baseline, at the expense of information loss.
- Huffman encoding : since the probability of lower codes is much higher than the higher ones, using a variable length encoding leads to a lossless data reduction. This reduction depends on the sample statistics; the implementations is quite heavy in terms of hardware requirements.
- Multithreshold zero suppression : a sample is set to zero depending on its value and on the value of neighbour samples. In this way the information loss can be greatly reduced with respect to single threshold zero suppression.

An FPGA−based prototype of the first 5 algorithms, with software tunable parameters, has been realized and is currently under test with the data taken from the ALICE SDD beam tests [5]. The sixth algorithm is currently under evaluation. A detailed description of this algorithm can be found in [6].

5. REFERENCES

[5] V. Bonvincini et al., ALICE/98−24 Int. note/SIL
[8] F. Anghinolfi et al., CERN SITP Note TR 101, Dec 1993
**Very Low Mass Microcables for the ALICE Silicon Strip Detector**

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**Abstract**

The ALICE Inner Tracker silicon strip detector layers will use kapton/aluminium microcables (12/14 μm thickness) exclusively for all interconnections to and from the front-end chips and hybrids, completely eliminating traditional wirebonding. Benefits are increased robustness and an extra degree of dimensional freedom. Utilising a low-power, low temperature and low-force (10-15 grams) single-point TAB bonding process, aluminium traces are directly bonded through bonding windows in the kapton foil to bond pads on the chip, detector and hybrid. The same technique is also used to interconnect these microcables to create multi-layer bus structures with "bonded via’s".  

Working in close collaboration, the SRTIIM Kharkov and NIKHEF UTRECHT groups are involved in the design, production and testing of these cables, as well as research of positioning and assembly methods. A double-sided detector using prototype cables has been installed in the NA57 experiment in 1998.

1. **Introduction**

The ALICE Inner Tracker (ITS) [1] consists of six concentric layers of detectors. Layer 1 and 2 are equipped with pixel detectors, layers 3 and 4 with silicon drift detectors and layers 5 and 6 with silicon strip detectors. Layer 5 has a radius of 390 mm. and consists of 34 ladders with 23 modules each, layer 6 (radius 435 mm.) has 38 ladders with 26 modules.  

The Silicon Strip Detector (SSD) system consists of 1770 modules, 782 in layer 5 and 988 in layer 6. A front-end module consists of a double-sided (stereo) strip detector with 1536 strips and a double-sided hybrid on which the 12 (2x6) ALICE128C readout chips [1],[2] are mounted. The total number of channels is approximately 2.5 million.  

Layer 5 ladders are 990 mm long, layer 6 ladders 1100 mm long, the ladders are carbon-fibre space-frame constructions and are connected to carbon-fibre end cones to form cylindrical shapes.  

A freon cooling system consisting of two stainless steel tubes running along each ladder cools the hybrids. These tubes have diameter of 2 mm and the wall thickness is 40 μm.  

On the ladders detectors are mounted in “high” and “low” overlapping positions to eliminate the dead areas of the detectors in the Z direction (parallel to the beam). Alternate ladders are also mounted in “high” and “low” overlap positions on the circumference to eliminate these area’s in the R direction.  

Heavy-ion physics with particle multiplicities up to 8000 dictate a very low-mass design.

2. **Microcable Technology**

The microcable technology described here was originally developed by the SRTIIM as a low-mass interconnect system for use in space electronics, with microcables with minimum pitch of 150-200 μm and bus assemblies with up to 10 layers.  

For use in detector systems, the technology has been scaled down to a pitch of 88 μm with typical trace widths of 35-40 μm.  

A microcable is made up of a kapton (polyimide) foil with aluminium traces. The cables are available in 12 μm kapton with 14 μm aluminium or 20 μm kapton with 30 μm aluminium.  

Bonding windows are etched in the kapton foil, so as to be able to press the traces through these windows and bond them directly to the bonding pads beneath.  

The technique is similar to Tape Automated Bonding (TAB), but with several important differences. In TAB bonding, traditionally gold bumps are used on the pads and all connections are gang bonded in one go with a thermode using heat and force.  

A more recent development by Bull and Dassault, supported by the European Community ESPRIT program is bumpless single-point TAB bonding.
The kapton foils used are much thicker, typically 70 μm thick and traces are 17.5 μm copper covered with 1-1.5 μm gold. Bond force is typically 20 grams for TAB bonding, compared to 10-15 grams for the microcables. TAB bonding is an industrial high-volume process which utilizes a kapton foil with sprocket holes for fast and accurate positioning and handling, it is uncertain if it will be possible to use such a system for microcables which have much thinner foils and traces and so are much more fragile.

Also, automatic bonding machines often do not react kindly to trying to use bond forces of around 10 grams! The TAB direct bonding technique is being investigated by the Strasbourg and Nantes groups and is used in the STAR silicon strip detector [3]. Also the possibilities to modify this industrial process using aluminium instead of copper is under investigation.

In this paper we describe solely the Utrecht/Kharkov aluminium microcables designs.

3. INPUT CABLES

A front-end module, see Fig.1, consists of a double-sided strip detector and a double-sided hybrid on which the 12 (2x6) 128 channel readout chips are mounted. The detector and the hybrid are decoupled mechanically, the detector is mounted on the ladder with high accuracy while the hybrid is connected to the cooling pipes running along the ladder. These pipes are loosely coupled to the ladder structure except for one fixed point in the middle to accommodate differences in thermal expansion. The hybrids are mounted in a different plane than the detector, so the connection between the chips and the detector must be made with flexible microcables, at the same time eliminating the need for fan-outs, as this can be done in the cables.

The input cables, shown in Fig. 2, are made of 12 μm thick kapton foil with 14 μm thick aluminium traces, width 40 μm and 88 μm pitch on the chip side and 95 μm on the detector side. The traces are directly bonded to the bonding pads through bonding windows in the kapton foil with specially designed bonding wedges. The kapton foil is glued to the silicon surface to increase the mechanical strength. As the chip input pitch of 44 μm is too small for the cable design, half the traces run straight from the first row of bondpads and the other half folds around to connect to the fourth row. The cable also includes the output connections of the chip to the hybrid, this side of the pattern has a fan-out which fits in a 22 pin ZIF connector. In this way it is possible to test bonded chips before mounting them on the hybrid.

After testing of the chip, the test fan-out is removed, leaving only the pattern to be bonded to the hybrid.

4. HYBRID BUS CABLE AND LADDER CABLE

The double-sided hybrid is 0.3x10.5x68 mm, just big enough to fit 12 chips and associated SMT components and the two cooling clips connecting the hybrid to the cooling pipes. On one side of the hybrid the front-end chips of the P-side are placed, on the other side the chips of the N-side.

To save material the read-out and power bus connecting the chips and components consists of a multi-layer microcable. This part does not have to be supported by the hybrid, allowing reduction of the hybrid to the minimum size needed to support and cool the chips. Fig. 3 shows a prototype of the hybrid and bus cable assembly including chips with input cables. The via’s in this cable are made by bonding traces in different layers directly to each other through bonding windows in both cable layers. The layers are glued together after the bonding process. Here the kapton foil is 20 μm thick and the aluminium 30 μm and trace widths range from 70 μm to 2 mm.

Only the part of the cable containing the bondpads for connecting the chips and the solder/glue pads for the SMT components is glued to the hybrid, the rest of the bus is floating free in the air. The bus has a short “umbilical string” on one side which is bonded to the ladder cable. This is a similar cable of variable length (depending on module position) which runs along the ladder to the endcap module at the end of the ladder. This cable end is bonded to a very small PC-board, which has a trace pattern that fits into a ZIF connector, so again a completed front-end assembly can be tested before mounting it on the ladder. To make assembly easier, the ZIF connector system is also used to connect the ladder cable to the end-cap electronics.
5. TEST RESULTS

5.1 Introduction

Bond tests and bond pull strength tests have been done and are still ongoing. Also research has been and is still done on several subjects: glue pull strength for the input cables, tests using different bond wedge foot profiles, bonding and assembly methods and jigs to accomplish them.

This is necessary, as there is little or no industrial know-how concerning this kind of cables. Bonding these cables looks deceptively easy compared to traditional wire bonding, but one has to realize that to make a reliable bond connection, now not only the workpiece (chip, detector, hybrid) has to be held stable in position, but the microcable template as well. The cable must be held absolutely flat and tension-free against the surface to be bonded to get reliable, consistent results.

Also visual inspection of the bonds is not easy, it is difficult to discern any difference between a successful bonding and a total failure!

5.2 Results

For a typical input cable the pull strength of the aluminium trace with 40 μm width has been measured, a consistent value of 6 grams was found.

Also for the input cable, the glue strength of a narrow glue strip (200-300 μm) was determined, values of 40-60 grams were found. The glue pull strength is much larger than the total weight of a single module, about 7 grams, so that it can effectively protect the aluminium traces during handling of the module.

In Fig. 4 bond pull strength figures as a function of bonding energy for four different bonding wedge foot profiles are shown. The results are quite good, there is a sufficiently wide energy range in which acceptable bonds are realized. In nearly all cases the trace is pulled off the pad leaving a patch of aluminium behind, see Fig. 5, it does not tear off in the “heel” of the bonding.
widths vary from 100 µm to several mm for power lines, in the case of power lines several bondings are made in parallel, the trace width in the bonding window area is always 100 µm wide. Bond pull strength of these bondings is 18-20 grams.

6. CONCLUSIONS

The use of microcables gives the designers of front-end modules and inner tracker structures more possibilities; 3D freedom, longer interconnections, some relative movement allowed, robust and yet low mass. Bonding on active surfaces is inherently safer compared to wire bonding, no lost wire bonding possible and low settings of bonding parameters. Component qualification can be taken one step further, it is possible to do chip acceptance tests with bonded chips. The SRTIIM institute and production facilities in Kharkov have much experience with large-scale use of this technology using minimum pitch 150-200 µm.

One should keep in mind that this is a new technology for this field, that there is –especially for small pitch cables– not yet very much experience. Also there is no industrial production know-how in industry here yet, although at the moment two firms (Selmic, Detexis) seem interested. But we are convinced that without these microcables it would not be possible to assemble the inner tracker layers and get anywhere near the present specs concerning mass and coverage of active area.

7. REFERENCES

TAB BONDED SSD MODULE FOR THE STAR AND ALICE TRACKERS

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Abstract

A novel compact detector module has been produced by the “IReS”-“Subatech”-“Thomson-CSF-Detexis” collaboration. It includes a Double-Sided (DS) Silicon Strip Detector (SSD) and the related Front End Electronics (FEE) located on two hybrids, one for the N side and one for the P side. Bumpless Tape Automated Bonding (TAB) is used to connect the detector to the hybrids by means of microcables with neither wirebonding nor pitch adapter. Each of the six dedicated ALICE128C FE chip [1], located on the hybrid, is TABed on identical single layer microcables, which connect its inputs to the DS SSD and its outputs to the hybrid [2]. These microcables are bent in order to fold over the two hybrids on the DS SSD. This module meets the specifications of two experiments, ALICE (A Large Ion Collider Experiment) on the LHC accelerator at CERN [3] and STAR (Solenoid Tracker At Rhic) on the RHIC accelerator at BNL (Brookhaven National Laboratory) [4]. It can be used with air cooling (STAR) as well as with water cooling (ALICE) [5]. This mechanically self-consistent FE module has been tested on the SPS beam at CERN. Preliminary results are presented.

1. INTRODUCTION

During the summer 1998, a prototype module, including a DS SSD (according to the ALICE ITS Inner Tracking System and STAR SVT Silicon Vertex Tracker specifications) and two sets of ALICE128C FE chips, was tested on the SPS and PS accelerators at CERN and on the Vivitron at IReS. Two talks presented at Rome during LEB98 provided extensive information on the ALICE128C chip [6] and on the test results [7]. Complementary documents have also been produced [8]. These tests revealed an operation meeting all the specifications of the Technical Proposals (TP), the mechanical aspect excepted. Actually, the integration of this prototype on the ladders was impossible because of its size as well as of its flat layout imposed mainly by the wire bonding connecting the chips to the detector via the pitch adapter. So, based on the same components, a compact detector module using TAB technology has now been produced to fit the geometrical ladder hermeticity requirements and the different cooling options of STAR and ALICE.

2. DOUBLE SIDED SSD MODULE

Fig. 1: Detector module in full size

The module consists of the mechanically self-consistent DS SSD and FEE hybrid assembly. Figure 1 represents
this module in top view i.e. from the hybrid side.

One can see the detector's N side through the gap between the two hybrids folded over the detectors. One hybrid is connected to the detector's N side facing the hybrids whereas the other hybrid is connected to the back on P side. On each hybrid, the three lower FE chips have their input microcables back-folded from the chip in order to lower the coupling with the input amplifiers. Two thin Al pins on each hybrid will allow the mechanical fastening and heat connection of the module onto the ladder. The outside frame holds mechanically the module onto the spectrometer used for the beam tests. This "credit-card-like" module has the size of the detector and a thickness of about 4 mm.

320 such modules are needed for STAR and 1770 for ALICE.

2.1 Detector

The $75 \times 42 \times 0.3$ mm DS SSD includes 768 AC coupled strips on each side with a pitch of 95µm at a stereoscopic angle of ±17.5 mrad. Guard and bias rings are all together ≤1 mm wide.

2.2 Front End Electronics

- The FEE is located on two separate but identical hybrids, one connected to the N and one to the P side of the detector.
- The component side of the two hybrids faces the same orientation.
- At least one of the hybrids is electrically floating.
- Hybrids are double-sided printed circuits made of 50 µm thick Kapton with 17 µm Cu, Ni and Au plated, on top.
- One COSTAR multipurpose control chip is located on each hybrid for temperature, low and high voltage and leakage current monitoring, and also for the ALICE128C analog output offset compensation.

3. TAPE AUTOMATED BONDING

3.1 Manufacturers

Two French companies, Bull and Dassault have first developed the bumpless Tape Automated Bonding in a joint EuroTAB project. Meanwhile the TAB department of Dassault migrated to Thomson under the name Thomson-CSF-Detexis. These companies which lead this market in France have a great expertise in TAB for the consumer market as well as for air, space and military high level applications. They provide the microcables, the TAB, the bending and the assembling of the module.

3.2 Microcables

They are produced on long tapes as in figure 2. Each single frame is cut away and fixed into a plastic frame holder for easy handling and labeling as presented in figure 3, seen from the metal side. The black ALICE128C FE chip is then TABed upside down near the middle of the microcable.

The outer part, including the test pads, will be removed after testing. The inputs on the left side will then be TABed onto the detector and the outputs on the right side onto the hybrid.

The microcables have the following characteristics.

- One layer only.
- One identical layout for all the FE chips.
- One unique cable for inputs and outputs.
- Two TABing steps are implemented:
  - Inside Lead Bonding (ILB) for testing and
  - Outside Lead Bonding (OLB) for assembling.
- A so-called “UIIU” ILB input topology to meet the 44 µm input pitch of the chip by splitting the TABs on two staggered rows having an 88 µm pitch each.
- 135 µm ILB output pitch.
- 95 µm OLB detector pitch.
- 240 µm OLB hybrid pitch.
- Thickness: 17 µm Cu, Au layered, on top of 70 µm Kapton.
• Kapton is removed on bonding locations.
• Kapton is also removed on bending locations in order to avoid mechanical stress on the metal at the bending area.
• TABing is possible from both sides of the microcables, allowing for the components on the hybrids to face any appropriate side of the detector.
• There is no lost channel between 2 neighboring microcables.

The standard industrial Cu cables have been used because they proved their mechanical and electrical ruggedness and reliability on various applications.

Use of Al cables of same geometry is presently investigated.

3.3 Test features

From the early project step, this FE module has been designed for being tested all along its manufacturing, assembling and operating [9]. Everything can be remotely set, tuned, tested, checked and monitored at each step [10]. This convenience dictates all the steps of assembly of the DS SSD module.

3.4 Steps of TABing and assembling

• ILB TAB. Each FE chip is first TABed on its unique single layer microcable (Figure 4), with test pads extensions, fixed inside its plastic frame holder (Figure 3).

Fig. 4: X shaped TABs on the right side of the ALICE128C FE chip.

• Chip test. The frame with its test pads is plugged on a test socket for chip and ILB checking. This test, running on a laptop PC with LabView software, is interfaced by a National Instrument digital an analog I/O PCMCIA card and a compact JTAG module plugged on the printer port. It displays, in real time, the progress of the tests and produces an output file of the measurements corresponding to the data sheet.

• Extension removal. After completion of the tests, the surrounding test pads are removed with the associated plastic frame holder.
• OLB hybrid TAB. The remaining part of the microcable, inside the dotted area on figure 3, is then processed. The output side of this assembly is double folded in order to bring the microcable next to the hybrid surface and TABed onto the pads of the hybrid which has already been equipped before with about 50 passive components and one COSTAR chip. Six FE ALICE128C chips on their microcable are TABed on each hybrid in this way.
• Hybrid test. The full-equipped hybrid is then tested with the same equipment as the single chip, but via a flex cable connector which plugs on the connection towards the ladder end.
• OLB SSD TAB. The remaining free input side is then flat positioned onto the SSD pads and TABed on them.
• Location of SSD TAB. One hybrid is connected to one end of the SSD P side, the metal layer of the microcable facing the SSD, whereas the second hybrid is connected to the opposite end of the SSD N side, the Kapton of the microcable facing the SSD (Figure 5 top).
• Folding for air-cooling. The two hybrids are folded over the N side of the detector with their components looking outside the module for air-cooling (Figure 5, middle and bottom view).

Fig. 5: Assembling

• Folding for water-cooling. The hybrids can be folded over the detector with their components inside, facing the detector. They show then a flat surface appropriate for water cooling by means of a heat-bridge.
• Stiffening spacers. The detector is fixed on the hybrids by means of 100 µm thick carbon-fiber-epoxy stiffening spacers glued on the backside of each hybrid. A thin side extension protects the edge of the detector from mechanical shocks. (Figure 5, bottom).
• Ladder tightening pins. Each spacer is equipped with two pins to fix and to cool the module onto the ladder.
• Plan position on the ladder. The modules can be placed jointly on the ladder next to each other because of the thin microcables feeding all the signals on one face in
a 100 µm space. They present their insulated Kapton face to the outside. Thus they can be assembled onto the ladder on a single plane with a minimum of dead area (STAR).

- **Tile position on the ladder.** The modules can also overlap like tiles for a perfect hermeticity but with a higher material budget and a more complex geometric tuning (ALICE).

### 4. Radiation Length

Available computations on the radiation length of a whole silicon strip layer tend to a $X/X_0$ of 0.7 - 1%. $X_0$ = 14.3 mm leads to a $X/X_0$ of 0.12% for a uniform 17 µm thick Cu layer. This value must be weighted by the surface ratio which is about 0.25. So, the mean value of $X/X_0$ gets down to 0.03% which represents a weak fraction of the total radiation length for the layer. We consider that this value is acceptable, especially when air-cooling is used (STAR option) which reduces the material budget.

### 5. Aluminium Cables

The use of Al cables has been investigated by the Utrecht-Kharkov collaboration for the ALICE experiment [11]. These cables have a 14 µm Al layer on top of 12 µm Kapton. After having investigated different topological options, multilayer multicable input, separate input and output, the collaboration finally adopted the same topological “UIIU” input option, the single layer option, the grouping of input and output on a unique microcable and the addition of test pads. The collaboration kept nevertheless a different input microcable layout for the different FEE chips, depending on their location on the hybrid.

### 6. Beam Tests

The beam tests of different samples of the described module started on 15 September 1999 on the SPS at CERN and they are going on. The modules provided immediately coherent measurements.

#### 6.1 Beam test setup

In the background of the real STAR experiment, the beam tests have been performed with a setup as close as possible to the real experiment operation mode, with the real hardware, crates, boards, power supplies, cable length, locations and distances. The Device Under Test (DUT) i.e. the DS SSD module is located in the center of a high-resolution spectrometer provided by the LEPSI [12], (Figure 6).

Due to the peculiar geometric relationship between the SSD strips and the readout channels, a lookup table has been implemented in the DAQ in order to provide realistic real time display of the acquisition data.

The DAQ system using a MicroDAS program on OS9 Operating System (OS) is running on a VME processor located in the crate housing the hardware interfaces.

Another VME crate, running VxWorks, houses the CAENnet interface for driving and monitoring the power supplies and the JTAG interface for the detector and slow control.

An Ethernet connected SUN workstation, running Solaris OS, operates the higher level control on the VME VxWorks crate and operator interface (later GUI Graphic User Interface).

#### 6.2 Results

The baseline for the results is given by the measurements presented in LEB98 [7]. The analysis of the presently acquired data is going on and the plots on figures 7 and 8 are consistent with the results provided by the previous large size wire-bonded prototypes.

The preliminary S/N (Signal/Noise) plots of figure 7 present a peak value of about 50 on the P side and about 22 on the N side.
side. This latter low N side value is strongly dependent on the SSD sensor characteristics.

A spare prototype SSD remaining from the 1998 runs has been used for this module. Production SSD should improve this parameter.

![Fig. 8: Charge matching between side P and N.](image)

Figure 8 presents the charge matching characteristics of the module together with the spread of this value that is important for ambiguous multi-hit resolution.

The geometric resolution perpendicular to the strips provides a RMS value of 22.5 micron on the P side and 21.4 micron on the N side of the module.

7. CONCLUSION

These preliminary beam test results, based on a low statistic, are consistent with those presented earlier and provided by an older wire-bonded prototype assembled with the same components. Deeper investigations are going on for the extensive specification.

It has nevertheless been demonstrated now that this new TABed DS SSD module exists, that it works and that it meets the electrical, mechanical and cooling specifications of both the STAR tracker and the ALICE tracker.

This module uses safe and reliable options: separate but identical hybrids for ground level and for high voltage FEE, and single layer microcables which are identical for all the FE chips.

Though each module has about 3800 TABs, no defective connection has been observed up to now.

Its compact and monolithic design forming a single 75 × 42 × 4 mm module ensures an easy assembling on the ladders to form the detector barrels.

ACKNOWLEDGEMENT

We are greatly indebted to the Thomson-CSF-Detexis company and especially to A. Dravet, Y. LeGoff, E. Duriez, J. Pucci and Mr. Meriac for their highly effective contribution in this technical development.

REFERENCES


Abstract
A new version of the ABC (Atlas Binary Chip) has
been submitted to Honeywell. The design contains many
enhancements over the original ABC: new DAC circuitry
for improved radiation hardness, faster and more robust
logic parts and new interface elements to the CAFE chip.
Each of these design elements will be described in detail
as well as the status of the ongoing test program.
Additionally, plans for production testing of ABC’s will
be presented.

1. INTRODUCTION
The ABC is an integrated circuit developed for the
Honeywell rad-hard CMOS process to provide data
buffering and data compression for the binary readout
architecture used for the silicon strip detectors in the
ATLAS Semiconductor Tracker (ATLAS SCT) [1]. This
chip was developed to operate in the extremely harsh
environment of the Large Hadron Collider (LHC) and
meet the ATLAS requirements of low power, low noise
and high efficiency. The chip is designed to be used in
conjunction with a front-end IC which is being developed
for the Maxim bipolar process, and it is functionally
compatible with another technology option being pursued
on the DMILL biCMOS process [2].

The chip includes the following features:

• 128 independent input channels with fast low power,
  level translators to accept signals from the bipolar
  front-end chip.
• 128 channel by 132 deep pipeline buffer constructed
  as a fully dual-ported memory.
• De-randomizing buffer to stage data for output
  processing.
• Data compression to suppress output from non-hit
  channels and compact data from hit clusters to reduce
  data transmission time.
• Serialized LVDS output.
• Token passing scheme to allow multiple chips to
  operate in a chain with minimal interconnects.
• Redundancy schemes to allow continued operation
  when some chips in the chain become non-operational.
• Error reporting of some faulting conditions in trigger
  processing.
• DACs for control of analogue functions on the bipolar
  chip.
• Testability features to allow chip functionality to be
tested at wafer probe as well as in situ.

The binary readout architecture includes an amplifier-
discriminator chip, named CAFE, which amplifies raw
signals from the sensor strips and uses a single threshold
discriminator to distinguish hit from non-hit channels.
These discriminated signals are then fed to the ABC chip
for buffering and data processing. The main purpose of
the ABC is to provide pipelined data buffering until a
decision can be made by the ATLAS Level 1 trigger as to whether the data is sufficiently interesting to be read out. Upon receipt of such a trigger signal, the ABC must compress the data and serialize it for output through the optical transmission system of the ATLAS SCT. Data compression is required to meet the limits of the transmission system along with the expected trigger rate and occupancy. Likewise, an output or de-randomizing buffer is included to smooth out the fluctuations in the instantaneous trigger rate.

Since the accompanying CAFE chip does not have any digital circuitry to communicate with the control system, the ABC must provide various control signals to it when instructed to do so by the SCT control system. These include three DACs to control bias current, discriminator threshold level and calibration pulse amplitude. There are also signals to control the timing and addressing of calibration pulses inside the CAFE. All these control interfaces to the CAFE as well as the data exchange signals themselves must be designed to minimize any coupling of clock or other digital noise into the sensitive front-end circuitry. Care was also taken to make the interfaces self-correcting for variations in characteristics of the individual bipolar and CMOS chips.

The ATLAS SCT detector module contains 1536 sensor strips. These will be readout via 12 chip sets of 128 channels each. This group of 12 ABC chips must serialize data into two optical links. In order to accomplish this with a minimum number of interconnections on the interconnect hybrid, a token passing scheme was implemented. One design goal was to minimize the use of parallel busses because they complicate the interconnect layout and also because single chip failures can often disable the entire buss.

Furthermore, three redundancy features have been included. One allows the chain of readout chips to operate even if one of the chips in the chain should become faulty by having the token and data chain bypass the faulty chip. The second feature allows the readout chain to shift all of its data to one of the two normally operating optical links should one become faulty, and the third redundancy feature provides two independent clock and command inputs so that the backup one can be used should the primary fail. All these features were included in the design to increase reliability of the SCT where maintenance will be difficult. A block diagram of the chip is shown in Figure 1.

The first iteration of this chip was fabricated on Honeywell’s rad-hard bulk CMOS process, RICMOS-IV. Testing of the circuit revealed an error in the clock receiver circuit which prevented proper functioning. Using focused ion beam repair processing, the faulty circuit was bypassed on a few chips so that the rest of the circuitry could be tested. Following extensive tests, a...
redesign of the clock receiver circuit and further optimization of other circuit blocks, a second iteration was fabricated. Early test results of the second iteration will be presented.

2. TWO VERSIONS OF THE ABC

2.1 The first ABC

The prototype ABC was submitted to Honeywell in 1997. The first wafers were received November of that year. Some processing problems with the metalisation were identified by the foundry prior to shipping the wafers. Early tests of a few die confirmed that the ABC chips were not working. A follow-up lot was then processed and received February of 1998. Although largely functional there were a number of design problems discovered. These were then resolved and a second version (ABCH2) submitted. This has now been received and the results of preliminary tests with the new chip are presented below.

Figure 2: ABC version 1

The first ABC version is shown in Figure 2. Note that the standard cell blocks are separated into different regions and wired together at the ‘top-level’. This method was found to be very labour intensive and all the standard cell logic was combined into one larger region on the second version. Examples of design problems encountered were incorrect function of the Power-on-reset circuit and LVDS inputs as well as changes to the reset configuration of the chip to conform to the ABC specification.

2.2 The second ABC

In all, around 30 changes were made. Each was tracked with exhaustive design review procedures to ensure all were implemented correctly. Not all changes were due to design problems but rather improvements to the power routing and increasing the robustness of the input level translators and the introduction of power saving features. The ABCH2 chip is shown in Figure 3.

Figure 3: ABC Version 2

3. NEW DESIGN FEATURES

3.1 Test Port

Following the problems encountered in testing the first ABC a new test feature was incorporated into the ABCH2 design. It consists of a 128 input test multiplexer that gives access to 128 selected internal nets. These were then chosen carefully so that key timing signals and logic nodes were accessible. In the initial tests of the ABCH2 die this feature was then used to prove the functionality of the chip (see below). The multiplexer is controlled by a binary counter that is clocked from a dedicated input to a value that decodes the net of interest. That signal is then available at the ‘test out’ pin for observation. The full list of available signals is described in the chip specification document [3].
4. TEST RESULTS

4.1 Logic testing
The ABCH2 chips have been analysed with an IMS ASIC test system and have been proven to conform logically to the model of the circuit. The analogue parts of the ABC, however, require independent study and all cases so far have proven to be within specification. Examples are listed below.

4.2 POR circuit
By using the test multiplexer it is possible to measure the voltages at which the ABCH2 switches as the power supply is applied to the circuit. Results of a test sequence to switch between supply voltages of 2V and 4V are shown in Figure 4 and Figure 5. This method only tests the circuit response to slow edges but this is well within the ABC specification.

4.3 The Data Compression Logic
One of the critical timing issues for the ABCs internal logic is how fast the Data Compression Logic can scan through the 128 channels looking for data, one of the worst cases is when there is no hit at all. In this case a token has to ‘ripple’ through 128 gates. The important timing criterion is that this must happen in at least 200ns. Great care was taken in the design to optimise this. Simulations predicted a typical delay per channel of 0.55ns or 70.4ns for the full 128 channels.

Using the test multiplexer the point where the ripple starts and finishes can be measured. A measurement showing the traces overlayed is shown in Figure 6 below. This demonstrates a total delay of 85ns which is well within the 200ns limit and close to the simulator’s expected value. Further tests are necessary on more samples as well as some post radiation measurements to identify the circuit’s performance in such conditions.

![Figure 4: POR circuit switching from 2 to 4 volts](image4)

![Figure 5: POR circuit switching from 4 to 2V](image5)

![Figure 6: Oscilloscope trace showing DCL timing](image6)

4.4 LVDS IO Cells
In the ABCH2 chip, a simplified output circuit was implemented. Instead of using on chip band-gap type references, the IO levels are defined by ‘H’ network resistors which define the output levels based on resistor ratios and supply voltage. This method has proven extremely successful. We measure IO voltages matching those expected to a few milli-Volt. Another advantage was that such circuits are easy to shut down when not required (by switching all power branches off). This function was successfully implemented and the expected power savings achieved.
4.5 Power Measurements

At wafer test each die will be measured for power in differing configurations. So far only preliminary figures exist. One die on a test card was measured at 1, 10, 20, 30, 40 and 50 MHz in both Master and Slave modes. The results of those measurements (calculated in mW per channel) are shown in Figure 8. A constant difference of 0.14mW is shown between Master and Slave modes. This corresponds to an additional DC current of 4.7mA and is as expected due to the datalink output circuit that is enabled in Master Mode.

The Slave configuration slope corresponds to 363μW plus 11μW per MHz.

Figure 8: ABC Power (mW/Channel)

4.6 Logic test summary

So far detailed tests have been performed on 12 die of which 10 appear to work correctly. Testing at wafer level is just starting and many die will shortly be available to the collaboration.

5. OUTSTANDING ISSUES

Following submission of the ABCH2 a further problem with the protocol engine was identified in the design. This, although not fatal, is important to correct prior to production for the Atlas SCT. The required changes have been executed and a new layout generated in preparation.

The DACs have not yet been studied in detail at RAL so no data was available for this paper. It is known, however, that there is a slight problem that results in failure to achieve true 8-bit precision throughout the DAC range. This is still under study and it is not yet known if changes will be required to remedy the problem.

ACKNOWLEDGEMENTS

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REFERENCES


3. Project Specification: ATLAS Binary Chip (ABC) Version: 5.01
ANALOG DESIGN IN DEEP SUBMICRON CMOS PROCESSES FOR LHC

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Abstract

The feasibility of analog integrated circuits for LHC experiments in deep submicron CMOS technologies has been investigated. This paper discusses general design issues and presents a systematic study of fundamental analog characteristics of commercial deep submicron CMOS processes.

1. INTRODUCTION

Present state-of-the-art CMOS technologies integrate MOS transistors with a minimum gate length of 0.18 $\mu$m-0.25 $\mu$m and operate with a maximum power supply of 2.5 V. The thin gate oxide used in these technologies has a high tolerance to total dose effects. Therefore, circuits designed in these technologies using dedicated layout techniques (enclosed layout transistors and guard-rings) show a total dose resistance complying LHC specifications [1].

Some of the integrated circuits for LHC however have moreover strict requirements on integration and low power consumption, especially in the inner parts of the detectors. A deep submicron technology is therefore a very suitable choice for digital ASIC design, whereas its use for analog and mixed-mode circuits must be investigated more carefully.

Commercial submicron technologies are in fact mainly intended for large volume digital applications. The data available from the manufacturers concerning properties like noise and matching may be not completely satisfactory from the analog designer's point of view. The power supply allowed by a typical 0.25 $\mu$m technology (2.5 V) is almost at the edge of the use of standard analog design techniques. This is of particular concern, for instance, for circuits like switched capacitors analog memories, which are extensively used in high energy physics applications.

A submicron technology offers however attractive features also to the analog designer. The many layers of interconnects can be used to improve the quality of analog signals, especially in mixed-mode designs. Due to the squeezed design rules, also density can improve, though not in the same proportion as for digital circuits.

The aim of this work is to investigate the analog performances of commercial 0.25 $\mu$m CMOS technologies.

In section 2 we discuss the main design aspects which have to be considered in using a deep submicron technology for analog and mixed-mode design. Section 3 describes the test structures we have designed to investigate the analog performances of the technologies and in section 4 measurements performed on such structures are presented.

2. DESIGN ISSUES

2.1 Noise

The input-referred spectral density of the channel thermal noise can be expressed as [2]

$$V_n^2 = 4kT(1 + \delta)\gamma \frac{1}{g_m}$$

(1).

In the above equation $k$ is the Boltzmann constant and $T$ is the absolute temperature.

For an ideal device, $\gamma = 2/3$ in strong inversion and $\gamma = 1/2$ in weak inversion. $\Gamma$ is the so called excess noise factor and indicates how much the measured noise exceeds the theoretical value calculated using the long channel MOS equations. Values of $\Gamma$ reported in the literature for non submicron technologies range from 1 to 1.5 [3].

The correction term $(1 + \delta)$ is introduced to take into account the effect of fixed bulk charge on $g_m$ [2,4].

The transconductance $g_m$ in strong inversion is defined by the well known equation

$$g_m = \sqrt{2K(W/L)\mu_p}$$

(2).

Due to the thin gate oxide, the parameter $K=\mu C_{ox}$ improves in submicron technologies, as can be seen from table 1.
### Table 1: Technological parameter for different CMOS technologies (NMOS).

<table>
<thead>
<tr>
<th>( L_{\text{min}} (\mu m) )</th>
<th>( t_{\text{ox}} (\text{nm}) )</th>
<th>( K (\mu A/V^2) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>24</td>
<td>68</td>
</tr>
<tr>
<td>0.8</td>
<td>14</td>
<td>90</td>
</tr>
<tr>
<td>0.5</td>
<td>10</td>
<td>134</td>
</tr>
<tr>
<td>0.25</td>
<td>5</td>
<td>280</td>
</tr>
</tbody>
</table>

For instance, a transistor with \( W=20 \mu m \), \( L=2 \mu m \), and \( I_{\text{ds}}=100 \mu A \) will have a \( g_m \) of about 370 \( \mu A/V \) if implemented in a 1.2 \( \mu m \) technology and of 780 \( \mu A/V \) if produced using a 0.25 \( \mu m \) technology.

In a deep submicron process, however, the possibility of scaling the \( L \) of the transistors is not as useful as it could be argued form eq. (3). In fact, for short channel devices, the increase in transconductance predicted by (3) is limited by velocity saturation effects [4]. Additional effects like hot carriers and weak avalanche phenomena may also worsen the noise performances, increasing \( G_\text{2A} \) significantly above 1 [4].

The increase in \( K \) has anyway an interesting effect, because it increases also the current limit between weak and strong inversion. This current is defined as [5]

\[
I_{\text{lim}} = 2nK(W/L)U_T^{\frac{1}{n}}
\]  

(4)

where \( n \) is the slope factor and \( U_T \) is the thermal voltage.

This limit for a fixed aspect ratio is a linear function of \( K \). In other words deep submicron makes weak inversion operation easier. This is an attractive feature for low noise and low power amplifiers, since the weak inversion operation maximises the transconductance to current ratio and minimises the input referred noise for a given power budget.

The other source of noise which has to be considered is the flicker noise. The flicker noise spectral density can be expressed as [3]

\[
V_n^2 = \frac{K_a}{C_{\text{ox}}^2 \cdot WL} \frac{1}{f^n}
\]  

(5)

Due to the increase in \( C_{\text{ox}} \) the flicker noise for a given transistor area is expected to reduce if the device is implemented in a submicron technology [6].

#### 2.2 Matching

The matching between nominally identical components plays an important role in basic analog building blocks like differential amplifiers, comparators and current mirrors.

The threshold voltage mismatch of MOS transistors is characterised by measuring the difference between the thresholds of many couples of nominally identical devices. The standard deviation of the difference distribution is usually used as a measure of mismatch and is described by the following equation:

\[
\sigma_{\text{Vth}} = \frac{A_{\text{Vth}}}{\sqrt{WL}}
\]  

(6)

The term \( A_{\text{Vth}} \) is a constant for a given technology and is given by

\[
A_{\text{Vth}} = B \cdot t_{\text{ox}}
\]  

(7)

where \( t_{\text{ox}} \) is the oxide thickness and \( B \) can be assumed to be 1 \( \text{mV} \cdot \mu \text{m}/\text{nm} \) for many different processes [7].

Data available in literature clearly indicate that \( A_{\text{Vth}} \) reduces with the oxide thickness [8,9]. A submicron technology has therefore better threshold matching performances for a given transistor area.

The standard deviation in case of the current gain factors \( \beta = K(W/L) \) is expressed as

\[
\sigma_{\Delta \beta / \beta} = \frac{A_{\beta}}{\sqrt{WL}}
\]  

(8)

Values of \( A_{\beta} \) found in literature are 1-3 \%/\mu m [10].

However, in high energy physics applications enclosed devices are often required to guarantee an adequate radiation resistance. Results about matching properties of enclosed transistor are described in section 4.

#### 2.3 Power supply limitations

A 0.25 \( \mu m \) CMOS technology typically operates with power supply of 2.5 V. Transistor threshold voltages are in the order of 450-550 mV. The maximum signal swing is hence reduced compared to a 5 V technology, and can consequently affect the dynamic range.

The most serious drawback of the required low voltage operation may occur in switched capacitor circuits. The elementary sampling cell of fig. 1 is used as an example.

![Fig. 1: CMOS transmission gate.](image)

Let’s suppose that the switch is closed (\( ck = \text{Vdd}, ck_b = 0 \)). In principle, in these conditions, the switch should provide a low impedance path and any voltage between 0 and \( \text{Vdd} \) could be sampled on capacitor \( Cs \).

However, it can be shown that if \( \text{Vdd} \) is smaller than the sum of the threshold voltages of the two transistors, a region exists in which neither device conducts. Therefore, when the switch is closed a low impedance path for each value of \( \text{Vin} \) between 0 and \( \text{Vdd} \) is not guaranteed anymore. This, of course, affects very seriously the dynamic range of conventional switched capacitor circuits.
In evaluating the minimum power supply required by the circuit of fig. 1 to work properly care must be paid to the bulk effect, which can rise the threshold voltages up to 1 Volt [6].

The minimum voltage is therefore about 2 V, which is not very far from the maximum operating voltage of a quarter micron technology (2.5 V).

On the other hand, in switching circuits power consumption benefits a lot from the reduced supply. A capacitive ladder of a charge redistribution A/D converter operating at 2.5 V will dissipate only 25% of the power required by a converter operating at 5 V (provided, of course, that capacitor size and operating frequency remain the same) [5].

2.4 Digital noise coupling

The front end chip used in high energy physics applications are mixed mode circuits in which sensitive analog parts (low noise preamplifiers) are implemented on the same chip together with digital functions. In some cases, the amount of digital logic required can be very high.

In submicron technologies the devices are usually built in a relatively thin (few microns) high resistivity layer which is epitaxially grown on a highly conductive bulk. This bulk provides a medium by which the switching noise of the digital part can easily propagate to the analog circuitry.

The best way to overcome this problem is to physically glue the backside of the chip to a ground plane. This solution is not always practical, because the backside is often passivated and a thinning-metallization procedure would be required.

Actually, it is worth saying that this problem is not peculiar to deep submicron technologies only. A large fraction of the mixed mode technologies currently available are derived from former pure digital processes and use the low doped epitaxial layer grown on a highly conductive wafer.

Deep submicron technologies offer however a high number (5 to 7) of metal layers for the interconnections. These layers can be used to avoid any sharing of power and grounding paths between digital and analog circuits.

3 TEST STRUCTURES

To study the problems discussed above a number of test structures were designed in 0.25 μm CMOS technology, namely:

- transistor pairs for matching measurements;
- wide transistors for noise measurements;
- transimpedance amplifiers;
- an analog memory and a switched capacitor successive approximation A/D converter.

The noise structures and the transimpedance amplifiers were implemented in two different technologies, whereas the other structures were designed only for one technology.

Up to now it has been possible to measure wide transistors (in both technologies, hereafter referred to as tech_a and tech_b), matching structures and the amplifier implemented in tech_a.

The results of these tests are discussed in the following section.

4. TEST RESULTS

4.1 Noise measurements

The noise measurements have been carried out for all devices in the three different regions of operation. The appropriate bias current for each device has been selected through a measurement of the $g_m/I_d$ characteristic.

A typical $g_m/I_d$ curve is shown in figure 2.

In figure 3 and 4 typical noise spectra for NMOS and PMOS transistors are shown for both technologies. These spectra were obtained biasing the transistors in the moderate inversion region, with a current of 500 μA and applying a drain-source voltage of 800 mV.

From the measurements we have estimated the excess noise factor $\Gamma$ and the flicker noise coefficient $K_f$. The excess noise factors are reported in table 2.

We point out that for the moderate inversion region we have reported $\gamma$ since in this region the value of the inversion layer thermal noise coefficient (which is 2/3 in strong inversion and 1/2 in weak inversion) is not exactly known.

In weak and moderate inversion the excess noise factor is comparable to what is found in literature for non submicron technologies [2,3].
Figure 3: Example of noise spectra for devices of tech_a (Ibias=500 μA: moderate inversion) W/L=1000/0.35.

Figure 4: Example of noise spectra for devices of tech_b (Ibias=500 μA: moderate inversion) W/L=2000/0.78.

Table 2: Excess white noise factors.

<table>
<thead>
<tr>
<th></th>
<th>tech_a</th>
<th>tech_b</th>
</tr>
</thead>
<tbody>
<tr>
<td>W.I.</td>
<td>Γ = 1.1</td>
<td>Γ = 1.1</td>
</tr>
<tr>
<td>M.I.</td>
<td>γ = 0.85</td>
<td>γ = 0.65</td>
</tr>
<tr>
<td>S.I.</td>
<td>4 &lt; Γ ≤ 5.5</td>
<td>2 &lt; Γ ≤ 3.4</td>
</tr>
</tbody>
</table>

The higher values of Γ we have found in strong inversion are consistent with other results previously reported for submicron technologies [4].

However, it is worth pointing out that a typical input transistor of a low noise front-end amplifier (W/L from 200/1 to 2000/1 and bias current from 50 μA to 500 μA) would rather operate in weak or moderate inversion.

The highest value of the flicker noise coefficient K, we have measured for PMOS transistors is 6×10⁻²⁷ C/m². For NMOS transistors the maximum value is 3×10⁻²⁷ C/m². A value which is used in noise calculations for NMOS transistors in conventional technologies is 6×10⁻²⁷ C/m² [3], which is in the same order of magnitude.

4.2 Matching measurements

In this work we have investigated in particular the matching behaviour of enclosed devices. We have measured about 100 chips. Each chip contains 5 enclosed NMOS differential pairs with different gate area. For each device we have extracted the threshold voltage, the β and the standard deviations of the difference distribution have been calculated.

We have observed that enclosed devices follow equation (6) and (8) for small gate areas, whereas they exhibit a “saturation” behaviour for gate area above 50 μm².

We have therefore modified equations (6) and (8) as following

\[ \sigma_{Vth} = \sqrt{\left(\frac{\Delta V_{th}}{\sqrt{WL}}\right)^2 + \sigma_{Vth0}^2} \] (10)

and

\[ \sigma_{\Delta \beta/\beta} = \sqrt{\left(\frac{\Delta \beta}{\sqrt{WL}}\right)^2 + \sigma_{\beta0}^2} \] (11).

The value found for \( A_{\text{th}} \) is 5.4 mV/μm which is consistent with eq. (7) since \( t_{ox} \) is about 5.5 nm in this technology. The value of \( \sigma_{\text{var}} \) is 0.95 mV. For \( A_\beta \) we found a value of 1.5% μm, with \( \sigma_{\beta0} = 0.33\% \).

Due to these “saturation effects”, enclosed layout transistors tend to have worse matching performances. The values at which the saturation occurs are however still compatible with the needs of precise analog design.

4.3 Transimpedance amplifier results

The transimpedance amplifier uses the scheme detailed in [11,12] in which a current controlled g m stage in used as feedback around a single stage cascode amplifier. The input device of the preamplifier is a NMOS with W/L=500/0.35; an oxide capacitance per unit area of 6.9 fF/μm² and a g m of 7 mS for the input transistor have been used in the noise calculations. The transimpedance gain has been adjusted to 300 kΩ. In the test set-up, the capacitance seen by the input of the preamplifier was calculated to be 5 pF.

The output measured with a digital oscilloscope in these conditions is reported in fig. 5.

Figure 5: Preamplifier pulse response (input charge: 4 fC).
measured with a true r.m.s voltmeter and was found to be about 0.7 mV r.m.s, which corresponds to an input referred noise of 434 electrons. The noise slope was 81 electrons/pF. This value agrees with the one calculated for a second order system (72 electrons/pF) using the formulae proposed in [3].

5 CONCLUSIONS

In this work basic issues related to the use of deep submicron technologies for analog integrated circuits design have been investigated and dedicated test structures have been designed.

Particular care has been paid to the study of the noise performances of the technologies and of the matching properties of enclosed layout devices, which are needed in most applications in order to achieve the required radiation resistance.

The results on the matching of enclosed transistors show that the dispersion of the threshold voltage saturates at a value of 0.95 mV for transistor area above 50 $\mu$m$^2$. This, however, is not a serious drawback for most analog applications.

The noise excess factors found in weak and moderate inversion are close to the minimum theoretical values. Higher excess noise factor have been measured in strong inversion. This region of operation should be avoided in input transistors of low noise amplifiers.

A transimpedance amplifier has been completely characterised. For a power consumption of 1 mW, the amplifier gain is 9.4 mV/fC and the input referred noise for an input capacitance of 5 pF is 434 electrons r.m.s.

Test performed up to now show the compatibility of the measured devices with the requirements of low noise and precise analog designs. Some penalty can be paid if enclosed layout transistors are used in structures whose performances heavily rely on matching.

6 REFERENCES


The APV25 Deep Submicron Readout Chip for CMS Detectors

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Abstract

The APV25 is a 128 channel analogue pipeline chip for readout of silicon microstrip detectors in the CMS tracker at the LHC. Each channel comprises a low noise amplifier, a 192 cell analogue pipeline and a deconvolution readout circuit. Output data are transmitted on a single differential output via an analogue multiplexer. The chip is fabricated in a 0.25 micron CMOS process to take advantage of the radiation tolerance, lower noise and power, and high circuit density which can be achieved.

1. INTRODUCTION

The CMS inner tracker contains approximately $10^7$ channels implemented in silicon and gas microstrip technologies, read out by APV chips. For several years now these chips have been developed [1,2] to meet the demands of low-noise, low power and radiation hardness required for operation at the LHC. More recently it has been demonstrated that commercial deep submicron CMOS technologies currently available may exhibit radiation tolerance to levels in excess of those required [3], together with the possibility of operating with low noise and power consumption, as well as increased circuit density. Because of the potential for improvements we have embarked on a rapid development programme to produce a prototype APV chip in a deep submicron technology.

2. CHIP OVERVIEW

The APV25 chip has been designed in a 0.25 micron CMOS process and is very similar in concept to previous APV chips. It has 128 readout channels, each consisting of a 50 nanosecond CR-RC type shaping amplifier, a 192 element deep pipeline and a pulse shape processing stage which can implement a deconvolution operation to achieve the single bunch crossing resolution necessary at high luminosity. Analogue output samples are then multiplexed onto a single differential output for subsequent optical transmission to the DAQ system. The output data frame consists of these analogue samples preceded by a digital header which includes a digital address of the pipeline column from which the data originates. The chip can operate in one of three modes. In peak mode, following an external trigger, one sample for each channel (timed to be at the peak of the amplifier output pulse shape) is read from the pipeline and subsequently output through the multiplexer. In deconvolution mode, three samples per channel are read from the pipeline and combined in a weighted sum before output. In multi-mode a sequence of external triggers allows a number of consecutive pipeline samples to be transmitted in consecutive output data frames.

The pipeline is used to store the amplifier outputs, sampled at the 40 MHz LHC frequency, while external trigger decisions are taken. The pipeline depth allows a programmable latency of up to 160 bunch crossings (4 microseconds) the remaining locations being used for buffering of data from up to 10 events (in deconvolution mode). For technological reasons the pipeline storage elements have been implemented using gate capacitance which allows a very dense layout for this memory array. The APV25 deep submicron CMOS chip contains all the necessary system features, including on-chip bias and calibration pulse generation, and a slow control interface for programming these features and the operating mode of the chip. The active chip area is approximately $7.2 \times 6.5$ mm$^2$. However due to its manufacture on a multi-project run, the die size is $8.2 \times 8.0$ mm$^2$. 

Figure 1. APV25 chip
3. FRONT END

The front-end electronics of the APV25 chip are essentially the same as those for APV6, but with slight modifications to optimise it for the deep sub-micron process characteristics.

3.1 Preamplifier

The preamplifier is a charge amplifier made from a single-ended folded cascode amplifier with a 150fF feedback capacitor. The pFET input transistor has a size of $2000 \mu m / 0.36 \mu m$ and is biased at 400$\mu A$. Its source is connected to GND to reduce power consumption. The output is buffered by a source follower which also provides the level shift required for DC stability through the feedback transistor. The feedback transistor also provides a discharge path in order to avoid excessive pile-up in the preamplifier. A switchable unity gain inverter is employed when detectors of opposite polarity are used to allow full use of the shaper dynamic range (limited by the 2.5V power supply). Feed-through is eliminated by pulling the centre of the switches to VSS when the switches are off. The preamplifier (including the inverter) has a gain of 18.7mV/mip (25 000 electrons) and a power consumption of 0.9mW.

3.2 Shaper

The shaper is an effective CR-RC filter producing a 50ns shaped voltage pulse. The shaping is adjustable, over a limited range, to offset the inevitable degradation of the pulse shape which is caused by irradiation.

The shaper is composed of a single-ended cascode amplifier (non-folded) with a feedback capacitor of 150fF and a coupling capacitor of 1.4pF. The pFET input transistor has a size of $200 \mu m / 0.36 \mu m$ and is biased at 48$\mu A$. The shaper has a power consumption of 0.25mW, giving a total front-end power consumption of 1.15mW. The total front-end gain is 100mV / mip with a non linearity of less than 2% over a 5 mip range. (measured at point a in figure 5, corresponding to the third samplet of the troplet used in Deconvolution mode).

3.3 Noise

By far the largest contribution to the front-end noise is the input transistor of the preamplifier. In simulation, the noise has been shown to be 246 electrons + 36 electrons / pF. With 18pF of detector capacitance, this gives 900 electrons of noise.
4. PIPELINE

The pipeline buffers data on-chip for sufficient time for the level 1 trigger to make a decision. Thanks to the smaller geometry of the deep sub-micron process the pipeline length could be increased from 160, in previous versions, to 192 thus increasing the maximum latency time up to 4µs. The FIFO depth (which determines the number of triggers which can be reserved for read-out at any one time) has also been increased from 20 to 32.

4.1 Analogue Memory

The pipeline consists of 128 channels by 192 columns of switched capacitor elements. One side of the capacitor connects to VSS and the other to the shaper output bus through a write switch, and the APSP input bus through a read switch. Due to a limit on the total area of metal-insulator-metal capacitors allowed within the chip, the pipeline capacitor has been implemented using the gate of a 7µm x 7µm nFET (280fF). Given the DC operating point of the shaper output, the nFET gate capacitor is always in strong inversion which guarantees the best linearity for voltage to charge conversion.

4.2 Digital Control

The pipeline control sequences the writing, triggering, storing, and retrieval of data from the analogue memory. A write pointer continuously circulates the pipeline sampling the shaper output from each channel at intervals of 25ns. A trigger pointer follows behind the write pointer, separated by the trigger latency. When a trigger is received, depending on the mode of operation, either one, or three columns, marked by the trigger pointer, are reserved for reading out. Once reserved these columns cannot be overwritten until the data have been read out.

The column pairing present in previous versions of the chip (due to area limitations) has been removed. In addition, the time taken to release consecutively triggered columns in the pipeline, once they have been read, has been reduced. Latency error detection has also been improved from previous versions.

5. ANALOGUE PROCESSING

Signals from silicon strip detectors arrive at the inputs to the APV25 as single impulses of current which are integrated in the preamplifiers and then CR-RC shaped into well defined voltage pulses. These signals are then continuously sampled every 25ns, and the samples stored in the pipeline awaiting read-out.

In Peak mode one sample is reserved in the pipeline for reading out – this corresponds to the peak voltage of the CR-RC shaped signal. Peak mode is generally used when data rates are sufficiently low so that the effects of pile-up of detector signals are not significant. In this mode, the signal-to-noise ratio is maximised and the non-linearity of the signal is minimised. However, if pile-up does become significant – at higher rates of data – then to sample just the peak of the signal is not enough since the CR-RC shaped signals will superimpose. In this situation, the chip is operated in Deconvolution mode.

In Deconvolution mode three samples are reserved in the pipeline. The third sample corresponds to the voltage at point a shown in figure 5. The second and first samples correspond to the voltages 25ns and 50ns (respectively) earlier. In order to determine which 25ns period the original signal occurred it is necessary to deconvolute the three samples. This operation is performed in the APSP (analogue pulse shape processor).

The APSP (figure 6) is a three weight FIR filter composed of a charge amplifier and a switched capacitor network. It is DC-coupled to the pipeline read bus and so the operating point of the charge amplifier is matched to that of the shaper.

The operation of the APSP in Deconvolution mode is shown in figure 7. The charge on each of the triggered pipeline elements is read out, in sequence (during the active low periods of ri1, ri2 and ri3), integrated onto the APSP feedback capacitor, and the resulting voltages sampled on the three weighted capacitors. The charges
stored on these weighted capacitors are then summed (during the active low periods of ro1, ro2 and ro3) and again integrated onto the feedback capacitor which has now been increased in size (using last_cycle) to reduce the gain. The resulting voltage is stored on the hold capacitor during the signal store (active low). This must be done while the analogue multiplexer is outputting the digital signal. The DC output level of the resulting signal can be adjusted using the backplate bias Vadj.

The charges stored on these two capacitors are then summed and integrated on the APSP feedback capacitor during ro1 and ro2. The resulting voltage is sampled on the hold capacitor during the signal store. As with Deconvolution mode, the DC output level of the APSP can be adjusted using the bias Vadj. This method of performing the Peak mode operation of the APSP differs from previous versions of the chip, but was implemented to ensure that in both Peak and Deconvolution modes the polarity of the output signal is consistent.

Figure 8. Output of APSP in Deconvolution mode.

Figure 8 shows the output of the APSP (before the hold capacitor) operating in Deconvolution mode. If the shaper signal is an ideal CR-RC shape then the first two samples should contain no signal. However it can be seen from figure 8 that there is a small signal in the second sample. This is due to a slight knee in the rising edge of the shaper signal, and this has been taken into account in the weighting of the APSP capacitors. The gain of the full analogue chain up to this point is 100mV/mip with a non-linearity of less than 2.11% over a 5 mip range.

Figure 9. Operation of APSP in Peak mode.

The operation of the APSP in Peak mode is shown in figure 9. The charge stored in the single pipeline element is read out during ri1, integrated onto the APSP feedback capacitor and the resulting voltage sampled on the first of the weighted capacitor. During ri2, the APSP reset level is sampled onto the second weighted capacitor during ri2. The charges stored on these two capacitors are then summed and integrated on the APSP feedback capacitor (during ro1 and ro2). The resulting voltage is sampled on the hold capacitor during the signal store. As with Deconvolution mode, the DC output level of the APSP can be adjusted using the bias Vadj. This method of performing the Peak mode operation of the APSP differs from previous versions of the chip, but was implemented to ensure that in both Peak and Deconvolution modes the polarity of the output signal is consistent.

Figure 10. Output of APSP in Peak mode.

Figure 10 shows the output of the APSP (before the hold capacitor) operating in Peak mode. The gain of the full analogue chain up to this point is 100mV/mip with a non-linearity of less than 0.6% over a 5 mip range. The non-linearity in Peak mode is better than deconvolution mode because in deconvolution mode the shaper signal is sampled on the rising edge which may be prone to slewing effects for large signals. The power consumption of the APSP is 0.2mW.

6. ANALOGUE MULTIPLEXER

The analogue multiplexer uses the same three level current mode architecture as with previous versions of the chip – with a few refinements. Firstly, the resistor used to convert the APSP voltage into a current has been made programmable with a choice of five values. This is to trim the multiplexer gain since the resistor value is only known to 20% accuracy. In addition, to overcome problems found in previous versions, channels which are not connected through to the output have their currents dumped into a load device. This is wasteful of power, but it ensures that channel readout does not affect the voltages generated on nodes within the multiplexer. The analogue gain at the output of the multiplexer is 100µA/mip. A digital header, which precedes the output of the data from the 128 analogue channels, takes the value of +/- 400µA (HI / LO respectively). With the input bias set to 50µA the power consumption is 22mW.
7. OUTPUT BUFFER

The multiplexer output is converted into a differential bi-directional current by the circuit shown in figure 11. The output has an analogue gain of +/- 1mA / mip and a digital header of +/- 4mA (HI and LO respectively). The buffer has a power consumption of 20mW. Format of the data produced at the output of APV25 is shown in figure 12.

8. RESULTS

The APV25 was received back from fabrication immediately prior to submission of this paper and is currently under test. The chip is fully functional and initial results demonstrate it is working well as shown in figures 13 and 14.

9. CONCLUSIONS

A new analogue pipeline has been designed in a deep sub-micron process. It is based on the APV6 with modifications which make use of the increased circuit density achievable using this process. Radiation tolerance to LHC requirements has been made using special design techniques, however SEU tolerance will not be achieved until the next version. Currently being tested, the APV25 is fully functional and radiation tests are imminent. Further information and test results can be found on http://www.rl.ac.uk/med/.

10. ACKNOWLEDGEMENTS

We would like to acknowledge technical support provided at CERN. Particular thanks are due to Sandro Marchioro and Kostas Kloukinas.

11. REFERENCES

Abstract

This paper presents the design and simulation results of components for a new LHCb readout chip for the silicon vertex detector, the inner tracking system, the pile-up veto trigger and the RICH. It is planned to use the same readout chip for these subdetectors. However, different versions of the analog input stages might be developed depending on the choice of the detector type.

In section 1, the specification of the new readout chip named Beetle with respect to the different subdetector systems is described. Sections 2 and 3 describe the design and the simulation results of two test chips. The first chip contains different types of frontends for the vertex detector and the second chip bias generators. Section 4 gives a brief overview on the future plans for the development towards a readout chip for LHCb.

1 Specification of the readout chip

The Beetle readout chip will contain 128 channels. Each channel consists of a charge sensitive preamplifier, a pulse shaper, an analog pipeline of a programmable maximum latency of 160 stages with an integrated derandomizing buffer of 16 stages and a serial readout for up to 40 MHz readout speed. In case of using the chip in the binary pipeline mode, the discriminated output of the shaper is stored into the pipeline and a fast binary multiplexer is used to read out the chip at a speed of 80 MHz. Readout multiplexing can be done in several modes: for fastest readout speed of analog data, four ports can be used at 40 MHz, each multiplexing 32 channels. Two ports multiplexing 64 channels running at 80 MHz can be used for readout of binary data. For applications which do not demand a fast readout, a single port multiplexing 128 channels can be used and several chips can be connected to build up a readout daisy chain, sharing a single readout line. In addition to the pipelined data path the combined signals of four neighbouring discriminators, that are located behind the shaper, are routed off the chip. All digital control and data signals are realized as low voltage differential signals (LVDS). The chip is programmable via the standard I^2C interface and by another serial interface, yet to be defined [1].

The requirement on the radiation tolerance is driven by the application of the chip in the silicon vertex detector. A radiation level of 2 MRad per year is expected for the frontend chips. With an expected usage time of 5 years, this leads to a total accumulated dose of 10 MRad [4]. In order

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Table 1: Summary of the requirements on the LHCb readout chip. Empty or multiple entries depend on the detector type decision

<table>
<thead>
<tr>
<th>silicon vertex detector</th>
<th>pile-up veto trigger</th>
<th>RICH</th>
<th>inner tracker</th>
</tr>
</thead>
<tbody>
<tr>
<td>sampling frequency</td>
<td>40 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L0 trigger rate</td>
<td>1 MHz</td>
<td></td>
<td></td>
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<tr>
<td>readout speed</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>max. latency</td>
<td>160 - 25 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>multi event buffers</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>consecutive L0 triggers</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>slow control interface</td>
<td>FC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>number of channels</td>
<td>220,000</td>
<td>400,000</td>
<td>220,000</td>
</tr>
<tr>
<td>overall readout pitch</td>
<td>50 µm</td>
<td>50 µm</td>
<td>60 µm</td>
</tr>
<tr>
<td>max. power consumption</td>
<td>4 mW per channel</td>
<td>4 mW per channel</td>
<td>2 mW per channel</td>
</tr>
<tr>
<td>irradiation dose per year</td>
<td>2 MRad</td>
<td>2 MRad</td>
<td>few 100 kRad</td>
</tr>
<tr>
<td>detector capacitance</td>
<td>10 pF</td>
<td>4 pF / few pF</td>
<td>1 MRad</td>
</tr>
<tr>
<td>required S/N</td>
<td>&gt;14</td>
<td>&gt;8 /&gt;20</td>
<td>&gt;10</td>
</tr>
<tr>
<td>dynamic range [electrons]</td>
<td>±110,000</td>
<td>45,000 /76 · 10^6</td>
<td></td>
</tr>
</tbody>
</table>

Design and simulation of the BeetleFE-1.0 frontend chip

The BeetleFE-1.0 chip contains three different sets of a prototype input stage, one of which is intended to be used in the Beetle readout chip for the silicon vertex detector and the pile-up veto trigger. Each of the three sets consists of four identical channels to allow studies of channel to channel crosstalk. Two of the sets use a PMOS device as input transistor, whereas the third set uses an NMOS transistor. All numerical values given below refer to the third set, since it is expected to most closely match the requirements. Figure 1 shows a layout view of the chip. The size is 2×2 mm². The input pads are located on the left side, the output pads on the right side. The remaining pads are used for probing purposes and for the power supply.

Each of the amplifier channels consists of a charge sensitive preamplifier, an active CR-RC shaper and a subsequent buffer. A schematic drawing of this configuration can be seen in Fig. 2. The transistors in the feedback of both stages are used as adjustable resistors. The buffer is realized with a standard source follower. The opamp cell of the preamplifier and the shaper use the well established folded cascode configuration. To a good approximation the noise of this amplifier circuit is determined by the input transistor of the preamplifier and its biasing. The power consumption is restricted by the silicon vertex detector specification to 4 mW per channel, for which the preamplifier has been optimized. The thermal noise as a function of the input capacitance $C_{input}$ can be calculated by

$$\frac{EN_{G_{thermal}}}{C_{input}} = e^{\frac{(1 + \eta) \cdot kT}{3 \cdot T_{peak} \cdot g_{m}}}$$

where $T_{peak}$ is the peaking time, $g_{m}$ the transconductance of the input transistor and $\eta$ the bulk-source transconductance of the input transistor. The $1/f$ noise can be neglected in this application, since the band pass characteristic of the shaping stage attenuates the low frequencies. In principle, the designer can choose the shaping time and the $g_{m}$, which is defined by the transistor geometry and the bias current. The pulse shape is constrained by the LHC bunch crossing.
frequency, since any shaped signal needs to return to zero 25 ns after its maximum to avoid a possible pile-up. The geometry can be optimized for minimum noise, since \( g_m \) rises proportional to \( W/L \) whereas the gate capacitance (which contributes to the load capacitance of the amplifying stage) rises with \( W \cdot L \). The value of \( \eta \) rises with decreasing \( L \). However, for this first submission, a set of values has been

<table>
<thead>
<tr>
<th>power consumption</th>
<th>slope of the noise function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.88 mW</td>
<td>46.5 e(^{-1})/pF</td>
</tr>
<tr>
<td>1.13 mW</td>
<td>41.4 e(^{-1})/pF</td>
</tr>
<tr>
<td>1.38 mW</td>
<td>37.5 e(^{-1})/pF</td>
</tr>
<tr>
<td>1.63 mW</td>
<td>35.5 e(^{-1})/pF</td>
</tr>
<tr>
<td>1.88 mW</td>
<td>33.6 e(^{-1})/pF</td>
</tr>
</tbody>
</table>

Table 2: Slope of the calculated noise function for different values of power consumption

chosen that distribute around the optimum set of values to make a comparison between the calculated noise values and the measurements. Table 2 lists calculated values of the slope of the noise function for different bias settings as a function of the total power consumption for one frontend channel of the third set. The offset of the noise function is not calculated, since the final layout of the input protection diodes and the input pads, that contribute a considerable amount of the input capacitance, is not yet defined.

![Figure 3: Transient response on a delta-shaped signal of 11,000 electrons](image)

The pulse shape of the frontend depends on the bias settings of the preamplifier as well as on the time constants of the shaping stage. Figure 3 shows an example of a simulated pulse shape from a signal of 11,000 electrons (which corresponds to a minimum ionizing particle in the silicon strip detector) with optimized settings for the silicon strip detector. The falling edge of the shaped pulse leads to an acceptable remainder of 25% of the peak voltage at 25 ns after the peaking time.

![Figure 4: Peak voltage at the output of the frontend as a function of the input charge (1 MIP = 11,000 electrons) for a load capacitance of 0 pF (upper curve), 4 pF and 10 pF (lower curve)](image)

The frontend has been designed to have a dynamic range between –10 MIP and +10 MIP, as demanded by the specifications of the subdetectors. A deviation from linearity of 5% is accepted. Figure 4 shows the simulated peak voltage as a function of the input charge for three different values of the load capacitance. The gain of the complete frontend is simulated to be 20.4 mV/MIP, 19.0 mV/MIP and 14.5 mV/MIP for a load capacitance of 0 pF, 4 pF and 10 pF, respectively.

![Figure 5: Frequency response of the pulse shaping stage](image)

The frequency response of the pulse shaping stage is plotted in Fig. 5. As expected for a semigaussian pulse shape, the frequency sweep shows a maximum at \( f_{\text{max}} = 1/(2\pi t_{\text{peak}}) \). This closely resembles the value for \( t_{\text{peak}} = 20 \) ns obtained from the transient simulation.
Table 3: Specifications for the three different current source options

<table>
<thead>
<tr>
<th>type of current source</th>
<th>maximum load</th>
<th>small signal resistance</th>
<th>power consumption</th>
<th>size [μm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) opamp feedback</td>
<td>1.06 V</td>
<td>4 MΩ</td>
<td>2.35 mW</td>
<td>164 x 61</td>
</tr>
<tr>
<td>(2) opamp feedback and regular cascode output</td>
<td>1.94 V</td>
<td>14 MΩ</td>
<td>2.5 mW</td>
<td>189 x 61</td>
</tr>
<tr>
<td>(3) regular cascode</td>
<td>1.93 V</td>
<td>17 MΩ</td>
<td>599 μW</td>
<td>84 x 23</td>
</tr>
</tbody>
</table>

3 Design and simulation of the BeetleBG-1.0 bias generator chip

The bias generator chip BeetleBG-1.0 contains 3 different types of current sources, a voltage digital-to-analog converter (DAC), a current DAC and test structures that will be used to study the change of transistor parameters under irradiation. Figure 6 shows a layout view of the chip. The size of the chip is 2 × 2 mm² and the components are laid out in such a way that the chip can be directly bonded to the BeetleFE chip to allow for frontend biasing and coupled testing.

![Figure 6: Layout of the BeetleBG-1.0](image1)

The three different current sources vary with complexity and performance. Table 3 lists the three different types with their simulated values. The current source (1) uses an opamp feedback. The second also uses an opamp feedback system but improves the small signal resistance by using a regular cascode at the output. The third choice uses only a regular cascode and relies on the fact that the chosen process has minimum threshold voltage shift and will not need compensation for radiation damage. The nominal current of the opamp feedback with a regular cascode output is 300 μA, whereas the others are 100 μA.

The voltage DAC uses an R-2R-ladder configuration with a resolution of 10 bit and an output range from rail to rail, that is from 0 V to 2.5 V. The 3.0 kΩ resistors are of the n+ diffusion type. The power consumption of the DAC is 690 μW. Figure 7 shows a plot of the output voltage for the least significant bit set as a function of the load resistance. A change in the output voltage of 1% is simulated at a load resistance of 70 kΩ. The lower curve in this plot shows the offset voltage, which has an acceptable value of 1.2 mV. The differential non-linearity caused by the resistance of the switches simulates to be 8 mV. The resolution of the DAC will be lowered for the final version, the high resolution of this prototype version has been chosen to learn about mismatch of devices in this technology.

![Figure 7: Output voltage of the voltage DAC (LSB is set in the upper curve) and offset voltage versus the load resistance](image2)

The voltage DAC uses an R-2R-ladder configuration with a resolution of 10 bit and an output range from rail to rail, that is from 0 V to 2.5 V. The 3.0 kΩ resistors are of the n+ diffusion type. The power consumption of the DAC is 690 μW. Figure 7 shows a plot of the output voltage for the least significant bit set as a function of the load resistance. A change in the output voltage of 1% is simulated at a load resistance of 70 kΩ. The lower curve in this plot shows the offset voltage, which has an acceptable value of 1.2 mV. The differential non-linearity caused by the resistance of the switches simulates to be 8 mV. The resolution of the DAC will be lowered for the final version, the high resolution of this prototype version has been chosen to learn about mismatch of devices in this technology.
The current DAC consists of 1024 conventional PMOS transistors with a W/L ratio of 0.6\(\mu\)m/3\(\mu\)m to optimize the current source to the LSB. Each bit switches on 2 \(^n\) parallel transistors, acting as a current source. Figure 8 shows the simulated output current for the LSB set as a function of the load voltage. A change of 2% occurs at a load of 1.5 V. The lower curve in the plot shows the simulated leakage current of 6.5 nA, which can be neglected in this application. As for the voltage DAC, it is foreseen to go to a smaller resolution in the final version of the current DAC. The study of leakage current and the transistor mismatch will be performed on this prototype version.

The test structures contain minimum size conventional PMOS and NMOS transistors, PMOS and NMOS transistor with an edgeless layout and conventional transistors with the same effective geometric values as the edgeless transistors. In addition, the sizeable NMOS input transistor, used in the third set on the BeetleFE-1.0, has been added. The behaviour on irradiation will be studied on these devices and compared to results, obtained from other processes.

4 Future milestones

It is intended to submit further components by the end of 1999, which include

- an iteration of the frontend,
- a calibration pulse generator,
- a comparator stage,
- a pipeline capacitor array including a pipeline control logic
- a multiplexer with an output buffer.

We plan to submit the first version of a complete readout chip in October 2000. A final version that can be used in the LHCb experiment, should be submitted by the end of 2001. Status reports will be available in [1].

References


[2] F. Faccio et al., Total Dose and Single Event Effects (SEE) in a 0.25\(\mu\)m CMOS Technology, CERN/LHCC/98-36


Optical links for the CMS Tracker

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CERN, Geneva (Switzerland)

Abstract

The development phase of the optical data transfer system for the CMS tracker is nearing completion. This paper focuses on three types of validation tests carried out by CERN on Commercial-Off-The-Shelf electro-optic devices: functionality tests, environmental tests and reliability tests. The project status and the preparation for production are also reviewed.

1. INTRODUCTION

The architecture of the CMS tracker analogue readout system is shown in Fig. 1. The ~50000 uni-directional links are based on edge-emitting laser transmitters and pin photodiode receivers operating at a wavelength of 1310nm. In every single-mode fibre, 256 electrical channels are time-multiplexed at a rate of 40MSamples/s. Two in-line patch-panels fan-in the fibres originating from the transmitters, first to a 12-way ribbon, and then to an 8-ribbon cable carrying 96 fibres away from the detector to the counting room. All system components situated inside the detector volume (drivers, lasers, fibres and connectors) must be non-magnetic, radiation resistant and reliable.

The analogue link requirements are summarised in Table 1. They are modest in comparison to what is typically achieved in other analogue distribution networks such as cable TV, but must be met at a very low cost, in a harsh environment, and for a large quantity of channels.

The ~2000 bi-directional digital links (Fig. 2) used for control and timing distribution are based on almost identical components as the analogue readout system, since the small number of digital channels does not justify the effort of selecting and qualifying specific devices.

The only differences between analogue and digital systems are the number of fibres per ribbon (8 compared to 12) and the fact that the receiver modules placed inside the detector need to be built with radiation resistant photodiodes and discriminating amplifiers.

Table 1: Analogue optical link requirements

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Typical requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analogue coding scheme</td>
<td>Pulse Amplitude Modulation</td>
</tr>
<tr>
<td></td>
<td>40MSample/s</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>48dB (250:1)</td>
</tr>
<tr>
<td>Integral linearity</td>
<td>2 %</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>100MHz</td>
</tr>
<tr>
<td>Settling time to 1%</td>
<td>18ns</td>
</tr>
</tbody>
</table>

The digital link requirements are summarised in Table 2. The operation frequency will be 40Mb/s for the data and 40MHz for the clock channels.

The development options, choices and component types selected to be used in the tracker optical data transfer system have been described elsewhere [1]. Also, results obtained with 4-channel prototype parallel

Fig. 1. Block diagram of the analogue readout link

Fig. 2. Block diagram of the digital control link

Table 2: Digital optical link requirements

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Typical requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Rate</td>
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</tr>
<tr>
<td>Bit Error Rate</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>-30dBm</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>100MHz</td>
</tr>
<tr>
<td>Jitter</td>
<td>&lt;0.5ns</td>
</tr>
</tbody>
</table>
analogue links have been reviewed in [2]. This paper presents the validation tests performed on commercial components before specifications are frozen and the production phase can be started.

2. COMPONENTS VALIDATION PROGRAM

Apart from the custom designed electronics for the laser-drivers [3] and photodiode-receivers [4], all optical link components to be used in the CMS tracker are based on Commercial-Off-The-Shelf products (COTS). Slight deviations from the standard manufacturing process are only allowed to meet specific functionality requirements such as low back-reflection (for analogue performance), or particular environmental constraints such as high magnetic field. For instance, whereas distributed feedback (DFB) edge emitting lasers are known for their superior analogue performance, and even though pure silica core fibre is usually recommended for radiation sensitive applications, standard low-cost Fabry-Perot lasers and telecom-grade single mode fibre is specified for the CMS-tracker optical links. This development strategy has the advantage of minimising development and system cost, but dictates the launch of extensive validation programmes to confirm that as wide a range of COTS as possible can be used reliably in the CMS tracker environment.

The optical link COTS devices consist of semiconductor lasers and photodiodes, as well as optical fibre and connectors. They are targeted at the telecom market and are of the single-mode, long wavelength type. Such telecom components are usually qualified for digital data transmission and for operation in standard (but nevertheless stringent) environmental conditions. Their use in an analogue system and in an environment like LHC must thus be carefully checked.

The components validation programme, devised to minimise the risk of using COTS in the CMS-tracker application, has three parts:

a) The in-system functionality tests must demonstrate that the telecom-grade components being evaluated meet the system-level requirements. For instance, standard Fabry-Perot lasers must be shown to satisfy the low noise requirements of an analogue readout system.

b) The environmental tests must subject the devices under evaluation to stress conditions not part of the standard telecom qualification programmes. For instance, telecom-grade single-mode fibre must be shown to be radiation-resistant, and components packages must be proven to be non-magnetic.

c) The reliability tests finally must ensure that environmentally stressed components (in particular irradiated devices) will have sufficient reliability to operate within specs during the lifetime of the experiment.

The validation programme described below in more detail is thus not simply a clone of standard telecom qualification procedures. It is an additional test, specifically matched to the operational and environmental requirements of the experiment. In this paper, we illustrate, as an example, the description of the validation-programme with results obtained with Fabry-Perot edge emitting lasers supplied by ITALTEL (Milano). Similar validation tests are being performed on all components considered to be used in the CMS-tracker optical links.

2.1. In-system functionality tests

The in-system functionality tests evaluate the system performance with the device under test embedded in a reference analogue optical link. It is assumed that devices meeting the analogue link requirements will also be good candidates for the digital links. The investigated system parameters are dynamic range, linearity and pulse response. The measurement procedure is described in [5]. The results are compared with the system-level specifications and presented in a way that allows comparison between devices and manufacturers.

Figure 3 shows, for example, the optical link static transfer characteristic measured with 20 laser transmitters of the same type. The spread in gain is due to variations in laser output coupling efficiency and connector insertion loss. The output noise in the full system bandwidth is also plotted in Fig. 3, normalised by the full scale signal amplitude, as a function of link input voltage.

This set of plots is reduced to 1 point per device in Fig. 4, where deviation from linearity and noise are computed, and normalised to a chosen fraction of the full scale signal. Integral deviation from linearity and peak signal to noise ratio can thus be quickly evaluated for any device operating in a given range. For instance, assuming an input voltage full scale of 800mV, one can quickly assess that in the first quarter of the operating range (i.e. 200mV input), a peak signal to noise ratio better than 140:1 and a linearity deviation of less than 0.6% are typically obtained with the tested devices. In the full operating range (i.e. 800mV), the peak signal to noise ratio of the same devices is greater than 300:1 for a linearity deviation of less than 1%.

The pulse response of the system is dictated by the custom designed transmitting and receiving electronics. It shows little dependence on the COTS under test. Typical rise time values are of the order of 3ns.

The in-system test results for laser transmitters shown above indicate that the investigated devices meet the CMS-Tracker analogue link requirements, despite the fact they were developed as digital transmitters for telecom applications.
2.2. Environmental tests

In the environmental evaluation procedure, the front-end components are tested for resistance to magnetic field and radiation. It is assumed that other usual qualification tests such as temperature cycling, vibration, etc. will have been performed by the manufacturers as part of the standard telecom qualification programmes.

The magnetic field resistance test is a simple mechanical test whereby the force exerted by the field on the device under evaluation is estimated.

The irradiation tests monitor in-situ the changes in the device performance resulting from radiation damage and subsequent annealing. They are carried out at room temperature with the devices operated under typical bias conditions. Both neutron and gamma irradiations are performed.

Figure 5 compares the threshold currents of 30 irradiated lasers to pre-irradiation values. The devices were irradiated with neutrons at room temperature to a total fluence of the same order of magnitude (2.5 to 6 x10^14 n/cm^2) as the maximum expected hadron fluence (pions, neutrons, protons etc. combined) in the CMS tracker over 10 years of operation. The irradiated samples were stored, electrically shorted, at room temperature for up to 15 months. Based on our earlier studies[6], we estimate that 30% of the initial radiation damage in the lasers annealed during this period.

A thorough discussion of the radiation damage effects for this particular type of laser can be found elsewhere for tests carried out using neutrons and other radiation sources [7]. Test results have also been published for optical fibre [8], connectors [9] and pin photodiodes [10]. Comparative validation results obtained in the framework of the market surveys for lasers and connectors will be available soon.
2.3. Reliability tests

Manufacturer-qualified, telecom-grade COTS are known to be highly reliable. However, it is not known if radiation damage will influence this reliability. Component reliability is often categorised into three domains: early, mid-life, and old-age failure, each with several different mechanisms [11] that contribute to the failure rate.

Early failures (sometimes termed ‘infant mortality’) are usually intrinsic to the device and are eliminated by a burn-in, or purge-test, inducing weak devices to fail before the components are employed in the field.

The mid-life failures can be subdivided into two parts, the first being simply due to the tails of the early and long-term failure distributions. The remaining failures are collectively grouped together as ‘sudden’ or ‘random’ failures, which are catastrophic failures often triggered by external factors such as electrical or mechanical shocks, depending upon the operating environment.

Long-term failures are usually dominated by ‘wearout’. For the optical link components inside the CMS tracker the most important wearout failure modes are likely to be resulting from a combination of radiation damage and intrinsic wearout degradation.

Ageing tests of irradiated components have been performed on semiconductor lasers and photodiodes, as well as optical connectors. As example, we show in Fig. 6 ageing test results obtained with 30 neutron-irradiated (see 2.2) and 10 unirradiated lasers. The laser threshold current versus time is plotted for all the devices tested. At 80°C (20°C) the unirradiated devices have initial threshold currents of 21-31mA (8-11mA) and the irradiated devices have values of 28-55mA (12-19mA), this larger variation being mainly due to the different neutron fluences received by the various devices. Overall, the rates of wearout degradation of the laser threshold currents are very small, <0.4mA/1000hours in the unirradiated devices. For the irradiated devices, annealing of the radiation damage is the main effect. Only a few of the irradiated devices show increases in threshold current. The device labelled A, which has the most degradation, should have actually been rejected by the supplier following burn-in, based on its high threshold current increase during the purge phase.

The irradiated lasers continued to anneal throughout the 4000 hours at 80°C, therefore the ageing related wearout was obscured for these devices and a wearout rate could not be accurately determined. However, as the annealing rate decreases with increasing time[6], the results suggest that the wearout rate of the irradiated lasers is not significantly greater than in the unirradiated samples.

Failure rates can be extrapolated from ageing test results such as shown in Fig. 6, by defining failure criteria and calculating acceleration factors. A detailed estimation of the reliability of irradiated lasers and photodiodes in the CMS tracker is in progress. Reliability tests have also been performed on optical connectors: repeated mate/demate tests on irradiated MT ferrules are reviewed in [9].

3. PROJECT STATUS

The feasibility of an analogue optical link meeting the CMS-Tracker requirements (both in terms of functionality and environmental resistance) has been demonstrated [2]. The elements not yet in their final form are: the laser driver ASIC, which is still implemented in a radiation soft technology, the 12-channel analogue receiver ASIC, which is currently under test, and the receiver module (combining photodiodes and amplifiers in one housing), which is being developed in industry. Options are still open for the optical connectors of the first patch panel, inside the CMS detector. They will remain so until the exact layout and modularity of the tracker is frozen.

Digital links operating at 40Mb/s and based on driver, laser, connector and fibre components identical to the analogue-link ones have been successfully tested in the laboratory. A full custom rad-hard digital receiver chip has been designed [4]. A radiation resistant InGaAs pin diode in a low-mass non-magnetic package has been identified, tested and validated.

An effort is now being made to integrate the optical links into complete readout and control systems. For instance, prototype 4-channel analogue links have been distributed to various institutes involved in the construction of the CMS tracker. A complete system evaluation in a 25ns test-beam at CERN is scheduled for May 2000.

In an attempt to reduce the uncertainties of optical link cost, a tendering procedure has been started for the best-
defined components in the system. Market surveys have been issued for semiconductor lasers and single-mode optical connectors. Samples from various manufacturers are currently being evaluated, following a validation programme consisting of interleaved functionality and environmental tests similar to the ones described in sections 2.1 and 2.2. Market surveys for optical fibre, ribbon and cable, as well as detector modules will follow in 2000. It is planned to issue the first calls for tender in the first half of 2000.

4. CONCLUSION

The combined needs for radiation resistance, high reliability and analogue functionality at low cost present a unique challenge. The use of COTS lasers, fibres, connectors and photodiodes benefits from the rapid progress made by telecom components suppliers and allows to reach cost levels compatible with the experiment budget. It however dictates the need for a thorough validation programme.

Three types of validation tests are being carried out on COTS electro-optic devices supplied by industry: a) functionality tests (compliance to system specifications), b) environmental tests (resistance to radiation and magnetic field) and c) reliability tests (ageing of irradiated components).

a) Functionality tests have confirmed that a variety of commercially available lasers, fibres, connectors and pin diodes can fulfil the CMS-tracker application requirements. Due to the stringent installation schedule, emphasis has first been placed on the evaluation of laser transmitters. A validation scheme has been worked out to compare different devices proposed by various manufacturers. Similar programmes are being prepared to evaluate optical connectors and cables.

b) Irradiation tests have been carried out extensively on lasers, pin-diodes, fibres and connectors with various sources and at different energies. In order to better understand the real long-term performance of irradiated components in the CMS-tracker environment, the annealing behaviour of laser damage versus operating temperature and bias current is also being investigated. A model extrapolating laser parameter drift as a function of detector operation time and position is under development.

c) Reliability tests of irradiated lasers and pin-photodiodes have been performed with devices operated for over 4000 hours at 80°C. Also, irradiated connectors have been subjected to repeated mate/demate cycles. Results suggest that only a minor fraction of the optical links is likely to fail during the lifetime of the experiment. Qualification tests on significant quantities of devices will take place during the pre-production phase of the project.

To have a better understanding of the volume costs of both analogue and digital optical links, the tendering process has been started for laser transmitters and connectors. Cost information will be available in the middle of 2000.

5. REFERENCES

OPTICAL LINK DEVELOPMENTS FOR THE CMS RPC

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Abstract

The rather general data link component testing and evaluation work done at the Helsinki Institute of Physics has become more and more focused on providing a working solution for the CMS RPC fibre optic trigger and data links. A new test board, LINX, has been designed to fill the specific needs of RPC links prototyping, including implementation of a data compression scheme. In this paper the LINX board is described in some detail, and a link solution based on commercial components available at the moment is proposed. Gamma and proton irradiation test results for some of these components are also presented.

1. INTRODUCTION

The CMS RPC muon detector system has almost 200,000 channels, but a very low occupancy. Significant savings on the number of high speed data links needed are possible using data compression and multiplexing.

As illustrated below in Fig. 1, the readout system is divided into the following components: Frontend Readout Board (FEB), which performs the digitisation of the data, Link Board (LB) containing synchronisation and data compression functions and the optical link. In the control room data from one link has to be split to several destinations to be forwarded to the Level-1 trigger by a Trigger Board (TB) or to the DAQ by a readout board (RB). At this end, too, the design will be modular, consisting of a separate link boards (TLB and RLB) with the decompressor and demultiplexer circuit DEMUX and the dedicated processor boards TB and RB.

The chambers will be served with different numbers of links according to their occupancy. Up to three chambers are connected to one link in the barrel, whereas in the endcap some relatively high occupancy chambers have two links per chamber. The first plan was to use one compressor circuit per chamber, but now it seems it may be possible to combine the data from up to three chambers in one LMUX, meaning that we would only need one kind of link board. This would add another multiplexing stage between the FEBs and the LBs, or alternatively we would have to accept a very

Fig. 1. Block diagram of the CMS RPC optical links
high pin count for the LMUX (3×96 inputs).

Presently it is envisaged to mount the link boards on two different locations on the muon chambers: the first four layers will be served with LBs in the space between muon stations MB/x/2 and MB/x/3, and the two outer layers with LBs on top of MB/x/4. Short LVDS links are needed to realise the connection between the frontend board and the link board. The synchronisation unit has only recently been moved away from the FEB to the LB, preliminary tests show the jitter levels introduced by this connection to be acceptable [1]. A detailed configuration for the endcap has not been proposed yet.

![Fig.2. The link boards will be mounted on the detector in two different locations for each sector](image)

2. CURRENT DESIGN BASELINE FOR THE RPC LINKS

2.1 Data Compression Scheme

The data compression scheme to be used is described in [2], only a short summary is presented here. The RPC chamber consisting of 96 strips is divided into 12 or 8 strip partitions. Only the non-empty partitions are sent, together with a partition number and a delay value. Two additional bits are added at the multiplexing stage of LMUX to denote the chamber number if data from more than one chamber are sent through one link. Flag bits are set if there is a cluster in between two partitions or if the data transfer is aborted because the maximum delay value has been reached. Very reliable operation is reached with a 24-bit data word, which would also leave one extra bit for error coding purposes, for example. With a partition size of 12, it would be possible to send the full raw data from the chamber in eight bunch crossings. The maximum delay value could then be set to around four bunch crossings (bx) for normal operation.

2.2 Components Chosen

The most suitable components available at the moment for our application are Gigabit Ethernet based serialiser/deserialiser chips which include data encoding for DC balance and which can be run at a variable bit rate, such as the AMCC S2061. In particular, we need to operate at a multiple of the LHC bunch crossing rate 40.08 MHz, and we plan to use a PLL component to multiply this by three. The bit rate of the link would then be 1.2 Gbit/s, or 120 Mbyte/s of data.

Commercial transceivers based on VCSELs and PIN diodes will be used for the electric-optic conversion and vice versa. They work with multimode fibre, and are relatively inexpensive even though they are bidirectional and thus include extra components not needed.

Two alternatives are being investigated for the splitter: Channel Link and regular LVDS line drivers/receivers at 120 MHz. The latter would mean that more cables are needed, but the overall solution would be more elegant as we would not have to include yet another multiplexing stage.

In case the commercial components we plan to use do not prove to be radiation tolerant enough, the submicron link being developed at CERN [3] would directly fit into our design. The CMS ECAL G-link [4], on the other hand, only allows a 16-bit word to be sent during a bx. A more efficient and more complicated data compression scheme would be needed to cope with this slower speed, as with the current scheme, a 3-bit data partition would have to be used, giving a 32 bx buffer for sending raw data. One such compression scheme is proposed in [5]. Another solution would be to try to clock the ECAL chip outside of its specifications at 60 MHz and send a 24-bit word in 1.5 bx, which would be very likely to cause synchronisation problems.

3. LINX PROTOTYPING ENVIRONMENT

3.1 Design Goals

The LINX test board has been designed as a higher speed replacement for a similar board described in an earlier paper [6]. The board can be used to study the characteristics of different link components and to evaluate their suitability for use in CMS data links. It can also be used in radiation tolerance tests to monitor, for example, single event effects during irradiation. Special attention has been paid to providing a programmable test bench for the CMS RPC fibre optic trigger and data links. Together with some additional hardware, the board can be used to replace the missing components of the RPC readout system during the development phase, and when the final link boards have been manufactured, it can serve as a programmable debugging device to facilitate their maintenance. All aspects of the CMS RPC data transfer can be studied with a modular test bench built from LINX boards and simple adaptor/driver daughter cards.

3.2 Specifications

LINX is a PCI board that can also be used in stand alone mode through either an RS-232 or a USB interface.
The key component on the board is Xilinx Virtex FPGA, containing from 50,000 to 800,000 logic gates and offering operating speeds well in excess of 100 MHz. Different size FPGAs having the same footprint will be mounted on the boards to test the functionality of the VHDL code for LMUX and LDEMUX and to find the optimum FPGA/ASIC size for their implementation. In the PQF package chosen for the board, the components have over 120 configurable pins in total.

Fig. 3. LINX board

The LINX includes an on-board fibre optic interface based on the AMCC S2061 serial backplane device and a commercial short wavelength optoelectronic transceiver component (VCSEL+PIN diode). The DSP is used mainly for interfacing purposes. There are also numerous connectors where daughter cards or other external inputs/outputs can be connected. Several different daughter cards were designed for the old version of the board, and these can also be used with the new board. Daughter cards exist for Gigabit Ethernet transceivers from different manufacturers and the HP G-link, among others.

3.3 Test Program

Initial synthesis results show that the RPC data compression and decompression algorithms can almost certainly be fitted into the Virtex FPGAs in their full versions and that there will also be some space left for additional test logic. Essentially all the features planned for the RPC data link can be realised on the LINX board, and we should have a proof of principle for the most important features of the data transmission by the end of the year.

For a realistic setup, the system clock can be replaced with a 40.08 MHz input from a TTCTR board via a lemo connector, and RPC-like test data can be generated in the DSP or a host computer and stored into a look-up table on the Virtex, where it can be cycled at the required speed.

Another crucial task to be carried out with a setup based on LINX boards is the single event effect (SEE) testing of link components and FPGAs. Fig. 4 shows an RPC readout chain realised with two LINX boards (a) and a radiation test setup with one board (b). In addition to fibre optic link components, Channel Link and other LVDS components will be evaluated.

3.4 Status of the VHDL Development

The VHDL code for the LMUX and LDEMUX is virtually complete, only some of the test functions still remain to be implemented.

Simulation results show that the decompression could be realised even with a Xilinx Spartan series 40k FPGA, whereas the multiplexer part of the compressor seems to require the highest speed grade Virtex. These results are worst case estimates, since they were obtained for a design which did not use any optimisation techniques specific for the Virtex components.

The choice between ASIC and FPGA should be made soon. A decisive factor for the transmitter will be the radiation tolerance of the Virtex FPGAs. At the receiving end, FPGAs will almost certainly be used.

4. IRRADIATION TEST RESULTS

4.1 Gamma Irradiation Tests

Gigabit Ethernet and Fibre Channel components from several different manufacturers (see Table 1 for details) have been irradiated to see whether they would stand the dose present at the CMS muon detectors and in the
cavern. The work was carried out at the 60Co irradiation facility at the Department of Radio Chemistry, University of Helsinki. The dosimetry was based on doses measured for water at certain distances from the source. Since the samples were placed close to the source, the amount of scattered radiation present on them could be minimised, and the silicon equivalent accuracy was around 20%. This was considered to be enough for these first tests.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
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<tbody>
<tr>
<td>TQ9501-MC</td>
<td>Triquint Fibre Channel Tx</td>
</tr>
<tr>
<td>VSC7135QN</td>
<td>Vitesse GE transceiver</td>
</tr>
<tr>
<td>CXB1589R</td>
<td>Sony GE transceiver</td>
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<td>VSC7115QJ</td>
<td>Vitesse GE Tx</td>
</tr>
<tr>
<td>HDMP-1022/HDMP-1024</td>
<td>HP G-link Tx/Rx chipset</td>
</tr>
<tr>
<td>S2061B</td>
<td>AMCC GE compatible transce.</td>
</tr>
<tr>
<td>S2046B/S2047B</td>
<td>AMCC GE Tx/Rx chipset</td>
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<td>VCSEL Transceivers</td>
<td>Honeywell HFM2450</td>
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<td></td>
<td>Siemens V23826-K305-C73</td>
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<tr>
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<td>HP HFBR-5305F</td>
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</tbody>
</table>

The estimated worst case dose at the RPC detector is 100Gy, and this was used as the basic dose in the tests. A significant number of components was irradiated to 200Gy and some up to 300Gy. Components were mounted on small circuit boards and were powered up. On the transceivers with optoparts attached, a fixed data pattern was fed to the transmitter side to modulate the laser. Functionality of the components was checked immediately after the irradiation where possible. More detailed measurements were carried out with the help of an oscilloscope within few hours of the irradiation, after which many of the samples were put through an accelerated aging test at 100°C for one week.

No significant changes were observed in the operating current or functionality of any of the components neither immediately after the irradiation nor after the accelerated aging test. The biggest change in operating current, ΔI=70mA, was observed for the HP G-link components, for which the operating current increased from 880 mA to 920 mA after the irradiation and one month later, when the radioactivity of the samples had gone down to a more acceptable level. The only noticeable change occurred for the HP G-link components, for which the operating current increased from 880 mA to 920 mA after the irradiation and to 940 mA one month after the irradiation.

4.2 Proton Irradiation Tests

The sensitivity to displacement damage of the optoelectronic and bipolar components was investigated with protons. The proton irradiations were carried out with 75 MeV protons from a multicusp ion source at the University of Jyväskylä K130-cyclotron. The beam current was 180 pA, and the samples were all irradiated to a total dose (fluence) of 5×10^7 ncm⁻². The beam current was measured by a Faraday cup in the beam line. Fluence was measured by a set of four collimated CsI(Tl) scintillators with PIN diode readout, situated in front of the beam entrance to the vacuum chamber where the devices under test were placed. A more detailed description of the irradiation facility can be found in [7].

As with the gamma irradiation studies, no change was observed in the functioning of the components, or their operating current. The current was measured before and after the irradiation and one month later, when the radioactivity of the samples had gone down to a more acceptable level. The only noticeable change occurred for the HP G-link components, for which the operating current increased from 880 mA to 920 mA after the irradiation and to 940 mA one month after the irradiation.

Altogether the results from both kinds of irradiation test look promising: total dose or displacement damage effects are not likely to be a problem on the CMS muon detectors for the components we have chosen. In a way the results were also disappointing, since we were not able to exclude any of the components with these simple tests. It has to be noted, though, that the sample sizes were rather small (2-3 pieces of each component for the gamma irradiation and 1 piece of each component for the proton irradiation).

In addition to the link components, one Virtex XCV300 FPGA was also irradiated with protons to see whether it would suffer any permanent damage. We have not yet analysed the results.

The next step is to do single event effect tests. For technical reasons, it has been decided to perform the latchup and SEU tests with protons, which at energies above 20 MeV behave in a very similar way to neutrons, with possibly a neutron irradiation in a reactor to check for the effects of low-energy neutrons. Another reason that supports the use of protons rather than neutrons is that preliminary calculations show charged hadrons to dominate the SEU rate even in the CMS cavern, where they form only 1% of the total hadron flux [8].

The plan is to perform latchup measurements for different proton energies to establish the LET of the components, and SEU tests for the serdes components and Virtex FPGAs with the help of the LINX board. The FPGA configurations needed for these tests are under preparation.

5. CONCLUSIONS

The full RPC data transmission chain is to be built this year with LINX boards. This highly modular setup is very suitable for testing the data compression and multiplexing scheme, signal splitting at the receiver end and the overall integrity of the proposed solution.

In the first irradiation tests we were unable to exclude any of the candidate components on the basis of a poor radiation tolerance. It is to be stressed, however, that the
results are very preliminary and single event effect tests are still to be done. The sample size was also rather limited. More tests, concentrating on the components we have chosen for our baseline design, will be carried out soon.

References

Acknowledgements
We would like to thank Mika Huhtinen, Pertti Aarnio, Pierre Jarron and Federico Faccio for their help with planning the irradiation tests, Prof. Timo Jaakkola and Laboratory Manager Martti Hakanen of the University of Helsinki Radiochemistry Department, and Prof. Juha Äystö and Dr Ari Virtanen of the University of Jyväskylä Accelerator Laboratory, for the permission to use their facilities and their help.
Radiation Hard Optical Links for The ATLAS SCT and Pixel Detectors.

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Abstract

A full study of the optical readout package for the ATLAS SCT/Pixel detector data transmission is presented. Radiation hardness studies of VCSEL emitters, Epitaxial Silicon PIN diodes receivers and their associated chips have been carried out with fluences higher than $10^{13}$cm$^{-2}$ 1 MeV neutron equivalent and total ionising doses of 10 Mrad. The reliability was assessed by testing a large number of devices and accelerated ageing tests were also pursued over a period equivalent to more than the LHC operation time. Single Event Upset and magnetic field studies up to 6T have also been done on a new optical package design with positive results.

1 The Readout Architecture

The architecture and the overall performance of the optical readout to be used for reading out the ATLAS SCT/Pixel is described in [1, 2, 3]. For the SCT, a schematic view is represented in figure 1. Data will be readout by two fibres each transferring data at 40 Mbits/s. The Timing, Trigger and Control (TTC) data for each module will be distributed to the modules by optical fibre. Bi-phase Mark encoding will be used to encode the control data on top of the 40 MHZ bunch crossing clock. Similar architecture will be use for the Pixel detector but with a higher data rate of 80 Mbits/s.

![Figure 1: A schematic diagram of the ATLAS SCT links.](image)

The links are based on radiation-hard VCSELs and PIN diodes. The radiation hardness of these components is discussed in the following sections. The VCSEL will be driven by a VCSEL Driver Chip (VDC) and the PIN diode output is processed by the Digital Optical Receiver Integrated Circuit (DORIC) chip. The chips have been designed in the AMS 0.8 µm BiCMOS process. This is not usually used as a radiation hard process but a radiation hard design has been obtained by:

- using bipolar npn transistors only;
- operating the transistors with relatively large currents such that the DC current gain $\beta$ is large and less sensitive to radiation damage;
- using a design in which the circuits are very insensitive to changes in $\beta$. 
2 The opto-package

A radiation-hard, low mass, non-magnetic package containing two VCSELs and one PIN diode has been produced by Marconi. As seen on figure 2, the concept is based on a silicon baseplate on a ceramic tile where the PIN diode is mounted. The VCSELs are mounted on separate ceramic tile set on the silicon baseplate. An aluminised silicon mirror is used to turn the light from the vertical to the horizontal direction. The fibres are placed in v-grooves in a separate silicon lid which fits onto the silicon base. The use of a mirror gives some flexibility in the process of positioning the opto-components on the baseplate.

The opto-package will be mounted on a flex rigid support which also contains the VDC and the DORIC chips. The support allows for electrical connection to the SCT module and to connect to the low mass aluminium tape carrying the DC voltage.

3 Radiation hardness of the Package components

The radiation hardness of the optical fibres have been already studied and their results presented in the previous workshop [4].

3.1 The DORIC/VDC chips

Twenty DORIC chips have been irradiated to a total ionised dose of 100 kGy with a Co$^{60}$ source and a neutron beam to a total flux of 3×10$^{14}$n.cm$^{-2}$. No significant degradation was observed after irradiation. The chips were powered during the gamma irradiation. Nine VDC chips are under similar studies.

3.2 The MITEL VCSELs

Four VCSELs from MITEL$^1$ in ST packages have been irradiated up to 2.9×10$^{15}$n.cm$^{-2}$. The L-I curves before and after the irradiation are shown on figure 3. They were annealed during a short period of 3 weeks at the optimal 20 mA current. The low signal of one of them is due to a physical damage during the handling. A reasonable shift in the laser current threshold will not affect the performance of the VCSEL.

![Light-output vs current for nonirradiated and irradiated VCSEL MITEL 1A444](image)

Figure 3: L-I curves before and after irradiation.

Important reliability plots from manufacturers exist on un-irradiated VCSELs. Reliability studies on irradiated devices have been done on a sample of 20 irradiated VCSELs to a fluence of 4×10$^{14}$n.cm$^{-2}$. Ageing tests have been performed at an elevated temperature of 43°C. By considering an acceleration factor given by the Arrhenius law, and for an activation energy of 1 eV, an estimated accelerated period of 3768 ATLAS-years has been achieved. This result confirms the reliability of such an optical emitter even after irradiation.

3.3 The CENTRONIC epitaxial silicon PIN photodiodes

Ninety six epitaxial silicon PIN photodiodes$^2$, operating at the 850 nm wavelength of the VCSEL, have been irradiated with neutrons and protons during the last year. Previous study has shown that these photodiodes were sufficiently radiation hard$^3$. Three different levels of irradiation have been carried out, some of them at the -8°C SCT operational cold temperature, from 1.5×10$^{14}$n.cm$^{-2}$ to 1.05×10$^{15}$n.cm$^{-2}$ 1 MeV equivalent fluence. After a decrease of the responsivity at relative low fluence, there was no further degradation observed at higher levels as seen in figure 4. The final value of 0.3 A/W is adequate for

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1 MITEL VCSEL 1A444
2 GEC-Marconi part no 520 /1/02603/001
the optical readout. For the highest integrated neutron dose, the dark current is 60 nA at room temperature, decreasing to a negligible value at the cold temperature of the Inner Detector.

![Plot](image)

**Figure 4:** Distribution of the 96 PIN photodiodes responsivities at different irradiation level.

Figure 5 shows that the bias needed to obtain the full responsivity of the PIN diodes after an irradiation above $10^{15}$ n.cm$^{-2}$ is about 8 V. The rise/fall time at 5V is less than 1 ns and does not change with different irradiation dose levels.

![Plot](image)

**Figure 5:** Normalised responsivities of the PIN photodiodes as a function of the bias at different neutron cumulative doses.

An accelerated aging test was performed on ninety six components by using an elevated temperature of 60°C. The acceleration factor was calculated for an active energy of 0.6 eV as quoted in [6]. The estimation of a lower limit on the Mean Time To Failure after 3978 h of ageing, with no failure recorded, is more than 2720 years at 90% Confidence Level. This means less than 8 failures among 2112 for the SCT barrel and less than 53 for the Forward, which has a higher temperature of 15°C, for the 10 ATLAS-years.

### 4 Magnetic Field Study

Studies on the complete package itself placed in the equivalent 2T Inner Detector magnetic field have also been done. A superconducting magnet was used to create a magnetic field up to 6 T. Three different angles, between the package axis and the magnetic field steering, from 0 to 60° have been tested. As seen in the figure 6, no degradation was observed.

![Plot](image)

**Figure 6:** The package performance under different magnetic field value and positionning.

### 5 Single Event Upset

Single Event Upset (SEU) studies have been performed using an ionising source and neutron beams. By using a Sr$^{90}$ source with β flux of $4.3 \times 10^{7}$ cm$^{-2}$s$^{-1}$, no increase of the Bit Error Rate (BER) was observed. One test with a 9 MeV neutron beam at the Birmingham cyclotron with a fluence of $2 \times 10^{9}$ n.cm$^{-2}$s$^{-1}$ caused no increase of the BER. With a 14.7 MeV neutron beam energy and a flux of $1.07 \times 10^{7}$ n.cm$^{-2}$s$^{-1}$, increase BER was observed as seen in the figure 7. The BER decreases as the optical power at the entrance of the package increases. We can deduce that the source of SEU is the PIN photodiode receiver which has the largest Si area. With the right optical power, an acceptable BER is obtained at the SCT level. But the problem need to be evaluated for the higher flux of $4.5 \times 10^{7}$ n.cm$^{-2}$s$^{-1}$ expected in the Pixel detector. A test with pions beam have been scheduled for next year.
the 2T magnetic field of the Inner Detector. Single Event Upsets were observed at high neutron flux and could be reduced to an acceptable level at the flux expected in the SCT. Sixty packages are in production. Once they are evaluated, they will be integrated in a complete system test of the SCT.

8 Acknowledgment

We would like to thanks all the different technical staffs from all irradiation facilities: ISIS at Rutherford (UK), Ljubljana reactor (Slovenia), the National Physical Laboratory in London and the CERN PS accelerator (Switzerland).

References


6 Off-detector component

VCSELs and PIN arrays will be used in the off-detector electronics. A suitable candidat has been provided by MITEL$^{3}$ where the components are mounted in MT packages. A good uniformity of the VCSELs signal have been measured as shown on figure 8. The measurements of the PIN diode arrays show a responsivity greater than 0.5 A/W and rise and fall times less than 1 ns.

Figure 8: LI curves from 4 MITEL VCSELs array.

7 Conclusion

Radiation hardness tests of the individual components of the ATLAS SCT/Pixel opto-package have been performed, showing no major degradation for each of them. The global package is unaffected by

$^{3}$MITEL 4 VCSEL array: 4D469, MITEL 4 PIN array: 4D468
An amplifier with AGC for the 80 Mbit/s Optical Receiver of the CMS digital optical link

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Abstract

An 80 Mbit/s amplifier has been developed for the optical receiver of the CMS tracker control link. Four channels of the circuit have been integrated in a 0.25 µm commercial CMOS process using radiation tolerant layout practices to achieve the required radiation tolerance. An Automatic Gain Control (AGC) loop allows for detection of wide dynamic range input signals (10 µA to 500 µA photocurrent) with minimum noise, compatible with the maximum expected radiation-induced drop in quantum efficiency of the PIN photodiode. A second feedback loop compensates a photodiode leakage current up to 100 µA.

1. INTRODUCTION

The CMS tracker control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals [1]. These digital signals, transmitted serially at a bitrate of 40 Mbit/s (80 Mbit/s for the clock signal), will be converted into electrical signals by a PIN photodiode at the receiver end. As one of the transmission channel ends will sit inside the CMS detector, hence in a radiation environment, its components need to be radiation hard.

The front-end element of the optical receiver is a transimpedance amplifier, which has to amplify the photocurrent delivered by the PIN diode and detect the presence of a reset signal, coded in the foreseen protocol as missing pulses for more than 2 µs. In the CMS control system, the PIN diode is a commercial component and its performance will be affected by radiation. To compensate for the radiation-induced degradation of the photodiode quantum efficiency, the amplifier should have a wide dynamic range (current signals between 10 and 500 µA). Moreover, it should be able to compensate a photodiode leakage currents of up to 100 µA.

The amplifier circuit has to be radiation tolerant up to a total integrated dose of 10 Mrad. As no commercial amplifier satisfying all these conditions exists, the development of an ASIC was necessary. To meet all the specifications, a commercial 0.25 µm CMOS technology has been chosen for the development of the amplifier. This advanced technology allows to easily meet the speed requirements with minimum power consumption: the bandwidth of 80 MHz can be achieved without large currents, resulting in a power consumption below 25 mW per channel at the nominal voltage of 2.5 V.

Moreover, the thin gate oxide of this deep submicron process is inherently total dose hard, and the systematic use of enclosed (edgeless) NMOS transistors and guardrings allows the design of circuits with radiation tolerance exceeding the specified 10 Mrad [2]. Such design techniques have also been demonstrated to significantly increase the Single Event Latchup (SEL) immunity of the circuit [3].

2. CIRCUIT DESCRIPTION

The global architecture of the amplifier circuit is shown in Figure 1, and it is mainly composed of four blocks: a transresistance preamplifier, a chain of limiting gain amplifiers, an LVDS driver and a block to detect and generate the reset signal.

Figure 1: Global architecture of the amplifier circuit, DC connected to the external PIN diode. The transresistance preamplifier is followed by a chain of limiting amplifiers (L.A.), where a Balancing Feedback (B.F.) block ensures that the average of the two differential signals is identical.
The PIN diode is DC coupled to the preamplifier, which also supplies the bias voltage to the photodiode (about 1.8 V). This solution also allows for an easy integration of a feedback loop to sink the radiation-induced leakage current of the photodiode.

2.1 The preamplifier

The architecture of the preamplifier is shown in Figure 2. The transresistance amplifier transforms the current signal from the PIN diode into a voltage signal, with a variable transresistance. This sort of Automatic Gain Control (AGC) is necessary to cope with the large dynamic range required for the amplifier, from 10 to 500 µA current signals. The high gain on small signals, desired for high signal over noise ratios, is in fact incompatible with the big signals because the voltage excursion at the preamplifier output is limited. The presence of an AGC mechanism, other than ensuring a constant output signal irrespective of the input current, allows for optimum noise performance: maximum gain (maximum transresistance), hence minimum noise, is used for small signals.

The AGC is implemented by a transistor in parallel with the 16 kΩ polysilicon resistance, having its gate voltage controlled by a slow feedback loop. The AGC loop is actually a minimum detector followed by a slow transconductance amplifier acting as an integrator. For high input currents, this block detects a minimum signal below a fixed reference voltage and decreases the transresistance by acting on the feedback transistor gate. This feedback loop needs to be slow so as to be negligible at the signal frequency, as it needs only to compensate for the radiation-induced drop in the quantum efficiency of the photodiode. Such drop occurs during the whole LHC life cycle (10 years). The simulated transfer function of the preamplifier is shown in Figure 3, for both high and low signal levels. The transresistance changes from about 16 kΩ for a 10 µA signal to about 175 Ω for a 500 µA signal. Correspondingly, the bandwidth passes from 105 to 858 MHz.

Figure 3: Transfer function of the preamplifier.

The single ended architecture chosen for the preamplifier front end allows the correct biasing of the PIN diode but, as all single ended structures, has an inherently poor Power Supply Rejection Ratio (PSRR) compared to differential architectures. To improve this important characteristic, a pseudo-differential scheme has been used. The transresistance input stage has been replicated as a “dummy” circuit, as shown in the upper part of Figure 2. The output of both the true preamplifier and the dummy stage is used as the input to the differential limiting amplifier chain. Therefore, from the preamplifier output to the LVDS driver output, the signal is fully differential.

This pseudo-differential scheme requires good matching between the input capacitance of the true and dummy branches. To match the PIN diode capacitance, we have integrated a dummy capacitance at the input of the dummy branch. Its value has been chosen to match as well as possible the capacitance of the PIN diode after irradiation. In this way, the PSRR of the preamplifier will improve during operation, and finally be optimum when the signal delivered by the photodiode is at its minimum.

The output of the dummy circuit is moreover used as an input to the additional feedback loop controlling the photodiode leakage current sink. Two peak detectors, sampling the output signal from the true and dummy branches, and a slow transimpedance amplifier form the leakage control circuit, as shown in Figure 4. In the presence of a photodiode leakage current, the output maximum of the true branch tends to decrease. This decrease is detected by the leakage control circuit, which then acts on the gate of the sink NMOS transistor to drive the leakage current to ground and re-establish the
equilibrium condition. As for the Automatic Gain Control, the leakage control feedback needs to be very slow compared with the lower signal frequency. In fact, this circuit has to compensate for the increase in the photodiode leakage current, which is a slow radiation-induced process occurring during the whole LHC life cycle.

Figure 4: Architecture of the Leakage control block.

2.2 The limiting amplifier chain

The output of the preamplifier is not fully differential, the signal coming from the dummy branch being DC. The first limiting amplifier of the chain needs therefore to be unbalanced for its output signal to be fully differential. This is implemented through the action of a “balancing” feedback block, as shown in Figure 1. This circuit block senses the peak of the output signals from the second amplifier of the chain, and controls the current unbalance between the two output branches of the first amplifier. The amplifier chain performs an amplification of the signal and limits it to a pre-fixed peak-to-peak value, preparing it for optimum input to the LVDS driver.

The four amplifiers composing the chain are differential gain stages with diode-connected transistors as loads to limit the signal excursion. To linearize their output signal, a polysilicon resistance has been added between the two branches of each amplifier.

2.3 The LVDS driver

The specifications of the circuit require the output to be Low Voltage Differential Signaling (LVDS). LVDS is a high speed, low power general purpose interface standard using differential data transmission, and it is independent of a specific power supply [4]. The standard peak-to-peak signal is 400 mV, and the common mode voltage is 1.2 V. To generate the differential output voltage, a termination resistor (typically 100 Ω) is required at the receiver end.

The LVDS driver has been designed as a differential amplifier with load resistors. The use of resistors as loads achieves good signal linearity, and helps matching the impedance requirements of the driven transmission line. To correctly generate an LVDS signal, the value of the load resistors has been designed to be 275 Ω, with 4.7 mA current flowing in each branch. Such resistors have been integrated as high precision p-diffusion resistors (10% spread). The speed performance of the designed driver is well above the required 80 Mbit/s.

2.4 The reset block

The transmission protocol foresees that the reset signal is coded as missing pulses for a long time period (2 µs or more) [5]. The amplifier circuit is required to detect the transmission of the reset and respond to it by changing the status of a flag on a dedicated output line.

Figure 5: Architecture of the reset block.

To perform this task, we have integrated a reset block in the amplifier, connected to one of the differential outputs of the limiting gain amplifier chain as shown in Figure 1. The schematic of the reset block is depicted in Figure 5.

The input of the reset block is connected to a peak detector sensing the maximum of the signal. The output of the peak detector is compared with a reference voltage through a symmetrical operational amplifier. In the absence of a signal, the voltage at node A decreases with a time constant fixed by the value of the capacitance and of the current in the peak-detector circuit. If the absence of the signal is long enough, the voltage of node A eventually goes below the voltage of node B, and the output of the reset block changes.
3. CIRCUIT IMPLEMENTATION

3.1 Chip floorplan

The final ASIC includes 4 amplifier channels, each occupying an active area of 0.5x0.25 mm\(^2\). A picture of the chip is shown in Figure 6. The vast majority of the chip area is unused, the die size of 2x2 mm\(^2\) having been assigned to this circuit in the mainframe of a multi-project run. The distance amongst the pads has been chosen to be compatible with wire-bonding and low cost bump-bonding techniques. Input pads are on the left of the chip, LVDS output pads on the right, and the power is distributed along the y-axis with pads on both the top and bottom of the chip.

![Figure 6: Layout view of the amplifier chip.](image)

3.2 Radiation tolerance considerations

The total dose tolerance of the extremely thin gate oxide of transistors in the quarter micron technology used is well beyond the specified 10 Mrad level. Threshold shifts as low as 35 mV (for NMOS) and -70 mV (for PMOS) have been measured after an irradiation up to 30 Mrad [6]. Changes in mobility, transconductance and noise are also very limited after such a high total dose, always below 10%. Those radiation-induced changes are lower than the manufacturing spread in the same parameters. Therefore, the typical design procedure of varying the process parameters in the ±3\(\sigma\) range should be sufficient to ensure the correct functionality of the circuit even after irradiation.

Special attention has been devoted to avoid possible leakage paths under the still thick lateral and field oxides. Enclosed layout geometry has systematically been used for NMOS transistors to prevent source-drain leakage currents. Moreover, all n+ diffusions at different potential have been isolated from each other by a p+ guardring completely surrounding it. Both techniques have been shown to be very effective [6,7], and the use of guardrings has the additional advantage of decreasing the Single Event Latchup (SEL) sensitivity of the circuit [8]. Robustness against Single Event Upset (SEU), which can generate errors in the transmitted data path, is embedded at the system level through the use of an adequate transmission code allowing error detection and correction (EDAC).

4. SUMMARY

We have developed an 80 Mbit/s amplifier for the optical receiver of the CMS tracker slow control optical link. The use of a commercial quarter micron CMOS process enables us to meet the speed, low power and radiation hardness specifications for the amplifier. We used enclosed layout topology for all NMOS transistors, and guardrings to achieve the required level of total ionising dose tolerance.

The front-end of the circuit, a transimpedance preamplifier, has been designed to compensate for the radiation-induced performance degradation of the PIN photodiode: decrease in the signal amplitude and leakage current increase. AGC has been implemented to achieve optimum signal-over-noise ratio on both high and low level signals, corresponding to the maximum and minimum foreseen quantum efficiency of the photodiode. A feedback loop monitors the PIN diode leakage current and can compensate for its increase up to 100 \(\mu\)A.

Imbedded in the amplifier is a sub-circuit to detect the transmission of a reset signal. Upon detection, a flag is enabled on a dedicated output line.

REFERENCES

ABSTRACT
Several LHC detectors require high-speed digital optical links for data transmission in both data readout and trigger systems. Commercial components can be found that meet the bandwidth requirements of most of the LHC detectors subsystems. However, they fail to meet some of the requirements frequently encountered in the LHC-HEP environment, namely: resistance to high radiation doses and operation tolerant to single event upsets. To address these problems, a high-speed transmitter ASIC (1.2Gbit/s), containing a serializer and a clock multiplying PLL was developed. The prototype was implemented in a mainstream 0.25um CMOS technology and was designed using well-established radiation tolerant layout practices to achieve resistance to high radiation doses. This implementation serves as a base for the development of radiation tolerant IC’s that will make feasible the transmission of data using common local area networks protocols in typical LHC radiation hard environments.

The ASIC was embedded in a test setup that uses a commercial optical receiver and de-serializer. Error free data transmission at 1.2Gbit/s was achieved proving the prototypes to be fully functional.

1. INTRODUCTION
Several LHC detectors require high-speed (~ Gbit/s) digital optical links for transmission of data between the different sub-detectors and the data acquisition systems. Typically, high-speed data transmission is required for both the trigger systems data path and the data readout systems. In general, those links will be uni-directional with the transmitters located inside the detectors and the receivers situated in the control rooms. In this arrangement, the transmitters will be subject to high levels of radiation doses over the lifetime of the experiments. Additionally, the large numbers of high-speed optical links planned (of the order of 100K total for the four LHC experiments) impose strict constraints on both the cost and power dissipation allowed per device in the system. Moreover, in trigger links, data has to be transmitted with constant latency and synchronously with the LHC 40.08MHz reference clock - this to facilitate data alignment at the receiving end before the data is feed to the trigger processors. In other words, high-speed optical links for the high-energy physics environment require:
- hardness to total dose radiation effects (up to 10Mrad in some cases);
- operation tolerant to SEU;
- low power dissipation;
- low cost;
- and, in trigger systems, constant latency (synchronous) transmission.

Commercial optical links and components can be found that meet the bandwidth requirements of all of the planned systems. However, they fail to meet one or several of the requirements mentioned above.

To address these problems, high-speed radiation hard transmitter IC’s will have to be developed. In this paper, the feasibility of such an IC employing radiation tolerant layout practices in a mainstream sub-micron CMOS technology is assessed. A prototype has been developed and it is here described. It incorporates the most critical functions of a high-speed transmitter. It includes: a serializer that transforms 10-bit parallel words into a 1.2Gbit/s (or 1.25Gbit/s) serial bit stream, a clock multiplying PLL that generates the internal 1.2GHz (or 1.25GHz) clock from the 40.08MHz LHC clock and an high-speed 50Ω (PECL like) driver that allows the chip to interface with most common optical transmitters. The IC features a low operation voltage (2.5V) contributing to low power consumption. The prototype was conceived having in mind data transmission in trigger systems, thus allowing synchronous transmission of data at rates compatible with the LHC bunch-crossing frequency. However, the operating data rate and the data framing to be implemented have been chosen close to the industrial Gigabit Ethernet standard so that the transmitter can also be operated at a standard data-communications frequency (1.25Gbit/s) permitting testing using commercial equipment. Additionally, this will allow the IC to be used in conjunction with standard chip-sets for applications were synchronous transmission is not essential, e. g. event building, thus enlarging the users choice and allowing for flexible system development. Since data transmission will be encapsulated in an 8B/10B line-coding scheme, this will result in an effective data rate of 960Mbit/s when the transmitter is operated in the synchronous mode at

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1.2GHz (30 times the LHC clock frequency). In this mode, if the 8B/10B encoding is used, the user can thus transmit 24 bits every LHC bunch crossing. For asynchronous operation, a 1Gbit/s effective data bandwidth can be achieved if the standard 1.25GHz clock frequency is used.

In what follows, the architecture of the high-speed serializer, its main circuit details and the considerations that have lead to the particular implementation will be addressed.

2. Serializer Architecture

CMOS serializers capable of Gbit/s data rates have been widely reported in the literature (see for example [1] and [2]). In its most simple expression, a serializer is a shift register, clocked at the bit rate frequency that is periodically loaded with the data words to be serialized. Since a parallel-load shift register is usually composed of a cascade of D-flip-flops and of two-to-one multiplexers, the maximum achievable operation frequency is limited by the sum of the flip-flop clock to output propagation delay, the flip-flop setup time and the multiplexer propagation delay. For 1.25Gbit/s operation, the sum of those critical timing parameters has to be less than 800ps. For the sub-μm CMOS process used, the propagation delay and the setup time are given in Table 1 for a dynamic (DFF) and a static (SFF) flip-flop. Also shown in the table is the propagation delay of a two-to-one multiplexer. The reader should note that the propagation delays given here are slightly higher than what would normally be expected from a 0.25μm CMOS technology. This is a consequence of using enclosed transistor geometries to achieve radiation tolerance [3]. This technique introduces slightly higher capacitances in the signal path, resulting in circuits with relatively higher propagation delays.

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</table>

Table 1 Clock to output delay (tpd) and setup times (lud) for dynamic (DFF) and static (SFF) flip-flops. Also shown, two-to-one multiplexer propagation delay. Only typical and worst case process corners figures are given.

As can be inferred from Table 1, reliable operation of the simple shift register structure can not be guaranteed at 1.25Gbit/s under all process, power supply and temperature conditions using static flip-flops. To ensure this would require the use of the dynamic flip-flops. However, the operation of this type of flip-flops relies on the storage of charge in high impedance nodes during certain phases of the operation. This renders the dynamic flip-flops particularly sensitive to single event upsets (SEU) [4], a characteristic that is highly undesirable in radiation environments. Using static flip-flops to implement a 1.25Gbit/s serializer that will operate reliably under all process, temperature and power supply conditions requires thus the departure from the simple shift register structure. By looking at the numbers in Table 1, it can be seen that the SFF can be used to build a shift register that operates up to 770MHz under all conditions. This leaves enough room to implement a serializer where the parallel data word is split in two groups of bits that are shifted in two independent shift registers each operating at 625Mbit/s. If the shift order of the parallel data bits is properly selected and the two serial bit streams combined using a single fast multiplexer a 1.25Gbit/s serializer is obtained. This was the architecture adopted in this development because it avoids the need to use dynamic flip-flops and reduces the clocking frequency to half.

The implemented ASIC (whose block diagram is shown in Figure 1) operates as follows. The external 20-bit wide bus accepts parallel data at a rate of 60MWords/s. This data is time division multiplexed by the “Word Mux” into two 10-bit words which are then feed to the “10-bit Serializer” at a rate of 120MWords/s. Then, the serializer - as discussed before - converts the 10-bit words into an 1.2Gbit/s serial stream. Finally, the data out of the serializer is passed to the “50 Ω Output Driver” that converts the internal CMOS levels into Pseudo-ECL (PECL) levels to allow interfacing of the ASIC with commercial optical transmitters. The operation, as described above, requires several clocks and control signals at different frequencies. These are generated in the IC by the Phase-Locked-Loop (PLL) and the “Clock Generator” circuit. For operation at 1.2Gbit/s, the PLL takes as its reference the 40.08MHz LHC clock. (or a 41.66MHz clock for operation at 1.25Gbit/s) and compares it with its output signal divided by the “Clock Generator” by a factor of 30. In this way, a 1.2GHz clock is obtained at the PLL output. The “Clock Generator” provides the 60 and 120MHz clock signals required by
the “Word Multiplexer”, the 600MHz clock and the “load” signal needed by the high-speed serializer. The implemented IC as described here does not allow transmission at the reference clock rate. This would require the implementation of 30-bit to 10-bit word multiplexer. This was not done in the prototype to avoid a high penalty in silicon area due to a highly pad limited layout. However, data transmission at the reference clock rate can be easily obtained by the addition of simple external logic.

2.1 The High-Speed Serializer

The high-speed serializer is portrayed in some detail in Figure 1 and its operation can be described in the following way. Each “word-clock” cycle a 10-bit word from the “Word Multiplexer” is loaded into the “Register”. The output of this register is separated into two 5-bit words and loaded, some time later, into two 5-bit shift-registers (SR’s). As shown in Figure 1, splitting of the 10-bit word is done in such a way that adjacent bits are loaded into different SR’s. The output of one of the shift-registers (SR-1) drives one input of the output multiplexer while the other one (SR-2) drives a latch. This latch drives the other multiplexer input and its purpose is to delay the data shifting operation by half a clock cycle in relation to the output of the first SR. Since the select input of the output multiplexer is driven by the shifting clock (600MHz), it correctly selects between adjacent bits and constructs the desired 1.2Gbit/s bit stream. This is represented schematically in the timing diagram of Figure 3.

It should be clear that in this scheme the duration of each bit in the final 1.2Gbit/s serial stream depends on the duty-cycle of the shifting clock. That is, if the clock duty cycle is distorted the final serial data will have bits whose width will depend on the duration of the selecting level. This is of course undesirable since it translates into jitter in the transmitted data having potential ill effects on the clock and data recovery circuitry of the associated receiver. Note also that the same effect will occur if an unbalance exists in the output multiplexer. To avoid these situations two actions have been taken. First, the 600MHz-shifting clock is obtained by dividing the 1.2GHz VCO clock by two. In this way, a nearly 50% clock is obtained. This scheme has the obvious disadvantage of requiring a full speed running clock. However, this is only true for two components: the VCO and the divide-by-two flip-flop. Second, the multiplexer output data can be sampled by a flip-flop driven by the 1.2GHz clock to avoid both the effects of clock duty-cycle distortion and multiplexer asymmetry.

2.2 The Clock Generator

In the clock-generator circuit (Figure 4) the word-clock (120MHz), the bit-clock (600MHz) and the load signals for the shift registers are generated from the 1.2GHz PLL.
clock signal. The VCO clock is divided by two by a flip-flop and then again by five by a "ring" divider to obtain a 120MHz signal. The "ring" divider circulates a "one" and four "zeros". From this circulating "one" the load signal is directly obtained while the word-clock is produced by a SR flip-flop sensing the circulating one. The 120MHz clock after division by three is fed to the PLL where its frequency and phase are compared with the LHC 40MHz-reference clock.

2.3 The Phase-Locked-Loop
The PLL implemented in the ASIC uses a classical structure. It employs a three-state phase frequency detector, a charge pump, an RC loop-filter and a differential VCO with symmetrical loads [6], [7]. In this design the loop jitter and the sensitivity to the power supply noise were considered of major importance. Since the PLL and clock-divider multiply the reference clock by 30 a corrective action is only taken every 30 VCO cycles. To obtain a "jitter-free" clock signal, it is thus important to minimize the noise contribution of the VCO itself. In this design the VCO is composed of three differential cells. To reduce the VCO cycle-to-cycle phase noise to about 2ps a current of 1.1mA biases each cell. Behavioral level simulations were made that take into account the intrinsic VCO noise and the reference signal noise. From these simulations, assuming a reference signal with 160ps RMS jitter (1.1ns pp) the PLL is expected to generate a 1.2GHz clock with an RMS jitter of the order of 34ps RMS (232ps P-P).

3. TEST SETUP

![Figure 5 Serializer ASIC test-card block diagram.](image)

A test-setup has been developed for the serializer ASIC. The block diagram of the transmitter side of the setup is depicted in Figure 5. It consists of the serializer ASIC, an FPGA, a clock generator and an optical transmitter. To avoid the use of a special package to house the serializer – due to the high frequencies involved – the ASIC is directly bonded to the PCB. The reference clock to the IC and the FPGA device is provided either from an external source or from an on board 40MHz-clock generator. The ASIC interfaces with the optical transmitter through a 50Ω transmission line that can also be used to drive the serial signal out of the board for electrical measurements. The role of the FPGA device is threefold: it is used to program the serializer test configuration, it monitors the serializer’s PLL locking state and it generates the test data patterns to be serialized. At the receiver end of the test setup a commercial receiver is used to de-serialize the incoming data and check for transmission errors.

4. EXPERIMENTAL RESULTS
At the time of writing, the IC’s had been received from the manufacturer only a few days before. This made it impossible to present here a complete set of measurement results. Nevertheless, tests were made on prototypes that proved the design to be fully functional. An eye-diagram of the electrical output signal is shown in Figure 6 (top trace). This eye-diagram was obtained during the transmission of a 256-bit long pseudo random bit sequence at 1.2Gbit/s. The measurement was made using an “HP CSA803” Communications Signal Analyzer with a SDL4 sampling head (17.5ps rise time). The jitter numbers are given in Figure 6 together with the details of the measurement (bottom trace and histogram).
5. CONCLUSION

In this paper a 1.25Gbit/s serializer for use in HEP data and trigger links as been presented. The serializer was implemented in a 0.25µm CMOS technology using radiation tolerant layout techniques. The ASIC layout is pad-limited having a 4mm² footprint area. The implementation constraints imposed by the radiation environment on the circuit design were addressed and the circuit architecture was discussed in detail. Two samples were tested and proved to be fully functional. The experimental results presented here constitute a small fraction of the tests required. To qualify the IC for use in the different LHC radiation hard environments, total dose and single event upset radiation tests are now in preparation. Future developments will be focused on system functionality, external interface and link protocol.

References


STATUS OF THE RD48/ROSE COLLABORATION

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Abstract

The status of the RD48 or ROSE (R&d On Silicon for future Experiments) Collaboration is described.

1. INTRODUCTION

This paper describes the work of many groups working within the RD48 or ROSE Collaboration with the specific objective of defect engineering more radiation tolerant silicon detectors [1,2]. Defect engineering involves the deliberate addition of impurities to silicon in order to effect the formation of electrically active defect centres and thus control the macroscopic parameters of devices. The key ingredients to change are oxygen and carbon. Oxygen and carbon capture silicon vacancies and interstitials respectively. The carbon is converted from a substitutional to an interstitial position which is mobile at room temperature. It eventually forms stable defects with oxygen and substitutional carbon. Diffusing silicon interstitials and vacancies escape from a region of silicon where an intense concentration of Frenkel pairs are produced by a Primary Knock-On Atom (PKA). The PKA is produced by the incident radiation. Vacancies can react with one another to form multivacancy defects. This leads to clustering of intrinsic defects around the PKA production point. This so-called “cluster” region controls many of the electrical parameters of irradiated silicon.

Various types of silicon have been evaluated with resistivities above 500 ohm cm. These are high resistivity epitaxial, FZ Si-Ge, FZ Si-Tin, carbonated FZ and oxygenated FZ. Highly oxygenated FZ has been produced using a "jet" technique by ITME in Poland - this involves a quartz ring plus oxygen gas jet around the float-zone. Oxygen concentrations of a few $10^{17}$ cm$^{-3}$ are possible with this method. A key new technique is to diffuse oxygen into silicon wafers at high temperature – diffused oxygenated float zone (DOFZ), ref. [3]. Oxygen concentrations of a few $10^{17}$ cm$^{-3}$ are possible. Moreover, this technique can be used on any wafer and can be performed by the detector manufacturer. Results with this material are identical to the jet oxygenated float zone. Note that the saturation oxygen concentration is $10^{18}$ cm$^{-3}$. Such concentrations are found in CZ material. However, the maximum resistivity of such material is about 100 ohm cm. Moreover, problems with thermal donors occur in CZ material. Thermal donor problems do not occur in DOFZ. The thermal donor density depends on the third power of oxygen concentration. Processing temperatures around 450 °C should be avoided [4].

2. MACROSCOPIC EFFECTS

Several macroscopic effects are seen in high-resistivity diodes following irradiation by MeV neutrons. Similar effects are also seen following GeV proton and pion irradiation which also create cluster type damage. Macroscopic changes usually scale with the Non-Ionising Energy Loss (NIEL). This has been calculated and can be used to relate the damage caused by particles of different types and energies. Thus, one needs only to refer to an equivalent 1 MeV neutron fluence. A compilation of recommended NIEL values to use for various particles over a wide range of energies is given in reference [1]. The various macroscopic effects seen in neutron irradiated silicon are described in ref. [5] together with a discussion of the complex room temperature annealing behaviour. Briefly, four effects are seen;

- The leakage current increases.
- N-type silicon behaves effectively like p-type material after an “inversion” fluence which is approximately 20 times the starting concentration. The effective doping, and thus depletion voltage then increases linearily with fluence. This change is described by a parameter called $\beta$. This ultimately limits the detector lifetime. A low $\beta$ gives a longer operational lifetime.
- The space charge becomes increasing negative for a device that is left at room temperature after irradiation. This is called reverse annealing and can be inhibited by cooling below zero °C.
- The charge collection efficiency (CCE) degrades for fluences of several $10^4$ 1 MeV neutrons cm$^{-2}$ due to charge trapping. The CCE is dependent on the space charge, voltage and temperature so that comparisons between various results must be made with care.

3. KEY NEW RESULTS

The leakage parameter, $\alpha$, has been found to be material independent, [4]. Defect clusters are the main microscopic cause of the leakage current. The leakage current scales with NIEL and is a very reliable parameter for dosimetry and intercalibration of various radiation sources.

The one radiation parameter that can be altered and controlled, is the $\beta$ parameter. This parameter for various substrates is shown in Table 1. Note that this parameter scales with NIEL for standard material. It does not for oxygenated and carbonated substrates that have been irradiated by charged hadrons. The fluence is a 1 MeV neutron equivalent and the leakage current was used to
intercalibrate between the various radiation sources. DOFZ material has a lower $\beta$ after irradiation by charged hadrons compared to standard FZ. Since the radiation field closest to the beam at the LHC is dominated by charged hadrons, DOFZ material is an exciting prospect for silicon detectors.

Table 1: The $\beta$ parameter in various substrates, [6].

<table>
<thead>
<tr>
<th>Material</th>
<th>$\beta$ (cm$^{-3}$)</th>
<th>$\beta$ (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Standard FZ</td>
<td>Oxygenated FZ</td>
</tr>
<tr>
<td>1 MeV Neutrons (Ljubljana)</td>
<td>0.03</td>
<td>0.022</td>
</tr>
<tr>
<td>24 GeV/c protons (CERN)</td>
<td>0.03</td>
<td>0.010</td>
</tr>
<tr>
<td>192 MeV pions (PSI)</td>
<td>0.03</td>
<td>0.010</td>
</tr>
</tbody>
</table>

The $\beta$ parameter for charged hadron irradiation has been confirmed for DOFZ material produced by SGS Thomson, Micron Semiconductor, SINTEF, CIS, and ITE. A large number of diodes have been processed with different diffusion times, furnaces, crystal orientation and resistivities and then irradiated in order to optimise the DOFZ procedure. No significant effects have been seen. A thermal treatment at 1150°C for 16 hours is sufficient to achieve the low $\beta$ values shown in Table 1.

The physical explanation for the violation of the NIEL hypothesis in oxygenated material is now understood. Charged particles produce significantly more low energy PKA’s. These do not produce clusters and the resultant isolated vacancy/interstitial pairs then lead to impurity related defects. Macroscopic parameters that are sensitive to these defects are therefore dependent on impurity concentrations. The leakage current is only dependent on clusters and is not sensitive to impurity levels. It is thought likely that the divacancy-oxygen defect is responsible for a large fraction of the $\beta$ parameter. High oxygen concentrations inhibit the production of this defect. Recent microscopic measurements confirm that charged particles produce about twice the number of diffusing vacancies compared to neutrons when fluences are normalised using NIEL [7].

The lower $\beta$ in DOFZ material has allowed reverse annealing data to be obtained for very heavily irradiated detectors. The damage factor for this process is seen to saturate for fluences above 6 $10^{17}$ cm$^{-2}$; this is probably not material dependent. The time constant for this process is a factor 1.5 higher in DOFZ material; this is a preliminary result and needs further study. The increased time constant provides an additional safety factor for silicon detectors at the LHC.

Charge collection efficiency versus voltage data from diodes are consistent with depletion voltage information obtained using CV measurements. Data from strip detectors processed on DOFZ material will be available shortly.

4. OUTLOOK

The DOFZ technology has now been transferred to several detector manufacturers. Results from all manufacturers show improved hardness of DOFZ silicon diodes when irradiated with charged hadrons. Full scale prototype LHC microstrip detectors have been processed on DOFZ by both the CMS and ATLAS Collaborations. Irradiation results will be available shortly. Some oxygenated detectors will be installed in the HERA-B experiment next year. As in the past, experience in a real experiment will prove to be the ultimate test of a new technique. The violation of the NIEL scaling for DOFZ material irradiated by charged hadrons is a timely reminder of the danger of accepting useful hypotheses as dogma before the underlying physics is fully understood.

5. ACKNOWLEDGEMENTS

I am grateful to the other co-spokesmen of the ROSE Collaboration, Gunnar Lindstrom (Hamburg University) and Francois Lemeilleur (CERN) for their advice and help. The ROSE Collaboration consists of over 30 institutions worldwide. Without the efforts of these institutions, this paper would not be possible. In addition, the efforts of the various silicon wafer producers mentioned above, as well as diode processing by ITE, Poland, DIOTEC, Slovak, Canberra, Belgium, SINTEF, Norway, Micron Semiconductor, UK, SGS Thomson, Italy, and CIS Germany were vital for this work. Support from the UK Particle Physics and Astronomy Research Council (PPARC) and the EU TMR Network ENDEASD is acknowledged.

6. REFERENCES

AVALANCHE PHOTODIODES FOR THE CMS ELECTROMAGNETIC CALORIMETER

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Abstract

Avalanche photodiodes (APD’s) will be used as photodetectors in the CMS barrel electromagnetic crystal calorimeter for high precision energy measurements in a hostile radiation environment. Significant progress has been made in the characteristics of these devices being expressly developed for CMS. Parameters of the final structure APD’s together with demonstrations of radiation hardness and plans for quality assurance/control during the production phase are presented.

1. INTRODUCTION

In order to optimise the potential for discovering the Higgs, supersymmetry and other possible new physics and study a large variety of standard model processes, CMS requires a high performance electromagnetic calorimeter (ECAL) [1]. The CMS ECAL barrel will be made of 61200 lead tungstate (PbWO4) crystals. PbWO4 is a fast and compact scintillating crystal with peak scintillation emission around 420-450 nm. However, lead tungstate has a relatively low light yield which necessitated the use of a photodetector with a small nuclear counter effect, i.e., a small fake signal from ionising particles. It has to operate with a high quantum efficiency for the peak scintillation of PbWO4 in a rather hostile environment with a strong 4T magnetic field and unprecedented radiation levels. Avalanche photodiodes (APD’s) satisfy all these criteria and they will be used as photodetectors in a large scale HEP experiment for the first time in the CMS ECAL barrel. Each crystal will be equipped with two large surface (5x5 mm² area) APD’s operated at a gain of 50.

The resolution of an electromagnetic calorimeter can be expressed as:

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E(\text{GeV})}} + b + \frac{c}{E}$$

where the stochastic term $a$ is due to the intrinsic shower fluctuations combined with the photostatistics contribution, the constant term $b$ is related to the stability and reproducibility of the detector and $c$ is the noise contribution due to electronics, pile-up etc. The APD’s contribute to all three terms. Since, avalanche photomultiplication is a stochastic process, the so called excess noise factor, $F$, contributes to $a$. Gain variations with bias voltage and temperature contribute to the constant term $b$. The APD capacitance and dark current contribute to $c$. Therefore, aside from matching the properties of PbWO4, it is also imperative to optimise all these parameters for the APD’s destined for use in the CMS ECAL.

![Figure 1: Two APD’s mounted in a supporting structure, which is glued onto the crystal rear end.](image)

Two companies EG&G in Canada and Hamamatsu Photonics in Japan started the development work on APD’s suitable for use in the CMS ECAL in 1995 and some thirty prototypes were tested. The choice between the two vendors was made in favour of Hamamatsu in July 1998. Subsequently, an R&D contract was signed with Hamamatsu for further development. Currently, we are in the final stages of the development phase and a decision on the final APD structure was made in July 1999. Hamamatsu Photonics has developed an APD, which is well suited for this demanding application. Results from the measurements of 180 devices of this

* On leave from INR (Moscow).
type performed at a quality assurance/quality control facility at CERN and irradiations at PSI are presented. The plans for quality assurance/quality control during the production phase are also discussed.

2. PROPERTIES OF THE SELECTED APD

Figure 1 is a picture of two APD’s mounted in a supporting structure which is glued onto the crystal rear end. Hamamatsu APD’s are made by epitaxial growth on low resistivity N+ silicon followed by ion implantation and diffusion. A schematic diagram of the chosen structure is shown in Figure 2. The P material in front of the amplification region, the P-N junction, is made less than 10 µm thick to reduce the sensitivity to ionising radiation. The N layer is introduced to reduce the capacitance and the dependence of the gain on the bias voltage. The V-shaped grooves, which are some 50 µm deep and wide, help to suppress the surface currents.

2.1 Stability of the Gain with bias voltage and temperature

Gain is determined in DC mode by measurements of the differences in current when the APD is illuminated by a blue LED (420 nm) and the dark currents [1]. Figure 3 is a representative distribution of gain versus bias voltage for these APD’s. The dependence of the gain, M, on the bias voltage is rather steep in the region of interest, i.e., M=50. The average operating voltage for a gain of 50 for these APD’s is ~330V with a 20V spread. Since, a group of APD’s will be biased by the same power supply, the average variation of gain with the bias voltage, $1/M^*dM/dV$, has been found to be 3.3% for these devices. This is a great improvement compared to the earlier prototypes [2].

The gain depends on the temperature. This dependence, $1/M^*dM/dT$, has been measured to be – 2.2%/°C at a gain of 50, as shown in Figure 4. Lead tungstate crystals have the same temperature coefficient and hence, the detector temperature has to be stabilised to a tenth of a degree in any case.

![Figure 2: Structure of the selected APD.](image1)

Hamamatsu is trying to reduce this spread in the ongoing, fine-tuning phase.

![Figure 3: APD gain versus bias voltage for an APD.](image2)

![Figure 4: The temperature coefficient of the gain versus the gain for an APD.](image3)

![Figure 5: Dark current for gain 50 for all the APD’s.](image4)
2.3 Nuclear Counter Effect

Minimum ionising particles from the rare leakage of an electromagnetic shower create some 100 electron-hole pairs/µm in Si but only those electrons that are created in front of the P-N junction can start an avalanche. Since, light produces electrons close to the surface, all will be amplified in an avalanche. The nuclear counter effect, the electrical signal generated by the passage of ionising radiation through the APD, can be quantified in terms of the effective thickness of a silicon PIN diode with the same response to electrons from a source and can be defined as:

\[
I_{\text{eff}} = \frac{(\text{peak position})_{\text{APD}}}{(\text{peak position})_{\text{PIN}}} \times \frac{200 \mu m}{M}
\]

where M is the gain of the APD and the PIN diode used in this case is 200 µm thick. Figure 6 shows the resulting pulse height spectra for an APD and a PIN diode which gives \( I_{\text{eff}} = 5.6 \mu m \).

2.4 Excess Noise Factor

The fluctuations in avalanche multiplication are characterised by the excess noise factor, \( F \) which can be approximated by the following expression[3] at high gain:

\[
F = k \times M + \left( 2 - \frac{1}{M} \right) \times (1 - k)
\]

where, \( k \) is the ratio of the ionisation coefficients for holes and electrons. The excess noise factor for these APD’s has been measured to be \( \sim 2 \) for a gain of 50, as shown in Figure 7.

3. EFFECT OF IRRADIATION

Radiation damage on APD’s occurs via two mechanisms:

1) surface damage which causes defects in the front layer, increasing the surface dark current and reducing the quantum efficiency.

2) bulk damage due to the displacement of atoms from their lattice sites increasing the bulk dark current and potentially changing the gain for a given bias.

Figure 6: APD and PIN diode response to electrons from a \(^{90}\text{Sr}\) source.

Figure 7: The excess noise factor as a function of APD gain

Forty APD’s were irradiated at PSI in a 72 MeV proton beam. They were exposed to the beam for approximately 105 minutes which corresponds to a total 1 MeV neutron flux of \( 2 \times 10^{19} \) neutrons/cm\(^2\)[4]. This is equivalent to the fluence expected in the CMS barrel for 10 years of operation. Figure 8 shows the currents (dark and
ionisation) for the forty APD’s during irradiation as a function of time in the beam in seconds. All except two APD’s showed no anomaly during the irradiation. There was a steep rise of the currents for these two. The position on the wafer for this batch of APD’s is known and these two APD’s came from the edge of the wafer. Clearly, the APD’s from the edges of wafers will have to be discarded during production.

The irradiated APD’s were then annealed for one week at 90°C and all their parameters remeasured to ascertain the damage due to irradiation.

Figure 9: Change in bias voltage for a gain of 50 with irradiation versus the APD number.

Figure 9 shows the change in the bias voltage with irradiation for a gain of 50 versus the APD number. The average change was -0.7 V which corresponds to ~2% reduction in the gain for a given bias.

Figure 10 shows the change in the distance to the breakdown voltage from the bias voltage for a gain of 50 (breakdown is defined as the voltage when the dark current is 100 µA) for the irradiated APD’s versus the APD number. The change in the breakdown voltage is large for these APD’s. This is one of the APD properties being improved during the ongoing fine tuning phase. The two APD’s which have 0 and 5 V distance to breakdown are the same as the ones with high currents during irradiation.

Figure 11 shows the dark current versus the APD number for the irradiated APD’s measured at 25°C. The average dark current is ~3µA. It should be noted that at 18°C, the nominal temperature CMS will operate in, the dark current will be half of this. This translates to a noise contribution of 170 MeV due to the APD leakage current after 10 years of LHC operation.

Figure 12 shows the change in quantum efficiency post-irradiation versus wavelength for four of these APD’s. The quantum efficiency remains the same for the wavelengths of interest, i.e., 400-500 nm and a reduction is only seen for wavelengths larger than 600 nm. These measurements were performed with the APD at gain 1.

It was confirmed that all the other parameters for these irradiated APD’s remained the same within measurement errors.
4. APD QUALITY ASSURANCE AND QUALITY CONTROL

In order to ensure and control the quality of APD’s delivered during the production phase, a facility capable of fully characterising these devices has been set up at CERN. Radiation hardness tests will continue to be performed at PSI and a new facility with a $^{252}$Cf source, currently being set up at the University of Minnesota. On receiving a new wafer, the vendor will initially only package 2% of the devices from it and send them to PSI or Minnesota where they will be irradiated. The packaging of the rest of the APD’s derived from a given wafer will proceed if and only if all of the 2% successfully meet our radiation hardness criteria. In addition, another 2% of the devices will be subject to other destructive tests like long term aging at CERN. Hamamatsu will provide measurements of the gain curves, dark currents and the quantum efficiency at a given wavelength for all the devices using a set up designed by us. These measurements will be done at 25°C. The quality assurance/control facility at CERN will measure these devices on a sampling basis to track the Hamamatsu measurements. In addition, more detailed tests of production APD’s will also be performed on a sampling basis to track the production process as a whole.

The quality assurance/control facility at CERN became functional in April 1999 and will continue to do so till the end of production. In addition, the APD’s will also be fully characterised after mounting in the supporting structure which will be glued on the crystals, initially in Lyon and then at CERN.

5. CONCLUSIONS

Intensive R&D has led to the development of APD’s by Hamamatsu Photonics which are suitable for use in the CMS ECAL. The important parameters of these APD’s are summarised in Table 1. These APD’s have a small nuclear counter effect, low excess noise factor, low capacitance and they can withstand the radiation levels expected in the CMS barrel while maintaining the performance CMS is aiming for. The remaining concerns with these devices are the spread in the bias voltage for the operating gain of 50 and the change in the breakdown voltage with irradiation. The structure and manufacturing technology for these devices is being “fine tuned” by the vendor at the moment and these problems are being addressed. The final decision on the structure and manufacturing technology will be made in Oct 1999 and production will commence in Dec 1999. We expect to receive the first production devices in Jan 2000.

A facility capable of fully characterising APD’s for quality assurance/control is in place at CERN and fully functional. The testing for radiation hardness of these devices will continue at PSI and Minnesota.

<table>
<thead>
<tr>
<th>Active Area</th>
<th>5x5 mm$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating voltage</td>
<td>~330 V</td>
</tr>
<tr>
<td>Capacitance</td>
<td>70 pF</td>
</tr>
<tr>
<td>Serial resistance</td>
<td>3 Ω</td>
</tr>
<tr>
<td>Dark current</td>
<td>&lt; 10 nA</td>
</tr>
<tr>
<td>Quantum efficiency</td>
<td>72% @ 420 nm</td>
</tr>
<tr>
<td>$1/M\times dM/dV$ (M=50)</td>
<td>3.3%</td>
</tr>
<tr>
<td>$1/M\times dM/dT$ (M=50)</td>
<td>-2.2%</td>
</tr>
</tbody>
</table>

Table 1: Summary of APD parameters.

6. REFERENCES

1. Abstract

In the LHC experiments, standard voltage regulators are placed in the detector or in the experimental hall and have to function in a challenging radiation environment. At present, there is not radiation-hardened low-dropout voltage regulator available hardened to total dose and displacement damage. Charged hadrons and neutrons dominate the LHC environment and such particles induce displacement damage in semiconductors severely deteriorating in such a way the performances of voltage regulators manufactured in lightly-doped high-voltage bipolar technologies. In addition total ionizing dose effects contribute to the performances deterioration in a way that is difficult to quantify experimentally due to the presence of Low Dose Rate Effects (LDRE). Based on a previous study of a bipolar radiation-hardened technology presented at the LEB conference in Rome in 1998, a radiation-hardened voltage-regulator has been developed by STMicroelectronics under a CERN RD49 contract. Specifications, performances and radiation response to total dose, neutrons and protons are presented.

2. Device outline

During the last two years at STMicroelectronics Laboratories of Catane the elementary structures of a ST proprietary technology, RH Bip1, have been evaluated in its ability at working under irradiation and upgraded. The most relevant results have been presented at the 4th workshop in Rome last year [1]. A qualitative synthesis is shown in fig.1.
Following the outcomes concerning Total Dose Effects (TDE), Low-Dose Rate Effects (LDRE) and Neutrons, a radiation-hardened voltage regulator able to operate in LHC and Space applications has been developed. The initial target was that of getting a device still able to work after an exposure to a radiation dose of 500 krad with a degradation of the performances of no more than 30 percent compared to the pre-rad condition.

Fig 2 shows an overview of the block schematic.

Apart from the circuitry usually implemented (feedback regulation loop, thermal and current limit protection, internal voltage reference) it includes among other an overcurrent monitor. This latter operates under
the control of the current limit section giving on the pin OCM a voltage level of 0.4 volts whenever this protection intervenes at limiting the current at the OUTPUT pin. Being the OCM pulled-up by an internal resistor to VIN, under normal operating conditions the relative voltage levels are coincident.

Others features are:

. possibility of adjusting the short circuit current within 30 % of its typical value by placing an external resistor between the SH_CNTRL and VIN pins;

.a remote sensing, allowing the regulator to function with an the output load far from it;

. possibility of controlling the OFF/ON switching of the device trough an INHIBIT pin.

Even if the general architecture is basically similar to that of a conventional linear regulator, each block has been designed in order to minimize as much as possible the performances degradation under radiation operation. This has been achieved by making use of proper rules during both the schematic and the layout phases, some of them coming from the experimental issues told before and others are in ST proprietary know-how in rad-hard design practice.

An overview of the main target specifications is given in fig. 3.
3. Characterization tests results.

Some of the tests have been performed at CERN laboratories in Geneve. Up to now the responses in terms of line and load regulation have been checked by using the following radiations sources:

- Co-60 up to 1.3 Mrad at ESA-ESTEC
- Total dose by X-ray 10 KeV up to 4 Mrad
- Neutron fluence up to \(10^{13}\) n/cm\(^2\)
- Proton fluence up to \(5 \times 10^{13}\) p/cm\(^2\)

A selection among the most significant results is presented at page 6. All values on y-axis are expressed in percent units with respect to the nominal output voltage.
Others measurements have also been done at ST Catane. They are not set out in this paper because of no concern for an evaluation of the response under radiation.

4. Conclusion

So far this first study has demonstrated that this regulators is radiation-hard, as it was designed to be. It survived protons, neutrons and gamma rays with few changes of their line and load regulation graphs. Further study will be done for various biasing conditions, in order to check the variation of other important parameters such as dropout voltage and output noise voltage. Finally, another important investigation will be pursued to different fabrication lots for a quantitative analysis of the parameters spreading.

References:

Load regulation before radiation

Load regulation after 3.9 Mrad x-rays

Load regulation after $10^{13}$ neut./cm$^2$

Load regulation after $10^{13}$ prot./cm$^2$

Line regulation before irradiation

Line regulation after 3.9 Mrad x-rays

Line regulation after $10^{13}$ neut./cm$^2$

Line regulation after $10^{13}$ prot./cm$^2$
OVERVIEW OF THE ATLAS LARG ELECTRONICS

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Abstract

This document briefly reviews the main detector characteristics relevant to the read-out electronics of the ATLAS Liquid Argon calorimeters, lists the main requirements and discusses briefly the general architecture and the basic building blocks. The next steps in the construction of the ATLAS electronics are outlined.

1. INTRODUCTION

The Liquid Argon sampling calorimeter technique is used for all electromagnetic calorimetry covering the pseudorapidity interval $|\eta| < 3.2$ and also for hadronic calorimetry from $|\eta| = 1.4$ to the acceptance limit $|\eta| = 4.8$. The global layout is shown in Figure 1. The central cryostat contains the barrel electromagnetic calorimeter (EMB). Each end-cap cryostat houses an electromagnetic calorimeter (EMEC), two hadronic wheels (HEC) and one forward calorimeter (FCAL). Close to ~190 k high precision, high dynamic range and low noise electronic channels are needed to read out this detector.

Common electronics is used everywhere, with the exception of the very front-end where the HEC uses cold preamplifiers. This minimizes design effort, standardizes hardware and will facilitate maintenance.

A great deal of work has been done to define this electronics system and to prototype it. Samples of nearly every front-end board have been built for a total of about 6000 read-out channels. They are now being installed in the test beam at CERN. This electronics is being used to test and qualify ATLAS calorimeter modules. This provides a very valuable experience with the system.

Figure 1: 3D view showing the Liquid Argon calorimeter system and the location of the front-end electronics

This note briefly reviews the main detector characteristics relevant to the read-out electronics, lists the main requirements and discusses briefly the general architecture and the basic building blocks. The next steps in the construction of the ATLAS electronics are outlined.

More detailed information can be found in [1, 2].

2. DETECTOR CHARACTERISTICS

The calorimeters are finely segmented both longitudinally and transversally for a total of ~190 k active read-out channels. These channels are grouped consistently to form ~ 5120 trigger towers (see figure 2).

Figure 2: Typically 60 cells are summed to form pointing trigger towers with a size $\Delta \eta \times \Delta \phi = 0.1 \times 0.1$.

As sketched on Figure 3 the detectors deliver on their electrodes a triangular-shaped current signal with a fast rise time (a few ns) decreasing to zero at the end of the drift time of ionization electrons in liquid argon (~ 450 ns). For the FCAL, since the argon gap is smaller, the pulse duration is shorter (~ 50 ns).

Figure 3: Signal shape as produced in the detector (triangle), and after shaping (curve with dots). The dots represent the position of successive bunch crossings.
The amplitude of the current varies from one sub-detector to another. A value of 2.8 µA/GeV is typical for the EM accordion calorimeters; this drops down to ~0.3 µA/GeV for the HEC. This signal is delivered on the detector impedance, which, to a very good approximation, is a pure capacitance from as low as 75 pF to as high as 2 nF. More information can be found in the LARG TDR Section 10.2. [2]

3. REQUIREMENTS

The main requirements for the read-out electronics can be summarized as:

- The dynamic range of the input is at least 16 bits. The degradation introduced by the read-out system should be minimal.
- The read-out system should be inter-calibrated to better than 0.25% over the whole energy range, in order to achieve a small constant term in the energy resolution.
- The amount of coherent noise per cell should be less than 5% of the level of incoherent noise.
- A pipeline with a depth of at least 2.5 µs should be provided; in addition a large enough derandomizing buffer and a fast enough read-out should allow for a maximum Level-1 trigger rate of up to 75 kHz.
- Cells should be summed in trigger towers ∆η  ×  ∆φ = 0.1 × 0.1 and the result sent out to the Level-1 processor. The required precision for the analog trigger sums is 5%.
- A fair fraction of this electronics will be located in an area with limited access. High reliability is thus a concern. In addition, although radiation levels at that location are not very large (10^12 n/cm²/yr; 20 Gy/yr; 10^10 ionizing particles/cm²/yr), this electronics has to be radiation tolerant.
- The large number of channels (~ 190 000) involved requires development of a system with low power consumption and moderate cost.

4. READ-OUT ARCHITECTURE

Signals from the detectors are processed by various stages before being delivered to the DAQ system. Figure 4 shows the read-out architecture as well as the basic elements of the system: preamplifiers, shapers, pipeline memory, digitization, and digital filtering. The data are then sent off to the Level-2 buffers. Much of the digital electronics: control, digital filtering, and Level-2 buffering, is located off the detector, in a control room. This limits digital activity close to sensitive analog electronics to the absolute minimum. The off-detector electronics will use standard non radiation-hard techniques. It will be easily accessible, and can be delivered relatively late; the latest available technology can be used. It will also be more easily upgradable.

Figure 4: Block diagram of the read-out electronics. In the drawing warm preamplifiers are located on the front-end board, which is the case for the EM and FCAL calorimeters. For the hadronic end-cap calorimeter, a preshaper - that interfaces preamplifiers located in the liquid argon to the standard shaper chip - replaces them.

The clock and control signals (level 1 accept, resets...) are generated in the trigger room, where special care has to be taken to minimize trigger latency, and fan-out to the various boards using the TTC system developed by the RD12 collaboration. The global system is split into 8 partitions, which can run independently if needed.

The sensitive analog electronics is housed ‘on-detector’, in a front-end crate attached to the cold to warm feedthroughs, in the crack between the barrel and end-cap calorimeters and at the rear of the end-caps (see figure 1). This crate is positioned on top of the warm feedthrough flange, effectively becoming an extension of the cryostat Faraday cage. This should efficiently shield the LARG read-out electronics against external electromagnetic radiation. In addition, this keeps the warm part of the signal and calibration cables to a minimum length and therefore minimizes the associated attenuation and noise.

The design of the crate system is now well advanced as explained in [3]. It strives to minimize pick-up noise that might be coherent over many channels. It also provides
for an efficient water cooling of the ~3kW dissipated power. Crate production will start early 2000.

5. THE FRONT-END SYSTEM

In the cold, a system of G10 boards gangs electrodes together to form readout cells and holds precision resistors that inject calibration pulses. Small diameter coaxial cables connect to these boards and bring signals to the cold to warm feedthroughs. All these parts are already in production [4, 5].

The front-end crate (FEC) contains several types of boards. The calibration board houses 128 precision pulsers which inject precisely known current pulses, covering the whole dynamic range, as close as possible to the read-out electrodes through high-precision resistors located in the cold, to simulate energy deposits in the calorimeters. The timing of the calibration pulses is set to reproduce the timing of physics signals, taking into account the variation of time of flight. More information can be found in the G. Perrot’s contribution to these proceedings and in [6].

Front-end boards (FEBs) [7] also house 128 channels:
• They amplify and shape the input analog signals. Three gains are used to cover the full dynamic range [8].
• They sum calorimeter cells by trigger tower within each depth layer, and drive the summed signals to the tower builder board.
• They store the signals in a 144 cell deep analog memory (SCA) waiting for the decision by the first level of triggering.
• They digitize the selected pulses, and transmit on optical fibres the multiplexed digital results.

Production of amplifiers is now well-advanced [9] as can be seen from H. Brettel’s and M. Citterio’s contributions, and a preproduction run is going to be ordered very soon for shapers and SCAs.

For the EM barrel and endcap calorimeters, Tower Builder Boards (TBBs) [10] are used to perform the final level of analog summation to form trigger tower signals and to transmit the analog signals to the Level-1 cavern for digitization and processing by the Level-1 trigger processor. A prototype has been built and tested in the test beam. For the HEC and FCAL calorimeter, Tower Drivers (TDB) transmit the signals to the level 1 cavern.

Control boards receive and distribute the 40 MHz clock, the level-1 trigger accept signal, as well as other fast synchronous signals and information to configure and control the various boards in the crate.

Monitoring boards read out various monitors, like liquid purity and temperature sensors.

More information about the content of every crate in the system and on how every calorimeter cell gets routed to its FEB can be found in [11].

Quite a substantial amount of power (~ 250 kW) is needed to supply the large number of electronics channels in the front-end system. None of this power should be transferred to the surrounding detectors and liquid cooling is mandatory. To minimize the risk for leaks, the cooling fluid will be circulated below atmospheric pressure, typically 600 mb into heat exchanger plates mounted on every front-end board. Heat conductive pads will be used to eliminate air gaps between components and cooling plates and maximize heat transfer. Much more information can be found in the contribution by H. Takai and in [3].

The distribution of this large amount of power has to be done carefully. Each front-end crate will have its own low voltage power supplies. Compact high power DC-DC converters with good noise properties have been identified. First tests seem to indicate sufficient radiation tolerance. The current base line is then to locate these supplies on top of each crate, minimizing the length of the low voltage lines and associated loss of power. As this is a poorly accessible area, redundancy is to be built into the system. See contribution by M. Citterio for more on this. These supplies will be “isolated”. Strict control of ground loops will be observed, and there will be only one location allowed where connection to ground is made. The cryostats with all their cryogenic lines and services will be electrically insulated [12].

6. “MODULE 0” ELECTRONICS

To test, in beam, calorimeter modules and to qualify their production, a read-out electronics was needed. This was used as an opportunity to prototype the front-end
ATLAS electronics. About 6000 channels of ATLAS like electronics have been produced and ~2000 are already installed in the beam. In this exercise, we learnt a lot about the real ATLAS electronics and some preliminary results look already quite encouraging:

- The boards were efficiently cooled; the board temperatures were between 25 °C and 28 °C (i.e. below ambient at the time of the test) and very stable with time.
- The pedestal stability is very good: 0.1 ADC counts over a 3-week period.
- The incoherent electronics noise closely matches expected values i.e. ~20/50/35 MeV for the EM front/middle/back cells.
- The coherent noise is slightly larger (5-7%) than the ATLAS goal of 5%. However this is already a very good result as in the test beam we are not yet using optical links.
- The measured integral non-linearity is below 0.25% on all three shaper gains.

Figure 6 shows samples measured on a single 100 GeV electron pulse in a middle layer cell. The pulse shape is nice and follows expectation.

7. OFF-DETECTOR ELECTRONICS

For reasons connected with the construction schedule of the experiment, the front-end electronics has received considerably more attention than the electronics that will reside off the detector.

7.1 Trigger clock and control system

In the Level-1 cavern, ~50 meters away from the detector, signals from trigger towers are received and delivered to the calorimeter Level-1 trigger processor. The central trigger processor (CTP) will deliver not only physics triggers but also calibration signals and triggers. These signals, together with the 40 MHz clock and other synchronous commands, are transported to the front-end crates and to the read-out crates by the TTC system (timing trigger and control) developed in the RD12 project. To benefit from the excellent intrinsic time resolution of the detector (50 ps at high energy), clock jitter should be kept as low as possible (< 100 ps).

To ease the timing in of the system, fibers distributing the clock will be cut to length and/or their transit time measured and programmable delay lines in calibration boards will be preset to reproduce the timing of physics signals. This should allow not only to align in time the various calorimeters, barrel, end-cap... but also to time in the level 1 processor, the CTP and the distribution of the level 1 accept signals. These adjustments will be checked and refined by analyzing real shower pulses from collisions.

7.2 Read-out driver system

To each front-end crate is associated a read-out driver crate. A set of such front-end crate - read-out driver crate pairs, together with a TTC driver form a partition controlled by a master CPU. Eight such partitions are considered for each end of the experiments. This would allow running independently the EMB, the EMEC, the HEC and FCAL calorimeters.

The read-out driver crate contains:
- a CPU connected to the network to control this crate and the associated front-end crate;
- a SPAC master module to configure or down-load parameters into the various boards of the front-end crate or to read back registers [13];
- a TTC and BUSY module to receive the TTC information, fan it out to the RODs and collect their BUSY signals
- Read Out Driver (ROD) modules, which receive raw data from the FEBs and produce the corresponding energy, time, and some form of data quality measure, sending the result to the DAQ, i.e. to the Read Out Buffer (ROB) modules.

Fast unidirectional, 1 Gbit/s optical links connect the FEBs to the RODs. A frame of typically five samples centered on the bunch crossing of interest is sent down the link to the ROD module for digital processing. This is accomplished using the well-established method of optimal filtering. In practice one obtains a weight for each sample which results in the minimum error on the energy subject to the constraint that the pulse can be moved in time without affecting the result to first order. Any loss in energy resolution due to small phase jitter between the pulse and the clock is minimized. The weights are chosen to minimize the total noise (electronics pile-up) for the current value of the luminosity, and the quality of the waveform can be checked to detect events subject to large...
out-of-time signal overlaps. The available computing power in these modules will also be used to monitor every channel. Examples include checking for drift in the phase of the clock with respect to the particle signal, histogramming energy spectra, and the preprocessing and histogramming of data during calibration runs. More detailed information can be found in the contribution by W. Cleland.

8. NEXT STEPS

A major milestone in the development of the LARG electronics has been met with the production and successful running in of ~ 6000 channels of ATLAS like electronics. However, several short cuts had to be taken given the rather tight schedule:

• Digital optical links to connect the FEBs to the RODs: We are currently using shielded twisted copper pairs. These will be replaced by optical links. We already have hints that this will reduce the amount of coherent noise. A lot of work has been done to assess commercial solutions i.e. based on the HP G-Link chip set. The main pending issue there is radiation tolerance and more specifically SEE effects. A lot of information can be found in R. Stroynowski’s contribution.

• Distribution of TTC signals: In ATLAS, we are planning to use the standard TTC system as developed by the RD12 collaboration. We plan to test this distribution scheme in the test beam set-up as soon as enough standard TTCRx chips become available.

• Radiation tolerant electronics: Though the radiation tolerance of our main critical components (preamps, shapers, SCA,...) is now well established, there are many other areas where a lot of work is needed:
  a. Power regulators, (we are planning to use the work of P. Jarron et al. from RD49)
  b. Logic: we are working on moving logic circuits described in high level languages (i.e. VHDL) and prototyped in FPGAs to custom ASICs using the DMILL technology.
  c. ...

All this effort aims at producing two full crates of hopefully final front-end electronics by mid 2001. This would allow exercising these crates for some time before launching the board production for ATLAS by mid 2002. Note however, that some parts of the front-end electronics will be needed even sooner – i.e. the front-end crates or the front-end chips: shapers, SCA - or are already in production like preamplifiers.

9. REFERENCES

Most of the references below are accessible from the Web, using the EDMS system, starting from the ATLAS main page.

1 Overview of the LARG electronics: ATL-AL-EN-0003
2 ATLAS Liquid Argon Calorimeter TDR: CERN/LHCC/96-41
3 Liquid Argon Front-End Crate: ATL-AL-EN-0004
4 The LAR Mother Board System. Documentation: http://www.usatlas.bnl.gov/lar/mb/
5 PRR of LArg Cold Cables – Report: ATL-RA-ER-0003
6 The LARG Calorimeter Calibration Board: ATL-AL-EN-0005
7 Design of the ATLAS LAr Front End Board: ATL-AL-EN-0009
8 The LAr Tri-Gain Shaper: ATL-LAR-98-092
9 Report on the HEC Cold Electronics PRR: ATL-TC-ER-0013
10 The Level 1 Trigger and the Tower Builder Board: ATL-AL-EN-0007
11 Cabling of the EM calorimeters: ATL-AL-ES-0004
Characterization of the Coherent Noise, Electromagnetic Compatibility and Electromagnetic Interference of the ATLAS EM Calorimeter Front End Board

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Abstract

The ATLAS Electromagnetic (EM) calorimeter (EMCAL) Front End Board (FEB) will be located in custom-designed enclosures solidly connected to the feedthroughs. It is a complex mixed signal board which includes the preamplifier, shaper, switched capacitor array analog memory unit (SCA), analog to digital conversion, serialization of the data and related control logic. It will be described in detail elsewhere in these proceedings. The electromagnetic interference (either pick-up from the onboard digital activity, from power supply ripple or from external sources) which affects coherently large groups of channels (coherent noise) is of particular concern in calorimetry and it has been studied in detail.

1. COHERENT NOISE IN CALORIMETRY

Pick-up due to external causes can impose a serious limitation to the resolution attainable in calorimeters at certain levels of shower energy even when the level of pick-up in individual channels is small compared with the random noise. This is due to the fact that signals from a number of channels must be added to determine total shower energy. Pick-up signals tends to be correlated over a large number of nearby channels and, therefore, add linearly when sums are formed, whereas the random noise, being uncorrelated from channel to channel, adds quadratically. Thus, a pick-up signal at the level of 10% of the random noise becomes of equal importance to the noise when signals from 100 channels are added.

The coherent noise can come from a number of sources:
1. Noise on power supply lines, in particular that associated with switching power supplies.
2. Digital noise associated with the operation of logic circuits and analog-to-digital converters on the same board or nearby boards.
3. External electromagnetic interference which enters the enclosure through apertures in the shielding or which is conducted on power supply and control lines which penetrate the shielding.

1.1. Power Supply Noise

In the case of the Atlas EMCAL FEB enclosures, power supply noise has been reduced to an acceptable level by using resonant charging type switching power supplies in which the switches open only at zero current level. No increase in coherent noise has been measured with respect to linear power supplies. A separate paper in these proceedings will describe the power supplies.

By injecting radio frequency (RF) directly on the power supply lines by means of a loop antenna, it has been found that RF can couple through the power supply cables. Shielding of the cables is being considered and its effectiveness will be studied.

1.2. Digital Noise

It is the noise being generated by:

• Control signals carrying commands into the FEB (and spurious signals from the digital activity of the control cards).
• Digital activity on the FEB itself (40MHz clock, digitizer clock, serializer clock, SCA control lines.

Digital noise can be controlled by careful shielding of the input amplifiers by means of a local Faraday cage enclosing the preamplifiers and by shielding of the input connectors.

Good grounding, including ground continuity of the connector shield to the baseplane and additional ground contacts from the FEB to the baseplane further reduce the coupling of on-board digital noise to the input of the preamplifiers.

Use of fiber optic transmission of the control signals both eliminates the coupling of unwanted signal from the control cards to the FEB and breaks ground loops created by the connection of the control electronics to the FEB.

1.3. External EMI

The effect of external electromagnetic interference depends on the enclosure design, the intensity and nature of the electromagnetic field and its frequency spectrum. In general, in the closed environment of a colliding beam detector, we will be concerned only with so-called near field radiation coming from signal and command cables.

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† On leave from the Institute of Experimental Physics, SAS Kosice, Slovakia.
associated with other detector systems that pass close to the FEB enclosures.

2. SHIELDING PROPERTIES OF A METAL ENCLOSURE [1,2]

The enclosure housing the FEBs is designed to shield the FEBs from external radiated EM fields.

Its shielding properties are defined by the “shielding effectiveness”, defined as the attenuation ratio (in dB) of the field inside the enclosure with respect of the field outside as depicted in Fig1:

\[
\text{SE}_{\text{dB}} = 20 \log_{10} \left( \frac{F_t}{F_e} \right)
\]

Several effects play a role, and they will be discussed in the subsequent paragraphs.

2.1. Absorption loss

It is proportional to the ratio of the thickness of the enclosure to the penetration depth of the EM wave:

\[
A_{\text{dB}} = 131.4 \cdot (t \cdot \mu \cdot f)^{0.5} \quad (t \text{ in mm})
\]

\[A = \text{Absorption loss}
\]

\[t = \text{thickness}
\]

\[\mu = \text{relative permeability}
\]

\[\sigma = \text{relative conductivity (with respect to copper)}
\]

\[f = \text{frequency in MHz}
\]

2.2. Reflection Loss

The reflection loss depends on the mismatch between the wave impedance \(Z_w = E/H\) and the shield impedance \(Z_{\text{shield}} = \sqrt{(\omega \cdot \mu) / \sigma}\)

\[
R_{\text{dB}} = 20 \cdot \log_{10} \left( \frac{Z_w}{Z_{\text{shield}}} \right) \quad (\text{in dB})
\]

2.3. Total Shielding Effectiveness

It is the sum of the absorption and reflection loss and quantifies the quality of an enclosure. It is plotted in Fig. 2.

For near field magnetic fields, the most likely scenario in the densely packed environment of the calorimeter it increases with frequency. The rejection of electric fields is about 60dB higher than the one for magnetic fields at 10MHz due to the mismatch between the high wave impedance and the low shield impedance of the metallic body of the enclosure.

2.4. Effects of Apertures in an Enclosure

The shielding effectiveness of a closed box is reduced by the apertures necessary to feed control lines, power supplies etc.

The shielding (in)efficiency of \(n\) apertures is:

\[
\text{SE}_{\text{dB}} = 20 \cdot \log_{10} \left( \frac{\lambda}{2 \cdot L} \right) - 20 \cdot \log_{10}(n)_{\lambda/2}
\]

\[L = \text{maximum linear dimension (e.g. diagonal)}
\]

\[\lambda = \text{wavelength}
\]

\[n = \text{number of slots within } \lambda/2
\]

The shielding effectiveness is also reduced by the seams where the front panels of the FEBs butt when inserted in the enclosure. It is improved by the presence of the cooling plates, which provide additional shielding (they can be modelled as a transmission guide below cutoff, limiting penetration of an EM wave underneath).

In conclusion, the metallic enclosure body presents a very effective reflecting mismatch to the high impedance near field environment so that electric fields are strongly attenuated before entering the enclosure.

The most troublesome potential source of interference, is likely to be near field RF magnetic fields produced by currents in nearby cables.

3. MEASUREMENT OF COHERENT NOISE

Three techniques were used in an effort to quantify the effects of external RF magnetic fields. In all cases, a magnetic field was generated by a small loop (about 15cm in diameter) driven from a 50W broadband power
amplifier excited by a variable frequency source and mounted about 25cm from the power bus side of the enclosure. The driving coaxial cable was passed through a number of ferrite toroids, acting as baluns to reduce the radiated electric field strength. A calibrated loop antenna (COM-Power AL130) was placed 25cm in front of the transmitting loop.

Fig. 3: Magnetic Field H measured by the monitoring antenna 25cm in front of the transmitting loop.

The signals from the 128 channels on each FEB are summed in four groups of 32 channels for trigger purposes. In one of the techniques, these sums were used, rather than the individual channel signals, to increase the level of coherent noise relative to the random noise.

3.1. Measurement of Coherent noise with a Network Analyzer

The first technique makes use of a network analyzer (HP4395). The RF output of the spectrum analyzer is connected to the power amplifier (see Fig. 4) as the source of electromagnetic interference. The calibrated antenna output is connected to the “A” input of the analyzer and the amplified sum signal is connected to the R (reference) input. The network analyzer is swept over the range of 1 to 40MHz, using a narrow filter bandwidth (100Hz). The narrow bandwidth suppresses all frequencies except the exciting frequency, and the instruments displays a plot of the RF level measured on the sum signal, normalized to the excitation field as measured by the receiving antenna. The results, normalized to the coherent noise per channel assuming an equal contribution of each channel, are shown in Fig. 5a as a solid line for the “slice” of the board (i.e. the sum top and bottom of one quarter of the FEB) nearest to the power supply bus (worst case). Fig. 5b plots the coherent noise of each slice; the noise decreases as the distance from the transmitting antenna and the

Fig. 4: Block diagram of the experimental setup to measure the coherent noise due to an external electromagnetic field by means of a network analyzer. The Tektronix AWG2020 is used to provide an external time base phase locked to the 40MHz clock to phase lock the RF interference signal when necessary.

3.2. Measurement of Coherent Noise with the DAQ and Non-coherent Clock

The second technique makes use of the complete FEB digitizing and data transfer capability of the FEB data acquisition system (DAQ). The 40MHz digitizing clock is asynchronous with respect to the electromagnetic interference frequency. The RMS fluctuation of the pedestal values for all 128 channels over a large number of software generated triggers (10,000), each 32 samples deep, taken by the switched capacitor array is measured. Channels more sensitive to pick-up than the average (due, for example to less effective grounding or shielding) show higher levels of total noise. Fig. 6 shows the plot of the rms noise versus channel number for a frequency of 28.5MHz, at which the average coherent noise is maximum. It can be seen that the first half of the FEB (ch.1-64) is barely affected. The worst coherent noise is for the channels nearest to the transmitting antenna and also nearest to the slots for the power supply, the timing, trigger and control (TTC) cable and the SPAC cable.

This coherent noise is due to EMI coupling into the input of the preamplifiers: it is greatly reduced when the capacitors connected to the input of the FEB on the pedestal are removed.

The plot of Fig. 6 shows also an odd-even effect, related to the length of the pins of the right angle connector at the input of the FEB. This technique is useful...
for finding defects in the board design and did, in fact, show that additional spring contacts between the two FEB external ground planes and the ground planes of the back-plane are very helpful, but it cannot detect a coherent noise less than about 10% per channel of the random noise. To increase the sensitivity, digital sums over large groups of channels are formed. The rms noise in the digital

Table 1: FEB Coherent Noise

<table>
<thead>
<tr>
<th>Sum type</th>
<th>Intrinsic FEB noise [%/ch]</th>
<th>External RF f=28.5 MHz H=7.2 mA/m [%/ch]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>3.76 mA/m</td>
<td></td>
</tr>
<tr>
<td>Bottom</td>
<td>4.03 mA/m</td>
<td>22.40</td>
</tr>
<tr>
<td>Left Half</td>
<td>3.69 mA/m</td>
<td>11.21</td>
</tr>
<tr>
<td>Right Half</td>
<td>4.50 mA/m</td>
<td>48.87</td>
</tr>
<tr>
<td>Top Left Quarter</td>
<td>4.04 mA/m</td>
<td>10.61</td>
</tr>
<tr>
<td>Bottom Left Quarter</td>
<td>3.80 mA/m</td>
<td>12.25</td>
</tr>
<tr>
<td>Top Right Quarter</td>
<td>5.13 mA/m</td>
<td>34.95</td>
</tr>
<tr>
<td>Bottom Right Quarter</td>
<td>4.86 mA/m</td>
<td>63.02</td>
</tr>
<tr>
<td>Slice 0, Quarter</td>
<td>4.54 mA/m</td>
<td>9.06</td>
</tr>
<tr>
<td>Slice 1, Quarter</td>
<td>4.00 mA/m</td>
<td>14.07</td>
</tr>
<tr>
<td>Slice 2, Quarter</td>
<td>4.39 mA/m</td>
<td>24.38</td>
</tr>
<tr>
<td>Slice 3, Quarter</td>
<td>5.64 mA/m</td>
<td>75.01</td>
</tr>
<tr>
<td>Total (128 ch)</td>
<td>3.62 mA/m</td>
<td>29.78</td>
</tr>
</tbody>
</table>

Fig. 5: Coherent noise vs. frequency of the external RF interference normalized with respect of the measured H field

a: Noise of “slice 3” (i.e. sum of 1/4 of the FEB channels, top and bottom nearest to the power supply) measured with various techniques. Solid line: Network analyzer Squares: DAQ with non-coherent clock and trigger. Circles: DAQ and coherent clock and trigger.

b: Comparison of the coherent noise summed by “slice”: the noise decreases with distance from the FEB side nearest to the transmitting antenna

Fig. 6: rms noise vs. channel number measured for an external RF at f=28.5 MHz inducing a field H=28.5 MHz.

The sum of the data from n channels is compared with the square root of n times the average rms noise per channel. If these are equal, there is no coherent noise. The quadratic difference is a measure of the coherent noise, but it gives no indication of the source of this noise nor of its frequency spectrum. The coherent noise of the digitally generated sum of the “slice” nearest to the power supply bus are shown as solid squares in Fig. 5a. Table 1 shows the coherent noise of various subsets of the FEB for the noise sources intrinsic to the FEB itself and for an external
RF at a frequency of 28.5 MHz and a field intensity as measured at the monitoring antenna of \( H = 7.2 \text{ mA/m} \). Both Table 1 and Fig. 6 show that the pick-up decreases approximately exponentially with distance from the side of the enclosure, the 1/e distance being about 8 channels. This shows that the assumption made, in the other two measurement modes, that the pick-up is uniform over 32 channels is not really valid.

3.3. Measurement of Coherent Noise with the DAQ and Coherent Clock.

The technique described in the previous paragraph is sensitive to coherent noise down to the level of 1 - 2 per cent of the random noise.

To increase the sensitivity, the RF interference source is phase-locked to the 40MHz sampling clock. Also the trigger is synchronized to the RF frequency. The 32 successive samples saved in the SCA plot out the waveform of the interference signal. Averaging over many events (10,000) suppresses the random noise and leaves only the coherent noise. Coherent noise measured with this method is shown as circles in Fig. 5.

4. AN EXAMPLE

The measurement of the effect of an external interference on the FEB allows an estimate of the maximum currents allowable in nearby cables.

For example assuming a sensitivity of 10%/(mA/m)/ch, the maximum field allowable to induce a 10% coherent noise per channel would be 1 mA/m. The maximum magnetic field created by two parallel wires normal to the plane of the wires is \([1,3]\):

\[
|H| = \frac{1}{2\pi} I \cdot \frac{2d}{r^2} \quad \text{for} \quad d < r
\]

where \( I \) is the current in each wire (in opposite directions, of course), \( d \) is the distance between wires and \( r \) is the distance from the wire pair. As an example, the differential current flowing in parallel wires 1 mm apart necessary to create a magnetic field of 1 mA/m at a distance of 10 cm is \(~30\) mA. However in a practical system the wires are twisted and the field will be much lower, and it will be lower still if the wire pair is shielded.

A system test has been performed to measure the possible interferences between the LAr read-out and the Transition Radiation Detector (TRT) read-out.

A board emulating the TRT driver and measuring the bit error rate at full speed was brought at the LAr test stand at BNL. Four TRT cables, each with 20 twisted pairs were looped on the side of the FEB enclosures, in the location where the TRT cables will be in the final setup.

The effect of the EMI emitted from this cable on the FEB was exceedingly small, with an increase of the average coherent noise of \(~0.3\%)/ch at 20 MHz, and only \(~0.08\%)/ch at 40 MHz.

Also the effect of the FEB and associated controls on the TRT bit error rate was so small not to generate any error over a 60 hours run at 40 Mbit/s. This corresponds to a BER \(<10^{-14}\).

5. CONCLUSIONS

The FEB enclosure provides an effective shielding against EM fields: no effect is measured unless strong EM fields are generated with a power amplifier. The maximum effect is of the order of 10%/(mA/m)/ch at a frequency of 28.5 MHz.

Its shielding effectiveness is lower for magnetic fields: the most potentially troublesome source of EMI are therefore near fields from currents in cables nearby the FEB enclosures. The openings on the enclosure and the penetrations to carry external signals to the FEB are weak spots. Possible improvements are:

- Use optoelectronics transmission whenever possible.
- Extend the Faraday cage to include the power supply bus bars, cables and switching power supplies crate.

To limit the coherent noise of the digital activity on the FEB itself careful shielding of the input connectors and ground continuity from the FEB to the baseplane are mandatory.

Low noise switching power supplies using a resonant charging technique do not add to the coherent noise in a measurable way.

6. ACKNOWLEDGEMENT

The TRT test was made possible by the efforts of M. Mandl and M. Newcomer, who were the principal contributors throughout the test.

7. REFERENCES

[2]: A good practical reference is the product catalog of Instrument Specialties, Delaware Water Gap, PA
COLD ELECTRONICS FOR THE LIQUID ARGON HADRONIC END-CAP CALORIMETER OF ATLAS

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Werner-Heisenberg-Institut
Foehringer Ring 6, D-80805 Muenchen

1. ABSTRACT

For the ATLAS hadronic end-cap calorimeter a monolithic Gallium Arsenide front-end chip has been developed. The full production (6600 chips) is completed. Basic characteristics and results of mass measurements are presented. The manufacturing of 360 preamplifier and summing boards, equipped with these chips, is in progress. Boards undergo the ATLAS quality assurance procedure in an automatic equipment. Special front-end boards - a subset of the circuitry of standard FEBs - have been built with pole-zero compensation hybrids instead of warm preamplifiers. At the recent beam runs in June and August 99 they where installed in a standard front-end crate on top of a LAr-feed through. Beside physics studies and calibration of the stacks mainly the coherent noise has been investigated.

2. OVERVIEW

HEC MODULE
⇒ HEC module has 4 longitudinal segments
⇒ GaAs chips are mounted on preamplifier and summing boards (PSB) at the top of the module.

ELECTRONICS CHAIN
⇒ Cold Electronics: LAr gap, HEC cables, GaAs chips, Quadrant cables
⇒ Warm Electronics: Preshaper, Monolithic shaper, DAQ

3. ELECTRONICS CHAIN

![Figure 1 Summing scheme](image1)

![Figure 2 Electronics chain block diagram](image2)
4. COLD ELECTRONICS

Figure 3  HEC module. Left: Readout board with pad structure Right: Cross section with a trigger tower

4.1 Preamplifier and Summing Stages

⇒ ASIC GaAs designed by MPI
⇒ Process: TriQuint QED-A (1µm)
⇒ Internal: 8 preamplifiers and 2 drivers
⇒ External: decoupling capacitors, driver feedback components, summing connections
⇒ Quantity: 67 chips/Module, 4288 chips/HEC
⇒ 6600 chips on 18 wafers produced and delivered
⇒ Detailed studies of several chips warm and cold

Figure 4  Circuit diagram of preamplifier (left) and driver stage (right)
4.2 Dynamic Characteristics of Chip

⇒ Input impedance close to 50Ω

Figure 5  Input impedance of different chips

⇒ Nonlinearity in full LHC range less than 1.4% for preamplifiers and 1.6% for complete channel
⇒ Signal rise time close to expected value T=Ri*Ci
⇒ Transfer function is adjusted by driver feedback

4.3 Signal to Noise Ratio of Chip

⇒ Equivalent noise current is 20% less than specified value. Peaking time in ATLAS is 50ns.

Figure 6  Equivalent input noise current

⇒ Some excess noise appears at LAr temperature if Vee exceeds the normal working range.
⇒ For nominal Vee the noise sources are:
  * white serial Rs=35Ω
  * white parallel Rp=800Ω
  * parallel flicker corner Ff=1.5 MHz

4.4 Chip Selection

⇒ Each chip is measured at room temperature before being soldered on the board.
⇒ Criteria are:
  * gain of each preamplifier
  * gain variation between channels
  * noise
  * risetime
⇒ 2 types of measurements: summing 8 preamplifiers to one driver and summing 4 preamplifiers to one driver
⇒ By now all 6600 chips are measured with summing 8. The summing 4 measurement is in progress. 5600 chips are measured, the remaining will be finished at end of October.
⇒ 7% of chips dead, 80% keep HEC specifications

4.5 Preamplifier and Summing Boards

⇒ 12 to 16 chips/PSB, 5 PSBs/module
⇒ 320 PSB / HEC, 134 produced
⇒ 59 tested in liquid N, 6 PSB/load (2 days)
⇒ 2 loads/week = 12 PSBs

Figure 7  PSB test setup
4.6 PSB Test procedure

The production includes a visual inspection after the cleaning process. Warm and cold functional tests of each board have to prove, that no chip has been damaged by handling or soldering, before the PSBs are measured by the automated setup in the cryostat. The PSBs are inserted in groups of six, the cryostat is evacuated, cooled and filled with liquid nitrogen. A full measurement of all channels is carried out according to ATLAS quality specifications and all data are recorded for later reference. Then the nitrogen is removed and the cryostat warmed up. The whole procedure lasts about 2 days.

4.2.2 Results

Even if the statistic up to now is low, we can see already a trend. We found 10 problems at 134 boards, mainly bad soldering. 3 chips out of 1680 (on 59 PSBs) did not meet their specifications in cold.

5. TESTS at CERN

5.1 Modules and Cold Electronics

PSBs are installed on the modules and undergo the foreseen procedures in the cryostat. If no problems show up, the boards remain in position and the complete modules with electronics are stored until the assembly of the wheel.

5.2 Entire Electronics Chain

Beside its main purpose as a test and calibration tool, the setup at CERN offers valuable possibilities for test of electronic circuitry in an environment comparable to the situation at ATLAS.

In contrast to the other liquid argon calorimeters the preamplifiers and summing stages of HEC are inside the cryostat and emerged in the liquid argon. The motivations for the cold electronics were:

* less thermal noise
* short input cables reduce pickup
* local summation requires less feedthroughs
* less interference from digital part

The front-end boards (FEB) outside are standard, with the only exception that preshapers are mounted at the signal input instead of warm preamplifiers. A pole-zero cancellation in these hybrid circuits compensates the effect of different gap capacitances on the signal rise time.

A gain stage with an appropriate time constant delivers the correct signal shape, amplitude and polarity for the following monolithic shaper.

5.2.1 Final Setup at ATLAS

The FEBs are mount in the front-end crates, which are an integral part of the Faraday cage (cryostat). The output signals are transmitted to the data acquisition (DAQ) via optical links (Fig. 8).

5.2.2 Test Setup at CERN

As the final FEBs are not yet available and the link to the DAQ is still missing, we applied FEBs which contain only a subset of the final circuitry, namely preshapers, monolithic shapers and drivers for coaxial cables. The analog to digital converters (DAQ) are contained in a separate crate together with a VME interface for the Test DAQ (Fig.9). An additional branch has been established which delivers the same data format as the final FEB. If required, transmission to the central DAQ will be possible, in parallel to current local test activities.
5.3 Results

The mechanics of the front-end crate FEC which we have there, is far from the final one. It has no top cover and at our first run during this year there was not even a base plain. The cables, coming from the feedthrough have been connected directly to the inputs of the FEB. As a consequence we had a high level of coherent noise. After installation of a base plain the coherent noise was reduced dramatically. The total noise of all channels is shown at fig. ... There are a few channels (1, 100, 200 for example) which have excessive noise. We tried to find the nature and origin of this noise. The fig. ... and ... show a the auto-correlation function of a good and a noisy channel. We find that the excessive noise is not white, but there must by an oscillation. When the power of the preamplifiers was switched off, the white noise of all channels diminished but the oscillations remained. The origin is obviously not a preamplifier. It seems that the inputs of the pre-shapers are sensitive to capacitance and the edges of connectors or strip-lines are not perfect (wrong impedance). This has to be improved. At the correlation plot (fig. ...) we see that the bad channel influences the next neighboring channels.

![Figure 10: Total noise RMS at input of ADCs](image)

![Figure 11: Auto-correlation good channel](image)

![Figure 12: Auto-correlation bad channel](image)

![Figure 13: Cross-correlation](image)

6. References

1. Cold Electronics for the Liquid Argon Hadronic End-Cap Calorimeter of ATLAS, presented by L.Kurchaninov, VIII International Conference in High Energy Physics
Photodiode read-out of the ALICE Photon Spectrometer PbWO$_4$ crystals

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Abstract: The PHOton Spectrometer of the ALICE experiment is an electromagnetic calorimeter of high granularity consisting of four detector modules with a total of 17280 lead-tungstate (PbWO$_4$) crystals of dimensions 22x22x180 mm$^3$, read out by large-area PIN-diodes with very low-noise preamplifiers. The crystals are operated at $-25^\circ$C to increase the crystal light yield a factor of ~3 higher than at room temperature. A 16.1x17.1 mm$^2$ PIN photo-diode, optimized for the PbWO$_4$ emission spectrum at 400-500nm, has been developed. The charge sensitive preamplifier is built in discrete logic with two input JFETs for optimum matching with the high capacitance (~150pF) PIN-diode. The PIN-diode and preamplifier are integrated by mounting them to common ceramic frame. Coupled to a matching shaper circuitry, the ENC measured at the operating temperature is less than 600 e$^-$. Beam tests demonstrate that the required energy resolution of the PHOS is reached.

1. Introduction

The PHOS (PHOton Spectrometer) of the ALICE experiment[1] is an electromagnetic calorimeter of high granularity optimized for measuring photons, $\pi^0$'s and $\eta$ mesons in the momentum ranges $\sim$0.5-10, $\sim$1-10 and $\sim$2-10 GeV/c, respectively. Furthermore, PHOS will also detect charged and neutral hadrons: pions, kaons, protons, neutrons and antineutrons. For additional rejection of charged hadrons a charged-particle veto detector is placed in front of the PHOS detector. The design and physics performance of PHOS calorimeter are described in [2].

![PHOS](image1)

**Figure 1.** The ALICE detector with PHOS calorimeter.

![PHOS](image2)

**Figure 2.** The geometry of the PHOS calorimeter.

1 ENC = Equivalent Noise Charge
2.1 Properties of PbWO₄ crystals

Lead tungstate PbWO₄ (PWO) is a fast scintillating crystal with a rather complex emission spectrum with two main components: a blue component peaking at ~420 nm and a green component peaking at ~500 nm. The light yield of PWO at room temperature is low compared with other heavy scintillating crystals, for instance BGO. However, the yield depends strongly on the temperature with a coefficient of ~-2% per °C. At the selected operating temperature for PHOS at -25 °C the light yield is about a factor of 3 higher than at room temperature.

<table>
<thead>
<tr>
<th>Table 1: Properties of PbWO₄</th>
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<tbody>
<tr>
<td>Density</td>
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<tr>
<td>Radiation length</td>
</tr>
<tr>
<td>Interaction length</td>
</tr>
<tr>
<td>Molière radius</td>
</tr>
<tr>
<td>Melting point</td>
</tr>
<tr>
<td>Hardness</td>
</tr>
<tr>
<td>Refractive index along ζ axis (λ = 632 nm)</td>
</tr>
</tbody>
</table>

The optical and mechanical properties of PWO crystals have been extensively studied as part of the PHOS R&D program, see [2]. An optimization of the crystal growth, annealing and machining technology has been carried out. In a light-yield measurement of more than 200 crystals, performed with a²²Na radioactive source, the relative width of the light-yield distribution was ~10%. In radiation damage studies no irreversible processes were observed during irradiation up to doses above 1000 Gy; the initial light transmission property of the samples was restored by heating to 200 °C.

3. The PHOS photodetector

3.1 Energy and spatial resolution requirements

In order to reach the energy and spatial resolution requirements for the PHOS detector, the following conditions must be met:

- To achieve a sufficient high light yield the crystals will be operated at -25 °C with a stability of 0.3°C.
- At this operating temperature the ENC noise in the PIN photo-diode unit must be less than 600e⁻. This is a very low value taking into account the high capacitance of 150-200 pF of the large PIN-diodes.
- The dead zones between neighbouring crystals should not exceed 0.6 mm and the material in front of the detector must not exceed 5% of a radiation length, which is equivalent to 4 mm of Al.

3.2 The PHOS PIN photo-diode

In collaboration with the PHOS project, the company AME¹ has designed and produced a PIN photo-diode optimized for the cross-section and spectral response of the PHOS PbWO₄ crystal [3]. The PIN-diode has an active area of 17.1x16.1 mm² and is fabricated on n-type Si material of thickness 280 µm. The wafer specific resistivity is between 3000 and 6000 ohm-cm, which corresponds to a depletion voltage of ~70V. The dark current is ~5 nA. The PIN-diode response is optimized for the spectral region 400-500 nm in order to match the emission spectrum of the crystal, see Figure 3. The diode capacitance is ~150 pF.

3.3 Mounting of PIN-diode and preamplifier

The PIN-diode is mounted on a ceramic substrate 0.65 mm thick. On this substrate the diode is surrounded by a ceramic frame with outer dimensions 19.5 x 19.5 mm². The frame is 0.5 mm high with wall thickness 1.1 mm. The preamplifier PCB of dimension 20x20 mm² is attached to the back side of the frame using SMD technology, and bonded to the PIN-diode. The PIN-diode and the bondings to ground and preamplifier are protected by an optically transparent epoxy layer.

Table 1: Properties of PbWO₄

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Density</td>
<td>8.28 g/cm³</td>
</tr>
<tr>
<td>Radiation length</td>
<td>0.89 cm</td>
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<tr>
<td>Interaction length</td>
<td>19.5 cm</td>
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<td>Molière radius</td>
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<td>Melting point</td>
<td>1123 °C</td>
</tr>
<tr>
<td>Hardness</td>
<td>4 Moh</td>
</tr>
<tr>
<td>Refractive index</td>
<td>2.16</td>
</tr>
</tbody>
</table>

Figure 3. PbWO₄ emission spectrum and quantum efficiency of the PHOS D8501 PIN-diode.

Figure 4. Mechanical mounting of the PIN-diode and preamplifier. The connector P1 carries power, bias voltage and preamplifier output.

1 AME AS, POB 83, 3191 Horten, Norway
3.4 The preamplifier

For obtaining an ENC noise value of less than 600e− with the large area PIN-diodes a PHOS specific preamplifier has been developed.

The circuit diagram is shown in Figure 5. The charge sensitive preamplifier (CSP) is an operational amplifier with the feedback capacitor C10 and with two JFETs (BF861A) T1 and T2 at the input. Using two JFETs in parallel gives the lowest noise for detector capacitance >100 pF, see section 3.6. The resistor R3 is direct current feedback and determines the full time of the CSP’s output signal which has been set to 200 µs. The drain of T1 and T2 feeds the emitter of transistor T3, whose base potential determines the operation voltage of the JFETs. The operating currents of T1 and T2 are determined by the resistors R4 and R5. The characteristics of the JFETs determine the preamplifier’s noise level and output pulse rise time. The CSP is supplied from +12V and -6V. The power consumption is <200 mW. A detailed description is given in [4].

3.5 The shaper

A prototype shaper has been designed and built in discrete logic. The shaper circuit is shown in Figure 6. It comprises three amplification stages with a gain equal to 7 for each stage. The measured equivalent noise referred to the shaper input is 12 µV r.m.s. The input differentiation stage includes a ‘pole-zero’ compensation. Calculations for a PIN-diode with C ~150 pF and a leakage current <1 nA under cooling, gives a noise corner time constant of 6 µs. For this value the optimum time constants of differentiation and integration are 3.36 µs.

3.6 Electronic noise measurement

The noise sources and characteristics of several preamplifier circuits and the preamplifier-shaper chain have been extensively studied, both experimentally and by SPICE simulations. Some of the results are presented in Figure 7.

Figure 5. Circuit diagram of the preamplifier.

Figure 6. Circuit diagram of the PHOS prototype shaper.

Figure 7. Measured and calculated ENC values.
A: ENC vs. C\textsubscript{i} for a single JFET circuit
B: ENC vs. C\textsubscript{in} for a dual JFET circuit
C: ENC vs. shaping time

The PHOS preamplifier can be used with a wide range of PIN-diodes. As shown in Figure 7 the preamplifier with
one JFET in the input stage has the lowest noise levels for detectors with \( C_{in} < 100 \) pF. For detectors with \( C_{in} > 100 \) pF the circuit with two input JFETs in parallel gives the lowest noise. Figure 8 shows calculated curves for ENC vs. noise source and \( C_{in} \) for a dual JFET input stage. It is seen that the largest term is \( 1/f \) noise. This noise is mainly determined by the technology of making FETs.

Figure 8. Calculated noise terms vs. input capacitance.

4. Integration of the photodetector

The mechanical integration of the PbWO\(_4\) crystal and the PIN-diode with preamplifier is shown in Figure 9.

The front side of the PIN-diode is glued onto the end-face of the PbWO\(_4\) crystal with optically transparent glue\(^1\). Each crystal is wrapped in White Tyvek to ensure maximum light collection efficiency and optical insulation between the crystals. The crystal pitch is 22.6 mm, which includes the wrapping and the crystal side cover. The construction of the crystal detector unit is shown in Figure 10. Eight crystal detector units are assembled in one row and constitutes the basic mechanical assembly unit, the strip unit. One PHOS module comprises 90 x 6 strip units.

A PHOS module is divided into a ‘cold’ and a ‘warm’ volume by thermoinsulation. The crystal units in the ‘cold’ volume are operated at -25 °C. The operating temperature is provided by forced cooling using a 1.2 propanedol-water coolant. The power dissipation inside the ‘cold’ volume from the preamplifiers is \( \sim 1 \) kW per PHOS module.

5. Laboratory and beam tests

The PHOS photo-detector R&D program was started in 1995. The first tests with a cooled crystal assembly were carried out in 1996, using a 10x10 mm\(^2\) PIN-diode and two prototype preamplifiers.

A laboratory measurement on a detector matrix of 64 units is presented in Figure 11. At -25 °C the measured ENCs are between 450-550 e\(^-\), well below the required value of 600 e\(^-\).

\(^1\) Melt-Mount Quick-Stick, Cargille Laboratories, USA
Figure 12 shows the spectrum registered from a 180 mm long crystal in a 10 GeV electron beam. No significant tail from the ‘punch-through’ effect is seen.

A summary of all beam test results are presented in Figure 13. They demonstrate that the energy resolution requirement defined in the ALICE Technical Proposal has been reached.

6. Read-out electronics

Integrated read-out electronics for the PHOS detector - shaper, ADC and front-end buffering - are under development.

7. Conclusions

The R&D program for the photodiode read-out of the PHOS electromagnetic calorimeter was started in 1995. Choosing PbWO₄ crystals of size 22x22x180 mm³ as detection material, operated at ~25 °C to increase the light output yield, and coupled to specially developed PIN-diodes and preamplifiers, have led to a design that satisfies the spatial and energy resolution requirements for the PHOS electromagnetic calorimeter.

8. References

[3] D-8501 Custom Photo Diode for the PHOS Project, AME Data sheet, see also http://www.ame.no/

Acknowledgement

The development of the PHOS PIN photo-diode and the preamplifier was funded by the Norwegian Research Council.
THE ATLAS CALORIMETER PREAMPLIFIER: PERFORMANCE, RADIATION DAMAGE, ELECTROSTATIC DISCHARGE RESISTANCE, RELIABILITY AND MANUFACTURING ISSUES*

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Brookhaven National Laboratory, Upton, NY 11973-5000

Abstract

The requirements, design, measured specification of the ATLAS liquid argon (LAr) calorimeter preamplifiers are reviewed. The experience gained so far in production, the quality assurance and testing, as well as the reliability estimate according to MILSTRESS standard will be discussed.

1. INTRODUCTION

The preamplifiers are the first amplification stage in the LAr readout architecture, which set the noise performance of the calorimeter. They amplify the analog signal generated at the calorimeter electrodes.

Figure 1 shows a picture of the liquid argon Front-End Board (FEB). The preamplifiers are at the input of the board and are connected via a transmission line to the detector electrodes. The space allocated on the FEB for the preamplifiers have dictated the aspect ratio of the circuits and, up to certain extent, the technology adopted for the production.

Figure 1. Photograph of a FEB board. The input signals come into the board from the two external connectors at the bottom. The preamplifiers are immediately above the input connectors. Eight hybrids are encircled in the picture.

Each FEB contains 128 channels of amplification, 64 channels on each side of the card grouped in two block of 32 channels each. The preamplifiers are moreover grouped in block of four channels and have been realised in a hybrid package the dimension of which are 53.3 mm in length and 23.0 mm in width. The preamplifier hybrids are independent units that plug into the FEB.

About 190,000 read-out channels or about ~ 47,500 hybrids are needed for the LAr calorimeter.

More than one type of preamplifier/hybrid is required to accommodate the different characteristics of the detector. The detector structure (impedance, capacitance, etc.), the estimated maximum energy deposited per readout cell as a function of rapidity, together with the need of a maximum output signal of about 3 to 4 Volt, determine that three types of preamplifiers must be used. These three type of preamplifiers share a same general circuit diagram which has been properly “optimised” for the different sections of the calorimeter.

2. PREAMPLIFIER DESIGN

2.1 Requirements and Specification

The preamplifier requirements and specification are described in detail in the ATLAS LAr Technical Design Report (TDR) [1].

The most important ones can be summarised as follow:
- Noise: as low as possible with respect to pile-up, $R_{\text{noise}} = 10 \Omega$, typical Equivalent Noise Current (ENI) values are in Table 1.
- Uniformity: TDR: < 5 % in amplitude for trigger sums (< 1 % meas.), TDR: < +/- 2 ns timing (< +/- 1 ns meas.).
- Power dissipation: TDR: < 100 mW/ch.
- Environment: must tolerate 20 Gy/year (2 krad/year) and $10^{12}$ n/cm²/year.
- Reliability: < 0.5 % missing channel per year.
- ESD discharge: must withstand 4 mJ multiple discharge without damage (i.e. 2 KV on 2 nF typical).
- Stability: must be stable even in case of presence of faults in the signal chain (short, open).
- Output impedance: must be able to drive a 50 $\Omega$ load (i.e. the shaper input impedance).
- Dynamic range: up to 10 mA, depending on rapidity range.

*The U.S. Department of Energy supports this work: Contract No. DE-AC02-98CH10886.
Table 1: Typical noise values

<table>
<thead>
<tr>
<th>Preamp type</th>
<th>ENI [nA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 Ω / 1mA</td>
<td>50 @ C₀ = 330 pF, tp = 46 ns</td>
</tr>
<tr>
<td>25 Ω / 5mA</td>
<td>125 @ C₀ = 1500 pF, tp = 53 ns</td>
</tr>
<tr>
<td>25 Ω / 10mA</td>
<td>270 @ C₀ = 2200 pF, tp = 40 ns</td>
</tr>
</tbody>
</table>

2.2 Preamplifier circuit

The LAr preamplifiers are coupled to the detector by a transmission line. As the signal duration is long compared to the shaping time, current preamplifiers are used which provide a voltage output directly proportional to the input current.

The main characteristic of the ATLAS preamplifier is the use of a local feedback in the input stage to attribute the functions of low noise and high dynamic range to two different transistors. This circuit configuration allows to improve the linearity and to reduce the noise while reducing the power dissipation by a factor of three (to about 50 mW) with respect of the first generation RD3 preamplifier [4]. The gain (i.e., the transresistance) and the input impedance can be chosen independently without changing the power supply voltages and power dissipation.

The principle of coupling a preamplifier to a high capacitance detector and a detailed description of the ATLAS implementation are described in ref. [2, 3]. The circuit schematic is shown in Figure 2.

2.3 Preamplifier Technology

The preamplifiers have been manufactured by means of thick film hybrid technology. This technology is a well-known technology with predictable time schedule for production and high reliability, as proven in many high-energy physics experiments. Moreover each device can be chosen to optimise its function (e.g. low noise) and many different type of devices (NPN, PNP, decoupling capacitors, etc.) are available.

Use of a more advanced monolithic technology was rejected because of the higher development costs (a complementary bipolar process featuring low noise, radiation resistant transistors was necessary) and higher risks associated with the research and development, both in terms of performance and schedule.

The hybrid design has been carried out with very conservative design rules (10 mils line, 10 mils separation) to both expand the pool of manufacturers and to improve the production yield. The layout is shown in Fig. 2.

3. PREAMPLIFIER CHARACTERISTICS

The hybrid preamplifier design has been tested and verified through the productions of 200 prototypes first and 1600 hybrids to equip LAr Mod0, subsequently. The information gathered during these preliminary phases would be used to optimise the final production.

Gain, peaking time, noise and input impedance were the main parameters of interest. Radiation tolerances to ionising radiation and to neutrons were also measured.
The results obtained are summarised in the following sections.

Finally stability analysis was performed. The preamplifiers were found stable for any value of cable length and detector capacitance foreseen for the LAr calorimeter [5].

3.1 Parameter Distribution

The preamplifier characteristics meet and exceed the specification. Figure 3 illustrates peaking time, amplitude and noise distribution for the preamplifier type $Z_n/I_{max} = 50\,\Omega/1\,mA$.

All the preamplifiers are within +/- 3σ from the average value. Similar results were obtained for the other preamplifier types.

The preamplifier input impedance for each hybrid type is summarised in Table 2.

<table>
<thead>
<tr>
<th>Preamp Type</th>
<th>$Z_n$</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 $\Omega$ / 1 mA</td>
<td>51.4 $\Omega$</td>
<td>+/- 2.9 %</td>
</tr>
<tr>
<td>25 $\Omega$ / 5 mA</td>
<td>25.8 $\Omega$</td>
<td>+/- 1.8 %</td>
</tr>
<tr>
<td>25 $\Omega$ / 10 mA</td>
<td>26.3 $\Omega$</td>
<td>+/- 1.7 %</td>
</tr>
</tbody>
</table>

3.2 Preamplifier Radiation Tolerance

Expected gamma doses over the life of the preamplifiers is estimated to be approximately $2 \times 10^4$ rad silicon. It is expected that the total possible dose would be no more than five times this number or $10^5$ rad. Two hybrid preamplifiers under power were exposed to a total of $10^5$ rad. One was a 50 $\Omega$ impedance device and the other was a 25 $\Omega$ impedance device. Both hybrids were measured for gain, peaking time, ENI, and input impedance before irradiation and after total doses of $5 \times 10^4$ and $10^5$ rad of $^{60}$Co gamma radiation. Gain, peaking time, and ENI changed by less than the measuring error for both hybrids after $10^5$ rad.

Average input impedance (of 4 channels) at selected doses for the two devices is shown in Table 3.

<table>
<thead>
<tr>
<th>Dose Type</th>
<th>$Z_n$</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 $\times 10^4$ rad $^{60}$Co</td>
<td>50.1 $\Omega$ (2.3% change)</td>
<td>48.8 $\Omega$ (4.9% change)</td>
</tr>
<tr>
<td>50 $\times 10^5$ rad $^{60}$Co</td>
<td>25.3 $\Omega$ (0.4% change)</td>
<td>25.2 $\Omega$ (0.8% change)</td>
</tr>
</tbody>
</table>

Preamplifier hybrids were irradiated with fast neutrons at the SARA facility, Grenoble [6].

No noise degradation was measured till a fluence of $5 \times 10^{13}$ n/cm$^2$. The neutrons induce a degradation of the forward-gain $\beta$ of the NEC856 (NPN) transistors used in the circuit. The $\beta$ degradation follows the Messenger-Sprat relation and, at first order, is inversely proportional to $f_c$.

The impact of the $\beta$ degradation of transistors on the preamplifier gain is very small. The 25Ω preamplifiers exhibit about 3% of gain loss after $1.1 \times 10^4$ n/cm$^2$, while the 50Ω preamplifier, has about 7% gain loss after the same fluence.

The measurement of input impedance of all irradiated preamplifiers indicated that there is no stability problem with irradiation. All of them have positive real part of input impedance in a frequency range 1-200 MHz.
4. QUALITY ASSURANCE

4.1 Burn-in study

The first series of hybrid produced (200 units) after being tested for electrical functionality was subjected to 168 hours of an environmental stress screening (or burn-in) at ambient temperature to identify and eliminate deficiencies and early failures. Moreover few hybrids (eight units randomly chosen) were fully characterised in term of gain, peaking time and noise before and after burn-in to detect any possible variation of performances due to ageing effects.

At the conclusion of the burn-in only one channel failed to meet specification. The unit failed because a PNP transistor (Q4) in the white follower broke during burn-in. After replacing the transistor the channel was tested again and it met specification.

The hybrids that were fully characterised before burn-in did not show any performance variation due to the environmental stress.

The burn-in results brought to the conclusion that the environmental conditions adopted for the test were not sufficient to rule out all the early failure mechanisms. A more extensive burn-in study was adopted for the batch of hybrids produced for Mod0. The temperature was elevated to ~ 70°C and the time were extended up to 432 hours. The combination of elevated temperature and extended time did not increase the number of failures. The only source of failures for thick-film hybrids was a “cold solder joint”.

Under the assumption that the same failure mechanism dominates in the ATLAS hybrids, was concluded that a burn-in of 168 hours at an elevated temperature of 70-80°C, will be used to eliminate all causes of infant mortality. A higher burn-in temperature/shorter time is not achievable because some of the components used in the preamplifiers are not rated for temperatures higher than 100°C, namely the inductors.

4.2 Reliability Evaluation

The reliability of the hybrids has been evaluated based on the internationally recognised method of calculating electronic equipment reliability given in “Military Handbook MIL-HDBK-217” (published by the US Department of Defense). This standard uses a series of models for various categories of electronic components to predict failure rates that are affected by environmental conditions, quality levels, stress conditions and various other parameters. These models are fully detailed in MIL-HDBK-217.

Most of the models in MIL-HDBK-217 use ten or more parameters for the calculation of the component failure rate. Commercially available programs, such as “Milstress” from ITEM software have been written to facilitate the calculation of failure rates. The calculation was performed using the Milstress software package.

The TDR specification for channel failure rate is “0.5 missing channel per year” or “868 missing channel per year”. If the worse case condition is taken, i.e. one channel missing means a full hybrid missing, the maximum tolerable failure rate per hybrid is “217 missing hybrid per year” or 0.57 frmh (where frmh stands for failure per million hours of operation) or 1.75 $10^6$ hours “mean time between failure” (MTBF).

![Figure 5. Significant component failure rates](image)

The technology/component/design adopted for the hybrids has to be evaluated against this benchmark.

The reliability prediction presented in this section is for guidance, the purpose of this calculation is to establish, by means of a consistent and uniform method, the reliability of what has to be considered a “mature design”. The calculation is based on the two methods known as “Part Count” and “Part Stress Analysis” and the following assumptions have been made:

- Most of the details used in the project are known, in term of material and components.
- In a hybrid package, resistors and inductors are considered to contribute insignificantly to the overall hybrid failure rate and for this reason are assumed to have a failure rate of zero.
- The hybrid temperature has been assumed to be know and equal to 35 degree centigrade.
- The power dissipation of each hybrid component has been estimated from an actual hybrid sample and from design analysis. It has been compared with the maximum power from the component data sheet to obtain the “stress factor” for each individual hybrid component.
- The stress factor has been always rounded up to the second figure.
- The hybrid quality has been chosen equal to “class B microelectronic” as defined in Mil883-C screening procedure method 5004.9.
- The quality of the individual component used for the manufacturing has been set to “industrial grade, RE”.
- The environment has been set to “ground benign”.

Based on this information a failure rate of 0.48 frmh has been calculated. This result shows that the solution adopted has a predicted reliability similar to the one requested by ATLAS TDR.

Figure 4 shows the significant component failure rates of a hybrid. The transistor Q5 (the NPN NE856) used in the white follower is the single largest contributor to the hybrid failure rate.

The failure rate is also temperature dependent as shown in Table 4.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>frmh</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.44</td>
</tr>
<tr>
<td>30</td>
<td>0.48</td>
</tr>
<tr>
<td>40</td>
<td>0.59</td>
</tr>
<tr>
<td>50</td>
<td>0.70</td>
</tr>
<tr>
<td>60</td>
<td>0.76</td>
</tr>
<tr>
<td>70</td>
<td>0.93</td>
</tr>
</tbody>
</table>

4.3 Highly Accelerated Life Tests

As an aid in testing the reliability and design limits of the preamplifier a Highly Accelerated Life Test (HALT) of a selected group of preamplifiers was performed at a Qualmark Corporation facility in Marlborough, Massachusetts. The purpose of this testing process was to induce failure in the tested product(s) in a non-destructive way so as to expose weaknesses in design or manufacture. This information then can be used to improve the devices and to select the manufacturing processes used in producing the devices.

Twelve preamplifiers, six 50Ω / 1mA and six 25Ω / 5mA, were mounted on a board with power and signal input/output lines so that the response could be monitored during the test. The board with the mounted preamplifiers was inserted in a computer controlled environmental chamber and tightened to a “platform” which can be vibrated by simultaneous triaxial shakers in a frequency range of 0 to 2 kHz.

The testing process was divided into 3 stages. The initial stage consisted of varying the temperature of the preamplifiers, first gradually and then in rapid temperature cycling (between -100 °C and 100 °C). The second stage involved accelerating the preamplifiers at a fixed temperature (30 °C) starting at 5 Grms (Gravities root mean square) and increasing the acceleration in steps of 5 Grms up to a maximum of 50 Grms. In the final stage, both acceleration and rapid thermal cycling were combined.

The only preamplifier failure during the test was observed after many thermal cycles and at a vibration ~ 50 Grms, where all four channels of one hybrid became intermittent. The failure was caused by the failure of the +3 Volt power pin. The edge pin solder joint broke due to the “fatigue” accumulated in the test. At the conclusion of the test the pin was replaced and the hybrid was found working in specification.

A visual inspection identified that some of the hybrid power pins (the four pins on the longest side of the hybrid) were not centred into the pad and they were soldered to an angle in respect to the ceramic substrate. The pins were the last components to be assembled were hand-soldered in place. The input/output pins on the contrary were assembled through “dipping and flowing” in one step operation. The pin assembly is the less automated part of the manufacturing process. A more stringent inspection will be required for the final production.

5. CONCLUSIONS

The design and technology used for the construction of the LAr calorimeter preamplifier have been extensively tested on 1,800 hybrids. These devices have met all physics requirements. No changes in design are expected. The hybrid quality has been successfully inspected. The final hybrid production is in progress.

6. ACKNOWLEDGMENTS

The authors wish to thank F. Densing for the realisation of the hybrid layout and Qualmark Corporation personnel for the assistance during the tests of the preamplifiers.

7. REFERENCES

1. Technical Design Report [Sec. 10, 401-410].
6. G. Battistoni et al., ATLAS internal Note LARG-NO-083.
The Front-End Electronics for LHCb calorimeters

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1. ABSTRACT

The electronics for the electromagnetic and hadronic calorimeters of LHCb is under design. The 32 channel front-end board offers the complete front-end and readout electronics for every channel including original shaping, 12bit-40MHz ADC, digital filtering and latency for level 0 and level 1 triggers. The clipped PM input signal is integrated within 25ns, but also delayed then subtracted to itself 25ns later what allows performant pile up independence. This board also includes the first processing levels of the L0 calorimeter trigger.

A 16 channel prototype board has been designed and used at CERN in test beam last summer.

2. INTRODUCTION

The electromagnetic and hadronic calorimeters currently designed for LHCb are lead-scintillator sandwiches employing the “Shashlick” technology. The output of the plastic fibers is equipped with phototubes. The readout system will have to deal with 6000 channels for the Ecal and 1500 for the Hcal.

3. REQUIREMENTS

The main requirement for LHCb electronics is the pile-up rejection. Indeed the residue of a previous signal on the current sample has to be less than 1% after 25ns. This implies to work both on the PM signal and on the shaping. Shaped data has to be sampled at 40MHz on 12 bits then to undergo pedestal subtraction for rejecting LF noise and to be transcoded within LUTs into energy over 8 bits for trigger data and 12 bits for readout data. The latter has to be buffered during the L0 latency, to be derandomized and then rebuffered for the level 1 latency. After the level 1 trigger, an extended zero suppression has to be performed before sending the formatted event to the DAQ.

There are also trigger elements sitting in the front-end crate. The first stages concern the seek for local maxima inside groups of 512 channels, with a validation by the Preshower and Pad Chamber data.

4. FRONT-END OVERVIEW

Fig 1 describes the Front-End crate and its main interconnections. The PM side elements are connected to the Front-End board through 10 meters of coaxial cables. There are 16 FEBs in the crate, each receiving 32 signals. The output of these boards are connected to the custom backplane, sending signals using LVDS levels to the Event Filter. This board is in charge of performing the advanced zero suppression and the event formatting after level 1. Data is then sent to the DAQ through optical links. The Crate Controller is in charge of driving the serial link which is used for loading the hardware and distributing the TTC signals. At last, the Trigger Validation Board receives the local maxima coming out from the FEB, then validates it with the Pad Chamber and Preshower information and finally searches for the residual maxima over the two half crates. The resulting words are sent to the Trigger Main Selection crate through optical links.

5. THE FRONT-END BOARD

Fig 2 shows the block diagram of the 32 channel Front-End board. This is a 9U board using VME mechanics but deserting the VME bus. This one will be replaced by a serial bus which has still to be defined.

Let’s follow the main data path inside the board. It starts with the four 8-channel coaxial input connectors. Then signals goes into the PM and cable compensation before entering the analog chip. After a 12bit ADC conversion, data undergoes a pedestal subtraction with the smallest of the two previous samples. This subtraction is intended to reduce the high bandwidth noise of the integrator, and the two samples are used not to degrade the pile-up rejection. Then data is converted into energy...
within two LUTs, one for the trigger which outputs 8 bit words, the other for the readout data which outputs 12 bit words in a pseudo floating format. The latter data is then sent to the L0 latency pipeline, L0 derandomizer and L1 latency buffer. After L1 trigger, it is sent across the backplane using LVDS levels towards the Event Formatter.

At the right top of the board, trigger data is first added in squares of 4 cells while preserving the original granularity, then filtered looking for the local maximum on the board. The latter is sent with its address (total of 13 bits) using LVDS levels towards the Trigger Validation Board.

Fig 2: block diagram of the Front-End board

Beside those data paths, some utility functions have been implemented. One can adjust the sampling time of every ADC on the board thanks to programmable delay chips with a precision of 1 ns. A functional analog calibration has also been implemented to allow checking of the complete readout chain. This has already been useful during the test beam operations.

6. THE FRONT-END ELEMENTS

The purpose of those elements is to shape the PM pulses in less than 25 ns to avoid electronics pile-up. The specifications on both extremities are the following:

- At the input: the PM maximum current is 20 mA over 25 ohms.
- At the output: the ADC input dynamic range is 1 V under 250 ohms.
- The residue after 25 ns has to be smaller than 1%.
- The sampling area should cover ± 3 ns with a 1% precision.
- The RMS noise has to be < 1 ADC count (250 uV).
- The deterioration of the statistic fluctuation due to the apparatus has to stay under a factor 2.

To fulfill the above requirements, two problems will have to be solved. The first one concerns the PM signal. If one looks at Fig 3, the PM output current has a fast rise time but a slow decay that goes over at least the two consecutive samples at 40 MHz. It thus needs to be pulled to zero after 10 ns to ensure the zero pile-up requirement. The remaining area is on the order of 60% of the original one.

Fig 3: PM output pulse

To realize this cut on the signal, the clipping circuit on the left of Fig 4 will be used. It consists in a short 1 meter cable located at the output of the PM base. It derivates the signal towards a variable network which will send back an inverted part of the signal. As both the source and reflected signals are negative exponentials, their superposition leads to zero. The demonstration is given on the top plot of Fig 5.

Fig 4: Front-End Electronics

Now that the input signal has been shaped, we have to measure the energy deposited in the calorimeter. The corresponding information is the area of the PM signal. The best way to measure it without deteriorating too much the statistic fluctuation is to integrate this signal in a capacitor (Cf). The induced difficulty becomes to empty this capacitor. Two ways are possible:

- Use a switch mounted in parallel but this system induces a dead time when the capacitor is being emptied, what implies the use of two integrators in parallel and a multiplexor.
Subtract in a linear way the signal to itself thanks to a specific configuration.

The latter is the chosen solution. The configuration appears in the middle of Fig 4. The input signal of the analog chip is derivated, delayed by 25ns, then subtracted to itself thanks to the differential buffer. The latter has also in charge the division of the input current to adapt it to the small value of \( C_f \) which ensures a fast rise time to the integrator.

Between the buffer and the integrator, there is an external AC coupling that allows to separate the DC levels. The small value of \( C_f \) allows to load it fast and to offer a nice plateau at the top of the signal (see bottom plot of Fig 5).

The integrator schematics is based on a cascode amplifier. Its open loop gain is high (60dB), it’s fast as there is no Miller effect on the input PMOS, and it produces very low noise. On the other hand, there is a need for an emitter follower at the output not to degrade the gain by the charge impedance. In our case, as the charge is only 350 ohms, another follower has been mounted on the board using discrete elements. The decay time of the integrator is linked to the 2K resistor what leads to a value of 6us.

Fig 5 : simulated input and output pulses of the integrator

Fig 7 shows the layout of the current version of the analog chip. Up to now, three versions have been submitted in only 6 months. This is due to the pression of the test beam of last summer. The main difficulty that appeared was a resistor in the gate access to the input PMOS of the integrator. This was due to a bad polysilicon design and introduced noise and instability in the chip response. This problem was fixed and the chips received two days before the test beam were fully operational. When mounted on test bench at LAL, the chip offered the results shown in Fig 8.

Fig 6 : schematics of the analog chip.

Fig 8 : real signals on test bench

On this plot, the input pulse derives from a generator and is clipped as the real PM signal. The output signal shows a nice flat top in concordance with the simulations. The global preliminary results from this test bench are given in Fig 9.
These results show a good adequation between simulation and real circuit, except for the gm of the input transistor. This is due to simulation models and also explains the mismatches in the rise time and the input impedance of the integrator.

7. THE PROTOTYPE FRONT-END BOARD

The prototype FEB shown on Fig 10 is a 16 channel board which has been designed targeting the test beam of last summer. It comprises the same readout chain excepting the L1 buffer. Moreover, some extra functionalities as the spying of the raw data at the output of the ADCs have been implemented. This allows to crosscheck offline the subtracted data with their source.

Another interesting purpose of this board is the configuration state machine implemented in the VME interface Altera. It allows to configure all the other FPGAs on the board in an interactive way, permitting to debug the board easily (even far from home through ftp) and also to modify the functionality of the FPGAs for test purposes.

8. THE TEST BEAM Environment

This board was installed on test beam in the setup shown in Fig 12.

One can remark here that two VME master crates can be connected to the remote electronics. This is intended for debugging and monitoring purposes. Indeed, when electronics is installed at CERN for test beam, local DAQ still needs to be debugged. The MacIntosh interactive test software, which also provides data acquisition, and the possibilities of live insertion of the SPAC bus thus allow to start the debugging phase of the hardware while permitting crosscheck of the readout data with the one read by the standard DAQ. This is then a very efficient way of setting up the system in a very short time.

**Fig 9**: first results from the test bench

**Fig 10**: prototype of the Front-End board

**Fig 11**: top layer of the prototype FEB

**Fig 12**: test beam setup at CERN

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**Table 1:** Simulation Results vs. Current Test Bench Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Current Test Bench</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>1.4V</td>
<td>1.4V</td>
</tr>
<tr>
<td>Non Linearity</td>
<td>0.9%</td>
<td>to be measured</td>
</tr>
<tr>
<td>Residue after 25%</td>
<td>&lt;0.5%</td>
<td>&lt;1% (underest -3%)</td>
</tr>
<tr>
<td>RMS Noise after</td>
<td>1 ADC Channel</td>
<td>1.2 ADC Channels</td>
</tr>
<tr>
<td>subtraction</td>
<td>(± 25nV)</td>
<td>(± 30mV)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>40mW/Channel</td>
<td>30mW/Channel</td>
</tr>
<tr>
<td>Open Loop Gain</td>
<td>-60dB</td>
<td>-60dB</td>
</tr>
<tr>
<td>Gain (PM/0/5)</td>
<td>~34mV/A/V</td>
<td>~34mV/A/V</td>
</tr>
<tr>
<td>Fall Time</td>
<td>6ns</td>
<td>6ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>1.2ns</td>
<td>5.5ns</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>~90Ω</td>
<td>~240Ω</td>
</tr>
<tr>
<td>Determination of statistical fluctuation</td>
<td>&lt;2</td>
<td>&lt;1.2</td>
</tr>
</tbody>
</table>
9. TEST BEAM RESULTS

The first measurements made on test beam were related to the signal coming from the PMs. It is plotted on top of Fig 13.

![Fig 13: real signals on test beam](image)

One can remark that the width of the signal is much larger than on test bench. This was due to some problems with the quality of the fiber inside the Shashlick and of the microcoaxial cable. Nevertheless, the shape at the output of the integrator (bottom plot) looks quite good with a large top where sampling can be clean.

The following step was to compare the new 40MHz electronics with the "old" LeCroy one. Data was thus taken on the same channel through the two different paths. The comparison is plotted on Fig 14.

![Fig 14: new electronics vs LeCroy ADCs](image)

The straight line proved the good level of functionality of the new electronics and data was then taken with the latter.

Fig 15 presents the results of an ECal run. 6 samples are plotted successively. The signal is centered on the sample 5 (third one). On the sample 3, one can observe the noise distribution. This corresponds to a RMS of 2.5 ADCC. The sample 4 shows that the signal is wider than on the Fig 13 as there is already some data 25ns before the peak. This was due to some problems with the PM used at this occasion.

![Fig 15: 6 samples from an Ecal run](image)

On the samples 6 and 7 appears the result from the subtraction of the smallest of the two previous samples. On sample 8, we're back to the baseline.

10. NEXT STEPS OF THE DEVELOPMENT

The previous measurements made on test beam prove the consistency of the electronics which has been designed. We are currently concentrating on the various noise sources to reduce the total noise on the board under 1.5 ADCC.

The next steps of the developments for this electronics are the following:

- Concerning the Front_end Board:
  - A new version of the analog chip including a second emitter follower by early 2000
  - Implementation of the trigger part of the board
  - Study of the L1 buffering hardware
  - Extension to a 9U/32 channel board
- Study of the fast backplane using LVDS signals
- Study of the Event Filter (which provides advanced zero suppression and event formatting)
- Study of the Crate Controller (which includes serial access bus and TTC)
- Study of the Trigger Validation Board (which prepares the candidates for the L0 trigger Main Selection Crate)

11. REFERENCES

For completing the information given in this paper, one could have a fruitful look to the following notes:

- J.Christiansen, "Requirements to the L0 front-end electronics", LHCb technical note, July 30th 1999
- C.Beigbeder et al., “A Joint Proposal for the Level 0 Calorimetric Triggers”, LHCb 99-017, June 7th 1999
SELECTIVE READOUT IN THE CMS ELECTROMAGNETIC CALORIMETER

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Abstract

Algorithms suitable to reduce the volume of ECAL data passed to the CMS data acquisition (DAQ) system are investigated in terms of their performance. Various implementation scenarios are analysed which demonstrate the feasibility of the selective readout (SR) techniques proposed.

1. INTRODUCTION

The CMS Electromagnetic calorimeter (ECAL) [1] is a finely segmented detector, consisting of approximately 80000 PbWO4 crystals, organised, in the barrel region, in supermodules of 1700 crystals each. Each CMS ECAL upper level readout and trigger card, envisioned as a 9U VME module, is designed to handle 100 crystals. A single VME crate, located in the CMS counting room and consisting of 17 such cards, effectively handles an entire ECAL supermodule. The data from these 17 cards are concatenated in each crate, on an event-by-event basis, by the Data Concentrator Card (DCC), and sent to a memory which is read by the DAQ system.

If, for all channels, 10 time samples per channel (i.e., the preamplifier response for 10 consecutive 25ns bunch crossings in a window around the trigger) are to be read for each Level-1 triggered event (L1A), the ECAL will generate 2.4MBytes of data per L1A. To reduce the data volume down to 120kBytes per L1A, as required by the central CMS DAQ system, a data reduction factor of 20 must be achieved. A channel-by-channel zero suppression scheme might not be the best way to fully achieve this reduction. Only the reading of all neighbouring crystals in a shower, at least down to the noise-level of the electronics, guarantees the benefits of the high energy resolution of this detector. Also, the online extraction of an energy value from the crystal time samples would require a very good understanding of the pulse shape and pile-up effects. As the actual number of ECAL crystals containing information of use in reconstructing any given triggered event is small, a substantial reduction in data volume is possible, without any loss of information meaningful to the physics, by means of a selection of the channels to be readout per event.

An algorithmic data reduction in the ECAL has to be based on principles of calorimetric energy measurement. The energy of a showering particle is contained primarily within a compact array of crystals. Therefore, the energy reading in a compact array of crystals is a means to base a selection of crystals to be readout in an event. The region of crystals to be readout needs to be large enough to achieve the limiting angular and energy resolution of the ECAL.

2. TOWER BASED SELECTIVE READOUT ALGORITHM

To motivate the choice of a selective readout algorithm, the requirements imposed by the CMS physics goals to this detector can be summarised as follows:

- Clean identification of energetic (Et>5Gev) electrons and photons, i.e. showers contained within a compact array of crystals. For this purpose the fine granularity of the ECAL, allowing a detailed shower shape analyses, and its high intrinsic energy resolution are equally important.
- Identification of low energy clusters, \(|E_t|<1\text{GeV}\), for measurements of particles within jets or to be used in isolation criteria. This task requires the use of the fine granularity available but is less demanding in terms of energy resolution.
- Precise measurement of jets and missing transverse energy which require the readout of the full ECAL, eventually with a coarser granularity.

Considering the above, and keeping in mind that, at the Level-1 calorimeter trigger, the ECAL is organised into trigger towers, consisting, in the barrel region, of \(5\times5\) crystals, the ECAL data can be split into two potential data blocks. On one hand, a coarse-grain data block, consisting of the energy sums of all existing trigger towers, always passed to the data acquisition system; on the other hand, a fine-grain data block, consisting of the time samples of the individual crystals selected by an algorithm.

In the tower based selective readout scheme, proposed below, the energy sums in the trigger towers are used to generate the readout information. A tower transverse energy reading above a programmable threshold \(T_{\text{High}}\) will force the readout of 10 samples for all the channels in a \(3\times3\) array of trigger towers centred on the trigger tower of interest. An intermediate tower transverse energy, \(T_{\text{Low}} < E_t < T_{\text{High}}\), will force the readout of 10 samples for all the channels in that particular trigger tower. For towers with low transverse energy, only the coarse-grain data will be available.
Complementary, zero suppression is applied on a channel-by-channel basis with a threshold close to the noise level, independently of the selective readout algorithm. The zero suppression calculation is based on the peak amplitude of a prompt pulse arriving after the L1A.

3. POSSIBLE SELECTIVE READOUT IMPLEMENTATIONS

3.1 ECAL Upper level readout and trigger system overview

The ECAL upper level readout and trigger boards, called ROSE100 and described in [2], receive data digitised at 40MHz in the calorimeter very front end electronics via serial optical links operating at 800 Mbit/s. These signals are converted from optical to electrical, deserialised, and split into two parallel paths. On one hand, they are pipelined into memories, to wait for a trigger decision to proceed to the data acquisition system. Dedicated point-to-point links allow the transmission of the ROSE100 data from each module to the Data Concentrator Card in the same crate. On the other hand, they are used as input to the trigger primitive generation block, where the total trigger tower transverse energy, among other quantities, is computed.

Due to different flight paths to different parts of the detector plus different link lengths, temperature variations or mechanical stretching of links, the various trigger channels are not necessarily synchronized with each other. The synchronization circuits, placed at the output of the trigger primitive generation block, guarantee that for every subsequent processing stage the data are synchronised and belong to the same bunch crossing. The synchronization method [3] uses the LHC bunch structure to achieve synchronization. The timing adjustments are computed based on trigger data accumulated (histogramed) in each synchronization circuit, that should match the expected bunch structure. A few minutes of running should be enough to determine the settings needed for synchronization, which can be continuously monitored via the same histograms.

3.2 The Data Concentrator Card

The Data Concentrator Card performs the tasks illustrated in the functional diagram shown in figure 1: it is responsible for collecting the ECAL event data per readout crate, formatting it and transmitting it to the data acquisition system, via high speed links. The DCC allows data quality monitoring and, optionally, provides stand-alone triggers. Furthermore, the DCC plays an important role in the selective readout implementation, as described in the section below.

The DCC receives the data from the readout modules and stores it in input FIFOs (iFIFO) controlled by the Input Handlers, one for each iFIFO. The event fragments stored in the iFIFO are assembled and stored in output FIFOs (oFIFO) – the Event-oFIFO stores the data to be sent to the ECAL DAQ path, the Trigger-oFIFO stores trigger primitive data to be sent to the Trigger DAQ path. The data transfer from input to output FIFOs is controlled by the Data Concentrator (DC) Handler, which receives the selective readout information for each event as well as the L1 trigger. A list of L1 triggers waiting data transfer is kept in the DC Handler. Associated with each FIFO is also a list of events in the FIFO, updated by the relevant readout handlers.

3.3 Selective Readout implementations

In the present design, the energy of each trigger tower is compared with two (programmable) thresholds, and a 2-bit status word ("threshold flag") is set. This calculation is executed as part of the trigger logic and runs synchronously at 40MHz. These bit pairs are transferred on a dedicated bus to the corresponding DCC. Due to the selective readout algorithm presented, in which a particular trigger tower might force the readout of all crystals from a neighbouring one, there is a need to communicate selective readout information across crates, in order to cover all the submodule borders.

A possible implementation scenario is that the DCC acts as a local ‘reflector’, receiving the 2-bit words from boards within its own crate and from neighbouring DCCs, and transferring back to the boards the results of the tower selective readout decision, after performing the algorithm. By using the CMS Level-1 processing latency to exchange the selective readout information, readout may commence immediately upon the receipt of a L1 accept signal. This implementation is represented in figure 2.
Another possibility, currently under investigation and depicted in figure 3, is to implement a dedicated Centralised Selective Readout Processor (CSRP) in order to facilitate the information exchange across the hardware boundaries. The DCCs will identify the seed regions and communicate them to the CSRP where a map is created of the channels to be read. This information is returned to the DCCs where the selective readout is performed.

This scheme would allow for more flexibility of new selective readout algorithms, including the eventual use of long range correlations.

However, care has to be taken to guarantee that the selective readout decision is taken in a fraction of time small compared to the average time between L1 triggers, 100kHz, and also so that dead-time situations are avoided or minimised.

4. TOWER BASED SELECTIVE READOUT PERFORMANCE

The effectiveness of selectively reading out regions of the ECAL was studied with a full-detector Monte Carlo simulation of hard-QCD scattering events with a minimum generated parton transverse momentum of 100 GeV/c and in the presence of both in-time and out-of-time minimum bias pile up (luminosity $10^{34}$ cm$^{-2}$s$^{-1}$). A realistic model for the (preamplified) pulse height for a series of time samples and subsequent extraction of an energy value were included, and so was the effect of noise.

This simulation allows the study of the distributions of the number of channels to be transferred from a ROSE board to the DCC, and of the total number of crystals readout per DCC. It also allows the optimisation, in terms of data volume, of the assignment of channels per board and crate in the ECAL endcaps, where the geometry of the trigger towers is irregular.

In this studies the thresholds were set to $\text{ThHigh}=2.5\text{Gev}$ and $\text{ThLow}=1\text{Gev}$. The use of thresholds in $E_t$ rather than in energy insures that similar values can be used both in the barrel and endcap regions.

Results of the simulation are shown in figure 4 for the cases where no zero suppression was applied and where complementary channel-by-channel zero suppression was applied with a threshold equivalent to 0 or $\sigma$ of noise (30MeV in the ECAL barrel).

The overall percentage of channels readout out for the ECAL barrel and endcaps are given in table 1 — in the case where no zero suppression is applied, the average event size per DCC will be of the order of 2.5 Kbytes (10 samples per channel, 3 byte format), to be read at a L1 event rate of 100kHz.
Table 1: Data volumes after tower based SR

<table>
<thead>
<tr>
<th>Zero Suppression</th>
<th>ECAL Barrel</th>
<th>ECAL Endcaps</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>4.9%</td>
<td>3.9%</td>
</tr>
<tr>
<td>0σ</td>
<td>2.9%</td>
<td>2.5%</td>
</tr>
<tr>
<td>1σ</td>
<td>2.2%</td>
<td>1.9%</td>
</tr>
</tbody>
</table>

5. CONCLUSIONS

The tower based selective readout scheme presented, inspired by the characteristics of an electromagnetic deposit in the ECAL and by the physics requirements of this detector, allows the desired ECAL data volume reduction, a factor ≈20 with respect to the total data produced by the detector. The impact of such algorithm in particular physics channels is still under investigation, but it is believed to be quite small.

The tower based selective readout algorithm uses the level 1 ECAL trigger information, which is available in the ECAL upper level readout and trigger system.

Two possible hardware implementations for this (or similar) selective readout algorithm were described, with particular emphasis on the role of the Data Concentrator Card, demonstrating the feasibility of this technique.

Prototypes validating the concepts discussed here are expected by the summer 2000.

6. REFERENCES

2. B. Lofstedt, these proceedings.
3. J. Varela, CMS note-96/011.
The Digital Readout System for the CMS Electromagnetic Calorimeter

The CMS ECAL Collaboration
Presented by B. Lofstedt CERN EP-CME

Abstract

The readout system for the CMS ECAL detector [1], comprised of 80'000 PbWO₄ crystals, consists of two distinct parts; the on-detector Very-Front-End (VFE) electronics [2,3] and the Upper-Level Readout and Trigger system which is purely digital. The two parts are connected by a large number of optical links; one high-speed link per channel (~80'000) for the readout and two slow links per set of ten channels to distribute clock and control information to the on-detector electronics. This paper will concentrate on the Upper-Level electronics.

1. INTRODUCTION

The Upper-Level digital Readout and Trigger system of CMS ECAL consists of around 60 9-U VME crates, each serving up to 1700 readout channels corresponding to, in the barrel case, 68 trigger towers. This gives for the barrel one crate per supermodule. For the end cap, where the tower mapping is less uniform, the crate mapping will be slightly different. Fig.1 shows an overview of the CMS ECAL readout system.

![ECAL readout system](image)

Fig. 1. The CMS ECAL readout system

Each crate contains 17 100-channel readout modules (ROSE100), one Data Concentrator module (DCC) and one standard VME CPU card.

The system provides the necessary control information for the VFE electronics over two 40 Mb/s optical links per group of ten crystals, i.e. a detector submodule. The modules receive the data over one optical link per crystal at an 800 Mb/s sustained rate. It provides information to the regional trigger on the energy, shower profile and time assignment per trigger tower and stores the data during the first level trigger latency. In case of a positive LVL1 decision, the corresponding data is transferred to the DAQ system. In addition, it provides means to assure the synchronisation and integrity of the data, both internally and with respect to the LHC bunch-crossings. The system provides all monitoring and test facilities required to assure proper functionality of the hardware. Also, it performs a local acquisition of monitoring data, such as signals from the light monitoring system, test pulses injected into the VFE electronics, crystal temperatures, monitoring of the APD bias currents, etc.

2. THE ROSE100 MODULE

The ROSE100 readout module, see Fig. 2, is the main component of the ECAL readout and trigger primitives generation. It is implemented as a VME 9-U module and contains all the functionality required to control, read and provide trigger information from four 5x5 crystal Trigger Towers, i.e. a total of 100 channels. Physically, the module consists of a motherboard containing all common circuitry, such as Board Controller, VME interface, etc. and four daughter boards, called Tower boards, with all functionality’s required for one Trigger Tower.

![ROSE100 module](image)

Fig. 2 The ROSE100 module

Furthermore, each ROSE100 has, in the transition board area, two link interface boards. One board is called Opto-Electro-Board (OEB) and contains the opto-electro interfaces for the links from-to the on-detector Very-Front-End (VFE) electronics (120 fibres). The other one, called the Sync-Link-Board (SLB), contains two fast copper (Gb/s) links to the Level-1 local trigger crate as well as one bi-directional fast copper (Gb/s) link to the DCC.
to the Trigger Primitives Generator (TPG) where the tower data is compensated for differences in down the entire loop is in the order of a few µs (defined by the fibre loop length).

2.2 The Tower Board

Each of the Tower Boards contains the complete DAQ and Trigger path for 25 channels. The crystal data from the OEB arrives as LVDS signals and are applied to the deserialiser block (HP low-power G-link receivers). Thereafter, the data is compensated for differences in time-of-flight and length of fibres, linearised and applied to the Trigger Primitives Generator (TPG) where the tower energy, Bunch Crossing Identification and, eventually, the Isolation bit is generated (see 2.2.2). Simultaneously, the data is stored in a digital pipeline of programmable length during the LVL1 trigger latency.

Information about crystal temperature, APD leakage current is sent, by the VFE, over the same path as the data and this information is also stored in the pipelines but do not participate in trigger decisions.

2.2.1 DAQ path

In case of a positive LVL1 decision the corresponding set of consecutive samples, a time frame, is extracted and stored in one of the derandomisers. The derandomiser area consists of a memory with 256 word. The number of derandomisers and their length can be programmed within this area up to a maximum number of 32 derandomising buffers.

The special data from the VFE is identified at the input stage of the Tower board. It is stored in the pipeline and an internal trigger is generated in order to extract the data from the pipeline. This information is extracted from the normal data blocks and sent through the local DAQ path (see 2.4.1).

A Readout Controller builds, for each LVL1 Yes, a tower data block containing the information from the 25 channels and adds the trigger primitives information corresponding to that event. A first step in the data reduction, zero skipping, is done at this level (see 4.)

2.2.2 Trigger path

The TPG must, for each bunch crossing, calculate the trigger primitives and in case of a positive time identification provide the local LVL1 trigger with information about Tower energy, time origin and, if appropriate, tag the primitives with the information that an isolated electron was found.

The data from the 5 crystals in a phi rows are summed and a peak finding/bunch crossing identification is made. The five strip sums are summed in two ways; all five to generate a total tower energy information and, for the

Figure 3 shows the preliminary layout of the module including the transition boards.

2.1 Opto-Electro-Board

The OEB contains one hundred 800 Mbit/s optical receivers carrying the data from the individual crystals as well as 20 optical transmitters, two per group of the 10 crystal detector submodule, one distributing the 40 MHz sampling clock and one carrying, in serial form, the parameters required by the VFE. The 12 fibres for one submodule are assembled into one fibre bundle.

Currently, the Siemens Paroli receiver is used but for the final production a more cost-effective solution will be sought. The outputs from the Paroli receivers are LVDS compatible signals which are routed as strip lines through an impedance controlled connector and distributed to the Tower boards. Tests have shown that the 800 Mbit/s signals can be safely distributed over the motherboard.

A laser safety interlock system is implemented to assure that, in case of fibre disconnect or break, all the transmitters belonging to a submodule bundle are shut off. The principle is to monitor two crystal fibres per bundle and, as soon as no activity is detected, the clock and data sent down to the VFE is shut down. When the VFE detects absence of the clock it shuts down all the transmitters are used.

The OEB contains one hundred 800 Mbit/s optical receivers carrying the data from the individual crystals as well as 20 optical transmitters, two per group of the 10 crystal detector submodule, one distributing the 40 MHz sampling clock and one carrying, in serial form, the parameters required by the VFE. The 12 fibres for one submodule are assembled into one fibre bundle.
isolation criteria, two-by-two. The four two-by-two sums are compared and the largest one is compared to the total sum. If the two-strip sum is larger than a defined fraction of the total tower sum (programmable) an isolated electron has been found and the isolation bit is set.

The total tower sum is applied to a look-up table where it is converted to an 8-bit non-linear representation.

The primitives from two trigger towers are combined and sent, via the SLB, to the local LVL1 trigger process.

The algorithm described above is according to the current understanding. However, the algorithm is implemented in FPGAs thus allowing future changes.

2.3 Sync-Link-Board

This board is the interface between the ROSE100 and the external functions. It contains the link and synchronisation for the trigger information and the bi-directional link to the DCC module.

The trigger primitives from all towers in ECAL must be lined up in time at the outputs from all SLBs. To assure this the board contains an accumulator where the presence of information vs. machine clocks is histogrammed and compared to the BC0-signal from the TTC system. If the output is correctly timed, i.e. all latencies being compensated for, the histogram should reflect the LHC timing. Fig. 5 shows the content of the accumulator for different timings.

2.4 ROSE100 Motherboard

All common function blocks, e.g. Board Controller, VME interface and TTCRx, are implemented on the Mother board.

2.4.1 Board Controller

The Board Controller supervises all functions in the ROSE100 module. One of the main functions is to separate the data going, via the DCC, to the central DAQ system and data that is to be sent to the local CPU in the crate. The first path is called the Global DAQ and the latter the Local DAQ.

It builds the complete Global DAQ data block and checks for inconsistencies, such as wrong event or BC identifiers, separates the information about temperature, leakage current, etc. and sends it via the Local DAQ path.

When the VFE sends this special information the data is recognised before entering the pipeline and the Board Controller is informed that it should, with the proper delay, provide an internal trigger to the Tower boards.

The controller is also responsible for the dispatching, over the internal serial bus, of the set-up information to the various function blocks. It also, over the same bus, executes continuously various monitoring tasks.

It is built around two FPGAs and two dual port memories, one for the Global path and one for the Local path.

2.4.2 VME interface

A standard chip-set from Cypress™, the CYC7C960, is the heart of the implementation of this function. The interface is slave-only and supports all VME64 functions.

2.4.3 TTCRx

A single TTC opto-electro interface is centrally placed in the crate and a twisted pair is distributed to each one of the ROSE100 modules. Each module has a TTCRx chip which provides the clock, trigger and event number with the proper delays.

3. DATA CONCENTRATOR CARD

The Data Concentrator Card (DCC), see Fig. 6, assembles the event data from the ROSE100 modules including the corresponding trigger primitives.
The Trigger primitives data is stripped off from the data block and sent to both the Selective Readout Algorithm function and the Trigger output FIFO. A data reduction is performed, using the Trigger Tower information as described below.

In the barrel case a complete supermodule data block is created and, upon request from the Readout Unit (RU) in the central DAQ system, pushed up through the RU to the event building switch network.

The Trigger Primitives information, stored in the Trigger output FIFO, is sent to the Trigger readout system where it is combined with the rest of the information from the trigger system.

A VME interface is provided to allow set-up as well as test and monitoring of the DCC functions.

If the CSRP (see 4) is implemented the DCC provides to the CSRP the information about the seed regions and gets back a map of channels to be read. This information is derived from the Trigger primitives. The links required for this option are not shown in the figure.

4 SELECTIVE READOUT

During high-luminosity LHC operation, physics triggers arrive in CMS at an average rate of up to 100kHz. The background physics interactions occur at a much higher rate. An average of 17 minimum bias events occurs per bunch-crossing, i.e. at a 40 MHz sustained rate. In order to isolate the front-end signals, which are in-time with the triggered bunch-crossing, the pulse shapes are digitised over a duration of several consecutive crossings, before and after the trigger, and stored in a time frame for analysis. The length of the time frame expands the data volume of the calorimeter to 2.4 MB/trigger. To reduce the data size down to 120kB/trigger in blocks of 2kB, as required by the central CMS DAQ system, a readout architecture incorporating data reduction algorithms was specially designed for this purpose.

A first step in this reduction is a zero skip operation performed at the Tower board level. The energy is estimated from the stored time frame and the frame is kept only if the estimated energy is above a defined threshold.

A more refined reduction is then done. The baseline for this data reduction architecture is to use the information extracted for the Level-1 trigger process and to execute the reduction, per crate, in the DCC module. Another possibility, currently under investigation, is to implement a dedicated Centralised Selective Readout Processor (CSRP) in order to facilitate the information exchange across the hardware boundaries. The DCCs will identify the seed regions and communicate them to the CSRP where a map is created of the channels to be read. This information is returned to the DCCs where the selective readout is performed.

5. CONCLUSION

The ECAL Upper Level Readout and Trigger system has been extensively prototyped over the last years. A first prototype readout system was built for the 1997 test beam period and during this year a ROSE50 module has been produced with all the functionality’s required for the final system. It will be used to verify all functional blocks and allows a continuous evolution of the hardware implementation up to the point where the final production starts. This helps to avoid the problem with obsolete hardware already at the time of production as the current evolution of technologies is extremely fast.

A set of “stripped down” ROSE100 modules are currently under preparation for the different test systems required for the production of the individual ECAL components. Also, a 1700-channel system for the precalibration of the ECAL Supermodules is in the implementation phase.

6. REFERENCES


THE ATLAS TILE CALORIMETER DIGITIZER

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Abstract

We describe a digitization and readout system built to serve 10800 PMT channels in the Atlas Tile calorimeter. Six or eight digitizer boards in each calorimeter module each receive six pairs of analog signals (high and low gain) to be digitized by 10-bit ADCs every 25 ns. Two custom designed gate arrays (CX-3161 from Chip Express) on each board each store data from three channels until validated by the first level trigger. Selected data are then formatted for subsequent read out. Clocks and control commands are distributed via the TTC system. The system is designed to achieve good fault and radiation tolerance. It was tested in test beam during summer 1999, and is intended for volume production in 2000.

1.1 INTRODUCTION

The Tile calorimeter (TileCal) [1] is divided into two barrel and two extended barrel parts. Each part is divided into 64 wedge-shaped modules (i.e. 256 modules in all). Each barrel module is read out by 45 PMTs, and each extended barrel module contains 31 PMTs.

The PMTs and the front end electronics are located inside "drawers" in the base of each module. Attached to each PMT base is a 3-in-1 board [2] which amplifies and shapes the PMT output. The shaper outputs are connected to the TileCal Digitizer system.

The digitizer system fits within a space 2.8 meters long and 10 cm wide, with sufficient clearance for two layers of circuit boards. Up to eight digitizer boards, each serving 6 channels, will fit into each module, along with a central readout interface. The drawers provide a well-shielded, water-cooled environment kept at a temperature of about 25 degrees centigrade. A power dissipation of about 70 Watts per module is allowed for the digitizer system.

The digitizer system samples incoming data every 25 ns. using 10-bit ADCs [3], and stores them in a fixed-length pipeline to await a first level accept. The level-1 latency is stipulated to be no longer than 2.5 μs. Each triggered event is recorded over an extended time frame, with a length programmable up to 16 samples.

The time frames are stored in readout buffers (derandomizers) awaiting readout via the readout link interface.

Fig. 1: Data flow of Tile Cal. electronics

The digitizer samples high and low gain signals in each channel, with a gain ratio of 64. A selection mechanism determines which gain to use for a specific pulse, reading out only the high gain data unless it overflows or underflows, in which case the low gain data are used.

Since the digitizer system is situated inside the calorimeter with a non-negligible radiation level and limited access for maintenance, it is important to make the design extremely reliable and sufficiently radiation tolerant. For these reasons the digitizer system has been implemented to reduce the impact of single point errors. This is done by decoupling the different parts of the readout chain (Fig 1), so that a fatal error in one component causes limited disruption. In the final design all components in the system will be at least radiation tolerant.

Two prototype digitizer systems have been tested at CERN during summer 1998 [4] and summer 1999. The design was subjected to a production readiness review (PRR) in June 1999, where it was provisionally accepted. However it must be subjected to a final review when the pre-production version is available.
2. SYSTEM ARCHITECTURE

2.1 General

The TileCal Digitizer consists of two chains of digitizer boards connected to a readout interface in the center of the drawer (Fig. 2).

Fig. 2: Two chains of digitizer cards connected to the readout interface in the center of a module.

Each digitizer board samples and stores data from 6 channels. The digitizer boards contain 3 main types of components:

- 12 ADCs (two for each channel)
- 2 Tile-DMUs, which are custom devices containing pipeline memories for three channels, together with readout buffers and control functions.

The readout from each Tile-DMU is connected to the link interface card via point-to-point links (Fig 3). Differential LVDS is used to provide a safe transmission path with a minimum of digital noise fed back to the analog inputs. The signals pass through intermediate boards via pass-through links with no active components. This is done to insure that the consequences of a digitizer board malfunction will be limited to the possible corruption of its own data.

Fig. 3: The data flow along a chain of digitizer boards.

One consequence of this design are distance-dependent variations in the timing of data sent to the link. By adjusting the phase of the output data from the Tile-DMUs, however, this skew can be reduced to within 1 ns. This is performed by adjusting the timing of output data from each board.

The current readout interface consists of an interface card which buffers and transmits data to an S-link source card [6]. Connections between the digitizer boards and readout cards are made using surface mount connectors and printed circuit foils. The lines within the circuit boards and in the foils are given matching impedance to avoid reflections.

The placement of the readout board in the center of the module reduces the maximum readout path length. It also places the fiber-optic readout link in an environment with better radiation shielding than at the ends of the module.

2.2 The Digitizer Board

The digitizer board (Fig. 4) is divided lengthwise into analog and digital parts, each with separate power and ground planes. Low and high gain analog signals for each channel are received differentially from the 3-in-1 shapers via shielded twisted pair cables. The receiving network is fully passive and adapts the signal to the ADCs and also creates the pedestal level. Separate ADCs digitize the low and high gain signals for each channel.

The ADC used is the Analog Devices AD9050. It uses a successive approximation scheme with 5 cycles of latency. Pedestal levels are adjustable in groups of 3 channels via a DAC programmable via the TTC interface.

Fig. 4: The digitizer board.

A TTCrx chip on each board receives signals via a coaxial cable from the interface board, which converts and electrically fans out the signal from the TTC fiber.

2.3 The Tile-DMU

The Tile-DMU (Fig. 5) is implemented in a custom gate array. It receives ten-bit high gain and low gain inputs from three different channels. The data are stored in a pipeline memory, pending a Level-1 trigger decision. On an accept, a programmable number of consecutive samples are sent to derandomizer readout buffers implemented in a dual port RAM. The derandomizers use a scheme with memory pointers, where the start address for a stored event is stored in an address FIFO. Between 16 and 32 such derandomizer buffers are available, depending on the length of the time frame used. It is also possible using this memory-pointer scheme to read out events with overlapping time frames.
Four parity bits are added to the data before they enter the pipeline memory. Each parity bit covers overlapping regions of 20 bits.

The data rate from the Tile-DMU can be controlled by two different methods to adapt to different types of readout. One method is programming the readout controller inside the Tile-DMU to introduce a delay between each consecutive readout cycle. The second method is the use of direct flow control protocols between the readout interface and the Tile-DMU. For example, the Tile-DMU is capable of generating all necessary signals for the S-link readout protocol.

2.3 Readout protocol

The header word contains information about the gains and error bits.

The link control lines (link Reset, Ctrl, Test and Write_enable) are generated by all Tile-DMUs. This means that a drawer will have 16 versions of each signal, one for each Tile-DMU, although only one set is required. To improve fault tolerance, it is possible for the interface board to combine control signals from several digitizer boards, using majority vote to initiate changes.

2.4 System Control

The Tile Digitizer is programmed by commands sent via the B channel of the TTCrx system. The following items are programmable:

- Length of the pipeline
- Length of the time frame
- Phases of the input and readout clocks
- Readout mode (normal, calibration or test mode)
- Readout rate (delay between readout cycles)
- External flow control enable
- Threshold values for high/low gain selection
- Seed for the test pattern generator
- Pedestal DAC value settings

The ADC input clock phase is adjusted to ensure that the PMT pulses are all sampled at their maxima. This adjustment is performed using test pulses produced by the 3-in-1 cards and the TileCal laser system.

The clock phase of the Tile-DMU outputs is adjusted to ensure proper readout timing. The timing in of this clock is performed by varying the phase while running the Tile-DMUs in test mode with a suitable data pattern.

2.5 Testability

There are a number of test points that are continuously monitored via flags in the headers. Single and double bit errors occurring in the TTCrx are reported, as well as the occurrence of parity errors in the memory. There are also means to supervise the combined parity of all programmable registers as well as dynamic registers such as address pointers and state variables. The combined dynamic parity bits from each Tile-DMU should be identical.
The sample data are protected by CRC-16 check sums and horizontal parity bits. The alignment of the data is routinely monitored at the receiving end of the readout link.

3. PRODUCTION AND VERIFICATION

3.1 Tile-DMU design and production

The Tile-DMU is implemented using the CX3161 gate array from Chip Express [7]. This device has 33-48k usable gates and is produced in 0.35μm CMOS, with up to 208 I/Os and 64 kbit of embedded 3 ns memory. The maximum system speed in this device is nearly 200 MHz, which is much greater than the 40 MHz nominally required for the Tile-DMU design. The gate array consists of a large number of identical predefined blocks, which simplifies the design of clock distribution networks. A large number of available macros help to reduce the design effort. These macros include RAMs, PLLs and I/O-driver configurations. The Tile-DMU was synthesized from a high level description in VHDL, using Leonardo from Exemplar logic. Design checks were performed using the Chip Express design kit.

Two small rounds of prototypes were received for evaluation. These prototypes have been used in test beam tests at CERN. One prototype round proved to have occasional parity errors in the memory, while in the other round, these errors have not been observed.

3.2 Radiation tolerance

Expected radiation levels in the drawers are 0.2 krad/year from ionizing radiation, and a neutron fluence of $10^{11}$ 1-MeV-equivalent neutrons/cm$^2$/year [1]. Adding appropriate safety margins, the CMOS components of the system should be able to operate after being exposed to 10 krad of ionizing radiation and $5 \times 10^{12}$ neutrons/cm$^2$. For bipolar components the corresponding numbers are 50 krad and $7.5 \times 10^{12}$ neutrons/cm$^2$.

We have performed tests of 10 to 25 samples of all active components used in the design except the Tile-DMU. Only a few components have to be replaced and the AD converter has passed the tests without failure.

The Tile-DMU technology has been shown to be radiation tolerant [8]. We have tested a ring counter implemented in the same technology with both ionizing and neutron radiation with good results. A sample of the production Tile-DMU will be tested later this year. The production version of the TTCrx is implemented in radiation-hard DMILL technology [9].

3.3 Experiences from Test-beam

The TileCal Digitizer was tested in Module 0 beam tests during the summer of 1999. The noise contribution from the digitizer boards proved to be small. The total high frequency noise in the high gain channels was approximately 1.3 ADC counts (200 MeV), and the corresponding number in the low gain channels was about 0.6 ADC counts (600 MeV) (Fig.6). These numbers include noise contributions from both the digitizer and the 3-in-1 system. The contribution from the digitizer alone was estimated to be 0.5 ADC counts in both cases. This estimate was based on SPICE simulations on the 3-in-1 system.

The electronics system is calibrated using charge injection pulses provided by the 3-in-1 cards. Five reconstructed pulses of varying charges in one high gain channel are seen in Fig. 7.

![Pedestal noise for high and low gain channels](image1.png)

![Five reconstructed pulses of varying charge](image2.png)
from the linear fits are well below 1%, thus fulfilling the linearity requirement on the system.

The digitizer system proved to be mechanically and electrically stable except for some problems with SMD connectors.

![Graph showing linearity of the digitizer system]

**Fig. 8: Linearity of the digitizer system**

4. FUTURE UPGRADES

Final production of the Tile Digitizer is scheduled for 2000. Several changes in the design, are being considered, including minor modifications to the Tile-DMU, mechanical improvements, and a new readout link technology.

4.1 Modifications to the Tile-DMU

Some minor modifications to the Tile-DMU design were motivated by test beam experiences. These modifications include inserting the bunch crossing identification number (instead of the even number) in the header, as well as possible improvements to the flow control scheme to simplify communication with the link interface.

4.2 Mechanical improvements

Integration of the TileCal digitizer in the summer 1999 beam tests revealed reliability issues with the SMD and power connectors used in the prototype digitizer boards. Replacements have been found for these parts, and will be included in the final pre-production version of the digitizer system.

The next version of the digitizer boards will also feature a slightly reduced board length to ease drawer assembly.

4.3 Readout Links

The readout interface used in beam tests of the prototype digitizer systems used fiber-channel S-link cards. Unfortunately, there is currently no sufficiently radiation tolerant version of this technology.

The production version of the digitizer system will require a new readout interface with better radiation tolerance and higher bandwidth. Possible solutions are currently being investigated.

5. CONCLUSIONS

A pre production version of the digitizer system for the ATLAS Tile calorimeter has been designed, built and tested. Most design requirements have been satisfied. Experiences from the system integration and the analysis of test beam data have suggested minor changes which will be implemented in the final version. A small pre production version will be tested towards the end of next year.

ACKNOWLEDGEMENTS

Many people have been involved in the design work of the TileCal digitizer. We would like to thank our commercial partner Sicon, and Chip Express for their help during the design of the Tile-DMU. We would also like to thank Magnus Ramstedt who has been developing software for verification and data acquisition, and finally all of the members of the Tile test beam group.

REFERENCES

FIRST TESTBEAM RESULTS FOR THE QIE-DEMONSTRATOR READOUT FOR THE CMS HADRONIC CALORIMETER

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Abstract

First results of QIE based electronics used to readout the HE calorimeter in the H2 testbeam at CERN are presented. Beam, LED, and calibration data are discussed along with descriptions of the system and DAQ.

1. QIE CONCEPT AND DISCRIPTION

The basic concept of the QIE (Charge Integrate and Encoder) is to allow the input charge from a phototube to be measured over a very large dynamic range with good precision over the entire range. The QIE is designed to continuously put out an exponent (range) and an analog voltage within that range corresponding to the integrated charge within one clock period[1]. The QIE and DBC (Driver-Buffer Clock) ASICs used for the demonstration in the test beam were originally designed for the KTeV experiment at Fermilab[2,3] and provide continuous charge sampling at up to 60MHz. The QIE system was run at the nominal LHC beam RF rate of 40 MHz.

The QIE is a pipelined device with 4 stages in the pipeline. The output of the QIE is a 3-bit range number and an analog voltage corresponding to the value in that range. This analog voltage is converted to digital by an 8-bit FADC and the data is stored in the DBC ASIC until readout is requested. In the lowest range, with the preamp installed, each LSB corresponds to about 2000 electrons within a 25 nsec time interval. This is equivalent to 13 nanoamps/LSB. Each event is comprised of 32 time slices of the input signal where each slice has an "Exponent" (Range) and Mantissa (FADC) as well as a Capacitor ID which indicates which of the 4 integrating capacitor banks produced the data. These 32 slices allow the charge input to be studied as a function of time; thus we can get a time profile of the beam signal.

2. TESTBEAM SETUP

2.1 HE calorimeter

The testbeam readout system consisted of 21 channels of KTeV style QIE electronics that were used to instrument the HE (Hadronic EndCap) Figure 2.

![Figure 2: HE Channel Map Beam's eye view.](image)

The HE calorimeter is made up of alternating layers of scintillator and 2 cm brass layers with 18 layers being read out for each tower[4]. The light is collected via waveguiding fibers and brought to the readout-decoder box via clear waveguide fibers. The light is converted using HPDs (Hybrid Photo Diodes)[5], which have a quantum efficiency of about 13% and a gain of about 2000.

This low gain and the fact that the charge pulse is positive required a pre-amplifier, which inverted the signal and had a gain of 20. This allowed the output of the HPDs to match the existing KTeV QIEs, which expect a negative current pulse typical of photomultiplier tubes. The final version of the CMS QIE is under design at this time and will accept both positive and negative polarity signals.

2.2 Beam

The beam trigger was comprised of two small scintillator counters in coincidence. The H2 beam line could deliver muons and pions at several energies. Muons were available even when the beam stop was installed. The pion beam still contained muons. We used a motion table to position the calorimeter so that the beam was
approximately centered in channel 5 (see Fig 2.) An LED calibration system and a moving wire radioactive source were available for calibration purposes.

2.3 DAQ

The Data Acquisition system used for the QIE calibration was based on a PC running Windows NT 4.0 and Visual Basic 6.0, which could communicate with a CAMAC crate. The DAQ provided both data recording and data analysis capabilities. Pedestals, energy sums, timing plots, and various histograms were available online. This allowed us to adjust the system timing and verify that things were working very quickly.

3. PEDESTAL DATA

One important way to study the noise performance and stability of the readout system is to study the behavior of the pedestals as a function of time. The pedestal value and RMS width are good indicators of the performance of the system, especially with the added complication of a pre-amplifier in front of the QIEs. During KTeV's running the pedestals were stable and had an RMS width of 0.3 LSBs. However, each LSB for KTeV was equivalent to about 40,000 electrons. For the HE system each LSB is only 2000 electrons due to the use of the pre-amplifier.

In the previous year's testbeam effort we had serious oscillation problems with the pre amps at a very low frequency (~ 0.5 Hz). This problem was fixed and we could no longer see this low frequency oscillation. The HPDs, however, were grounded to the detector, and from tests done at Fermilab, we knew this increased noise in the system. Figure 3 shows the pedestal for a "good" channel, (channel 12) it has an RMS of about 4.3 counts or about 9000 electrons.

Figure 4 shows the same pedestal distribution in log mode. Unfortunately some channels were much noisier; Figure 5 shows a noisy channel.

4. BEAM DATA

4.1 Pion Data

The H2 testbeam at CERN was able to provide pions at several energies. We took data at 250, 200, 125, and 50 GeV with pions. One of the first things we needed to study was the timing of the signal. Using the online DAQ we were able to set the pion signal to be in time slice 6 of the 16 slices we were reading out.

Figure 6 shows the time structure for 250 GeV pion and indicates the pedestal and data regions. The ringing and undershoot are artifacts of the pre-amp used in front of the QIE.

Figure 3 Pedestal distribution for channel 12 RMS=4.3 LSBs.

Figure 4: Pedestal distribution for channel 12 log scale.

Figure 5: Pedestal distribution for a noisy channel.

Figure 6: Time structure for 250 GeV pion signal.
4.2 Muons

We were able to take Muon data during open access to the test beam. One of the main goals was to verify that single muons could be seen above pedestal. We also wanted to study the time response of the calorimeter to muons. Figure 9 shows the time response of the system to muons, Figure 10 shows a single Muon event. The pedestal noise can be seen in the single event, and future work is needed to reduce this noise.

An energy histogram of the pion data also shows a Muon peak. Figure 7 shows the pion energy sums for the four beam energies used. Figure 8 shows the pion beam energy plotted vs. the central tower pulse energy sum. The algorithm used to make the pedestal subtracted energy sum was to sum slices 6 through 9 and subtract the sum of slices 2 through 5 (see Figure 6). The response is reasonably linear with only slight deviations, which can be explained by shower leakage to adjacent towers, which are not included in the sum.

Figure 7. Pedestal subtracted energy Histograms for 250, 200, 125, and 50 GeV Pions. Axis is in counts/10 where each count equals about 2000 e. A clear muon peak is also observed at the low end of the scale for each distribution.
5. CALIBRATION

5.1 LED system

The calorimeter was equipped with an LED flasher system, which could be used to illuminate all channels of the detector; fiberoptic signals were delivered to each HPD channel. We took several LED runs in order to study the uniformity of the response to the LED signals. Figure 11 shows the time response of channel 5 (the beam channel) to the LED system. The LED pulse is longer than a normal beam pulse. Figure 12 shows the energy sum response to the LED system. Note that the distribution is narrow and gaussian over several decades. The conclusion is that the LED system will work to track the performance of the detector.

5.2 Source Calibration

The calorimeter is also equipped with a moving wire radioactive source calibration system. This system allows the response of each tile to be measured. The source calibration system will be used to correct for radiation damage to the tiles as the detector ages. The instrumentation problem with the source system is the very small size of the source signal, only 0.5 LSBS. The method of measuring this small signal is extreme oversampling[6]. The basic method is to measure the pedestal to great precision both with and without the source. The difference between the two measurements is the source signal. This method requires a stable pedestal during the measurement time, some noise (usually not a problem), and the taking of lots of pedestal data.

At this time we did not quite meet 2 of the 3 requirements and stumbled on the third. The pedestals were stable but had a remnant of the low frequency oscillation that plagued us during last year's test beam. Figure 13 shows the pedestal vs. time for a single channel. Note there still is a 0.2 to 0.5 Hz oscillation at about the 0.2 LSB level. This oscillation can be removed manually.
as it occurs on all channels at the same phase. However, when you are trying to measure a source of 0.15 LSBs to a precision of .01 LSBs, any extra coherent noise is a problem.

![Pedestal deviation of mean as a function of time. Full scale is +/- 0.2 LSB.](image)

Figure 13: Pedestal deviation of mean as a function of time. Full scale is +/- 0.2 LSB.

The second problem we had was that the source driver was temporarily broken. This prevented us from moving the source to one of the quiet channels. The noise level on the channel where we could position the source had an RMS of about 12 counts. For that RMS, we would have needed about 1,000,000 pedestal measurements to recover the source to .01 LSBs. At the time we were taking data we did not realize this and only took about 100,000 to 200,000 pedestals. The statistical nature of this measurement combined with an RMS of 12 only allows for a precision of about +/- 0.03 LSBs in the measurement of the pedestal.

Given that the pedestals were not quite stable, (low frequency oscillation) and that the noise was too large (RMS of 12, we expect final system to be 1.5-2) and that we did not take long enough pedestal runs, we were unable to achieve our goal of measuring the pedestal and hence the source to 0.01 LSBs. We did however, measure the pedestals to a precision of 0.03 LSBs, and we understand why we were limited to that resolution.

6. CONCLUSIONS

The QIE overall run was a success. The DAQ worked very well and provided good online displays.

The response of the system for Muons, Pions and LED pulses was measured. Muons were clearly separated from the pedestals. The Pion energy response was linear. The LED system produced very gaussian pulse distributions.

The time structure of the response of the calorimeter was measured for Muons, pions and the LED system. The LASER calibration system was not yet online during our run, so we have not yet measured the response of the system to the LASER pulse.

We did have some shortfalls. The cross talk and ringing in the pre-amplifier compromised our ability to study shower energies that were shared across more than a single tower. The channel to channel cross talk corrupts the energy sum for the calorimeter, and we will be working to correct this problem. We observed that we still have a pedestal oscillation, which coupled with increased noise, compromised our ability to do detailed radioactive source measurements. We did measure the source at the level of 0.15 LSBs +/- 0.03 LSBs, but did not reach our goal of +/- 0.01 LSBs. Further work on this front will continue using low level LED signals.

7. REFERENCES

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Abstract
The ATLAS Liquid Argon electromagnetic calorimeter needs a very accurate calibration system in order to fulfill its physics requirements. A set of 10 calibration boards has now been produced to test the calorimeter modules in electron beam. These boards contain a programmable sequencer which allows the loading and execution of a complete calibration run (various DAC values, delays and patterns) and provide 128 signals which are injected to the electrodes through high precision resistors. Measurements have demonstrated a good uniformity and a good linearity though small distortions have been identified. Radiation tests with both neutrons and gammas have shown many shortcomings in the pulser and control logic. New developments to address these shortcomings are discussed.

1. INTRODUCTION
The precision in physics aimed in ATLAS requires a good energy resolution over the full acceptance and thus a small overall constant term, better than 0.7%. Part of this constant term is related to the ability to calibrate 200000 channels with a good accuracy [1].

Due to the fast shaping times used at LHC experiments, the readout electronics is current sensitive and thus the traditional charge calibration through a precision capacitor is no longer valid. Moreover, the parallel noise is smaller at these shaping times and thus it is possible to use a current calibration with precision resistors.

2. REQUIREMENTS
- **Signal**: it should be as close as possible to the real signal which has a triangular shape. The initial current must be very precise and injected close to the electrodes. The rise time must be 1 ns and the decay time 450 ns.
- **Dynamic range**: from 200 nA (noise level) to 10 mA (nearly 3 TeV in one cell).
- **Non uniformity between channels**: 0.25% including the board itself and the signal distribution (cables, mother boards).
- **Linearity**: the integral non linearity must be less than 0.1% for each of the 3 gains of the shaper [2].
- **Timing between the real physics signal and the calibration pulse**: within ±1 ns to keep the sensitivity to any jitter as small as possible
- **Radiation hardness**: the board must tolerate radiation fluxes of gammas (20 Gy/yr) and neutrons ($10^{12}$ n/cm²/yr).
- **Magnetic tolerance**: ~100 Gauss

3. CALIBRATION PULSER DESIGN

3.1 Principle:
The calibration pulses are generated by pulsers the principle of which is described on Figure 1.

The fast output voltage pulse is obtained by interrupting a precise DC current I_p that flows in the inductor. When a pulse command is applied on Q2, Q1 is cut off and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay across the parallel...
combination of the cable characteristic impedance $Z_c$ and a termination resistor $R_o$ of the same value. This pulse is propagated inside the cryostat through a 7 m long 50 Ω cable adapted at both ends and is applied across a precise injection resistor $R_{inj}$ (0.1%) in the cold, directly to the electrodes. The resulting current is given by:

$$\text{Ical} = -\frac{R_o}{Ipe} - \frac{t}{\tau} \text{ with } \tau = 2L/Ro \quad (R_o = R_a = Z_c)$$

An amplitude up to 10 mA can be achieved by applying a 5V pulse in a 500 Ω injection resistor.

The main difficulty of this calibration system is to distribute uniformly throughout the calorimeter a very precise voltage pulse. To minimise the attenuation due to skin effect, the pulsers are located close to the feedthrough.

3.2 Complete design:

The current $I_p$ is generated from a 18 bits DAC voltage through a voltage to current converter. The current in the output branch is $I_1 = V_{DAC}/R_{20}$, as negligible current flows in the gate of the JFET transistor. A low offset op amp as OP 07 must be used, as $V_{offset} = 100 \mu V$ already corresponds to 15 LSB.

To insure good linearity, the base current of $Q_1$ (which varies non linearly with $I_p$ (β varies with the collector current and the temperature) is measured and added to $I_p$.

$Q_1$ is made of 4 transistors in parallel to share the large DC current for $I_p$ (up to 200 mA) and to keep a low $R_{cc}$, necessary for the wide dynamic range.

Five precision resistors (0.1%) determine the calibration pulse accuracy.

4. CONTROL LOGIC:

The control logic (Figure 3) incorporates a memory to store the calibration parameters of a full run, a sequencer and registers for the current parameters.

These parameters are:
- DAC values (ramp for linearity measurements)
- Delay values (for timing studies)
- Pattern values (to select channels and enable crosstalk measurements)
- Number of triggers (stored in the sequencer)

The memory and the sequencer are initialised at the beginning of a calibration run using the SPAC protocol [3]. The sequencer controlled by the calibration signal loads the registers from memory using an

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**Figure 2** : Schematics of the analog part

**Figure 3** : Control logic
algorithm with 3 embedded loops as shown in Figure 4.

Figure 4: Sequencer algorithm

No access to the board is necessary during one run, but the parameters stored in the registers can be read back before each calibration pulse if required.

5. PRACTICE REALISATION

A board with 128 pulsers has been realised (Figure 5).

Figure 5: Calibration board

The size of the board (490 mm x 410 mm) is determined by the front end crate dimensions [1].

The analog part contains 64 pulsers on each side of the board. The pulsers are aligned in a single row close to the output connectors to ensure good uniformity distribution. As the density is very high, surface mounted components have been used (9000 components).

The control logic is located on the top of the board, inside 13 Alteras FPGAs (EPM7128ELC84-7).

6. EXPERIMENTAL MEASUREMENTS

6.1 Signal shape

A signal measured at the output of one pulser is shown in the following plot. The pulse shape nicely follows an exponential decay as shown by the fit and the rise time is 1 ns.

Figure 6: Signal shape

6.2 Pulse Uniformity

There are 2 sources of non uniformity:

- A dispersion in the exponential decay time of the pulse which is dominated by the inductance dispersion and a dispersion in the pulse amplitude which is defined by five 0.1% precision resistors.

- The dispersion of the inductance value has been measured in 3 different ways.
  - Directly on the board using an RLC meter at 1 MHz. The relative rms dispersion is about 1.7%.
  - Fitting the exponential decay time of each channel when no shaping is applied. The average decay time is 346 ns with 5.7 ns dispersion resulting in a 1.6% inductance dispersion.
  - Measuring the uniformity with a longer shaping \( t_p = 350 \text{ ns} \) to be more sensitive to the exponential decay time. The rms amplitude dispersion is 0.73% which translates in a 1.5% inductance dispersion.

These inductance dispersion measurements are in good agreement and a 0.11% non uniformity can be deduced at ATLAS shaping time.

The pulse amplitude uniformity has been measured with a 12 bits ADC after the atlas shaper (CRRC\(^2\) shaper with \( t_p = 45 \text{ ns} \)) at various DAC amplitudes for each board. Figure 7 shows the results for a set of 8 boards. The sigma of the dispersion is about 0.19% and a clear structure is observed corresponding to the two output

Figure 7: Signal shape results for a set of 8 boards.
connectors. This is entirely explained by the difference in copper length between each pulser and the output connectors. Consequently it was decided to apply a software correction as a function of the channel number (the same for all boards). The sigma of the dispersion is then 0.11% as shown in Figure 8.

6.3 Linearity

The linearity has been measured with a 12 bits ADC, sampling the signal at the peak, over the 3 gains of the ATLAS shaper (\(t_p = 45\) ns). The time at which the signal is sampled is set on a large signal. The integral non linearity is within ± 0.1% for all gains as shown in Figure 9. On the medium range and more obviously on the low gain a parabolic shape is observed. This is explained by a small change in rise time of the calibration signal. After shaping the position of the peak is shifted by about 1 ns but as the signal is measured at fixed phase, it results in a small non linearity.

6.4 Command feedthrough and injected charge

A small positive spike (15 mV – 1 ns) is due to the capacitive coupling of the command pulse (CMD) through the \(C_p\) capacitor of Q, whereas Q, is still on. It generates a small signal on a disabled channel which is lower than 0.1% of full high gain scale after shaping (30 MeV).

A small negative spike (30 mV – 2 ns) is present when the DAC is set to zero. It corresponds to the injected charge. When Q, is cut off by the command pulse, the very fast voltage variation on its collector, 3V in 1 ns, results in a charge which is injected in the output through a ~1 pF parasitic capacitor between the emitter and collector of Q. It translates in a signal after shaping which is 3% of the full high gain scale (1 GeV) but only 0.1% at the peak sampling time (30 MeV).

6.5 Crosstalk

The crosstalk over one output connector has been measured in the ATLAS configuration (a warm cable following by a pin carrier, a vacuum cable, a second pin carrier and a pigtail [1]). The 64 channels are 50 \(\Omega\) terminated.

The crosstalk is concentrated on 2 adjacent channels on each side of the pulsed channel and 3 channels on the opposite side. The maximal peak to peak amplitude is 0.3% reduced to 0.1% at signal peak position.

6.6 Board stability and noise

The signal stability has been measured by performing identical measurements at a few hours interval. The DAC output and its temperature have been monitored over a long period. The signal drift is fully explained by the DAC offset variation with temperature which is 30 \(\mu\)V/°K.

The calibration board should not introduce sizeable electronic noise in the readout system. We have measured it not to be higher than the noise generated by the FEB (Front End Board) in high gain.

6.7 Timing

Two four channels delay chips [4] are used per board in order to align the time of the peak of the calibration signal with respect to the physics one. The delay chips has been measured linear to ± 0.2 ns over 0 to 25 ns range with a 0.996 ns step.

The jitter dependance with the delay value has also been measured. It starts at 100 ps and increase to 300 ps.
for the maximum delay value. The chips used on the calibration boards are from the earliest version and do not reflect their actual performance.

7. MAGNETIC TOLERANCE

In the front end crate, the boards will be exposed to a magnetic field of approximately 100 Gauss. Such a field can modify the inductance and then the decay time constant of the calibration pulse. The decay time constant change between 0 and 400 Gauss has been measured to be less than 1 % which correspond to 0.1% change in amplitude after shaping.

8. RADIATION TOLERANCE

Several components of the pulser have been irradiated to neutrons ($10^{13}$n/cm$^2$) in Grenoble and gammas (20 hours with 10 Gray/hour) in Saclay, and the most sensitive elements have been found to be low offset OpAmps. Many commercial OpAmps have been tried but died after neutron irradiation. The OP177 resists to neutrons and gammas, but the increase of the offset voltage from 10 µV to 100µV is not acceptable.

A commercial dual 18 bits DAC (PCM 1700P Burr Brown) has been irradiated, but the offset voltage drifted to 1 mV after irradiation.

All other semiconductors exhibited satisfactory behaviour.

The control logic has not been tested but the Alteras are known to be not radiation tolerant.

The delay chip is in a version not yet radiation tolerant.

The voltage regulators died during the tests.

9. NEW DEVELOPMENTS

New developments [5] are necessary to fulfil the ATLAS requirements in particular concerning radiation tolerance.

- Design of a specific PMOS transistor to replace the 4 PNP transistors in parallel in the current switch to reduce the injected charge effect.
- Radiation tolerant OpAmp used in the current source. We are developing a low offset OpAmp following two approaches: a CMOS autozero OpAmp [6] which has already been developed by Mainz University but needs to be adapted and a bipolar OpAmp using external precision components and trimming to get a low offset.
- Radiation tolerant 16 bits DAC. We study two designs: a ramp DAC (charging an integrator with a DC current during a well controlled time) and an R/2R ladder DAC where the resistor network is made of discrete precision components.
- Radiation tolerant control logic. It has been decided to replace all the control logic in the Alteras FPGA by DMILL asics. The control logic will be simplified by suppressing the sequencer and an asic incorporating all the basic functions required will be developed and used throughout the board. A few COTS might still be required.

10. CONCLUSIONS

Experimental measurements on the 128 channels calibration board [7] with final ATLAS density have given good results and fulfil the calorimeter requirements. Ten boards have been produced and 5 have been used on the test beam at CERN.

The next step is to ensure that all elements on the board exhibit satisfactory radiation tolerance, in particular the low offset OpAmp, the DAC and the digital part. New developments are underway and a decision for the production of a radiation tolerant calibration board is expected in the year 2000.

REFERENCES

[1] "ATLAS Technical Proposal"
CERN/LHCC/94-43 LHCC/P2, December 1994, 15

"A fast monolithic shaper for the ATLAS E.M. Calorimeter".
ATLAS internal note LARG-No-092

"SPAC : Serial Protocol for the Atlas Calorimeter"
ATLAS internal note LARG-No-93

"A PLL-Delay ASIC for clock recovery and trigger distribution in the CMS tracker"

"Development towards the final LARG calorimeter calibration board"
ATLAS internal note ATL-LA-EN-0006 June 1999

"An integrated calibration system for Liquid Argon Calorimetry"
Mainz Preprint, MZ-ETAP/99-1

"The LARG Calorimeter Calibration Board"
ATLAS internal note ATL-LA-EN-0005 June 1999
Jet Determination in Lar-Calorimeters using a Heavily Interconnected System of FPGA’s

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Abstract.

New fast and highly complex ‘Field Programmable Gate Arrays’ allow the design of sophisticated decision logic within the trigger latency time of detectors.

As an example we show the Jet Determination of the Hera-H1 detector at DESY Hamburg. It has to calculate all existing localized energy depositions (jets) in the calorimeter and deliver the result, sorted according to energy.

The system is implemented by a network of three times 440 high density FPGA’s which have to deliver the results in less than 1 µs. The computing power of the system is equivalent to 70 Billion operations per second.

1. The calorimeter trigger.

To understand the new system, it is necessary to give a survey of the environment in which it will be integrated.

The basic elements of the calorimeter trigger are built by about 700 projective, i.e. to the interaction region pointing, trigger towers.

These towers are the result of 40000 electromagnetic and hadronic channels which are readout and stored after the trigger decision.

The trigger towers are further summed to 512 so called Bigtowers (BT).

The electromagnetic and hadronic components of the BT-signals are digitized by 10 MHz Flash-ADC’s and are summed to different topological and global quantities.

The electromagnetic and hadronic fractions are individually weighted in lookup tables. Further lookup tables and summing stages calculate different quantities as there are: total energy, transverse energy, missing energy etc.

The energy sums are discriminated by programmable thresholds, and the outputs are fed to the central trigger logic, where the decision for storing all the experiment data has to be made.

All this complex signal processing has to be accomplished in less than 1 µs.

2. The FPGA - Jet-Trigger.

In the new proposed system, the summing over large calorimeter areas will be replaced by an intelligent algorithm identifying regions with signals well above the noise (jets).

The complicated scheme based on many thresholds at different levels can thus be replaced by an intuitive system where ideas popping up in a physics analysis can be easily implemented in the hardware.

All topological information will be available such, that physical correlations can be exploited to keep the trigger rate under control.

3. Design Principles.

The physical idea of the jet trigger is quite simple to formulate: It should find localized regions of energy depositions corresponding to a typical radius, together with the coordinates of the jet center.

In a trigger application a sequential algorithm is prohibitive because of timing limitations. A parallel hardwired solution is needed. The system is logically divided into four stages:

3.1 Preprocessor

Here, the analog pulses from the individual trigger towers, separated in electromagnetic (em) and hadronic (had) sections are sampled and digitized. The em and had sections are passed through look-up tables for thresholding and weighting and are subsequently added. The resulting 440 weighted towers are fed into the so-called bumpfinder.
3.2 Bumpfinder

The basic algorithm to find the jets is realized here. Each of the towers, formed in the previous stage, interrogates its nearest neighbors (known a priori by the fixed geometry of the towers) to determine whether any of them has more energy than the interrogating tower (called IT). If this is not the case the IT is a local energy maximum or "bump". The jet energy is then formed by adding all the energies of the neighboring towers to the energy of the bump. Since this algorithm only interrogates the immediate neighborhood, it is suited for parallel execution: All the trigger towers determine their bump property independent of the others. The result of the bumpfinder is a list of jets, defined by energy and coordinates. A finite number of jets (maximum of 24) is fed into the next stage, the energy sorter.

3.3 Energy Sorter

Here a fixed number of jets (24) are sorted according to energy. Again the algorithm is carried out in a parallel manner, similar to the bump identification algorithm: Each jet compares itself with all the others and determines the number of jets with smaller or equal energy. The jet with the number 23 is the largest, the one with number 22 the next etc. In case of equality in the energies, a unique ordering based on the topological location of the bumps is forced. From the 24 possible bumps only the first 12 (highest energy) bumps are passed to the next stage.

3.4 Trigger Quantity Determination

The trigger element generator (TQD) houses the necessary logic to construct the trigger decision from the jets found. Typical actions of the TQD is to discriminate the individual jet energies, count jets above certain thresholds and determine topological correlations on the basis of position information of the jets. The TQD is designed in a very flexible and expandable way, since the optimal strategies of triggering will largely depend on the changing physics interests.

4. Hardware Realization.

4.1 Design overview

The trigger towers have to be re-assembled to optimize their granularities depending on the position in the calorimeter. The re-assembly of the signals is done in the ACS system (ADC, Calculation, Summing).

The Bump Finder Unit (BFU) processes these signals to find "bumps" and their addresses. "Bumps" are defined as the maxima of local energy depositions, including their immediate next neighbors. The BFU consists of eight boards, mapping eight octants of the calorimeter, arranged in cylindrical form. Each board delivers the fifteen possible "bumps" to its Primary Sorting Unit (PSU). This unit selects, for each octant, the three bumps with the highest energies and transfers them to the central Secondary Sorting Unit (SSU). Here the total of 3 * 8 bumps are sorted by energy in decreasing order. The 12 largest bumps are sent to the Trigger Quantity Determination box (TQD), where the trigger elements will be generated.

Fig. 1 shows the timing of the pipelined system, in time units of particle crossings of the accelerator. Note that one unit is 0.1 µs and that only a total of 8 units are available for the digital part of the jet algorithm.

If one considers the sample N at unit 0, the digital value is obtained at unit 1. The ACS unit can complete its processing within one unit. With cable delay the BFU receives the data at unit 3. At unit 4 the output of the BFU is available and PSU and SSU finish their work until unit 6. In the remaining two units the final trigger elements are generated.

4.2 ADC-Calculation-Storage Unit (ACS)

The ACS cards convert the signals from the 568 EM-Trigger Towers and the 624 Had-Trigger Towers in 1192 8 Bit words, weight them,
calculate the EM- and Had-sum, send the resulting 440 Bytes to the BFU (Bump Finder Unit) and store simultaneously the data in circular buffers.

Except the AD- conversion, the logic is implemented in 440 FPGA’s. (Altera 10K30).

4.3 Bump Finder Unit (BFU)

The current energy content in each input tower is compared with the eight or nine (depending on the local granularity) nearest neighbors (see fig2).

This operation is done for all input towers in parallel. The towers which win, i.e. have the highest energy value compared to the neighbors, are bump centers. They sum the neighbor energies to their own energy and put the result onto the Three-State output bus, together with the address of the bump center.

The Input Towers are grouped to tower clusters. Only one member in a group can be a “bump”. Fig.3 shows one of the eight boards with Input Towers, Tower Clusters and the bus connections of a single Input Tower. Note that there are eight 8 Bit input busses from the neighbor towers, output address bus, 8 Bit output bus for the summed energy and a fanout of eight 8 Bit busses to the neighbor towers.

The bump energy (8 Bits) and the address within a cluster (2 Bits) are transferred to the PSU (Primary Sorting Unit). The evaluation of bump centers and the formation of the bump energies is done in large FPGA’s (one for each Input Tower, 440 all together), which are all networked together. The total computing power of the BFU sums up to about 70 Billion calculations per second. Because of the high complexity of networking, it is necessary to arrange the system in form of a cylinder, just like the calorimeter itself.

4.4 Primary Sorting Unit (PSU)

One of the eight identical sections in the cylinder contains 55 FPGA’s with the BFU function. The fifteen bump energies (8 bits wide) and two address bits for every group are prepared for the Primary Sorting Unit (PSU). In the PSU the energies of each of the 15 bumps are compared with all others. The result is a coded position in the hierarchy of energies. After decoding, the three biggest bumps and their addresses are stored. They are sent to the Secondary Sorting Unit (SSU) for the next sorting step. The PSU needs one time unit (0.1 µs) to process its function and is implemented in one large FPGA for each section.

4.5 Secondary Sorting Unit (SSU)

The 24 biggest bumps together with their addresses (3 maxima from each section), are collected in the PSU’s for the whole calorimeter and are transferred to the SSU for the final sorting operation.

In the SSU the energies of each of the 24 bumps are compared with all others. If two bumps are
equal, the global position in the calorimeter is taken into account to force a strict ordering. Therefore the result of each comparison is an unambiguously coded number which gives the position in the hierarchy of energies. After decoding, the 24 energy bumps and their addresses are stored in decreasing order. The 12 largest energy bumps are distributed to a general bus system („jet container“), where trigger quantities can be calculated in the remaining time units. The Secondary Sorting Unit will be implemented in few large FPGA’s (250 k gate equivalents).

4.6 Trigger Quantity Determination (TQD).

The output of the third stage of the jet trigger is the list of 12 largest jets found, ordered by energy. In the forth and last stage of the trigger, this list is used to generate the trigger elements leading to an actual trigger. Since the „jet container“ is a bus system, an arbitrary number of modules may have access to it and trigger elements can be easily added if needed without disturbing the determination of the already implemented trigger elements in the jet trigger. The amount of complexity of trigger elements is limited by the two time units (.2μ) which are left for the TQD.

5. Status of the Project

The project was started in the second half of 1997. The simulations for the different components (ADC Unit, Bump Finder and Primary and Secondary Sorting units) showed that the processing time can be kept in the available time units. The logic synthesis of all FPGA’s was successful. A first demonstrator model of the Bumpfinder for one octant showed its functionality.

6. Conclusions

The proposed level 1 jet trigger is the last missing piece of an ambitious upgrade program for the HERA H1 Liquid Argon Calorimeter. The physics idea of the trigger is to find the localized energy depositions in the calorimeter, order them by their energies and provide decisions in a very flexible way based on the multiplicity, energy and topological information of the jets. The trigger will overcome the limitations of the present global trigger philosophy and will allow to select specific physics reactions with higher efficiency and higher background rejection.

The realization of this ambitious project is possible due to the fact that very complex and fast FPGA’s came to the market and the second important fact is the availability of reliable design systems.
A mixed analog/digital shaper for the LHCb Preshower

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ABSTRACT
This note describes, first, the experimental and theoretical studies of the LHCb’s preshower signals performed with a prototype cell. Four designs of the very front end electronic are then discussed and a choice is proposed.

1 INTRODUCTION
Figures 2 and 1 show the results of the experimental study of the LHCb preshower signal, produced by a minimum ionisation particle (MIP). At this very low energy, dominant effects on the shape are the statistical fluctuations of the photoelectron collection and of the PM gain, so that the signal shape is quite unpredictable. As we have to handle energy down to 5 MIP’s with a 0.20 MIP accuracy, we have to take care of this effect. The important points for the following are:
- the fraction of the energy collected during a LHC beam crossing time (25ns) which is found to be 83% ± 10% for a MIP signal;
- the error due to fluctuation of the signal itself decrease to 4% for a 5 MIP’s signal, corresponding to our trigger threshold;
- the shape fluctuation decreases when the energy increases and becomes negligible at large energy;
- the comparison between experimental data and simulation is quite good, except about the little secondary signal (figure 1) at 60ns which is due to a cable reflection in our test set-up.

2 ELECTRONIC FUNCTION
As for all the LHC experiences, the frequency of the signals is 40MHz. The number of channels is 6000, the criterium of cost is decisive. Due to the fact that the signal shape is not constant and the duration greater than 25ns, we have to develop a specific electronic.

The readout electronic of the preshower has two different functions: the trigger and the correction of the energy measured in the calorimeter. Moreover, it takes part in the calibration of the detector.

The 4% resolution of a 5 MIP’s signal is precisely the size of the LSB set at 1/5 MIP which should be used as indicated below.

The energy collected in the preshower is a very low
part of the total energy collected by the calorimeter for an electron. It is so necessary to measure it to correct the value observed in the main part of the calorimeter. This is for all the dynamic of the signal. At the moment the maximum energy for an electron of 200 GeV is 500 MIP’s. The minimal dynamic of the signal is about \(5 \times 500 = 2500\). It corresponds to 12 bits. The required accuracy is 1\%, corresponding to 7 bits.

We plan to use a 64 channels multianode PM tube. We know that there’s some difference of gain between the 64 channels of the PM with a factor as large as 4. The precise studies of these variations remain to be done.

If the first electronic stage is more than 10 cm away from the P.M., the signal should be carried on a suitable, carefully adaptable cable. In this case the PM gain correction has to be included in the electronic dynamic range (14 bits).

So we prefer to include the first electronic stages closer to PM tube (the 64 channels); the gain correction can be made very easily by changing the load resistor of each channel and for each PM tube. This advantage involve to have a compact layout including the PM tube and the associated electronic. This electronic will have to include all or just a part of the readout electronic.

3 BASIC CHOICE FOR THE READOUT ELECTRONIC

Two decisive arguments suggest integrating the signal and not only considering its maximum value. On the one hand, we have only an absolute time at our disposal which prevents us to measure the signal at its maximum value, because of its jitter. On the other hand, for the low energy signals, the shape isn’t reproducible at all and the integration permit a statistic “pseudo-addition” even for signals of few MIPs.

We have to accept an inaccuracy of one nanosecond when we consider the integration time. To obtain the best precision of the electronic system, the integration time must be as long as possible. The maximum integration time is 25 ns since the probability to have two interesting consecutive signals is high. So to integrate the signal during 25 ns and then to reset it, we need two bunch crossing. The frequency is divided by two and we have to use two interleaved integrators and one multiplexer by channel which don’t raise a lot the price of the system.

As this shaping includes both analog and digital signals we decide to design it in a fully differential way.

We had to design a switched integrator able to come back to ground and with an adequately short integration time at this frequency. This integrator is full differential. It is made from an amplifier with high gain and large bandwidth. To provide a good reset, the differential inputs and outputs are short-circuited with the ground by CMOS switches, as shown on figure 3.

![Integrator Principle](image1)

In each design, there’s a multiplexing at the output. Here, we choose a differential multiplexer which selects the channel by the switched on/off the current generator supplying the selected differential stage, see figure 4.

![Multiplexer Principle](image2)

The physical signal duration is higher than the bunch crossing period (\(\simeq 70\) ns compared to 25 ns). To avoid false data and wrong trigger action, there
are two solutions:

1. Erase the data of the periods n+1 and n+2 if we consider the period n.

2. Measure the collected energy in the preshower with a sufficient precision during the period n+1 and n+2 and treat the signal with these two results. As in LHCb the probability to have two consecutive signals is not negligible, the solution 1 is excluded.

First of all, we consider that the electronic signals for the period n, n+1 and n+2, for a signal without pile-up, are proportional with a coefficient $\alpha$ of the order of 15%.

So we have:

$$\text{energie } n = (\text{integrate } n) - \alpha \times (\text{integrate } n - 1)$$

With more precision, $\alpha$ is different according to the circumstances. The $\alpha$ of the period n+2 is a little smaller than the $\alpha$ of the period n+1. We propose to take the value of $\alpha$ for the period n+1 into account. We have obviously a small error when we compute the energy during the period n+2. The result is that we lose some triggers during the period n+2. Nevertheless, we avoid wrong trigger actions. We will have to measure exactly the effects of this method and check its efficiency. Afterwards, we will have to correct off line the data during this period n+2. This point must be discussed according to the tests and the simulations.

4 BASIC DESIGNS

There are mainly four designs with subtraction analogic or digital, with one or two gains.

The first one uses analog subtraction and one gain. We store the integrated value on 25ns in a track and hold, and this value during a second period of 25ns with a second track and hold, at this moment the second track and hold give the value n and the first one give the value n-1. Each amplifier subtract the value n-1 from the value n, with two different gains (1 and $\alpha$). At the output of the multiplexer, during a period of 25ns, we have a value corresponding to 83% of the energy collected by the preshower cell during the previous period. This value is analog and can be digitalized with an ADC, see figure 5.

The second one uses analog subtraction and two gains. The same as the last, but we add a gain system, see figure 6.

The third one uses digital subtraction and two gains. It’s the basic choice twice copied, see figure 7.

5 THE MAIN CHOICE

The choice is one gain and digital subtraction. In fact if the subtraction is analog, the $\alpha$ coefficient is a hardware implementation: it’s dangerous to choose now this solution because it will be impossible to correct this coefficient. We prefer a digital subtraction to correct precisely the $\alpha$ coefficient by software. One gain is probably sufficient, if two gains are necessary we use the solution of figure 7.

The first part is near the detector, see figure 8. There are:
- a first stage to transform common mode to differential mode;
- 2 parallel integrators, one for the bunch-crossing \( n \) and another one for the bunch crossing \( n + 1 \);
- 2 T/H and a 20MHz multiplexer;
- and a buffer to drive a 100Ω twisted pair.

**Figure 8: the first part**

The second part is at 10m length from the detector cell, see figure 9:
- a commercial 12 bits converter;
- a digital stage with:
  - a look-up tables for gains and pedestal
  - a converter to a good numerical format, probably 9 or 10bits (floating point)
  - the weighted subtraction
  - the trigger output with a digital comparator (the precise threshold value is adjusted by software).
- a memory to wait the L1 trigger decision and to send the value to the DAQ.

**Figure 9: the second part**

The first chip, in BiCMOS 0.8\( \mu \)m technology by AMS has been sent in January. In this, there are: an integrator and a T/H, and a channel with the common mode to differential mode translator, an integrator, a T/H and a clock generator. A second chip was sent in April with a full channel with two gains without subtraction.

### 6 TEST RESULTS

The first chip is fully tested. The track and hold works very well, in fact a little better than predicted in simulation. Its dynamic is good and its linearity is found better than 1%, which is the precision of our measurement, see figure 10.

**Figure 10: scope reproduction**

The clock generator and the input stage which realise the conversion to the differential mode are also working well. The surprise comes with the switched integrator itself which shows a parasitic oscillation (see figure 11). We try to reproduce this oscillation in simulation by retroannotation everything including the test environment. We don’t succeed. We measure the gain, it is correct and the reset time is also correct.

**Figure 11: scope reproduction**

As all the other cells show better performance than predicted, we think (without proof) that the open loop gain of the operational amplifier is too large. Another design, with a lower gain, was sent to AMS foundry.
The second chip is under test. The integrator is the same and is also unstable, but by decreasing externally its current source to reduce the gain, we obtain a stability sufficient to test the full chip functionality. We will do these tests soon.

7 CONCLUSIONS

A mixed analog-digital shaper included T/H was designed for the LHCb preshower. Every functions are working except an oscillation on the integrator. A new integrator design was sent to AMS foundry in September. A full chip and test bench is excepted by the end of 2000.
Trigger implementation in the KLOE experiment

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Abstract.

The KLOE detector at present under operation at the Frascati phi-factory DAΦNE is a general-purpose detector for the study of CP violation in the neutral kaon system.

The KLOE trigger uses signals from both the electromagnetic calorimeter and the central drift chamber. Within 150 ns after an interaction the calorimeter and the drift chamber provide a set of signals which form the basis of the trigger decision.

The design of the modules providing the trigger decision for each sub-detector, the final trigger decision together with the modules for distribution and synchronization in the experiment is presented.

Particular emphasis will be given to the presentation of the use of modern design methodologies that could be also implemented for the realization of electronics for LHC experiments.

Outlook

The KLOE trigger uses signals from both the electromagnetic calorimeter and the central drift chamber. The final trigger decision and the its distribution are performed by VME modules with two data acquisition interfaces: The VME one and a custom designed KLOE AUX-bus backplane.

VME is used for setting and calibration purposes, while the AUX-bus provides the interface the data acquisition system. Monitoring of the data at each stage of triggering process is necessary for data consistency checks and to keep the entire system under control.

Actually this data allow the determination of all trigger efficiencies with the required precision togethei with a detailed investigation of possible systematic effects due trigger system.

The modules of which perform the trigger decisions for each subdetector contain counters, shift registers, status registers, and a fast data acquisition interface.

The trigger distribution system contains the logic for trigger handling and the logic for broadcasting the synchronization cycle, needed to check the proper distribution of the exact trigger number to all the front-end boards of KLOE.

All control and acquisition logic is implemented in FPGAs. In the design of the trigger modules HDL (Hardware Description Language) code for simulation was used, together with synthesis tools to target the function in FPGA devices. ECLinps logic and analog sum are used for fast part. The use of HDL permits the reuse of code for new design in different targets and an easy way to upgrade existing boards with new function, without PCB redesign.

The DAΦNE Factory and the KLOE detector.

DAΦNE is high luminosity e+e-collider, built in Frascati, Italy. Its CM energy is set at the Φ meson resonance, 1020 MeV. About 35% of the Φ decays in K_L K_S (K_L in πππ and K_S in ππ) while only a small fraction (about 0.3 %) are CP violating events (with K_L decaying in ππ).

Fig 1. The KLOE detector inside DAΦNE.
The designed peak luminosity is $5 \times 10^{32} \text{ cm}^{-2} \text{s}^{-1}$ which corresponds of $\Phi$ rate of about 2.5 kHz.

The Kloe experiment [1], currently on run at DAΦNE, has been optimized for the measurement of the CP violation parameter $\text{Re}(\epsilon'/\epsilon)$ to a precision of $10^{-4}$.

It consist of a large helium tracking chamber for momentum measurement and lead scintillating fiber electromagnetic calorimeter with excellent timing performances. The entire detector operates inside a 6 kGauss solenoidal field provided by superconducting magnet.

**The KLOE Trigger.**

The KLOE trigger [2],[3] strategy is based on local energy deposits in calorimeter sectors and multiplicity information from the drift chamber.

A two level scheme has been adopted in order to both produce an early trigger with good timing information to start the FEE operation and to exploit as much information as possible from the drift chamber, whose typical response time are in the microseconds scale.

Therefore after the arrival of a first level trigger, additional information is collected from the drift chamber, which is used, together with the calorimetric information, to start the DAQ system.

The trigger decision can be vetoed at the first level in the case the event is identified as Bhabha scattering or at the second level in case of cosmic ray events.

**The Trigger distributor.**

Due to the very stringent timing requirements one of the most critical signals is $T_1\text{sync}$, which is distributed to the ADCs and TDCs via the AUXbus backplane by using two differential lines [4].

Actually if a precision of 1 ns is already an issue, 50 ps require a more sophisticated and cautious design of the line.

The Trigger Distributor (TD) distributes to the FEE the $T_1$, directly received from the TORTA, after having synchronize it at 92,06 MHz, i.e 1/4 of the DAΦNE machine clock (368.25 MHz). The synchronized $T_1$ is then fan-out, via a dedicated coaxial cable.

Laboratory mesasuraments give for these module the following performances:

- Max Temperature jitter <5 ps/°C
- Max jitter for each channel ~7 ps
- Delay time for each channel ~14.2 ns

**The Trigger Supervisor and FIOs crate.**

The trigger supervisor (TS) [5] is a 9U VME board housed in a dedicated crate (Fig.3) with a custom backplane.
In the same VME crate are housed also 10 Fan In-Out (FIO) modules, one for each readout chain, that distribute the trigger signals to the ROCK and the ROCKM boards, the controllers of the readout chain. Every FIO module receives the T2 and the SYNCREQ signals from the TS via backplane, and redirects the BUSY and SYNCFAIL signals, coming from the ROCK (M)s to the TS, using dedicated backplane lines.

The TS main purpose is to provide an interface between the TORTA and the DAQ system. Its responsibility is to synchronize the distribution of the triggers with the event readout and to block the validation of new triggers while the readout system and the front-end electronics are busy.

During the synchronization cycle [4] the trigger supervisor and the FIOs check that in the entire system all the modules have the same trigger number. When a synch request is forwarded from the TS to the FIOs and from the FIOs to the respective chain, each ROCK module checks the trigger number inside the corresponding crate, each FIO in the corresponding chain and finally the TS checks the status of all the FIOs.

The TORTA trigger box.

The Trigger ORganiser and Timing Analyser (TORTA) Board is the board that implements the trigger logic of trigger as shown in Fig2. As previously stated the T1 logic must be as fast as possible; therefore it is implemented on a ECLinps daughter card.

The use of a small daughter card gives a sufficient flexibility if a change of the T1 logic is needed. The rest of the logic is implemented in a 9U VME Auxbus board.

![Fig 4. The TORTA block diagram](image)

Four complex (~2000 flip-flops) Xilinx 4020EX are used.

The T2 Xilinx implements the T2 logic by setting registers to define the T2 configuration. The Monitor Xilinx implements a series of monitor registers to control dead time, arrival timing of critical signals and to latch the input patterns. The downscale Xilinx contains a set of counters to perform the downsampling of particular signals as the cosmic veto or bhabha vetos.

Finally the DAQ interface is implemented in the AuxBus VME Xilinx.

The CAFFE Chamber trigger Box.

In the Chamber Activity Fast FEtch (CAFFE) board the first and second level drift chamber triggers are produced.

For trigger purposes signals coming form adjacent layers are grouped toghether, defining ten concentric “superlayer”. This allows to avoid multiple counting spiralizing tracks of low energy particles produced in background events.

In the CAFFE the ten signals corresponding to the hit multiplicity of these superlayer are added.

The analog sum of layers 2-9 provides, after a discrimination to a proper threshold, the chamber level one trigger T1D.

The inner layer is used to produce the TCR signal used in the definition of the cosmic rays veto.

![Fig 5. The CAFFE block diagram](image)

Moreover the analog sum of the 2-9 layers is digitally integrated with a running sum circuit implemented inside an FPGA.

After the receipt of the first level trigger, the number of hits in the chosen time interval is obtained by subtracting the values of two appropriate words in the register, corresponding to the integrated multiplicity just before the first level trigger and after 2 µs.
All the signals produced by the CAFFE are also digitized and are available for monitor purposes via either VME interface or during the KLOE acquisition via the Auxbus interface. VME is used for setting of the the thresholds and for the definition of the integration time of the integrator.

Fig 7. The CAFFE Board.

Conclusions

In the realization of these modules we started from the beginning using HDL (Hardware Description Language) and synthesis tools. In the meantime we observed from the very beginning the evolution of these tools from a source of new bugs to a mature technology. The use of FPGAs give to us enough flexibility giving an easy way to upgrade existing boards with new features when necessary.

All the described modules are steadily running since more two years.

Acknowledgements.

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References:

1) The KLOE detector technical proposal
   The KLOE collaboration
   LNF-93-002
   Date:01/21/1993

2) The KLOE Trigger system,
   Addendum to the Technical Proposal
   The KLOE Collaboration
   LNF 96/043 (IR)
   Date : 03/95

3) KLOE note No.02
   A concept for the trigger of the KLOE Calorimeter
   F. Bossi, C. Schwick, A. Sciubba, R. Di Stefano
   Date : 02/95

4) KLOE note No : 168
   Trigger Handling and Distribution in the KLOE Experiment
   V. Bocci, G. De Robertis, R. Messi, F. Ruggieri
   Date : 2/98

5) KLOE note No : 125
   The KLOE Trigger Supervisor
   V. Bocci, G. De Robertis, F. Ruggieri.
   Date : 12/97
Abstract

The addition of a Transition Radiation Detector (TRD) to the ALICE setup, coupled with a better understanding of the requirements of the front-end electronics, have led to a major re-appraisal of the central trigger system for the ALICE detector. The previous system was reviewed at the LEB Workshop in 1996. In the new system, the principal rate reduction in Pb-Pb collisions comes after 5.5 microseconds, in order to wait for the decision of the TRD. Data transfer to the data acquisition system is initiated after a positive level 2 decision, 100 microseconds after the event takes place.

1. INTRODUCTION

The last twelve months have seen considerable activity in all aspects of the design of the ALICE detector, resulting in the production of a series of Technical Design Reports (TDRs). This process has led to a number of improvements for the interface between the detectors and the data acquisition system, which in turn implies modifications to the trigger system. The overall layout of the ALICE detector is shown in fig. 1.
The ALICE trigger detectors are listed in Table 1, together with their functions. The Forward Multiplicity Detectors (FMD) and Zero Degree Calorimeters (ZDC) define an interaction inside a specified vertex region with given centrality; the dimuon and dielectron triggers select those events which also contain dimuon or dielectron pairs respectively. The function of the FMD, ZDC and dimuon trigger detectors has been described in previous LEB workshops [1, 2], and is not given here.

Table 1. ALICE trigger detectors.

<table>
<thead>
<tr>
<th>DETECTOR</th>
<th>Decision Time</th>
<th>DATA</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMD</td>
<td>≤ 500 ns</td>
<td>μ +, t₀</td>
<td>Define interaction diamond Beam-gas interaction rejection Centrality</td>
</tr>
<tr>
<td>ZDC</td>
<td>~1.5 µs</td>
<td>Eₑ_react</td>
<td>Centrality</td>
</tr>
<tr>
<td>DIMUON (DM)</td>
<td>≤ 600 ns</td>
<td>P₁µ</td>
<td>Selection of dimuon pairs above pₑ cut</td>
</tr>
<tr>
<td>DIELECTRON</td>
<td>~5.5 µs</td>
<td>P₁ₑ</td>
<td>Selection of dielectron pairs above pₑ cut</td>
</tr>
</tbody>
</table>

Recently, a major new detector, a Transition Radiation Detector (TRD) [3] has been proposed for ALICE. This device will identify dielectrons in the same acceptance window as the Time Projection Chamber (TPC). It also provides a dielectron trigger. The detector complements the dimuon arm, allowing ALICE to study a wide range of aspects of dilepton production for masses above ~1 GeV.

The structure of this paper is as follows. The Transition Radiation Detector is described briefly in section 2. Section 3 reviews the protocol for non-triggering detectors in ALICE, and section 4 gives some conclusions.

2. THE TRANSITION RADIATION DETECTOR

The ALICE Transition Radiation Detector (TRD) consists of 18 (φ) x 4 (θ) sectors each consisting of six layers. In total there are about six hundred thousand readout channels. It forms a barrel between the TPC and the Time of Flight (TOF) system.

The principle of the Transition Radiation Detector (TRD) is to exploit the radiation produced when a relativistic charged particle crosses the boundary between two media with different refractive indices. The photons are in the soft X-ray range, with energies of about 2 to 30 keV. In order to increase the number of transition radiation photons, a stack of foils is used.

A schematic diagram of a TRD of a similar type to that proposed for ALICE is shown in fig. 2.

The transition radiation photons are absorbed in a time expansion chamber (TEC), which is a wire chamber with a xenon-based gas mixture. The electrons created by the transition radiation tend to deposit most of their energy near the entrance window of the TEC, and thus the resulting electrons appear at the end of the drift time window for a passing charged particle.

The time structure of the transition radiation electrons allows the TRD to be used as a triggering detector. The idea is to identify tracks above a given momentum in the TRD, which can be done as their deflection in a magnetic field is small, and thus their ionization is associated with a small number of readout pads - typically one. The observation of a track with the characteristic TR pulse at the end of the drift time flags an electron. The occupancy of the TEC pads is being selected so as to avoid overlapping tracks in a given pad while minimizing the mean number of pads to be associated with a given pulse.

The pattern-recognition operations are nonetheless complex compared with those performed in the other ALICE trigger detectors, and therefore the TRD trigger algorithm takes longer than that for any other trigger detector. The decision is contributed to the ALICE level 1 trigger, which comes 5.5 microseconds after the time of the interaction. In order for the TRD trigger to be able to analyze as many interactions as possible, it means that the level 0 (L0) strobe to ALICE detectors, which in general are not pipelined, must be essentially a minimum bias trigger in Pb-Pb interaction mode. The strategies to be adopted in the other running modes are still under discussion.
3. ALICE TRIGGER-DAQ PROTOCOL

ALICE events are very large, which poses a challenge for the Data Acquisition System. The event sizes for the different detectors are given in Table 2

<table>
<thead>
<tr>
<th>DETECTOR</th>
<th>SUBDETECTOR</th>
<th>N°. of Channels</th>
<th>Event Size (Mbyte)</th>
<th>Max. Readout Time (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITS</td>
<td>PIXEL</td>
<td>$1.4 \times 10^6$</td>
<td>0.140</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td>SDD</td>
<td>$1.9 \times 10^6$</td>
<td>1.500</td>
<td>≤1000</td>
</tr>
<tr>
<td></td>
<td>SSD</td>
<td>$5.0 \times 10^6$</td>
<td>30.0 + 36.0</td>
<td>2000</td>
</tr>
<tr>
<td>RPC</td>
<td>PPC</td>
<td>$1.6 \times 10^6$</td>
<td>0.150</td>
<td>≤1000</td>
</tr>
<tr>
<td>TOF</td>
<td></td>
<td>$3.7 \times 10^6$</td>
<td>0.120</td>
<td>≤1000</td>
</tr>
<tr>
<td>PHOS</td>
<td></td>
<td>$1.4 \times 10^6$</td>
<td>0.120</td>
<td>≤1000</td>
</tr>
<tr>
<td>HMPID</td>
<td>RICH</td>
<td>$4.5 \times 10^6$</td>
<td>0.005</td>
<td>≤1000</td>
</tr>
<tr>
<td>MUON</td>
<td>Scint. TOF</td>
<td>1.0 $\times 10^6$</td>
<td>0.100</td>
<td>200</td>
</tr>
<tr>
<td>TRIGGER</td>
<td>TOTAL</td>
<td>700</td>
<td>0.115</td>
<td>200</td>
</tr>
</tbody>
</table>

It may be seen that the overall data volume is dominated by the TPC readout.

The mean readout rates are chosen to match the required data taking rates. A special effort has been made to shorten the readout times for the pixels, the dimuon arm and the trigger detectors in order to allow these detectors to read out by themselves, independently of the rest of the detector.

Two factors govern the read-out rates. There is a limitation on the global data flow rate from the ALICE detector, and there is a requirement that the data transfer time from the front-end to the data acquisition system should not be long, so as to avoid excessive dead time. The scheme described in the ALICE Technical Proposal envisaged fast data links between the front end and the data acquisition system, with buffering in the counting room (in "Front-End Digital Crates") where there are less space limitations. It has been found that this leads to inefficient use of the optical links (Digital Data Links or DDLs) between the front-end and the counting room, given the low physics event rate in ALICE during Pb-Pb running.

The favoured solution is to introduce front-end buffering; events are only transferred after the final (level 2) trigger decision, thus reducing data traffic in the DDL, and the transfer proceeds asynchronously, thus allowing the DDL to be used more efficiently. The number of buffers is chosen so as to ensure that buffer saturation occurs rarely, while keeping low the total number of DDLs (each with a 100 MByte/s transfer rate).

The new demands posed by front-end buffering and the timing of the TRD trigger signal mean that the trigger signal sequence given in the ALICE Technical Proposal has had to be revised.

In the current ALICE protocol, there are four signals sent to each detector, and one sent back from the detector to the central trigger. The signals are listed in Table 3, and their timing is illustrated in fig. 3.

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>Latency (µs)</th>
<th>Medium</th>
<th>Participating Trig. DetECTOR</th>
<th>ACTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>1.2</td>
<td>Fast Coax. Cable NIM)</td>
<td>F.M.D.</td>
<td>STROBE to some detectors (T/H F.E. electronics)</td>
</tr>
<tr>
<td>L1</td>
<td>5.3</td>
<td>TTC</td>
<td>T.R.D. + ALL</td>
<td>(optical)</td>
</tr>
<tr>
<td>L2a</td>
<td>100</td>
<td>Coax. Cable</td>
<td>ALL</td>
<td>Data Transfer to Multi-Event FIFO</td>
</tr>
<tr>
<td>L2r</td>
<td>≤ 1000</td>
<td>Coax. Cable</td>
<td>ALL</td>
<td>Reject Event in the Multi-Event Register</td>
</tr>
<tr>
<td>BUSY</td>
<td></td>
<td>Coax. Cable</td>
<td>ALL</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 3. Timing of ALICE trigger signals.

Level 0 serves as an early strobe to detectors; at this point rough vertex cuts and beam gas rejection can be applied. The FMD also delivers information on event centrality, which is employed at level 1. In addition, dimuon events can be identified at this stage, 1.2 µs after the collision.

At level 1, information from the ZDC and the TRD are also available; this information is enough to make a final event selection. For this reason, a substantial rate reduction can be made at this stage, and event identifiers are allocated. It is sent 5.5 µs after the collision. Trigger levels 0 and 1 have fixed latencies, and so the absence of a signal means it was not accepted.

The main purpose of level 2 is to apply past-future protection. Owing to the very high event multiplicity in ALICE (dN/dy ~ 8000), it is not possible to perform track reconstruction in cases when two events overlap (pile-up). The time window in which events can overlap is quite large, and extends to twice the drift time of the TPC,
i.e. 200 µs. At the nominal luminosity for Pb-Pb collisions, $L = 10^{27} \text{ cm}^{-2} \text{s}^{-1}$, the probability of pile-up is 63%. The central trigger logs, bunch-crossing by bunch-crossing, all cases in which an interaction has occurred, and will veto any event for which there has been a previous interaction within 100 µs (past protection). It will also abort any trigger for which a second interaction is detected for a period of up to 100 µs after the interaction has taken place (future protection). Unlike L0 and L1, two types of L2 are sent: a level 2 reject, (L2r), can be sent at any time up to the full past-future protection interval, while a level 2 accept, (L2a), cannot be issued until the full interval has elapsed.

It is a feature of the ALICE experiment that each detector is treated independently. A physics trigger can be issued if all the detectors required for it are not busy. Each detector contributes a BUSY signal to the central trigger. A BUSY signal should be set as soon as a detector receives an L0 trigger and the detector holds this signal until it is again ready to record an event.

Event numbers are issued at level 1 (L1) when the event rates are reduced to close to their final level.

Event numbering in ALICE is complicated by the fact that not all detectors need take part in a given event, which means that trigger numbers will not be sequential. ALICE uses the RD-12 TTC system to distribute event numbers. For this reason, bunch-crossing numbers, which are distributed to all detectors, are used to identify events. As the bunch-crossing counter uses 12 bits, it is not large enough to identify events uniquely over a range of more than about 100 µs.

For this reason, the bunch crossing is augmented by an orbit number. One LHC orbit takes 88 µs. By adding a 32 bit orbit counter, the time over which an event can be identified uniquely can be extended to about 100 hours. The orbit number is not automatically counted on the TTCrx chip. Instead, it can be transmitted, using the TTC B channel, and kept, off the chip, in a 32 bit register.

The inter-relation between the trigger system and the front end buffering is illustrated by the simple data flow model in figure 4.

Data flow is from left to right. Data are produced in the sub-detectors, and are stored in a front-end register (FER) on receipt of an L0 signal. If there is no L1 signal (L0 timed out) the register is freed. On receipt of an L1 signal, which means a positive L1 decision, the data are transferred to a Multi-Event Register (MER), awaiting the L2 decision. Data in the MER can either be rejected or selected for transfer to DAQ. Following receipt of a level 2 accept (L2a), the data cannot any longer be rejected. This is indicated in the figure by a transfer from the MER (from which events can be discarded) to the MEF, a Multi-Event FIFO (from which they cannot). Once in the Multi-Event FIFO, the data must be transferred to the RORC, as soon as data traffic on the DDL will allow.

Each of the data transfers can be halted if the buffering space ahead of it is full. Thus, the transfer across the DDL is controlled by the $X_{on}/X_{off}$ signal, transfer to the Multi-Event FIFO can only go ahead if there is space in the

Fig 4 Conceptual buffering scheme for an ALICE detector system.
FIFO, and transfer to the MER can only take place if there is space in it.

The way this scheme is implemented in a given detector may vary from one case to another, but logically the functions described above should be present.

4. CONCLUSIONS

The requirements for the ALICE trigger have been revised in the light of the introduction of front-end buffering in detectors, and in order to accommodate the TRD. The latency for the earliest (L0) trigger is unchanged in the new scheme, but the latency for L1 becomes 5.5 µs. Buffering allows a more efficient use of the DDLs and reduces the overall data flow in the detector.

REFERENCES

3 CERN/LHCC/99-13
5 CERN/LHCC/99-22
6 CERN/LHCC/99-5
THE READOUT BUS OF THE ATLAS LEVEL-1 CALORIMETER TRIGGER PRE-PROCESSOR

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Abstract

The input to the ATLAS level-1 calorimeter trigger consists of 7200 trigger tower channels. The Pre-Processor system of the Level-1 calorimeter trigger provides facilities to read out this raw data on which the trigger decision is based. A high-bandwidth custom bus system, built from parallel point-to-point links, is used to collect data from several VME modules. These data are fed to the S-Link transmitter used for sending the read out data to the ATLAS DAQ system. The architecture of this bus system and results of first tests, performed within a modular test system, are presented.

1 The Pre-Processor system

All trigger data coming from the ATLAS calorimeters have to pass the level-1 trigger Pre-Processor system before it can be processed by the trigger. The Pre-Processor system performs digitisation of analogue input data, bunch-crossing identification and energy-calibration and then sends the data to the succeeding level-1 trigger processors. These generate an accept signal, which selects events for readout and further processing. Figure 1 shows a diagram of the Pre-Processor system.

An important aspect of the Pre-Processor system is the readout of raw trigger data. This is required to monitor the function of the trigger and to verify that the trigger data and the data from the seperated path of full-granularity readout of the calorimeters are consistent.

The Pre-Processor system consists of 128 VME modules, the Pre-Processor Modules (PPM), which process 7200 channels of trigger input data. Most of the processing is performed by an ASIC, the Pre-Processor ASIC (PPRAsic). The readout to the standard ATLAS data acquisition (DAQ) system is performed by 16 Readout Drivers (ROD), which format the read out data and feed them to the standard ATLAS readout link, the S-Link [1]. The collection of readout data is done in two steps. First it is collected on board-level by the so-called Readout Merger ASIC (RemAsic) using serial links, to the PPRAsics. In the second step data are collected from several modules and sent to the ROD, which then transmits it to the DAQ. For the inter-module collection of data a custom bus system is used. It is built from pipeline elements, which are connected by point-to-point links in a ring-like fashion. This bus, called the PipelineBus, is presented in the following sections in more detail.

The PipelineBus can not only be used for readout but also for sending configuration data to the connected modules. The ROD takes the role as source of these data and sends them to all connected Pre-Processor modules.

2 PipelineBus structure

A PipelineBus ring consists of several bus nodes. For the Pre-Processor system three different kinds of nodes are used. One ring consists of a master node, a S-Link node and several readout nodes. Figure 2 shows this configuration. The nodes and their connections form a closed pipeline.

The master node controls the bus by putting control commands into the pipeline. The commands propagate through the pipeline from one node to the other and are finally received back by the master. Because of the ring structure of the bus the master is able to check the reactions of the other nodes, which resulted in new or modified data on the bus. It then can take
appropriate actions like starting or stopping readout operations or initiating error recovery procedures.

Each Pre-Processor module acts as a readout node for the PipelineBus. On request of the master it puts event data on the bus. The data then propagate along the other nodes until it reaches the S-Link node.

The S-Link node takes the event data, which it receives from the bus, formats it to the standard ATLAS event format and sends it to the DAQ system using the S-Link transmitter.

The I/O part of all nodes is constructed in the same way as shown in figure 3. It consists of a 35 bit wide register and a multiplexer. The latched input data are available to the node for further processing. By using the select line of the multiplexer the node can control whether it just passes on the received data to the next node or if it injects new or modified bus data. All nodes are controlled by a common clock signal. Therefore the bus could also be seen as a kind of parallel shift register or FIFO.

With each clock tick the bus data are moved from one node to the next. The data words propagate through the bus in a pipelined way. With a clock frequency of 40 MHz the bandwidth of the bus amounts to 166 MByte/s. This includes protocol information.
The connections of the bus nodes are done by point-to-point links of a width of 35 bit. The advantage of point-to-point links is, that they are electrically and mechanically simple. That allows fast and reliable signal transmission. Also there are no big driver strengths necessary. Signals can be transmitted from chip to chip without additional buffers.

## 3 PipelineBus protocol

The 35 bus lines include a parity bit for error checking and two control bits, which identify the type of the bus word consisting of the remaining 32 bits of data. There are three different types of bus words, empty slot, command and data. The fourth control bit combination of 'b11' is unused and considered an illegal bus state.

Empty slot is the default state of the bus and means that the bus is unoccupied. Empty slots can be used to put commands or data in without restrictions. The contents of the 32 bit bus word is arbitrary.

Commands are used to control the bus. They are injected by the master node into the pipeline and processed by all nodes that the command addresses. Therefore the command word contains a 6 bit address field. An 8 bit token field is used to identify the command. 16 bit of argument data are available for commands which require parameters. The same field is used to store return values, which are generated by nodes as response to a command.

Two additional one-bit fields are available: an accept bit, which is set, when a node has processed the command, and an error bit, which indicates that an error occurred. If a bus node detects an error, e.g. a parity error, this bit is set and an error code is put into the argument field. The bus master has to process these error words and take appropriate actions.

There exist 15 different commands. There are commands for address configuration, control of readout and input, status information and commands, which are used to delimit data blocks.

If the control bits indicate that the type of the bus word is data, all 32 bits are used for user data.

As an example for a PipelineBus operation the process of reading out a few data words is depicted in figure 4. It is shown in three steps each representing several bus clock cycles. The big horizontal arrow stands for the pipeline and indicates the direction the bus words propagate. The two boxes below represent two readout nodes.

In step one the bus master has injected the command StartReadout. It propagates through the pipeline and when it passes the first readout node, the node enters readout mode, which is indicated by the small arrow above the node. In readout mode the node waits for the command BeginOfData, which activates the actual readout.

When the node receives the BeginOfData command
it looks for empty slots following the command and fills them with data. This is shown in step two. When a complete data block is written to the pipeline it is terminated by the node by an EndOfData command. The argument of this command contains the number of the node the data block belongs to. Then the node waits for the next BeginOfData command to insert the next block of data.

In step three the BeginOfData command has passed the second node. The node waits for the next empty slots and lets pass the data block of the first node. Then it fills the empty slots with its own data block and terminates it with an EndOfData command. After that the readout operation is finished. The event block, which was built during this operation, is now propagating through the pipeline to the S-Link node, which adds header and trailer information and sends it to the DAQ system.

The structure of the PipelineBus fits well to the S-Link interface. So only a small amount of formatting is necessary to build standard event fragments.

4 Test system

For testing the PipelineBus and other components of the Pre-Processor a flexible test and development system was built. It is based on a general-purpose motherboard, which contains commonly used functionality. Special functionality is added by application-specific daughterboards.

The motherboard (see figure 5) is implemented as 6U VME module and provides two CMC slots for inserting daughterboards. In addition to standard CMC cards the slots can also be used for S-Link cards.

Circuitry on the motherboard includes 32 kByte of RAM, a FPGA and a clock generator. It also provides the generation of a 3.3 V supply voltage.

Two PipelineBus daughtercards are used in the test system. One card represents a readout node and uses a prototype of the RemAsic [2] (see figure 6). The other card represents a master node. The logic for the master is implemented in the motherboard FPGA.

CompactPCI connectors are used on the front panel for connecting the bus nodes. The actual connection is done by small printed circuit boards, which connect two adjacent modules. To close the PipelineBus ring a flat ribbon cable is used. The middle row of the connectors is used for common control signals like the bus clock or the level-1 accept signal. Figure 7 shows a motherboard equipped with a master CMC and an I/O control card, which supplies these control signals.
References

Software

Conclusions
Abstract

The CMS calorimeter regional trigger system is designed to detect signatures of isolated and non-isolated electrons/photons, jets, missing and total transverse energy in a deadtimeless pipelined architecture. This system is comprised of nineteen crates of custom-built electronics. Prototype backplane, boards and ASICs built to validate this design are described here.

1. INTRODUCTION

The CMS detector for the Large Hadron Collider (LHC) presents an extraordinary challenge for its trigger and data acquisition system. Its trigger system must carefully sift the 40 MHz data to retain only interesting physics signals at 100 Hz level while discarding the well-known QCD background. The CMS solution to this problem is implemented in two physical levels, one based on custom electronics and the other relying upon commercial processors. The level-1 system uses only coarsely segmented data from calorimeter and muon detectors, while holding all the high resolution data in pipeline memories in the front-end electronics, to produce a trigger decision in 3 ms. Level-1 triggered events at 100 kHz rate are sifted further in higher levels of triggers implemented as software filters.

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of physics objects such as photons, electrons, and jets, as well as global sums of $E_T$ and missing $E_T$ (to find neutrinos). Each of these physics is required to pass a series of $p_T$ or $E_T$ thresholds, which are used in making the Level 1 Trigger Decision.

The electron/photon trigger is based on the recognition of a large and isolated energy deposit in the electromagnetic calorimeter by asking for a small hadronic energy deposit in the HCAL in the cluster region. There are different thresholds for inclusive electrons/photons, dileptons, and for very high $E_T$ electrons. The isolation cuts are relaxed and finally eliminated for triggers with increasing $E_T$ thresholds.

2. DESIGN OVERVIEW

The calorimeter level 1 trigger system receives digital trigger sums from the front-end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers, for the same crossing, will be sent on a single link in eight bits apiece accompanied by five bits of error detection code and a 'fine-grain’ bit characterizing the energies summed into the trigger towers (i.e. isolated energy for ECAL, quiet first longitudinal compartment for HCAL).

The calorimeter regional crate system uses 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. These crates are cover the region $|\eta|<3$. The remaining crate covers both Very Forward Calorimeters that extend missing $E_T$ coverage to $|\eta|<5$.

Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum $E_T$, $E_X$ and $E_Y$. It also sends its 4 highest-ranked isolated and non-isolated electrons, and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide electrons and jets, as well as the total calorimeter missing and sum $E_T$ to the CMS global trigger.

The regional calorimeter trigger crate has a height of 9U and a depth approximately of 700mm [1]. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are seven rear mounted Receiver cards, seven front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 15 processor cards per crate. These cards and an additional clock and control card are plugged into custom “backplane” which provides point-to-point links between the cards. VME bus is also provided to these cards using high density connectors in top 3U section of the backplane. In addition there are two slots with standard VME backplane connectors for crate processor and monitoring cards.

2.1 Receiver Card

The Receiver card is the largest board in the crate. It is 9U by 400mm. The rear side of the card receives the calorimeter data on serial copper cables, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The

lookup tables translate the incoming information to transverse energy on several scales. They are also used to test for Quiet and Minimum Ionization thresholds for each trigger tower. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for inter-crate sharing.

Each card is designed to receive 32 high speed copper links from the calorimeter readout electronics. Each link transmits either two towers of hadronic or electromagnetic information per crossing for a total of 64 channels from 32 ECAL and 32 HCAL towers per card. The present design for the data uses a 24-bit frame including 18 bits of data and 5 bits of error detection code. The data consists of 8 bits of energy on a compressed scale and one bit of fine-grain information per tower. The error code is sufficient to detect all single and double bit errors as well as many multiple bit errors. The error bits are necessary for error logging and to zero problem channels. The 24-bit word uses 8/10 bit encoding, which implies a 1.2 GHz serial link. The cable length to the calorimeter electronics is estimated at 20 m.

The rear side of the Receiver card has serial receivers based on the specifications of the Vitesse 7214 4-channel Interconnect Chip. The design provides for cable/connector equalization and the option of transformer isolation on daughter cards.

The front side of the Receiver card contains the synchronization circuitry followed by the memory look up tables, adder tree and backplane drivers. The outputs of the receivers are not only unsynchronized with the local clock but are also not necessarily aligned to the same bunch crossing. The phase alignment circuitry is contained on an ASIC (Phase ASIC). The Phase ASIC desksews the data, decodes the error detection codes and multiplexes the output at 160 MHz. The Phase ASIC also provides test vectors for board and system diagnostics.

In order to achieve maximum utilization of board space, all the logic following and including the Phase ASIC is run at 160 MHz. There are also four Error Detection Codes (EDCs) associated with the four input channels of each Phase ASIC. After synchronization, each EDC is checked against the data. If an error is detected a single bit is set, one for each incoming channel, and appended to the original EDC code.

Lookup tables are required to translate the information coming from the calorimeter readout electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear $E_T$ with a resolution of approximately 1 GeV. These values are summed to provide total energy in 4 x 4 trigger tower regions of the calorimeter. The summation is performed by an Adder ASIC. Thirty-two towers, in a 4 x 8 array, are processed on each card. The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. These 13 bit numbers will be multiplexed onto a single set of 13 differential pairs at 160 MHz.

The electron/photon finding algorithm itself is implemented in a separate card. The data required for this algorithm is transferred between the Receiver cards and the Electron Isolation cards at 160 MHz. In order to retain point to point transmission data must be transmitted through separate drivers on separate backplane lines. Every Receiver card shares its data with at most 6 Electron Isolation cards within the same crate. In addition each Receiver card sends some of its data off crate at 40 MHz to two or three neighboring crates. Crate to crate communication is handled by special cables running between the Receiver cards. This distributes the inter-crate buffering among the eight Receiver cards in a crate rather than attempting to put it all on one or two special cards at the ends of each crate.

### 2.2 Crate Backplane

The crate backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. All signals in the trigger data portion of the backplane will be transmitted on point to point links at 160 MHz. This data rate was chosen because it offers the opportunity to compress the number of data lines on the backplane and in the pipelined data logic by a factor of four.

The front and rear insertion of cards in the data processing section of the crate was chosen to allow greater separation between cards to provide a more protected environment for the links connected to the rear mounted Receiver cards. The increased separation will promote better cooling of the cards, and will enable a wider selection of front panel components.

### 2.3 Electron Identification Card

Electron Identification algorithm within each 4x8 trigger tower region is performed on a smaller 240mm deep card. Data for thirty-two central towers and twenty-eight neighboring towers is required to determine isolation for towers on the edge of the 4 x 8 region. This card receives linearized transverse energy on 7-bit scale for ECAL and 4-bit scale for HCAL and ECAL fine-grain bit from corresponding receiver card. It also receives neighbor tower data from up to three other receiver cards in the crate. Neighbor crate data is transferred through the receiver cards where it undergoes any realignment of phase. The algorithm which finds isolated and non-isolated electron/photon candidates is implemented in an ASIC. Candidate with highest $E_T$ of both types in each of the two 4x4 regions covered by the card are transmitted to the Jet/Summary card.
2.4 Jet/Summary Card

Jet/Summary card receives 4x4 trigger tower energy sums from all Receiver cards in the crate and isolated and non-isolated electron/phonon candidate energies from all Electron Identification cards in the crate. It sorts these candidates and forwards top 4 jets, isolated and non-isolated electron/phonon candidates to the global calorimeter trigger crates on copper cables. In addition it also contains lookup tables to convert the 4x4 E_T to E_x and E_y and adder trees to sum up crate wide sums of all three of these quantities.

3. PROTOTYPES

3.1 Work Accomplished

The goals of prototype development for this trigger system are many fold. Our strategy was to build as far as possible full-scale prototypes so that system issues are confronted up front. Pictures of rear and front views of the prototype crate holding prototype backplane and cards are shown in Figures 1 and 2.

Figure 1: Rear view of prototype CMS calorimeter regional trigger crate showing the custom backplane and a receiver card.

To prove that high speed and high signal density can be handled, we have built a full sized backplane with point-to-point 160 MHz links and VME control. The backplane is a monolithic printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first two slots of the backplane use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME module can be inserted in the first two stations. The form factor conversion to the remaining slots is performed on the custom backplane. The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed controlled-impedance connector for both front and rear insertion. The design is based around a 340 pin connector, by AMP Inc., to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards. There are 1419 differential 160 MHz point-to-point links on the backplane between the various cards. The backplane is constructed with five ground and power planes and five signal layers with the differential pairs held to the same layer.

We built a clock and control card to provide the necessary signals to drive other cards in the crate. The signals on even the longest links on this backplane preserve their characteristics well. Results from testing clock signals on the backplane show rise and fall times of 0.8 ns from 20% to 80% height with reasonable signal levels even when measured at the farthest card slot. This performance meets the requirements of 160 MHz operation of the backplane.

Figure 2: Front view of the prototype crate showing the clock and control and electron isolation cards plugged into the custom backplane.

The receiver card is by far the most complicated item in our design. We have built a full scale prototype of this card, shown in Figure 3, with large amount of ECL SRAM for lookup tables, support circuitry for three Adder ASICs needed on this card and drivers for all backplane lines. In order conserve the board space and to reduce power consumption, the production boards will combine various discrete components used to stage the data on into a multipurpose ASIC that also provides certain card Boundary Scan functionality. VME, Adder ASIC and
inter-crate data sharing circuitry on this card have been tested to function with adequate performance.

![Figure 3: A picture of the front side of prototype receiver card showing the three Adder ASICs used for making 4x4 trigger tower sums used to find jets and determine missing $E_T$.](image)

The Adder ASIC sums 8 signed 10-bit operands to a single signed 10-bit result at 160 MHz. We fabricated prototype adder ASICs which sums eight 10-bit signed numbers in a total of 4 25 ns clock-steps. These ASICs, built by Vitesse in 0.6 $\mu$H-GaAs technology, chosen for its speed and ECL output capability, have been tested to work at 200 MHz, well above our specifications. The Adder ASIC consists of approximately 11,000 cells and uses 4 W. The tests of the Adder ASIC on the receiver card were successful so that we deemed this design of the Adder as final and are in the process of procuring production quantities.

### 3.2 Work in progress

The receiver card uses daughter cards mounted on its rear side to receive its input from calorimeter front-end crates. We have designed these daughter cards with serial link chips (Vitesse 7214) and associated signal equalization support. These circuits along and an independent test card are in fabrication. We plan to use these cards to test the feasibility of receiving data on 20 m long copper cables at 1.2 GHz.

Success of our Adder ASIC prompted us to select the same technology for making other ASICs in our system. We have made preliminary designs of Phase ASIC described above, Electron Identification ASIC, Boundary Scan/driver ASIC and Sort ASIC and have agreement with Vitesse to produce these ASICs. Detailed design work is now in progress.

We are also carrying over the knowledge gained in making the prototypes discussed here in designing final backplane and other cards. We are incorporating the refinements made to the electron finding algorithm that resulted in some changes in the dataflow. The Receiver card prototype prompted us to move most of the discrete logic, used on that card to stage data to EID and Jet cards, into the Boundary scan ASIC. Another change we made is to use on card DC-DC converters to distribute needed power at appropriate voltages.

### 4. SUMMARY

We have made several full scale prototypes of the CMS regional calorimeter trigger system. Successful evaluation of these prototypes has validated key elements of our design. We are in the process of evaluating serial link technology that is crucial for the feasibility of the system. Successful validation of the Adder ASIC on the prototype Receiver card has prompted us to begin design of all other ASICs required in our system. We have simulated the performance of this system using detailed Monte Carlo [2]. We believe that this system satisfies the CMS physics requirements, while meeting the bandwidth requirements imposed by the data acquisition system. This design with its extensive use of lookup tables has sufficient flexibility for tuning rates and optimizing efficiencies.

### 5. ACKNOWLEDGEMENTS

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The electron/photon and tau/hadron Cluster Processor for the ATLAS First-Level Trigger - a Flexible Test System

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Abstract

The electron/photon and tau/hadron first-level trigger system for ATLAS will receive digitised data from approximately 6400 calorimeter trigger towers, covering a pseudo-rapidity region of ± 2.5. The system will provide electron/photon and tau/hadron trigger multiplicity information to the Central Trigger Processor, and Region of Interest information for the second-level trigger. The system will also provide intermediate results to the DAQ system for monitoring and diagnostic purposes. The system consists of four different 9U-module designs and two different chip (ASIC/FPGA) designs. This paper will outline a flexible test system for evaluating various elements of the system, including data links, ASICS/FPGAs and individual modules.

1. INTRODUCTION

The cluster processor (CP) system for the electron/photon and tau/hadron first-level trigger [1] will receive digitised data from approximately 6400 calorimeter trigger towers from the Pre-processor system using serial links. The CP system consists of four crates of cluster processor modules (CPMs), each crate processing a quadrant of the calorimeter in φ and the complete η range (±2.5). This is carried out by using 13 cluster processor modules per crate, each processing a 0.4 × 1.6 (Δη × Δφ) region of the calorimeter. The partial trigger multiplicity from all the CPMs will be merged on separate cluster hit-counting modules (HCMs), and the final multiplicity result transferred to the central trigger processor (CTP) where the level-1 decision is made.

Read-out driver modules (RODs) in another crate will handle the DAQ data from all the CPMs and regions of interest (RoI) information for level-2 by using different firmware. The data will be transferred onto the RODs using high-speed serial links, and the RODs will further process and format the data before transferring it to the appropriate destinations via S-links. The DAQ data can be accessed using a single board computer in the ROD crate for system diagnostics and monitoring.

Figure 1. Cluster Processor System
Each of the crates in the CP system will include a timing and control module (TCM) which will interface to the LHC timing distribution system (TTC) and the Detector Control System (DCS).

Four different 9U-module designs and two different chip (ASICs or FPGAs) designs will be required for the CP system.

During the system development and commissioning phases we will require a source of data to drive the inputs of the devices under test, and a means of verifying the resultant outputs. We have designed a data source and sink (DSS) module to handle various test scenarios, including testing, ASICs, FPGAs high-speed links, RODs and CPMs.

2. DATA SOURCE AND SINK MODULE

The data source and sink module consists of a motherboard and daughter card combination (figure 2). The motherboard is a 6U VME board with space for two single Common Mezzanine Card (CMC) standard [2] daughter cards or one double CMC standard daughter card, and space for a timing card such as the CERN TTCrx test card [3] or a ‘custom’ timing card. The motherboard can also host the S-link standard [4] source and destination cards on the underside of the module.

2.1 Motherboard

The motherboard implements common functions, such as a standard A32/A24, D32 VME interface, control and status registers, and a TTC interface. Extensive use of FPGAs gives the DSS module the capability of generating, receiving and comparing programmable test data patterns in real time at least up to 40 MHz. Eight 32K × 32 bit dual-port RAMs and eight FPGAs (data FPGA) will handle the data source/sink requirements, as well as handle all the interface signals required by each type of daughter card. Figure 3 shows a block diagram of the DSS motherboard. Separate FPGAs (S-link FPGAs) and the dual port RAMs associated with the S-link FPGAs will handle the S-link data.

2.2 FPGA Implementation

The FPGAs used in this design are Xilinx XC4028XLA devices [5]. There are 10 FPGAs on the motherboard, out of which eight FPGAs (data FPGAs) handle data from the two CMC daughter cards, and the other two FPGAs (S-link FPGAs) handle S-link source and destination data and control. The `data FPGAs’ handle source data and sink data in two blocks of four, interfacing to the two daughter cards via the CMC connectors as shown in figure 3. The two blocks of FPGAs can be configured to be either a source or a sink, or both source or both sinks.

Figure 2. DSS Module

Figure 3. DSS Block Diagram
2.3 Source FPGA

The source FPGAs (figure 4) will perform the following functions:

1. Provide interface to the daughter cards.
2. Implements a Pseudo Random Bit Pattern (PRBP) generator and checker. Other data patterns such as ramps can also be implemented if required.
3. Directly connect the dual-port RAM data bus on to the connector pins, allowing various test patterns to be generated.
4. Implement the Serialiser FPGA readout logic to test the prototype readout driver.

2.4 Sink FPGAs

The sink FPGAs (figure 5) will interface between the dual-port RAM and the daughter cards, recording the data on to the dual-port RAM from the daughter cards, which can then be accessed via the VME. It will also provide:

1. Bit error checking facility on the PRBP data. This data is also written onto the dual-port RAMs.
2. Bit error checking between the received data and pre-loaded data on the dual-port RAM.
3. When an error occurs the data word is recorded onto an internal register with the contents of the address counter, which can be read out via the VME.

2.5 Configuring the Data FPGAs

Since the DSS will be used in various test scenarios, to give the maximum flexibility for the module users the data FPGAs can be configured in the following ways.

1. EEPROMs (equivalent to Xilinx XC1701L) on the motherboard or on the daughter card itself (see section on daughter cards) can be used to configure the data FPGAs. These EEPROMs are socketed so they can be programmed with the configuration data using a standalone device programmer.
2. In-System-Programming (ISP) via a JTAG port is provided to download configuration data from a PC.
3. A port via a VME register is provided for downloading the FPGAs as well as the EEPROMs through VME.

2.6 VME Interface

An A32/A24, D32 VME interface, and common functions such as register decoding, and control and status registers, are provided by two CPLDs on the motherboard which can be programmed in-system via a JTAG port.

2.7 CMC Daughter Cards

The CMC daughter cards will implement the physical layer to transmit/receive data up to 80 bits wide. If required the daughter cards can ‘personalise’ the motherboard to perform the required functions by placing the configuration EEPROM on the daughter cards (automatically disables the EEPROM on the motherboard if present). Figure 6 shows some of the daughter cards required to test the trigger prototypes. The 960 Mbaud G-link receiver and transmitter cards, and the 480 Mbaud LVDS serialiser and de-serialiser cards, have been designed and manufactured to carry out the link tests, the prototype ROD tests and to test the prototype CPMs (see section on testing below).

2.8 Timing Cards

A plug-in daughter card provides the DSS module with the appropriate clock signals. This could either be the CERN TTCrx test card, a custom card or the prototype timing and control receiver module. A custom card has been designed and manufactured to deliver a clock and two de-skew clocks at 40 MHz, and a start/stop signal to the DSS module. These signals can be generated internal to this card or the clock and start/stop signals can be brought onto the card from an external source via the front panel connectors. This card can be used for standalone tests without the need for the TTC system. Using the TTCrx test card and the TTC system (TTCvi, TTCvx) allows you to generate test patterns simultaneously using a broadcast command.
2.9 S-Link Daughter Cards

There are connectors on the back of the motherboard for an S-Link source card and for an S-Link destination card. Commercially available electrical parallel S-Link cards will be used for the prototype ROD tests.

3 DSS APPLICATIONS

The DSS module with different CMC daughter cards will be used for testing various prototypes, including: LVDS links, FPGAs/ASICs, RODs, CPMs and HCMs.

3.1 LVDS Link Tests

In the demonstrator system [1] we have successfully shown that we can use the HP G-Links [6] at 960 Mbaud between the Pre-processor system and the cluster processor system up to 10 m with co-axial cables. However, due to the high power dissipation of these device we are considering the use of the newly available LVDS chip sets [7] from National Semiconductor to replace the G-links. Therefore the first use of the DSS module will be to test these LVDS chips with appropriate cables. The LVDS serialiser/de-serialiser chip sets will be used to serialise ten bits on to a 480 Mbaud (10 data bits + 2 start/stop bits) link. The complete data chain including the LVDS chip set, category 5 or 6 halogen-free cables, and 2mm BERG METRAL style connectors will be tested to establish the maximum (require at least 10 m) cable length with a bit-error-rate better than $10^{-9}$ per trigger tower for less than 1% false trigger rate. The BERG METRAL connectors are used to bring the signals on to the CPMs via the backplane edge to ease the removal of modules for maintenance, etc.

3.2 ROD Prototype Tests

For ROD prototype testing, the DSS module with the G-Link transmitter daughter card emulating the read-out logic on the CPM, and a S-link destination card receiving the processed and formatted data from the ROD, emulating the read-out buffer (ROB) function will be used in a test system as shown in figure 7.

3.3 Prototype CP System Tests

Figure 8 shows a test set-up which will test the CP system. Here the DSS modules are used: (a) with LVDS serialiser daughter cards to emulate Pre-processor modules (PPMs), sending test patterns to the CPMs; (b) with S-Link destination daughter cards to emulate ROBs and the level-2 RoIB builder module; (c) with LVDS parallel daughter cards to emulate the CTP, receiving the cluster-hit multiplicity from the hit counting modules.

![Figure 6. Daughter Cards](image)

![Figure 7. ROD Prototype Test Set-up](image)

![Figure 8. CPM Prototype Test Set-up](image)
3.4 Other Applications

The DSS module can also be used for other applications. For example, clock sequencers and data acquisition modules with an appropriate FADC daughter card. Figure 9 shows a possible implementation of a CCD readout module using the DSS module. In this application one daughter card is used to generate the appropriate clock sequences to the CCDs and a second CMC daughter card is used to receive the analogue data and convert to digital, which can then be read out via the VME. A maximum of eight 10-bit ADCs should be possible on one CMC daughter card (80 bits per CMC card).

4. SUMMARY AND CONCLUSIONS

We are now in a prototyping stage, and will soon move into designing, implementing and commissioning the final system in ATLAS. Prototypes represent the functionality of the final modules, with a smaller number of channels than in the final modules. To test these prototypes we require a source of data and a way of verifying the results from the prototypes. The DSS module we have designed with the motherboard and daughter card combinations is flexible and is reusable in many combinations, in testing the trigger prototypes, the pre-production and the production modules right through to commissioning and maintaining the system in ATLAS. Also the DSS module with the appropriate daughter cards could have other applications other than for test data source and test data sink. The first use of the DSS will be to test the LVDS 480 Mbaud serial links. We will maintain a FPGA firmware library on the web that will contain various FPGA designs for the DSS module user [8].

5. REFERENCES

[8] Contact viraj.perera@rl.ac.uk for further information.
Abstract

The endcap muon detector for CMS uses Cathode Strip Chambers (CSCs) to deliver precise muon position and timing information in a high background rate environment[1]. Trigger electronics for this system need to reliably identify the bunch crossing in spite of drift times spanning several crossings, and need to precisely measure the muon bend plane coordinate in each station to allow momentum measurement in spite of limited magnetic bending power. Prototypes were placed in test beams at CERN in the summers of 1998 and 1999. Results from these tests on pattern identification, timing efficiency, and spatial resolution are presented. Plans for future developments are also described.

1. CMS ENDCAP MUON CSC SYSTEM

Before discussing the details of the electronics, it is useful to review the general layout of the Cathode Strip Chamber system used in the CMS Endcap Muon detector. This detector is planned for 4 stations, however, at present construction money for only 3 stations is assured. There are 432 CSC chambers, each 10- or 20-degree trapezoidal 6-layer chambers in the 3-station detector as shown in Figure 1.

2. CSC TRIGGER PRIMITIVES

Simulations indicate that at maximum luminosity, several background clusters exist within each CSC at any given time. To reduce the otherwise huge background rate, CSC trigger primitives are formed from the spatial coincidence of clusters in the 6 layers of the chamber.

The cathode strip cluster position is determined for triggering to one-half of a strip width in each layer[2]. This is done with a 16-channel ‘comparator’ ASIC that inputs amplified and shaped signals and compares the charges on all adjacent and next-to-adjacent strips. If a strip charge is found to be larger than those on its neighbors, a hit is assigned to the strip. Also, comparison of left versus right neighbour strip charges allows assignment of the hit to the right or left side of the central strip, effectively doubling the resolution. The six layers are then brought into coincidence in ‘Local Charged Track’ (LCT) pattern circuitry (see Figure 2) to establish position of the muon to an RMS accuracy of 0.10-0.15 strip widths. Strip widths range from 6-16mm. Because of the slow 150ns rise-time of the cathode amplifier/shapers, the cathodes cannot uniquely identify the bunch crossing.

The anode wires are ganged 10-15 to a group, and their signals are fed into amplifier/constant-fraction discriminators. Since the drift time can be as large as 50ns, a multi-layer coincidence technique in the anode LCT pattern circuitry is used to identify the bunch crossing. For each spatial pattern of anode hits, a low coincidence level, typically 2 layers, is used to establish timing, whereas a high coincidence level, typically 4 layers, is used to establish the existence of a muon track. The algorithm is illustrated in Figure 2.

3. 1998 PROTOTYPES AND RESULTS

Electronics prototypes were tested on a full-size prototype of the largest CSC chamber in the summer of 1998 at CERN. Tests were done first at the H2 beam line, where a Silicon beam telescope was used for resolution studies. Later tests were done at the GIF (Gamma Irradiation Facility), where LHC-like backgrounds were provided by an intense gamma source. The chamber is shown at the H2 beam line in Figure 3.
3.1 Cathode Comparator ASIC Tests

The 16-channel cathode comparator ASICs that were tested during summer 1998 had 32 half-strip output bits. Six of these chips were mounted on a 96-channel comparator board (Figure 4) that attached directly through connectors to the cathode front-end board. The 192 half-strip bits were converted from TTL levels to differential LVDS and 96 of these signals were driven on cables to a cathode LCT card in a CAMAC crate, where they were recorded.

The efficiency of the comparator ASICs for identifying the correct half-strip was determined in two ways. First, the half-strip bits were compared to bits predicted by the precision charge determination of the front-end DAQ cards[3]. These cards employ switched-capacitor arrays (SCAs) for charge storage, and ADCs for digitization. Typical noise levels on the DAQ data were 1.6fC (1.6mV after the amplifier/shapers), while typically the total cathode charge read out was 100fC. The efficiency was found to be 90.4±0.2% for exact half-strip match, while a match window of ±1 half-strips yielded an efficiency of 98.3±0.1%. The second way to determine the comparator match efficiency is less biased but gives lower statistics. This method uses the precision DAQ data to track muons through the chamber, leaving out one layer (#3) from the fit. The extrapolated position in this layer is then compared to the half-strip bit found by the comparator ASIC. By this method, the efficiency for exact match is measured to be 88.2±0.7% for exact half-strip match, while a widened match window of ±1 half-strips yields an efficiency of 94.9±0.4%.

3.2 Cathode LCT Tests

The half-strip bits found by the comparator ASICs were sent to the cathode LCT card (Figure 5), which identified the multi-layer patterns of valid muon trajectories. A mezzanine card converted LVDS signals to TTL levels. These signals were distributed by a "front" Altera 10K50 FPGA to Cypress 128Kx8bit SRAMs, which found the patterns, while a "rear" Altera 10K20 FPGA collected the patterns (if any) found by the SRAMs and selected the best according to pattern number. Higher numbers corresponded to larger numbers of hit layers and straighter tracks. The CAMAC interface was implemented in another Altera 10K20 FPGA. Output trigger information was fed through a National Instruments Channel-Link to a "Trigger Motherboard" which sorted LCTs in the case of multiple candidates, and performed a time coincidence between cathode LCTs and anode LCTs.

Patterns having four or more hits corresponding to a straight line within a particular angular range were allowed. An additional feature of the cathode LCT card was the ability to trigger on high-angle tracks, which could be very low-momentum tracks in the case of CMS. This was done by grouping the half-strips 4:1 into di-strip units. At 40 MHz, the cathode LCT module searched for low-Pt patterns. When such a pattern was found, four subsequent clock cycles followed in which the module searched for patterns using half-strip bits. If di-strip patterns and half-strip were both found, the half-strip patterns were always favoured, except in the case of a 6-hit di-strip pattern and a 4-hit half-strip pattern.

The efficiency of the cathode LCT card for identifying muons was measured in one case by comparison with the precision DAQ data, and in the other by comparison to external muon tracking provided by a Silicon telescope. The position reported by the cathode LCT card corresponded to the track position at chamber layer 3. When DAQ data was found in Layer 3, the position of the cathode LCT was compared to the Layer 3 cluster center. Of these events, 95% were found as half-strip patterns, 4% were found as di-strip patterns only, and 0.8% were not found by the
cathode LCT card. The deviations in position between the DAQ data and the cathode LCT trigger are shown in Figure 6, in half-strip units.

Figure 6 Position resolution of cathode LCT as compared to DAQ data: on top for half-strip patterns, on bottom for di-strip patterns found. The "overflow" bin is for missing cathode LCTs.

The second method for estimating the efficiency, as well as resolution, of the cathode LCT card, is by using the Silicon tracking telescope. This telescope defines tracks to an accuracy of about 100 µm after 100cm extrapolation to the chamber. Half-strip cathode patterns were found for 96% of the tracks, with position residuals (Figure 7) very close to a box distribution one-half strip wide. Another 3.7% of tracks were found as di-strip patterns by the cathode LCT logic. The positions of these tracks in di-strip units (Figure 8), shows that di-strip patterns occur at the boundaries between half-strips, where the half-strip pattern tables were not optimally tuned. Another 0.25% of tracks were not found by the cathode LCT logic. The tracks for these events point mainly to the boundaries between di-strip units, where again the pattern tables were not optimally tuned. The net cathode LCT efficiency is found to be 99.75±0.04% in this study.

3.3 Anode LCT Tests

The anode LCT card differs from the cathode LCT card only in FPGA and RAM configurations. For the anode LCT card, there are two efficiencies to be evaluated: wire pattern-finding, and bunch crossing identification. The wire pattern-finding efficiency was found by comparison of the position of layer 3 TDC hits to the anode LCT position (Figure 9). It is found that 98.7% of tracks match exactly, 0.8% match within 1 wire group, 0.4% are further away, and 0.1% of events contain no anode LCT pattern. If ±1 wire group matching is allowed, the overall anode LCT pattern finding is then 99.5±0.1% efficient.

To find the bunch crossing efficiency, the anode LCT module uses an n-layer coincidence technique. At the test beam, the muons arrive asynchronously to the 40 MHz clock used by the synchronous electronics, unlike in the LHC conditions. The phase of the muon arrival was determined by using a TDC to measure the delay between the muon scintillator and the 40 MHz clock. An efficiency was determined by using only data which had the optimum phase, as shown in Figure 10. This figure also verifies the system timing accuracy specification of ±2 ns, since the bunch crossing efficiency is still high. Such curves were measured for all choices of layer coincidence, and the efficiencies for correct bunch crossing identification are shown in Table 1. Optimal efficiency is found for coincidence levels 2, 3, or 4.
Figure 10 Efficiency versus phase of the muon arrival with respect to the 40 MHz electronics clock.

Table 1 CSC bunch crossing efficiency versus coincidence level.

<table>
<thead>
<tr>
<th>Coincidence Level</th>
<th>Relative Timing</th>
<th>Bunch Crossing ID Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 ns</td>
<td>98.0±1.0%</td>
</tr>
<tr>
<td>2</td>
<td>+3 ns</td>
<td>99.2±0.3%</td>
</tr>
<tr>
<td>3</td>
<td>+8 ns</td>
<td>99.2±0.3%</td>
</tr>
<tr>
<td>4</td>
<td>+12 ns</td>
<td>99.1±0.5%</td>
</tr>
<tr>
<td>5</td>
<td>+14 ns</td>
<td>98.5±0.6%</td>
</tr>
<tr>
<td>6</td>
<td>+19 ns</td>
<td>98.0±0.8%</td>
</tr>
</tbody>
</table>

The bunch crossing efficiency of the anode LCT has also been studied at the GIF facility versus background rate. The efficiency stays above 99% up to the nominal maximum LHC rate of 20 kHz/wire group, dropping only slightly to about 98.5% at seven times the maximum rate, i.e. 140 kHz.

3.4 Trigger Motherboard Tests

It is anticipated that anode and cathode LCTs will be brought into time coincidence with a window of ±1 bunch crossing at the Trigger Motherboard. The mode of triggering and the high rate of test beam muons did not allow a background-free test. However, the relative timing between anode and cathode was found with some background by plotting all of the time differences between cathode and anode LCTs, which were stored in a FIFO in the Trigger Motherboard prototype. The efficiency for time coincidence within ±1 crossing was measured to be 98%. A higher efficiency could be attained by applying a phase correction for the muon arrival versus 40 MHz clock phase times.

4. 1999 ENGINEERING PROTOTYPES

During 1999, a number of design changes were made to improve system design and reduce costs. In particular, 4:1 data compression was added to the comparator ASIC, anode data was latched at the LHC frequency on the front-end boards, and the LCT modules were re-designed to allow higher channel density and faster processing. Both anode and cathode front-end cards used National Instruments Channel-Links to compress the data carried to the LCT cards by serialization. The trigger modules were tested at the CERN GIF facility during September 1999. Detailed results are not yet available from these tests.

The most important parameter for the comparator ASIC is the offset on the comparators. The measurements for 96 channels are histogrammed in Figure 11. The RMS spread of 1.9mV is similar to the amplifier/shaper noise level, and simulations show that a half-strip efficiency of about 93% may be expected with this level of threshold spread. The addition of amplifier/shaper noise results in a half-strip efficiency close to the observed 90% level described earlier in this note. The data compression algorithm used in this latest comparator ASIC takes advantage of the slow-developing preamp/shaper signals, which peak in 150ns and have a full width of about 300ns. Since comparisons of adjacent strip charges can result in only one half-strip within any di-strip unit, the four half-strip bits which were formerly produced can be replaced by a single-bit 40 MHz serial "triad". The first bit of the triad indicates the presence of a hit, and is followed by a 2-bit address of the half-strip hit within the distrip.

Figure 11 Histogram of thresholds (mV) on comparator ASIC channels.

During 1999, a 96-channel anode front-end board (Figure 12) was made, incorporating trigger features. Analog and digital sections were kept completely separate, sending only differential LVDS signals between the sections. The amplifier/discriminator ASICs included a fine-delay adjustment feature with 3ns per step. This allows data to be latched at the LHC frequency with the correct phase, regardless of time-of-flight and other delays. The data was latched at 40 MHz and serialized with National Instruments Channel-Links, then output on two 26-pin SCSI connectors to Skew-Clear cables for transmission to the LCT cards.

Figure 12 Anode front-end 96-channel board.
9U-size LCT cards produced in 1999 (see Figure 13) handle large numbers of front-end signals, due to the data compression in comparator ASICs as well as the use of Channel-Links. Cathode LCT boards take strip signals (480) from an entire chamber, while anode LCT boards handled 192 wire groups, one half of a chamber. Input signals are received by Channel-Links and fed into a single Altera 10K200E FPGA. Cathode and anode LCT boards differ only by the FPGA configuration. The LCT boards record input bits and found patterns to the DAQ system through a FIFO dump to a DAQ motherboard.

![LCT99 480- or 192-channel board.](image)

**Figure 13** LCT99 480- or 192-channel board.

### 5. FUTURE PLANS

The system as configured in 1999 tests is close to the expected CMS system. At present, the expense of cables and anode front-end boards looks to be greatly reduced if the anode LCT card is placed on-chamber. A prototype card handling an entire chamber will be produced next year. Radiation testing and comparator ASIC production may also take place during the coming year. Other work that may begin later will be to combine the cathode LCT and Trigger Motherboard functionality on a single card to reduce costs and improve trigger latency, and the use of TTC for clocking. The issues of slow control and remote configuration have not yet been fully solved for this system and will need to be addressed soon.

### 6. CONCLUSIONS

The basic design of the CSC trigger primitives for the CMS endcap muon system has been verified using prototypes running in muon test beams with and without LHC-like background conditions. A comparator ASIC has undergone three generations and may be ready for production. Two generations of re-programmable cathode and anode LCT modules have been produced, and are close to the final design stage. Some additional modifications to the system design are being contemplated mainly to reduce cost.

### 7. REFERENCES


### 8. ACKNOWLEDGEMENTS

The results presented in this paper depended on the efforts of many people. In particular, I would like to acknowledge J.C. Santiard, who developed the comparator ASIC; H.C. Shankar, who developed the comparator board; J.K. Smith, who developed the LCT cards; P. Padley and M. Matveev, who developed the Trigger Motherboard; Y. Shi, who produced and debugged many of the trigger boards; L. Gorn, W. Gorn, and B. Smith, who made it easy to do analysis of test beam data; and A. Attal and F. Petriello, who did important analysis of test beam data.
NEW APPROACH FOR THE CMS MUON TRIGGER TRACK FINDER PROCESSOR

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ABSTRACT
The CMS Group of HEPHY/Vienna develops the Barrel Track Finder Processor for the CMS Muon Trigger. Its first design approach proved its feasibility, but showed also many drawbacks caused by the numerous connections between Processors belonging to the neighbouring muon sectors. This implied further synchronisation problems as well. A new approach concerning required muon track elements allows to reduce the neighbour connections, but also enabled to elaborate a global track finding method that results in a faster process. As another result the hardware might utilise FPGAs instead of the planned ASIC technology. We cover the new design and its simulation results.

1. INTRODUCTION
In 1997 the first phase of the Muon Trigger Track Finder development finished. The design and the prototype built showed the feasibility of the basic ideas and the possibility to build a hardware of this type [1], [2]. It showed however many drawbacks that made it necessary to consider new solutions and improvements allowing to design a simpler and better maintainable hardware with the same functionality level. The main problem areas were the following:

- The design contained only the Track Finding Functions. It did not contain Input Receiver, Synchronisation and Redistribution modules.
- The Design consisted of a very large number of Neighbour Input and -Internal Result connections. Thus the electronics was limited by the chips’ pin amount rather than the logic components.
- The Track Linker and Selection blocks were hard to overview and their functionality difficult to analyse.
- As described in [3] the Parameter (Feature) Assignment Unit was not optimised, the decision for the most effective algorithms was open.
- The design could be considered too optimistic concerning the electronics - although feasible, probably only with expensive fast ASICs.
- No recommendations were issued concerning system-wide aspects, like system control and startup, layout and cabling.

Thus based on this design, called “Baseline Design”, a new development was made, the “Simplified Design”.

2. MAIN FIELDS OF IMPROVEMENTS
Considerations about the amount of information needed to separate and reconstruct muon tracks resulted in a basic simplification in the design [3]. It was proven that the follow up of the muon tracks at the sideways neighbours is not necessary. Those mouns changing the sector boundaries can be reconstructed based on their path before changing. This simplified approach has many consequences:

- The Track Finder Processor does not need to get Extrapolation Results from its sideways neighbours. This decreases the number of interconnections and eliminates one stage where extra synchronisation was necessary.
- The Track Finder Processor still needs Extrapolation Results from its neighbour in the next wheel (same sector). This is, however, result of one single set of Extrapolators, thus, to avoid the extra synchronisation mentioned above, it is simpler to perform the Extrapolation of the Next Wheel Neighbour. This brings some additional electronics, but simplifies the design considerably.
- Due to the suppressed follow up inside the neighbour sectors, the number of possible tracks decreases very much. This allows to use a very simple Track Linking and Selection algorithm that can more easily be implemented in electronic circuits.
- The independent sideways neighbours and the dual Extrapolation of the next wheel neighbours might result in muons which are found twice, by neighbouring Track Finder Processors. To avoid considering them as separate muons they should be cancelled out, a task for the Fake-Pair Cancellation Unit.
- As each Processor performs Extrapolations both in the Next-Wheel Neighbours (with follow up) and the Sideways Neighbours (w/o follow up), it should receive Track Segment Input Data from these Neighbours and also send its Track Segment Data to its Neighbours. To minimise the number of necessary synchronisation steps, every Processor should synchronise the Input Data from its own sector and send them synchronised to its neighbours[4]. Thus the Data from the Neighbours do not need to be synchronised again. This synchronisation and transmission happens in the Sector Receiver Unit of each Processor.
The Baseline Design has foresaw a unified Track Finding approach for both the Barrel Region and the Endcap Region. Later simulations [5] showed, however, that both the detector geometry aspects and the necessary algorithms require a different handling for these areas. Thus a separate Track Finder Processor will be developed for the Endcap CSC detectors and the Barrel DT detectors. The Overlap Region between them requires special attention. This region will be processed by both Processors, and the exact boundary between their field of activity should remain flexible. The Barrel Track Finder Processor will receive the CSC Input Data, reformat them to its own data format and synchronise with the DT Track Segments. After this the CSC Data will be processed in the same way as the DT TS Data, using a special Extrapolation Table.

![Diagram of Processor Blocks](image)

**Fig. 1.**

### 3. PROCESSOR BLOCKS

As seen in Fig 1., the Track Finder Processor consists of five basic units, the Input Receiver, the Extrapolator, the Track Assembler, the Fake-Pair Cancellation and the Parameter Assignment. The Processor uses the Track Segment Data as input of the Extrapolators, the rest of the Track finding process uses only the bitmap data of the successful Extrapolations. Only the Parameter Assignment requires the TS again. As this happens several clock cycles later, the TS Data should be pipelined in a FIFO.

#### 3.1. The Input Receiver

The Input Receiver should contain the Link Receivers that accept the Track Segments from the Trigger Server. After synchronisation they also send these data towards the neighbours, except the Track Segments of the 1st Station: these cannot be a target of an Extrapolation. As a further task the Input Data from the neighbours should be received, but not synchronised, as this already happened at the corresponding neighbour’s Input Receiver.

The Track Segments sent by the Trigger Server are composed of 11 bit Phi value, 10 bit Phi_b (Bending Angle) value and 3 bits of TS Quality [6]. As the final decision concerning the Optical Links between the Trigger Servers and the Track Finder Processors is not yet made, it is not clear how the Link Receivers will look like and how much space they require. According to agreements they will be built on daughterboards, which allows a greater flexibility both concerning the used technology and the later maintenance. The size of these boards is however still undetermined. As a consequence one cannot tell if the Link Receivers can be placed on the Track Finder Processor’s mainboard, or a separate Input Receiver board is necessary.

In the second case the Input Receiver Board will only receive the own sector’s Optical Links and performs their transmission towards the neighbours, but will not receive the neighbours’ data. This should happen on the Track Finder Processor’s mainboard reducing the number of required connections between the Input Receiver and the mainboard.
3.2. The Extrapolator

The Extrapolator Unit performs all Extrapolations that use the Processor’s own Sector as Extrapolation Source and additionally the sideways and next wheel neighbours’ as Extrapolation Target. To follow up Muon Tracks in the Next Wheel it also contains Extrapolators that use the Next Wheel’s Stations #2, #3 and #4 as Source and the same wheels Stations as Target - muons that have the next wheel as Source cannot have the same (previous for the next) wheel as Target.

![Fig. 2.]

As seen in Fig. 2, each Extrapolator contains two Lookup Tables (LUT), one for the Extrapolation Window’s upper limit and one for the lower limit. The Source’s Phi value will be added to both LUT results and the Target Phi position will be compared to these limits. An Extrapolation is considered as successful, if the Target Phi is inside the window.

This means each Source TS needs one set of LUT, but to make the procedure similarly simple for the Extrapolations, where the Target is at the sideways neighbour, there are separate LUTs for these cases. The number of Comparators corresponds to the number of Targets, that is 4 for the same wheel and 2 for the next wheel.

For the own wheel there are 1-2, 1-3, 1-4, 2-3, 2-4 and 4-3 Extrapolations required. Taking into account 2 TS in each Station and 3 directions (own Sector, right neighbour and left neighbour) this means 6x2x3=36 Extrapolators. For the next wheel no Extrapolations are performed from the #1 Station, thus the number of Extrapolators is 3x2x3=18. This makes in total 54 Extrapolators.

According to the simulations it is enough if the Extrapolators use only 8 Phi_b bits and 8 Phi bits, thus the LUTs are 256x8 bit tables. This results in 221’184 LUT bits, taking into account both the low and high limit LUTs. This amount of memory bits does not fit into present FPGAs, but even if the technology development would make this possible, another problem arises. When putting all Extrapolators in one chip, this would possess 480 input and 660 output pins, not counting the Clock and Reset inputs. Therefore a partitioning is necessary.

If the Extrapolator Unit is partitioned into 3 Chips, a possible scheme that results in almost the same size FPGAs can be the following:
- Chip A: 1-2 and 2-4 Extrapolations,
- Chip B: 1-3 and 2-3 Extrapolations,
- Chip C: 1-4 and 4-3 Extrapolations.

This partitioning tries to minimise the pin number too, as some Station’s Phi values are used both as Source and Target. Hardware level simulations were made with this scheme, and proved its feasibility using Altera EPF10K200EGC599-1 FPGAs. The timing simulation showed correct behaviour at full 40MHz clock and 2BX delay time. The design fills up the given Chip’s total Memory Area, leaves, however, 80% of the Logic Area free.

3.3. The Track Linker

The baseline design’s Track Segment Linker and single Track Selection unit used a complicated and hard to maintain procedure to find out the two highest priority muon tracks, and required many steps to perform - thus a doubling of the working frequency was foreseen to keep the requirements. This also meant using high speed ASICs in the final realisation.

The Simplified Design counts with a reduced number of possible Muon Tracks, as those ones that leave the Processor’s Sector aren’t followed up in the neighbouring sectors after they first crossed a neighbour Station. This allows a new approach for the Track Linker. The Linker can set up logic conditions for the existence of all different Tracks. To limit the number of conditions these don’t contain the very last Extrapolations’ Target, they just check their existence. The Linker forms a Priority List about the Tracks fulfilling these conditions and finds out the highest priority ones. The Priority List is composed of the highest priority Tracks towards the lowest ones:

1-2-3-4; 1-2-3; 1-2-4; 1-3-4; 2-3-4;
1-2; 1-3; 1-4; 2-3; 2-4; 3-4

As seen the longer Tracks have priority over the shorter ones, and among the Tracks of same length those originating in lower Stations have priority over ones originating higher. Inside one group the Tracks remaining in the same sector have priority over those leaving the sector.

As the Track Linker has the task to find two Muon Tracks, there is a certain possibility that the second found track will be a sub-track of the first one. To avoid this the Track Linker, after finding the first Muon Track, cancels out from the Priority Table all possible shorter Tracks that are sub tracks of the first one, and then it repeats the search after the highest priority track among the remaining track candidates. This way the block scheme of the Track Finder is the following:
This Track Finder Scheme was also simulated on Hardware level. It fits into an Altera EPF10K100EBC356-1 FPGA. The design was set up to perform the task in a 7 stage pipeline. The max. speed was 30MHz, which is still less than that required by CMS, but the technologic development allows us to expect higher speeds in the near future (Altera 20K series or Xilinx Virtex). If these expectations will not get fulfilled, one has to redesign the circuit with more pipeline stages of less functionality.

The Track Linker delivers the TS addresses of the two highest priority Muon Tracks found to the Fake Pair Cancellation Unit.

3.4. The Fake Pair Cancellation Unit.

As mentioned above, the Simplified Design does not follow up the Muon Tracks at the neighbours. This means also that Track portions that are parts of the same Muon Track might be found twice at neighbours. Theoretically they can be cancelled by the later Sorter stages based on their similar physical parameters, however this can be ineffective, as different parameter assignment methods might result in slightly different results for the same track in neighbouring sectors. The safest way is to cancel these tracks based on their identical TS location. This is easy to do for the next wheel neighbours as their Track Finder Processor is plugged into the same Crate, but more complicated for sideways neighbours; this requires Inter-Crate Connections. Therefore another solution is being considered, that foresees these cancellations in the Global Sorter, but requires forwarding the TS addresses there.

The simple Fake Pair Cancellation compares the TS addresses of the found Muon Tracks and cancels out those that contain lower priority TS combinations. This logic scheme requires a limited number of FPGA gates and can be implemented as part of the Track Linker Chip, adding one BX to the total delay.

3.5. The Parameter Assignment Unit

The last stage of the Track Finder Processor is the Parameter Assignment. The output of the Processor contains max. two found Tracks described with the Muon’s Pt in 5bits, Charge in 1bit, Phi in 8bits, Eta in 2bits and Track Quality in 2 bits.

The Track Quality here is a simple number showing how many valid Extrapolations were participating in the resulting Track. Later simulations should show if it makes sense to modify this number with the quality of the participating input Track Segments.

The Eta value in this stage simply shows where the Muon Track leaves the wheel towards the Next Wheel Neighbour. This value will be forwarded to the Eta Track Finder, that refines this value to 5-6 bits if a Track Matching is possible [7].

The Phi value will be calculated as the position in the #2 Station, as recommended in [8]. This means forwarding the #2 Station TS position for the case if the Muon Track contains #2 Station TS, and an interpolation or extrapolation for the cases if no #2 Station TS is available.

The Charge is a simple function of the Track bending and can be derived from the TS Phi_b values. For determining the Pt value the present high level simulations promise more effective methods than those used in the Baseline Design. The most probable solution will be to perform the Pt calculation always using two methods in parallel and choose the better one’s results. Both methods will use LUTs and as expected need 2BX delay to get results. No hardware simulation was made until now.
4. SYSTEM CONSIDERATIONS

It is planned to build the Muon Track Finder Processors on 9U high 340mm deep boards. They will contain one single VME connector, the other backside connectors will be plugged into a custom design motherboard. The simplified design requires to organise all Processors of the same sector (one Wedge) into one Crate as in this Design there are no more sideways neighbour connections (except Inputs) but there are next wheel neighbour ones. This also means that the Baseline Design’s Wheel Sorter will be replaced by a Wedge Sorter in each Crate.

If the Input Link Receiver size allows all parts of the processor to fit on one single board allowing to incorporate two Wedges (2x6 Processors plus Eta Track Finder and Wedge Sorter) in one Crate. Building 3 Crates into a Rack, 2 Racks are necessary. If the Input Link Receiver requires an own board, one Crate can only contain Processors of one Wedge. In this case we have to count with four Racks.

In order to have a constant environment, water cooled fan units are foreseen below each Crate.

5. HARDWARE DEVELOPMENT

As mentioned above the design of the Simplified version is made in a hardware-close environment. The modules are either described as Altera AHDL descriptions or general VHDL behavioural files.

![Fig. 4](image)

Fig. 4 shows the development path from the AHDL or VHDL description to the programmed chip or chip simulation. The VHDL behavioural description as design base offers a big advantage, as this case allows a direct comparison between the behavioural and the resulting chip simulation. Unfortunately the direct application of the VHDL files as inputs to the Altera MaxPlus® development system was not successful, because this program imposes strong limitations to the VHDL code in order to do a correct synthesis. Third party tools, like Leonardo® promise a better solution here, which is being investigated.

6. SYSTEM SETUP AND CONTROL

For the board level control, check and data spying the best way seems to apply the JTAG Boundary Scan methods. They allow testing the board’s connections, signals and program the FPGAs. To extend the JTAG chains beyond Board level, however, would introduce serious electrical and logistic difficulties. Therefore the JTAG chains are planned to remain board-internal loops controlled by the VME interface.

The system level control should be modular, easily maintainable and allow remote operation. Based on the results of the CMS DAQ groups at the Test Beams [8] we investigate the possibilities of a Java based environment that automatically allows web access to the Track Finder Processor group.


[4.] W.H.Smith, CMS Synchronisation Workshop Conclusions, CMS Note 1999/016


[6.] R. Martinelli, A.J. Ponte Sancho, P. Zotto, Design of the Track Correlator for the DTBX Trigger, CMS Note 1999/007

[7.] M. Kloimwieder, Improving the η-Assignment of the DTBX Based First Level Regional Muon Trigger, CMS Note in progress

[8.] G.Wrochna, Muon Trigger Objects, CMS Draft Note, see: cmsdoc.cern.ch/~wrochna/tmp/trobj.ps
Use of Programmable Logic in a Pipelined Trigger for ATLAS

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Abstract
We present an overview of the Jet and Energy Sum processor for the ATLAS Level-1 Trigger. The design system is based on the use of commercial off-the-shelf components, including large programmable logic devices. The architecture of the system is discussed, including implementation details that reduce latency and board complexity, and take advantage of the inherent flexibility in the design. The results of technology demonstrator programs confirm the feasibility of key elements of the processor design.

1. INTRODUCTION

The programmable logic industry has seen rapid development in recent years. Currently available programmable logic devices offer hundreds of thousands of usable gates, hundreds of user-definable I/O pins, system performance well over 100 MHz, and compatibility with a variety of I/O signal standards. These advances have been accompanied by reductions in price, making in-system programmable logic a serious alternative for applications which have previously favored ASIC solutions.

The advantages of using programmable logic are well understood. Prototyping cycles take hours or days, rather than weeks for ASICs. Belatedly discovered errors can be easily fixed, and system functionality can be modified or enhanced as requirements change. Programmable logic devices are fully tested at the factory, effectively providing 100% device yield. Finally, in-circuit programmability allows “design multiplexing”, where different functions (such as data taking and diagnostics) may be performed in the same logic, reducing the number of gates needed.

The Jet/Energy Sum processor system for the ATLAS First Level Calorimeter Trigger is a multi-crate trigger processor system designed to be built using FPGAs and other commercial off-the-shelf components. FPGAs are used to calculate transverse and missing energy in the calorimeter, identify energy clusters for use in jet calculations, send information for use by the Level-1 and Level-2 triggers, and read out time slice data to DAQ for trigger validation purposes.

In this paper, we present an overview of the proposed system, followed by implementation features which enhance performance, simplify the design, and exploit the flexibility of the system. Finally, we present results from technology demonstrator programs that have been used to validate key features of the system.

2. SYSTEM OVERVIEW

2.1 The ATLAS Level-1 Trigger

The organization of the ATLAS Level-1 trigger is presented in Figure 1. Data from the calorimeters and muon detectors are transmitted to respective trigger processors, which identify and count electron, tau and Jet candidates, calculate total and missing transverse energy, and reconstruct muon trajectories. The processors send results from every bunch crossing to the Central Trigger Processor (CTP) which makes a Level-1 Accept (L1A) decision based on them. If the CTP issues a L1A, the processors read out more detailed information on the types and locations of event features to the Region of Interest (ROI) Builder for use by the Level-2 Trigger.

![Figure 1: Organization of the ATLAS Level-1 Trigger](image-url)
2.2 The Jet/Energy Sum Processor

The Jet/Energy Sum trigger space consists of 960 Jet elements in the range \(-3.2 < \eta < 3.2\), as well as extra energy sums from the forward calorimeters. The system is subdivided into four quadrants in \(\phi\), which are each covered by a separate set of Jet/Energy Sum Modules (JEMs). Jet elements near the border of adjacent quadrants are duplicated in the preprocessor and sent to JEMs in both quadrants to provide the environmental information needed by the Jet algorithm.

Each JEM (Figure 2) receives 9-bit Jet element energy sums in 25 ns intervals via 400 Mb/s serial links (National Semiconductor LVDS). The demultiplexed input data are transmitted at 40 MHz to Energy Sum FPGAs, which sum the electromagnetic and hadronic energies. The \(E_T\), \(E_X\), and \(E_Y\), of each Jet element are calculated, and sums of these are transmitted to adder trees on a separate FPGA, which merges the results and transmits them to the Sum Merger Module.

The input and output data of each module, as well as the types and positions of clusters identified in the Jet algorithm, are stored in pipelines on the Energy and Jet FPGAs, to be read out to the DAQ and ROI Builder upon a L1A decision.

3. DESIGN FEATURES

3.1 The Energy Summation Algorithm

The Energy Sum FPGAs process input data using the algorithm shown in Figure 3. Separate 9-bit electromagnetic and hadronic energies for each Jet element are received at 40 MHz. Noise-reduction thresholds are applied, after which the electromagnetic and hadronic parts of the Jet element are summed. Lookup tables produce values of \(E_T\), \(E_X\), and \(E_Y\) for global summation, and the 10-bit Jet element transverse energy sum is multiplexed to 5 bits at 80 MHz and fanned out to the Jet FPGAs.

The Energy Sum algorithm is foreseen to be implemented on a Xilinx Virtex device [1], with typically four Jet elements processed by each FPGA. An additional Virtex device merges the results of adder trees in the Energy FPGAs to produce \(E_T\), \(E_X\), and \(E_Y\) values for the entire module.

Xilinx Virtex devices were chosen for the Energy Sum algorithm implementation for a number of reasons. Virtex offers large amounts of logic and I/O resources at relatively low cost. Large amounts of distributed and block memory are available for lookup tables and other functions, and DLLs are available for internal and external clock synchronization. Maximum system speeds are far higher than the 40 and 80 MHz necessary for the algorithms, relaxing the implementation.

3.2 The Jet Algorithm

The Jet algorithm is implemented in 64 Jet FPGAs, each of which covers a 2x8 Jet element area in \(\eta x \phi\). The positions of potential Jet cluster candidates are identified by summing the energies of Jet elements in 0.4x0.4 windows sliding in increments of 0.2, and identifying
local maxima. These are referred to as ROI or decluster positions. Jet clusters are identified by comparing transverse energy sums within windows of size 0.4, 0.6, or 0.8 that exceed predefined thresholds and are associated with an ROI position. All three Jet window sizes are calculated in parallel, and 8 combinations of energy threshold and window size are available for trigger menus. The Jet cluster sizes (dark areas) and their associated ROI positions (bold outlines) are shown in Figure 4. For Jet clusters of size 0.6, the ROI position can be in one of four positions in the cluster.

The baseline device for the Jet FPGA implementation is the Altera FLEX 10k250 [2]. The 10K series of FPGAs has a global routing architecture which is well suited for large designs with high clock rates and the large degree of data fanout and routing inherent in the Jet algorithm. It is planned to investigate alternative devices, including Xilinx Virtex and Altera Apex, before producing the final system.

3.3 Backplane Signal Transmission

The Jet/Energy Sum system has a full-custom 9U backplane. The baseline choice of card-edge and backplane connectors are 5+2 row, 2mm HM connectors which are an industry standard and commonly used in CompactPCI. The crate and front panel hardware are planned to be based on the IEEE 1101.10 standard.

All Jet element data are transmitted from the Energy Sum FPGAs to the Jet FPGAs via point-to-point links using low-voltage CMOS levels. This includes signals between FPGAs on the same board as well as data sharing between neighboring JEMs via short backplane links. Because the CMOS levels are compatible with the Jet FPGA inputs, no signal translators are necessary on the receiving end of the links. It is also considered to be possible to drive all 80 MHz signals directly from the Energy Sum FPGA output pins. This strategy promotes signal uniformity within the system, and simplifies the design of the JEM by eliminating large numbers of driver and receiver devices.

Transmission of JEM results to the Jet and Sum Merger Modules is also performed via point-to-point links. Studies of appropriate signal levels and termination schemes are currently in progress.

3.3 Making Use of Reprogrammability

It is planned to take advantage of the in-system reprogrammability of the FPGAs in the system. Configuration details-such as energy thresholds and lookup table contents-will be controlled by writing to registers implemented in the FPGA designs. However, more significant changes in functionality-such as modifications to the Jet algorithm-may be easier to make by downloading a different FPGA design altogether. It is conceivable that several FPGA configurations may be selected for different luminosity or noise conditions, for example.

The most important use of FPGA reprogrammability may be the ability to use special diagnostic configurations to perform fast and complete testing of all signal paths in the system. Such configurations could be routinely loaded and run during pauses in data taking, for example, during beam fills. They could also be used to quickly pinpoint the source of errors discovered by trigger monitoring and validation programs.
4. DEMONSTRATOR PROGRAMS

Technology demonstrator systems have been built and tested to confirm the feasibility of key elements of the design.

4.1 “Module –2” Technology Demonstrator

The JEM Module -2 was designed to study issues raised during the review of the Level-1 Technical Design Report [3]. These issues included the reliability of 80 MHz data transmission between FPGAs and across backplane links, the performance of algorithms at running at 40 and 80 MHz, and the reliability of high-speed serial links using different cable and connector options.

Each Module –2 board includes a Xilinx 4013XL and an Altera 10K50V FPGA with point-to-point links between them, and to a 2mm-pitch HM backplane connector which allows two such modules to be connected by a small 2-slot backplane. Another set of direct and backplane connections between the FPGAs pass through an ALVC buffer chip clocked at 80 MHz. Each of the four data paths is 10 bits wide. The timing of each FPGA and the ALVC buffer are independently controlled using adjustable delays.

Each board also includes a pair of HP Glink transmitter and receiver devices for link stability tests. A VME interface implemented on a separate Altera 10K30 FPGA is used for control and monitoring. A 40 MHz clock is provided by an external source.

Data transmission tests using the Module –2 system showed error-free CMOS data transmission over all paths, both with and without the use of intermediate ALVC drivers. Upper limits on bit-error rates were set at ~10^{-14}. The timing margin for 80 MHz data was measured to be 9.6 ns with buffers, and 7.3 ns with direct transmission between FPGAs. Sample “5-bit serial” calculations were tested at 80 MHz and found to work as expected.

Early experience with the use of serial links was gained, both with HP Glinks, and later with LVDS links that were added to the board using a small adaptor PCB. The results of these tests have been superseded by experiences with the Mainz Link Test Board.

4.2 Mainz Link Test Board

The Mainz Link Test Board was designed to gain experience with National Instruments LVDS serial links, and to identify and solve previously observed problems with link stability over long cables and differential PCB tracks.

The Link Test Board is a 3U card that fits in a J1 VME backplane slot. The board contains 8 LVDS receiver chips, which are read out by two Xilinx Virtex XCV100 devices. A VME interface is implemented on a Xilinx CPLD. Modified JEM Module –2 boards were used as data sources for tests.

Tests showed that an active pre-compensation circuit at the LVDS data source improves link stability and allows the cable range to be extended. Stable transmission of four links over 15m of category 5 twisted-pair cable plus 55 cm of differential PCB tracks was achieved using a pre-compensation circuit based on the Motorola MC10EL89 differential fanout gate [4]. Commercial off-the-shelf pre-compensation solutions for the final system are currently being investigated.

5. OUTLOOK

The Module –2 and Link Test Board programs have shown that the key design features of the Jet/Energy Sum processor are sound. Plans are currently underway for the first of two prototype systems planned before production.

The Jet/Energy Sum “System –1” will be a fully functional prototype system with reduced channel count. It is planned to be a single crate 6U system with JEMs, merger modules, and timing and VME modules connected via a custom backplane. It is hoped to have the system fully operational by summer 2000.

“System 0” will be a single crate, full size prototype system. It should be nearly identical to the production hardware, with only minor changes necessary. Construction and testing of System 0 should be completed by the end of 2001.

In addition to the planned prototype systems, additional technology demonstrators may also be produced to evaluate and gain experiences with new devices which appear on the market.

6. CONCLUSIONS

An overview of the Jet and Energy Sum processor for the ATLAS Level-1 Trigger has been presented. The design system is based on the use of commercial off-the-shelf components, including large programmable logic devices. The design includes implementation details that reduce latency and board complexity, and use FPGA reprogrammability to enhance system flexibility and diagnostic capability. Technology demonstrator programs have confirmed the feasibility of key elements of the processor design, and two fully functional prototype systems are planned before the start of final production.

7. REFERENCES

THE TRACK-FINDING PROCESSOR FOR THE LEVEL-1 TRIGGER OF THE CMS ENDCAP MUON SYSTEM

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Abstract

We present the design of a fast three-dimensional track-finding processor for the Level-1 trigger of the CMS Endcap Muon System. Each track is assembled from track segments identified in the Endcap Muon chambers. The processor measures the transverse momentum of the best muon candidates from the sagitta induced by the magnetic bending. The trigger algorithms are programmable since the processor is based on FPGA and RAM logic, allowing the experiment to adapt to different background conditions and colliding rates.

1. INTRODUCTION

The endcap muon system of CMS consists of four stations of cathode strip chambers (CSCs) on each end of the experiment. The coverage in pseudo-rapidity ($\eta$) is from 0.9 to 2.4. A single station of the muon system is composed of six layers of CSC chambers, where a single layer has cathode strips aligned radially (from the beam axis) and anode wires aligned in the orthogonal direction. The CSC chambers are trapezoidal in shape with a $10^\circ$ or $20^\circ$ angular extent in azimuth ($\phi$). The CSC chambers are fast (60 ns drift-time) and participate in the Level-1 trigger of CMS.

A “Local Charged Track” (LCT) forms the most primitive trigger object of the endcap muon system [1]. Both cathode and anode front-end LCT trigger cards search for valid patterns from the six wire and strip planes of the CSC chamber. The anode data provide precise timing information as well as $\eta$ information, and the cathode data provide precise $\phi$ information. A motherboard on the chamber collects the LCT information, associates the wire data to the cathode data, tags the bunch crossing time, and selects the two best candidates from each chamber. The end result is a three-dimensional vector, encoded as a bit pattern, which corresponds to a track segment in that muon station. It is transmitted via optical links to the counting house of CMS. To reduce the number of optical connections, only the three best track segments are sent from each chamber (18 track segments).

The Track-Finder must reconstruct muons from track segments received from the endcap muon system, measure their momenta using the fringe field of the central 4 T solenoid, and report the results to the first level of the trigger system (Level-1). This objective is complicated by the non-uniform magnetic field in the CMS endcap and by the high background rates; consequently, the design must incorporate full 3-dimensional information into the track-finding and measurement procedures.

The experimental goal of the Track-Finder is to efficiently identify muons with as low a threshold in transverse momentum ($p_T$) as possible in order to meet the rate requirement of the Level-1 Trigger of CMS. This translates into a single muon trigger rate which does not exceed about 1 kHz per unit rapidity at the full luminosity of the LHC. The resolution on $p_T$, therefore, should be less than about 30% at least, which requires measurements of the $\phi$ and $\eta$ coordinates of the track from at least three stations.

A version of the muon Track-Finder designed for the barrel muon system of CMS is under design [2]. Since it is intrinsically two-dimensional, it does not satisfy the requirements of the endcap system. Moreover, the large number of signals shared between trigger regions (because of the staggering of the barrel chambers) is not appropriate for the endcap. Therefore, we have rethought the entire Track-Finder architecture given that we are compelled to design a new trigger processor.

2. SYSTEM ARCHITECTURE

The Track-Finder is foreseen be implemented as 12 “Sector Processors” that identify up to the three best muons in $60^\circ$ azimuthal sectors. Each Processor is a 9U VME card housed in a crate in the counting house of CMS. Three receiver cards collect the optical signals from the CSC chambers of that sector and transmit data to the Sector Processor via a custom point-to-point backplane. A maximum of six track segments are sent from the first muon station in that sector, and three each from the remaining three stations. In addition, up to eight track segments from chambers at the ends of the barrel muon system are propagated to a transition board in the back of the crate and delivered to each Sector Processor as well.

A total of nearly 600 bits of information are delivered to each Sector Processor at the beam crossing
frequency of 40 MHz (3 GB/s). To reduce the number of connections, LVDS Channel Link transmitters/receivers from National Semiconductor [3] are used to compress the data by about a factor of three through serialization/de-serialization. A custom point-to-point backplane operating at 280 MHz is under design.

Each Sector Processor measures the track parameters ($P_x$, $\phi$, $\eta$, sign, and quality) of up to the three best muons and transmits 60 bits through a connector on the front panel. A sorting processor accepts the 36 muon candidates from the 12 Sector Processors and selects the best 4 for transmission to the Global Level-1 Trigger.

A prototype Sector Processor is currently under development, and a preliminary sketch of the functional layout on a 9U VME board is shown in Fig. 1.

3. TRACK-FINDER LOGIC

The reconstruction of complete tracks from individual track segments is partitioned into several steps to minimize the logic and memory size of the Track-Finder. The steps are pipelined and the trigger logic is deadtime-less.

First, nearly all possible pairwise combinations of track segments are tested for consistency with a single track. That is, each track segment is extrapolated to another station and compared to other track segments in that station. Successful extrapolations yield tracks composed of two segments, which is the minimum necessary to form a trigger. The process is not complete, however, since the Track-Finder must report the number of distinct muons to the Level-1 trigger. A muon that traverses all four muon stations and registers four track segments would yield six track “doublets.” Thus, the next step is to assemble complete tracks from the extrapolation results and cancel redundant shorter tracks. Finally, the best three muons are selected, and the track parameters are measured.

3.1 Data Input

The input data to the Sector Processor is de-serialized by Channel Link receivers and synchronized with the local 40 MHz clock before being sent into the Extrapolation Units. The Sector Processor is designed to have some ability to analyze track segments received on different clocks (different bunch crossings) because of the intrinsic timing spread of the trigger primitive formation.

To incorporate a multi-bunch mode, we take advantage of the sparseness of the data. Track segments from other bunch crossings are considered only if there are empty track segments in the current crossing; otherwise, the size of the extrapolation logic would grow enormously. We assume that track segments may be late (but not early), and that the earliest track segment defines the beam crossing of the muon. The simplest case is a window that is open for two bunch crossings, which should be sufficient for the CSC trigger system. Although the window is left open for more than bunch crossing, the Sector Processor must report triggers at the correct bunch crossing every crossing. In other words, overlapping time buckets are used. A flag is set to record which bunch crossing the track segment came from relative to the current crossing. This flag is used in the final track selection to inhibit double triggers.

3.2 Extrapolation

A single Extrapolation Unit forms the core of the Track-Finder trigger logic. It takes the three-dimensional spatial information from two track segments in different stations, and tests if those two segments are compatible with a muon originating from the nominal collision vertex with a curvature consistent with the magnetic bending in that region. The test involves the following:

- Determine if each track segment is in the allowed trigger region in $\eta$
- Compare the $\eta$ values of the two segments to determine if both lie along a straight line projection to the collision vertex
- Compute the difference in $\phi$ between the two track segments
- Check if that difference is consistent with the bending direction in $\phi$ measured at each station
- Compare the difference in $\phi$ to the maximum allowed at that $\eta$ for several $P_t$ thresholds
- Compare the quality of the two track segments
- Check that at least one of the track segments is not parallel to the beam axis
- Assign an overall quality to the extrapolation

Each test is accomplished by small look-up tables or arithmetic logic, as illustrated in Fig. 2. The resulting quality word is either 1 or 2 bits, depending on the stations involved. Its definition is programmable, but we use it to assign a coarse $P_t$ (low, medium, and high) to extrapolations involving the first muon station. Otherwise, the quality just represents whether the extrapolation was successful or not. This quality information is useful when track candidates must be ranked.

All possible extrapolation pairs should be tested in parallel to minimize the trigger latency. This corresponds to 81 combinations for the 15 track segments of the endcap region. However, we have excluded direct extrapolations from the first to fourth muon station in order to reduce the number of combinations to 63. This prohibits triggers involving hits in only those stations, but saves logic and reduces some random coincidences (since those chambers are expected to have the highest rates). It also facilitates track assembly based on “key stations,” which is explained in the next section.
The extrapolation logic should be programmable, and is presently implemented in the Xilinx Virtex series [4] field-programmable gate-arrays (FPGAs). The latency to accomplish this decision logic is expected to take 3 clocks.

3.3 Track Assembly

The track assembly stage of the Track-Finder logic examines the results of the extrapolations and determines if any track segment pairs belong to the same muon. If so, those segments are combined and a code is assigned to denote which muon stations are involved. The underlying feature of the track-assembly is the concept of a “key station.” For this design, the second and third muon stations are key stations. A valid trigger in the endcap region must have a hit in one of those two stations. The second station is actually used twice: once for the endcap region and once for the region of overlap with the barrel muon system, so there are a total of three data streams.

Each track segment of a key station, of which there are three for one 60° sector, is tested for extrapolations to the other stations. There are six track segments allowed from the first CSC muon station, and the extrapolation quality is 2 bits. There are three track segments allowed in each of the other non-key stations, and the extrapolation quality to those stations is 1 bit. Thus, 18 bits are interrogated. (The same is true for extrapolations to the barrel muon system.) Since the number of input bits is small, each of these “Link” units is implemented as a static RAM look-up memory as shown in Fig. 3. The latency, therefore, is just one clock. The output code is a 6-bit quality word giving the type and rank of the best assembled track, and a 9-bit word labelling the track segments used in each station. A memory of the same size is used for extrapolations to the barrel muon system as well.

3.4 Final Selection

The final selection logic combines the nine best assembled tracks, cancels redundant tracks, and selects the three best distinct tracks. For example, a muon which leaves track segments in all four endcap stations will be identified in both track assembler streams of the endcap since it has a track segment in each key station. The Final Selection Unit must interrogate the track segment labels from each combination of tracks from the two streams to determine whether one or more track segments are in common. If the number of common segments exceeds a preset threshold, the two tracks are considered identical and one is cancelled. Thus, the Final Section Unit is a sorter with cancellation logic.

A VHDL description of the Final Selection Unit has been synthesized using the Exemplar Logic engine of OrCAD Express [5]. The sorter part of the logic compares the qualities of all pairwise combinations of tracks from the Track Assembler data streams. The cancellation part of the logic does the same for the hit labels. Not all track segments need to be identical for two tracks to be considered identical. Bremsstrahlung, for example, might cause a single muon to deliver two track segments in one station, and this would lead to a fake di-muon trigger which should be suppressed. The actual criterion employed is programmable. The two comparison steps are done in parallel in one 25 ns clock. The next step of the logic examines the results of all these comparisons, cancels redundant tracks, and reports the identities of the three best and distinct muons. These two steps take two clocks. Finally, the track segment information of the selected muons is taken from a multiplexer and transmitted to the Assignment Units of the measurement system. Additional logic connected to the multiplexer determines if all track segments of a given muon come from a later bunch crossing, in which case the muon is suppressed to inhibit double triggers.

3.5 Measurement

The final stage of processing in the Track-Finder is the measurement of the track parameters, which includes the \( \phi \) and \( \eta \) coordinates of the muon, the magnitude of the transverse momentum \( P_T \), the sign of the muon, and an overall quality which we interpret as the uncertainty of the momentum measurement. The most important quantity to calculate accurately is the muon \( P_T \), as this quantity has a direct impact on the trigger rate and on the efficiency. Simulations have shown that the accuracy of the momentum measurement in the endcap using the displacement in \( \phi \) measured between two stations is about 30% at low momenta, when the first station is included. (It is worse than 70% without the first station.) We would like to improve this so as to have better control on the overall muon trigger rate, and the most promising technique is to use the \( \phi \) information from three stations when it is available. This should improve the resolution to at least 20% at low momenta, which is sufficient. We take advantage of the large multiple scattering for low \( P_T \) muons. Although there is a small probability that a scattering will offset the large magnetic bending between the first two stations (and thus appear as a high momentum muon), it is much less likely to offset the bending between all three stations.

In order to achieve a 3-station \( P_T \) measurement, one must be careful not to include too much data; otherwise, the size of the look-up memories will be prohibitive. We have developed a scheme that uses the minimum number of bits necessary in the calculation. The first step is to do some pre-processing in FPGA logic: the difference in \( \phi \) is calculated between the first two track segments of the muon, and between the second and third track segments when they exist. Only the essential bits are kept from the subtraction. For example, we do not need the same accuracy on the second subtraction because we are only
trying to untangle the multiple scattering effect at low momenta. The subtraction results are combined with the \( \eta \) coordinate of the track and the track type, and then sent into a 2 MB memory for assignment of the signed \( P_T \). Tracks composed of only two track segments are allowed also in certain cases. This scheme is illustrated in Fig. 4.

4. SUMMARY

The conceptual design of a Track-Finder for the Level-1 trigger of the CMS endcap muon system is complete. The design is implemented as 12 identical processors which cover the pseudo-rapidity interval \( 0.9 < \eta < 2.4 \). The track-finding algorithms are three-dimensional, which improves the background suppression. The \( P_T \) measurement uses data from 3 endcap stations, when available, to improve the resolution to 20%. The input to the Track-Finder can be held for more than one bunch crossing to accommodate timing errors, and the full latency is expected to be 14 bunch crossings. The design is implemented using Xilinx Virtex FPGAs and SRAM look-up tables and is fully programmable. The board layout and backplane design has begun.

REFERENCES


Figure 1: Functional layout of the Sector Processor on a 9U VME board showing the major components of the Track-Finder logic.
Figure 2: Logic diagram of a single extrapolation.

Figure 3: The Track Assembler Unit implemented as 9 static RAM memories.

Figure 4: The assignment of P_t using FPGA preprocessing followed by an SRAM look-up table.
Abstract

In an effort to reduce data transfer and rate requirements, the Higher Level Trigger of the ATLAS Detector uses Region of Interest (ROI) information forwarded from Level 1 Partitions on a Level 1 Accept. The ROI Builder receives these ROI fragments, which may be considerably skewed in time and may be interspersed with fragments from other events, organizes and formats from these fragments a record for each event accepted by Level 1, selects a processor to manage the event, and transfers via S-link the assembled ROI record to the target processor. The ROI Builder must fulfill these requirements at the Level 1 Trigger rate of 100 kHz while accommodating S-link flow control. A design for the ROI Builder was developed emphasizing parallelism, implemented in FPGA's, and has been run in testbeds at Saclay and CERN.

1. OVERVIEW

The Level 2 Trigger of ATLAS is envisioned as a multiplicity of processors connected by a high-speed switching network. Suitable candidates for this network might be giga-ethernet or ATM. Also connected to this network are the Readout Buffers (ROB's) which receive the global event data from the Front End Electronics, and the Supervisor which manages the operation of the Level 2 Trigger. To minimize data transfers on the network, the Level 2 Trigger uses Region of Interest (ROI) information from Level 1. This information is transferred to Level 2 on a Level 1 Accept in the form of ROI Fractions. Only data relevant to ROI's is used in the Level 2 trigger algorithms.

ROI information is transferred from a multiplicity (currently 7) of Level 1 processors to the Level 2 Trigger Supervisor as ROI Fractions. The ROI Fractions are received within the Supervisor by the ROI Builder. The ROI Builder must build an ROI Record by assembling the ROI Fractions corresponding to each event, allocate the event to an ROI Processor within the Supervisor, and transfer the ROI Record to the target ROI Processor. The selected ROI Processor manages the event through Level 2. It allocates the event to a processor on the Switching Network, forwards the ROI Record to this target processor, and waits for a Level 2 Accept or Reject.

2. OBJECTIVES OF THIS WORK

This prototype development is intended to demonstrate the feasibility of a suggested architecture capable of building ROI Records at the canonical Level 1 Trigger rate of 100 kHz without introducing dead time. Another objective of this work is to provide hardware support to the Pilot Project within the ATLAS Level 2 Trigger Group. The Pilot Project is a continuation of the Demonstrator Program of last year, and is an on-going hardware/software effort to emulate subsets or slices of the ATLAS Level 2 Trigger elements. Additionally, we hope later this year to be able to integrate the ROI Builder with Level 1 Trigger elements at RAL and DAQ-1 prototype hardware at CERN.

3. DESIGN PHILOSOPHY

This prototype must receive a multiplicity of ROI Fractions per event via S-Link from Level 1 Processors, must provide assembled ROI Records vis S-Link for as many as 8 ROI Processors, and must operate without introducing dead time at rates as high as 100 kHz. In order to meet these requirements, we have implemented the ROI Builder entirely in hardware, and have emphasized parallelism in the design. Our selection of hardware has been the Altera 10K family of FPGA's. As implemented to serve 8 ROI processors, the ROI Builder uses 76 10K40's and 8 10K50's. This extremely dense logic allows us to use an architecture where essentially we have 8 ROI Builders operating in parallel, connected only by the event selection algorithm (Round Robin in this implementation). The event selection algorithm, implemented in hardware, uses the Level 1 Event ID which is embedded in every ROI Fraction as its input.

The ROI Builder is tolerant of ROI Fractions which are skewed in time by as much as 100 μsec, are asynchronous to each other, and need not be in order. The ROI Record is built in 2 μsec after receipt of the last fragment of an event, and is immediately transferred vis S-Link to the target ROI Processor. As implemented, each ROI Builder card can build ROI Records from as many as 12 input data streams, and can service 2 ROI Processors. The ROI Builder is completely data driven and scalable. Accordingly, a Prototype ROI Builder using 4 ROI Processors uses 2 ROI Builder Cards, and a Prototype ROI Builder using 8 ROI Processors requires 4 ROI Builder Cards. Figure 1 shows the structure of the Supervisor in block form.

To improve rate capability and avoid bottlenecks, the logic is parallelized as much as possible. Each input ROI
Fraction is received simultaneously by the input buffer of each channel of ROI Builder logic, and the Level 1 Event ID is checked. The channel for which this number is relevant passes the Fraction to a second buffer where the record is built. All channels for which the Level 1 Event ID is not relevant immediately clear their input buffer and are ready for another Fraction. For this prototype, events are allocated on a round robin basis, however for later versions of this hardware, much more sophisticated algorithms are possible. Figure 2 shows one of the prototype ROI Builder Cards. There are 12 inputs for data streams from Level 1 carried via copper in S-Link format, six input FPGA’s which are configured as 12 input buffers, 12 FPGA’s which provide the two secondary buffers in which the records are built, and two FPGA’s on pin grid arrays which manage transfer of the assembled records to the two target ROI Processors served by this card.

4. ROI BUILDER TESTS

To facilitate diagnostic testing of the ROI Builder and for use as a Level 1 emulator in the test beds, an input card was designed and built. This input card emulates six Level 1 processors, and furnishes to the ROI Builder the ROI Fractions which would be transferred on Level 1 Accepts. This input card can be loaded from VME with ROI Fractions for 1024 events, and these events can then be initiated at one of 12 software selectable rates, or under VME control. This input card implements flow control precisely as S-Links from Level 1 Processors would. The input card is shown in Fig. 3.

Fig. 1. Organization of the Supervisor

Fig. 2. Prototype ROI Builder Card

Diagnostic codes were written in C++ which were capable of exercising all the functions of the ROI Builder. This self-contained program running under LynxOS on the CES RIO2 provided a menu-driven interface and had functions to:

- Set data clock (4 settings, 33-264 ns period).
- Set event clock (12 settings, 4-100kHz).
- Load and check event memory (1024 events).
- Set running mode, continuous at preselected rate or VME selected.

Fig. 3. Input Card
• Read out one S-Link port in either DMA or single word mode.
• Compare received with expected data and log errors.
• Measure actual event rate.

After testing the hardware, the system was set up and a series of tests was run. The test system components comprised:

• One input card emulating 6 Level 1 partitions
• Two ROI Builder cards
• Two S-Link output cards (4 S-Link output channels)
• Four i686 PC’s running under Linux or 4 RIO2’s running under LynxOS

The purpose of this testing was to make sure the system ran without errors, and to investigate the Level 1 trigger rates that could be supported without having the Supervisor create deadtime. In these measurements, 1, 2, and 4 nodes were used. The input was run freely at the 12 pre-selected rates with S-Link flow control implemented. The event rate was measured both for S-Link transfer only, and for S-Link transfer and data unpacking where the system output was checked for errors. Figure 4 shows the experimental setup, and Figure 5 shows typical data from this testing.

5. INTEGRATION AT SACLAY

In March 1999 the Supervisor/ROI Builder was integrated into a 32 node ATM network at Saclay and a series of tests was run. The goals of this work were to operate the ROI Builder in a 32 node network using 1, 2, or 4 Supervisor nodes, to find the limits of Supervisor performance using existing processors (200, 300 MHz RIO2’s), and to investigate the effect that S-Link flow control may have on the performance. Figure 6 is a conceptual view of the setup. Extensive testing was conducted, and a brief summary of results is presented in Figure 7.

![Fig. 4. Experimental Setup](image)

![Fig. 5. 1, 2, or 4 i686 Nodes, Data Unpacking](image)

![Fig. 6. ROI Builder – ATM Integration](image)

![Fig. 7. ROI Builder – ATM Integration](image)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Maximum rate (kHz)</th>
<th>usec/event</th>
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<td>15</td>
</tr>
<tr>
<td>1 Supervisor Emulator</td>
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<td>26</td>
</tr>
<tr>
<td>1 Supervisor - Rol Builder</td>
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<td>34</td>
</tr>
<tr>
<td>2 Supervisor - Rol Builder</td>
<td>27 + 28 = 55</td>
<td>18</td>
</tr>
<tr>
<td>4 Supervisor - Rol Builder</td>
<td>23 + 23 + 24 + 24 = 94</td>
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6. CONCLUSIONS

A prototype ROI Builder for ATLAS Level 2 Trigger has been built using FPGA’s in a highly parallel architecture, has been integrated in a 32 node ATM network at Saclay, and has been found to satisfy the requirements for the Level 2 Trigger of ATLAS. This prototype hardware has now been moved to an Ethernet test bed at CERN, and we hope soon to have results of ROI Builder performance from this setup.
The most difficult problems encountered in this work related to maintaining data integrity in the presence of flow control constantly turning on and off. Flow control tends to be raised in the S-Link connections from the ROI Builder to the ROI Processors, because the ROI records are typically longer than 128 words. If the ROI Processor does not promptly service the PCI port, then flow control will ripple back through the ROI Builder into the input S-Links. There is a considerable amount of buffering, however, the input S-Links eventually will be blocked.
Abstract
Some of the hardware components designed for the CERN - RD12 optical Timing, Trigger and Control system project [1] are presented, as well as some future developments.

INTRODUCTION
The Large Hadron Collider (LHC) experiments (ALICE, ATLAS, CMS and LHC-B) all require a means of distributing timing, trigger and control information to the different sub-detector Front End (FE) and Read Out systems. This information comes normally from the LHC machine, the Level-1 (LVL1) Central Trigger Processor (CTP), the Data Acquisition system and the Detector Control System.

A multipurpose Fibre Optic (FO) based distribution system, the TTC, has been developed for this purpose within the framework of the CERN - RD12 project. Accepted triggers, trigger information, event count, various calibration, control, reset and test commands can be sent over the TTC network.

THE TTC SYSTEM
System Description
The TTC system is a unidirectional optical fibre based transmission system, where two information channels, A and B, are Time Division Multiplexed (TDM) and Bi-Phase Mark (BPM) encoded using the LHC Bunch Crossing (BC) clock (40.08 MHz) as the carrier frequency. One channel (A) carries exclusively the LVL1 trigger accept (L1A) information and the other (B) carries packaged address and data information for the sending of various reset commands or calibration, control and test parameters.

The LHC BC clock is used as the TTC system master clock and is distributed to all destination systems by the receivers extracting it from the BPM encoded signal.

The data packages sent on the B-channel can either be of short format (8 data bits), used for broadcast commands or of long format (14 address, 8 sub-address and 8 data bits) for individually addressed commands or data transfers. Error correction coding is implemented by adding standard Hamming code, 5 respectively 7 bits, to the two data formats. Commands may either be transmitted asynchronously or in a fixed timing relation to the LHC BC Clock and Orbit signals.

Figure 1. The TTC system block diagram
A final system integrated in the experiment will comprise the following hardware components:

- The LHC Clock and Orbit signals receiver/fan-out crate, TTCmi
- The VMEbus interface module, TTCvi
- The modulator (TDM + BPM) and optical fibre laser transmitter unit
- The tree structured optical fibre distribution network
- The photo detector diode and the TTC receiver ASIC\(^1\), TTCrx
- The FE or Read-Out system specific modules carrying the TTCrx

New developments for TTC
A number of test and evaluation TTC systems are at the present being used at CERN and at collaborating institutes around the globe. In order to get compact and inexpensive TTC systems for such purposes, a low power optical fibre transmitter, with an integrated TDM/BMP

\(^1 \) Application Specific Integrated Circuit
encoder, has been designed into a VME sized module (TTCvx).

A simple receiver prototype module (TTCsr), in PCI Mezzanine Card (PMC) standard, carrying the TTCrx ASIC has been developed at CERN. Specifications of a second improved version of this TTCsr module are being prepared.

**VMEbus INTERFACE - TTCvi**

*Module Description*

Main functions of the TTCvi [2] are to select a trigger source from either the L1A input, test trigger inputs, an internal rate programmable random trigger generator or triggers generated by a specific VME access. The selected trigger source is made available on the communication channel A output and an internal event counter is incremented for each outgoing trigger.

Formatted address/data/command packages are sent on the communication channel B. This is achieved by a VME master writing data to the TTCvi, where it gets buffered in four FIFO's before being requested, then formatted, serialised and sent to the B-channel output. The preloaded data words in the FIFO's may be requested for sending in number of modes. Each of the four FIFO buffers is associated with a front panel input, B-Go[0..3], which can be used to trigger requests for sending packages, either asynchronously or in a programmable timing relation to the LHC Orbit signal. The B-Go signals may also be generated internally by specific VME accesses. Possibility exists to select a sending request mode where only the presence of data in the FIFO is checked in order to initiate B-channel transfers. Yet another mode permits the re-transmission of the content in the FIFO.

Four pulse generators, with programmable delay and duration timings and each associated with a FIFO buffer, are triggered by the LHC Orbit signal (11.245 kHz / 88.924 µs) to produce the signals INHIBIT[0..3]. The INHIBIT signals schedules, when running in a synchronous mode, the B-channel transfers from the FIFO buffers in a way that the commands arrive to the destination systems in a precise timing relation to the LHC bunch structure.

Un-buffered asynchronous long or short transfers on the B-channel may, as an alternative, be achieved by writing data to specific VME registers.

The content of the internal event counter, together with the trigger type code generated by the CTP are buffered and then transferred on the B-channel for each on the A-channel outgoing trigger.

An arbitration scheme is implemented in order to grant the different B-channel transfer request types on a priority basis, where the B-Go[0] ones has the highest and the VME register ones the lowest.

BC clock and Orbit signals may either come from an external source (TTCmi) or be generated internally for stand alone test purposes.

The TTCvi is a 6U/4TE size VME slave module with A24/D16 + D32 capabilities.

**Status**

Two batches of 20 TTCvi modules each have so far been fabricated of which 30 modules have been delivered to the users. Before launching fabrication of a subsequent batch a questionary will be addressed to all TTCvi users in order to collect some opinions. The milestones for the ATLAS requirements are a preliminary design report in December 1999, the final one in September 2000 and final version of TTCvi in June 2001.

**TTCvi Test Module**

A test bench has been set up for the testing of TTCvi modules before delivered to the users. For this purpose has a TTCvi Test Module been designed, which generates the necessary input signals to the TTCvi and de-serialises, strips and buffers packages generated on the B-channel. A menu driven test software has been written to check, among other features, data and Hamming code correctness.

**ENCODER AND FIBRE OPTIC TRANSMITTER - TTCvx**

*Module Description*

The TTCvx [3] module function is to multiplex and encode the A and B communication channels generated by the TTCvi and to transmit the resulting modulated signal to the destination TTCrx's via fibre optic cables. Time Division Multiplexing (TDM) is used where the A and B channels are sampled alternatively every half period of the basic clock. The encoding is achieved by using a Bi-Phase Mark (BPM) scheme.
The TTCvx has an internal clock, as well as an input for an external one. The switching between the two clock sources is automatic by the means of an external clock detection circuit. A PLL frequency synthesizer circuit handles the necessary clock multiplication for the encoding. The basic clock frequency from the PLL is available on the module front panel in both LVDS\(^4\) and ECL\(^5\) levels and is used for synchronization with the TTCvi. Up to four light emitting devices can be fitted to drive fibre optic cables. The encoded signal is also available on the front panel in both ECL and LVDS levels.

The TTCvx is a 6U/4TE size VME module without any signal connection to the VMEbus, only the +5V and -12V power rails are used. The design has been implemented using PECL\(^6\) technology.

The fibre optic transmitter works at a wavelength of 1330 nm and has an average output power of min. -19 dBm, which is sufficient for test set-ups, as fibre optic receivers normally have in input sensitivity of approximately -32 dBm. For example has a 100 m long fibre optic cable of 50/125 µm type a typical damping of -2 dB.

**Status**

25 TTCvx modules have so far been fabricated, whereof most have already been delivered to the users. A second batch will be put into fabrication as soon as some feedback has been collected.

**RECEIVER ASIC - TTCrx**

**Brief description**

The TTCrx [4] with associated photo detector diode and pre-amplifier receive and decode the signal on the optical fibre. Received packages are recognised as being either broadcast commands or individually addressed internal or external sub-address/data words. Each TTCrx has a unique 14-bit identification (ID) number serving as its system address. The ID is stored locally and read by the TTCrx on initialisation. The contents of the TTCrx internal bunch crossing and event counters, the LVL1 trigger decision and the received sub-address/data information are made available to external systems on the outgoing busses. The LHC clock is recovered from the incoming BPM encoded signal and is presented on output pins for system synchronisation. Internal programmable de-skewing circuits allow proper timing of the extracted clock, broadcast commands and the trigger decision. The TTCrx ASIC chip is available in a 100-pin BGA\(^7\) package.

**Availability**

The fabrication of a revised radiation hardened version has just been submitted and samples should be available towards the end of 1999. A limited number of the present version of the TTCrx is still available.

**SIMPLE RECEIVER INTERFACE - TTCsr**

The TTCsr [5] is implemented as a PMC module carrying the fibre optic receiver, preamplifier, the TTCrx, data buffers and the interface logic. The information on the different TTCrx busses is buffered in FIFO’s before presented to the PCI bus interface. Some of the clock,
strode and reset signals from the TTCrx are passed onto front panel connectors via level converters.

New specifications
A couple of TTCsr prototypes of the present version have so far been assembled and tested. The ATLAS data acquisition team foresees the integration of such a module into their system and is presently collaborating in writing the specifications of an enhanced performance version of the TTCsr.

TTC SYSTEM LATENCY

The latency between an input of the TTCvi module and an output of the TTCrx ASIC was measured in two cases, namely the one for the LVL1 accept signal and the other for a broadcast command. The following figures show the net TTC system latency:

- LVL1 Accept: \( \approx 100 \text{ ns} \)
- Broadcast command: \( \approx 230 \text{ ns (end of package to output strobe)} \)

EXPERIMENTS REQUIREMENTS

The future TTC system requirements, with respect to the number of partitions and destinations, of the LHC experiment have not yet been fully investigated. Estimates for the ATLAS experiment talk for at least 40 partitions with up to 10'000 destinations.

CONCLUSION

Complete sets of components and modules are now available for the TTC system. Feedback from the LHC experiments should be taken into account before a final specification is established. A subsequent production will then be launched within the two coming years.

REFERENCES

http://www.cern.ch/TTC/intro.html
http://pcvlsi5.cern.ch:80/MicDig/ttc/MANUAL22.PDF
STRATEGY FOR TIMING ADJUSTMENT OF ATLAS END-CAP/FORWARD MUON TRIGGER SYSTEM

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ABSTRACT

We present a strategy for timing adjustment of ATLAS end-cap/forward muon level-1 trigger system. A basic timing setup utilizing variable delays is described. The delays with sub-nanosecond precision are introduced for the timing setup in bunch-crossing identification. For all the downstream logic, the timing is set up using test pulses and course delays in the step of 25/2 ns. The delay adjustments can be obtained using measurable delay elements, such as TOF, cable delays, etc., and the BC clock offset obtained when beams are available. All the delay elements will be arranged into a database to achieve adequate timing setup.

1 INTRODUCTION

In the LHC, where the trigger rate is very high and the number of detector channels is very large, it is an important issue to make sure that all the signals generated at the same bunch crossing are read out optimally. Hence some procedures must be defined to set up and maintain the timing over the whole experiment.

In this paper, we present a strategy for timing adjustment of ATLAS end-cap/forward muon level-1 trigger system [1, 2]. The Thin Gap Chambers (TGCs) [3] are used for the system. Two type of TGCs, doublet and triplet, are arranged in seven layers (one triplet and two doublets) in each end-cap at ~14 m from the interaction point in the beam direction. The size of the whole TGC system is large and it has a large number of channels. Thus a large number of electronics boards is needed. Most of them will not be easily accessible after they are mounted on the detector surfaces. Hence a scheme to set up timing must be defined when the electronics boards are designed.

2 TGC TRIGGER SYSTEM

Figure 1 shows an overview of the TGC level-1 trigger system. The system is divided into several parts and a TGC signal is precessed as follows.

At first, the TGC signal is processed on an Amplifier-Shaper-Discriminator (ASD) board attached with the detector. The signal is then received by a Patch Panel (PP) to identify the bunch crossing. A Slave Board (SB) follows the PP to perform coincidence operations for low-$p_T$ tracks. SBs are directly connected to the corresponding PPs, forming a unit package (P-S Pack; see Figure 2). Output signals from the doublet and triplet SBs are sent to a High-$p_T$ Board (HPB) to be combined for high-$p_T$ tracks. A Sector Logic Board (SLB) follows the HPBs to perform $R$-$\phi$ coincidence operations. The result is sent to the Muon Central Trigger Processor Interface (MUCTPI) to be combined with the information on barrel muon trigger system. The result from MUCTPI is sent to the Central Trigger Processor (CTP) and combined with the information on calorimeter system. As a result, the CTP generate a trigger or a Level-1 Accept (L1A) signal. The L1A is sent to the Timing Trigger and Control (TTC) system to be distributed to the readout electronics with the LHC clock (BC clock) and the synchronization signals (BCR, ECR). Each readout electronics has a TTCrx chip to receive the signals from the TTCvi.

Since the TGC system contains a large number of channels and trigger planes (one triplet and two doublets) are separated each other, it is impossible to set up the timing of the system by only optimizing the locations of electronics boards and adjusting cable length. Hence the variable delays shown in Figure 1 are introduced. The timing setup with these delays for each part is described below.
Figure 1: Overview of the TGC first-level trigger scheme. The variable delays are shown as gray boxes.

2.1 Patch Panel

The timing setup in a PP is most important because the asynchronous TGC signals are bunched by bunch-crossing identification (BCID) circuit. The main point is to set up the timing relation between signal and clock to bunch all the signals in the same clock. Since the time jitters of TGC signals are \( \sim 25 \) ns, the required precision for the adjustment is less than 1 ns. We plan to set the variable delays in the step of 25 ns/\( D \), where \( D = 32 \) hence the step is \( \approx 780 \) ps.

The timing setup as follows. First, the clock arrival time \( (T_{i}^c) \) is adjusted to produce the simultaneous BCID output in each P-S pack. Since the BC clock is served by a TTCrx equipped in a P-S pack, the latency on clock from TTCrx to BCID \( (d\theta_i) \) is different at each BCID circuit. The adjustment is achieved using delays to cancel the relative difference in clock arrival time. In PPS, 16 channels are grouped in a signal cable, and one delay is used for each cable. The adjusted arrival time of \( n \)-th clock for \( i \)-th cable is then expressed in ns as

\[
T_{i}^c = \text{OFFSET} + d\theta_i + 25n_i + d\theta_i + \text{adj}\theta_i \quad (1)
\]

This is expressed using the measurable delay elements shown in Table 1 and the delay adjustment \( \text{adj}\theta_i \).

The important thing is that \( T_{i}^c \) includes the BC clock offset \( \text{OFFSET} \), which is the time when the first clock is distributed from TTCvi after the beam crossing. The \( \text{OFFSET} \) value is obtained only with beams. The method to obtain the value is considered later.

Second, the signal arrival time is adjusted to bunch the signals in the adjusted clock. The difference in the

Figure 2: A P-S pack. Showing the wiring of BC, L1A, BCR and ECR distributed from a TTCrx.
arrival time is due to differences in the time of flight (TOF) and cable delay from ASD to PP (dIi). With the delay adjustment of the signal (adjIi), the ideal (no time jitter) arrival time \( T_i^* \) is expressed as

\[ T_i^* = TOF_i + dI_i + adjI_i. \]  

(2)

Timing relation between \( T_i^* \) and \( T_i \) is shown in Figure 3. Because of the time jitter of signals, the earliest-arriving signal \( T_i^* \) must satisfy the following condition:

\[ 0 \leq T_i^* - T_i < \frac{25}{D} \text{ (ns)}. \]  

(3)

The earliest-arriving signal has the minimal time jitter; thus it almost corresponds to the ideal signal. Hence \( T_i^* \approx T_i \) and the timing has to be set up for all the signals to arrive at the BCID just after the clock edge.

![Timing chart for a bunch-crossing identification. adj0 and adj1 are delay adjustment on clock and TGC signal respectively.](image)

The variable delays can be set between 0 and 25 ns. We can obtain a set of simultaneous BCID output in each P-S pack if this range is enough to set up the timing. This possibility depends on the design of the P-S pack and the timing setup can be achieved in the current design (see Figure 2).

The settings of variable delays are obtained with only the measurable delay elements except OFFSET. Hence the unique timing adjustment is set up if the clock offset is obtained.

### 2.2 Slave Board

In Slave Boards (SBs), we have to consider the timing of the signals at the coincidence logic and level-1 buffer (L1B) for readout. Hence we need to adjust the arrival time of signals using variable delays at the entrances of coincidence logic and L1B. Since incoming signals in SBs have already been bunched, only coarse delays are needed. In principle, the delays in the step of 25 ns will work to set up the timing here. However, the step should be a half of 25 ns because we have to prevent signals from arriving near the edge of clock.

The delay adjustment is obtained with only the measurable delay elements (shown in Table 1) in principle. However, the delays are adjusted using test pulses to confirm the correct timing. Note that the delay adjustment for SBs are independent of the clock offset. Once signals are correctly bunched and synchronized in PPs, the timing adjustment in SBs are easily achieved.

The timing setups of L1A, BCR and ECR are also needed because of the difference in the signal-path length between the SBs in a P-S pack (see Figure 2). In our current plan, these setups are achieved by adjusting the L1B length.

### 2.3 High-P_T Board, Sector Logic, etc.

We should also consider the timing setups for the downstream logic of SBs, such as High-Pt, Sector Logic, etc. These setups are very similar to that for SB. However, much wider range of variable delays are needed since the incoming signals from different parts of upstream logic are combined to perform the coincidence operations. For instance, signals from both the doublet SBs and triple SBs are combined at HPBs and R and \( \phi \) signals are combined at SLBs.

### 3 SCHEME OF TIMING SETUP

In this section, a possible scheme of timing setup is described. There are three steps in it. First, the timing up to the CTP is set up using test pulses before beams are available. Second, the OFFSET value is obtained with beams. Last, the trigger and synchronization signals are adjusted at readout elements. Each step is described below.

#### 3.1 Timing Setup Using Test Pulses

For the TGC system, test pulses are generated in PPs and provided for ASD boards. They return the pulses back to the PPs instantly. These incoming test pulses can be treated as if they were TGC signals and hence the timing can be set up using them. However, the settings of variable delays \( \text{adj} \theta_i \) and \( \text{adj} l_i \) obtained above are not valid since the test pulses take no account of the difference in TOF. Hence the special timing adjustment is needed for the test pulses. The test-pulse generator has its own delay \( \text{adj} T_i \) and such the timing adjustment can be achieved using the delays. \( \text{adj} T_i \) is a function of \( \text{adj} \theta_i \) and \( \text{adj} l_i \), and it...
Figure 4: Timing chart of the TGC system with phase-adjusted clocks

is fixed uniquely if OFFSET value is known. Since OFFSET is not obtained before beams are available, we assume OFFSET = 0 at this time and consider it later. This assumption enables us to set up the timing relation between signals. The adjusted test pulses are sent out from the BCID circuits simultaneously in each P-S pack. The timing setup of the whole downstream logic can be achieved using these test pulses.

The outputs from Sector Logic are fed by MUCTPI and CTP and a L1A is generated by CTP. The L1A finally reach the L1B in the front-end electronics via TTCvi and TTCrx. Since the MUCTPI and CTP depends on other subsystems, the exact timing cannot be set up only within the TGC system. However, the total latency on L1A can be estimated with the estimated delay on L1A at the MUCTPI and CTP. Using this information, the timing of L1A at L1Bs can be adjusted. This timing can be readjusted when beams are available.

### 3.2 BC Clock Offset

The timing relation between signals is adjusted in the previous step. OFFSET value is then obtained with beams to set up the timing relation between signals and clocks.

The LHC bunch structure is utilized to obtain OFFSET value. As described in TDR [2], we can see the bunch structure in the histogram of the number of track hits as a function of BCID for correct OFFSET value, while no bunch structure appears for any wrong OFFSET. Hence OFFSET value is scanned until the bunch structure can be seen. Scanning the OFFSET value corresponds to adjusting the clock phase. Since the relative signal timing is adjusted using test pulses, the wrong timing of the TGC system is only due to an incorrect OFFSET. Hence we can set up the correct timing in BCID by adjusting the clock phase. To keep the timing setup achieved in the previous step, the clock phase is adjusted using the delays in TTCvi. Figure 4 shows the timing chart of the TGC system when the clock phase is adjusted with TTCvi delays.

### 3.3 Timing Setup of Trigger and Synchronization Signals

In the last step, the timing of L1A and synchronization signals (BCR and ECR) for readout (L1B) is set up.

When OFFSET is found and the LHC bunch structure is seen in the histogram above, the BCID may be assigned incorrectly there. This is due to the incorrect BCR timing. Hence the BCR timing is adjusted to see the correct BCID.

Next, the L1A timing is checked at, for the instance, BCID = 1. Though the trigger timing has been adjusted at the step using test pulses, small adjustment may be needed here.

Finally the ECR timing is adjusted to see the correct BCID and trigger.
4 DATABASE OF DELAY ADJUSTMENT

The timing setup described above needs a large number of settings of variable delays over the whole TGC system. Thus these settings should be arranged as a database to achieve adequate timing setup. The delay adjustment in PPs (including the setup of test pulses) is expressed using the measurable delay elements. Even though the timing is set up using test pulses for all the downstream logic from PPs, the initial settings of delays can be estimated from the measurable delay elements. Hence all the delay elements should be arranged into a database to achieve easy, quick setup using test pulses. Main delay elements of the system are listed in Table 1.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Delay Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>(PP)</td>
<td></td>
</tr>
<tr>
<td>OFFSET</td>
<td>BC clock offset</td>
</tr>
<tr>
<td>dφ0</td>
<td>Fiber delay from TTCvi to TTCrx</td>
</tr>
<tr>
<td>dφi</td>
<td>Latency on clock from TTCrx to BCID</td>
</tr>
<tr>
<td>TOF</td>
<td>Time of flight</td>
</tr>
<tr>
<td>d1i</td>
<td>Cable delay from ASD to PP</td>
</tr>
<tr>
<td>(SB)</td>
<td></td>
</tr>
<tr>
<td>Latency on clock from TTCrx to SB</td>
<td></td>
</tr>
<tr>
<td>Latency on signal from PP to SB</td>
<td></td>
</tr>
<tr>
<td>Latency in coincidence logic</td>
<td></td>
</tr>
<tr>
<td>(HPB)</td>
<td></td>
</tr>
<tr>
<td>Latency on clock from TTCrx to HPB</td>
<td></td>
</tr>
<tr>
<td>Cable delay from SB to HPB</td>
<td></td>
</tr>
<tr>
<td>Latency in coincidence logic</td>
<td></td>
</tr>
<tr>
<td>(SLB)</td>
<td></td>
</tr>
<tr>
<td>Latency on clock from TTCrx to SLB</td>
<td></td>
</tr>
<tr>
<td>Latency on signal from HPB to SLB</td>
<td></td>
</tr>
<tr>
<td>Latency in coincidence logic</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: Main delay elements used for the delay adjustment (up to MUTCPI)

5 SUMMARY

We have report on the strategy for timing adjustment of ATLAS end-cap/forward muon trigger system. A basic timing setup utilizing variable delays was described.

The timing setup in a Patch Panel is most important because the bunch-crossing identification (BCID) is performed. Since the TGC signals are asynchronized and their time jitters are up to 25 ns, the required precision for the adjustment is less than 1 ns. The delays in the step of 25 ns/32 ≈ 780 ps are introduced to set up the timing. The delay adjustments are calculable from measurable delay elements, such as TOFs, cable delays, etc., and the BC clock offset obtained when beams are available. For all the downstream logic, the timing is set up using test pulses and course delays in the step of 25/2 ns.

A scheme of timing setup using test pulses was described. The timing of test pulses provided by PPs is adjusted to produce a set of simultaneous BCID output in each P-S pack. The timing setup of the whole downstream logic can be achieved using these test pulses up to generating L1A signals. After setting up the timing with test pulses, OFFSET value is obtained with beams by utilizing the LHC bunch structure. The wrong timing of the TGC system is only due to an incorrect OFFSET; thus the correct timing is achieved by adjusting the clock phase. It is adjusted using the delays in TTCvi to keep the timing setup achieved in the previous step. Finally the timing of L1A, BCR and ECR is adjusted with similar scheme to the TDR.

A large number of settings of variable delays over the whole TGC system are arranged as a database. All the delay elements should be arranged into a database to achieve easy, quick timing setups of all the logic in the system.

REFERENCES


ABSTRACT

The SCT detector interfaces with the ATLAS Level 1 using the LHC-wide TTC (Timing, Trigger, and Control) system. The design of the TIM (TTC Interface Module), part of the SCT off-detector electronics [1], and the interface with the RODs (Read Out Drivers), is described.

Also described is the forerunner of the TIM, the CLOAC (Clock And Control) MASTER module, developed to provide a stand-alone timing and trigger capability in the absence of the TTC system. CLOACs are currently used in the SCT tests at CERN. They are also available to the SCT community for use in front-end modules testing.

1. INTRODUCTION

The SCT interface with ATLAS Level 1 receives the signals through the Timing, Trigger, and Control (TTC) system [2] and returns the SCT Busy signal to the Central Trigger Processor (CTP). It interfaces with the SCT off-detector electronics, in particular with the Read-Out Driver (ROD), and is known as the SCT TTC system.

The SCT TTC system consists of the standard TTC system distributing the signals to a custom TTC Interface Module (TIM) in each crate of RODs. In addition, a Busy module returns the SCT Busy signal.

This paper and the accompanying diagrams describe the essential features of the TIM. For further details refer to the interface specification documents [3] [4] [5]. The TIM module also has to satisfy the requirements set out in the SCT TTC Interface Requirements document [6].

( By the way – these documents have been shown to be useful in getting engineers in different countries, and continents, to come to an agreement on how to make their modules understand each other. Provided they are not too long, of course, otherwise there is no time and no inclination to read them! )

2. TIM

2.1 Functionality

The diagram (Fig.1) illustrates the main function of the TIM, which is to interface the off-detector electronics, in particular the ROD, with the outside world of Level-1 electronics. Diagrams showing an overview of the SCT system [7] and the TTC context [8] are also available.

Fig. 1: SCT TIM Context and Essential Model
The TIM transmits the clock, fast commands and event ID from the TTC system to the RODs with minimum latency. The clock is also transmitted to the Back-Of-Crate optocards (BOC).

- The TIM passes the Busy from the RODs via a Busy module to the CTP in order to stop it sending triggers.
- The TIM can send stand-alone clock, fast commands and event ID to the RODs under control of the local processor.
- The TIM has programmable timing adjustments and control functions.
- The TIM has a VME slave interface to give the local processor read and write access to its registers.
- The TIM is configured by the local processor setting up TIM's registers. They can be inspected by the local processor.

2.2 TTC Interface

The TIM receives the TTC signals and passes the required subset to the RODs (Fig. 2).

Fig. 2: TIM Functional Model

The optical TTC signals are received by a receiver section containing a standard TTCrx receiver chip, which decodes the TTC information into electrical form.

The TTC information, required by the RODs and by the SCT FE electronics, is the following:

Clock: BC  Bunch Crossing clock
Fast command: L1A  Level-1 Accept
Event Counter Reset
BCR  Bunch Counter Reset
Calibrate signal
Event ID: L1ID  24-bit Level-1 trigger number
BCID  12-bit Bunch Crossing number
TTID  8-bit Trigger Type

The TIM outputs the above information onto the backplane of a ROD crate with the appropriate timing. The event ID is transmitted with a serial protocol and a FIFO (First In First Out) buffer is required in case of rapid triggers (Fig. 3).

Timing of TIM Output Signals

Fig. 3: Timing of TIM Output Signals

An additional FER (Front End Reset) signal, which may be required by the SCT FE electronics, can also be generated, either by the SCT-TTC or by the TIM.

The TIM can also generate all the above information stand-alone at the request of the local processor. It can also be connected to another TIM for stand-alone multi-crate operation for system tests in the absence of TTC signals.
The TIM does a masked OR of the ROD Busy signals in each crate and outputs the overall crate Busy to a BUSY module [9]. It is intended to implement the monitoring functionality of the BUSY module on TIM.

2.3 Hardware Implementation

The TTC interface is based on the standard TTCrx receiver chip, together with the associated PIN diode and preamplifier developed by the RD12 group at CERN, as described elsewhere [10]. This provides the BC clock and all the signals as listed in section 2.2 above.

The BC clock destined for the BOCs and RODs, with the timing adjusted on the TTCrx, is passed via differential PECL drivers directly onto the point-to-point backplane tracks. These are designed to be of identical length for all the slots in each crate to provide a synchronised timing marker. All the fast commands are also clocked directly, without any local delay, onto the backplane to minimise the TIM latency budget [11].

Apart from the BC clock normally provided by the TTCrx, the TIM generates its own 40.08 MHz internal clock. This, as well as the externally input ECL or NIM clocks, can be selected by the local processor to drive the TIM and generate the backplane clocks. To ensure the identical timing relationship as when using the BC clock, an additional programmable delay is provided in the internal clock circuit.

Timing adjustments and setting of various delays is an important part of the TIM operation. There are fine and coarse delays for the BC clock and the TTC fast commands incorporated on the TTCrx. In addition, TIM provides further fine delay to the clock used for the timing of the backplane signals (Fig. 4).

The L1ID, the BCID and the TTID information for at least eight subsequent events (assuming the current ATLAS restriction of a maximum of 8x L1As in 80 usec) are required to be buffered and serialised onto two event ID backplane lines. Remaining circuitry consists mainly of the mapping required to provide 8 individually selectable signal lines to be output and bussed across the VME backplane, and of the necessary synchronising and buffering required to obtain sufficiently stable setup and hold times for all the RODs in each VME crate [12]. Most of this is implemented using MACH-5 programmable logic devices.

All the 8 backplane signals, which normally come from the TTC, are also capable of being either generated on the command of the local processor, or automatically by the TIM under local processor control. Further details of the stand-alone capabilities of the TIM are described below in the CLOAC MASTER Functionality section 3.1.

In addition, a sequencer, using 8x32k RAM, is provided to allow long sequences of commands and ID data to be written in by the local processor and used for testing the FE and off-detector electronics [13].

There is also a complete set of external inputs for clock and all the above signals on the front panel in both NIM and differential ECL. All the backplane signals are also mirrored as differential ECL outputs on the front panel to allow TIM interconnection.

Most of the logic circuitry required for the stand-alone operation is also contained on a number of PLDs, with only the buffering of the various inputs and outputs being done by separate integrated circuits [14].

The TIM has been designed as a 9U, single width, VME module, with a standard VME slave interface. A24/D16 or A32/D16 access is selectable, with the base address A16 – A23 (or A16 - A31) preset as required. A combination of FastTTL, ECL, PECL and LV BiCMOS devices is used, requiring +5V, +3V3 and -5V2 voltage supplies.

Fig. 4: Timing Flow of SCT - TTC Signals

3. CLOAC

To prototype some of the stand-alone functionality of the TIM, and to generate the clock and fast commands to enable front-end modules to be tested in
the absence of the TTC system, the CLOAC (Clock And Control) MASTER module has been designed [15].

3.1 Functionality

The CLOAC MASTER module generates the clock and all the fast commands as discussed in section 2.2 above, either on command from a local processor or fully stand-alone.

The triggers can either be issued singly or repetitively, with the number of triggers programmable (from 0 to 65535, or continuous) and their frequency fully programmable and selectable as either a single frequency (in the range 50 Hz – 600 kHz), or with an average random rate (between 12.5 Hz – 150 kHz). There is also a fully programmable “latency” delay (of 0 - 143 clock periods) between the receipt of an external trigger and the issue of the trigger to the FE module.

The calibration pulse is followed by an automatically generated calibration trigger after a delay, programmable in the same range of 0 – 143 clock periods, so it is received when data is at the end of the pipeline (of 132 BCs). Either single or multiple (0 to 65535) calibration pulses can be selected, with a minimum repetition period of about 84 usec (depending on the programmed calibration trigger delay).

The capability of being able to issue a precise number of triggers or calibration pulses very fast is useful for obtaining histograms from the FE readout data.

Internally generated Soft Reset signals are issued at a programmable frequency (between 0.05 Hz - 60 Hz) and BC Reset at a preset frequency of about 11.2456 kHz (the LHC beam orbit rate).

The CLOAC MASTER can also synchronise to an external clock and can accept external fast commands provided as NIM or differential ECL inputs. It can receive BUSY inputs to provide a masked BUSY output.

A basic trigger “window”, capable of being programmed in width and delay (0 to 24 nsec in steps of 1 nsec) with respect to the received clock, is also available to assist with random trigger tests (eg. using cosmics or test beams).

A combination of these fast commands, selected by the local processor, is synchronised to the selected clock. The commands are then converted to command strings (fully programmable, but normally set to the values specified by the SCT front-end ASIC chip protocol [16]) and mixed together, using a priority selector to avoid the issue of simultaneous commands.

Additionally, a programmable slow command of up to 64 bits long can be issued to provide a very basic setting-up capability for the FE modules.

The CLOAC MASTER provides four separate electrical outputs of the clock and command strings in differential ECL to allow direct connection to four FE modules in the absence of RODs.

(Note: The TIM will not be capable of issuing command strings since normally this functionality will be provided by the RODs).

3.2 Hardware Implementation

The CLOAC MASTER module has been implemented as a 6U PCB with a standard A24 / D16 VME slave interface (Fig. 5). All the logic circuitry, including the VME interface, reside on three MACH-5 PLDs. A combination of FastTTL and ECL devices has been used, requiring +5V and -5V2 supplies.

![Picture of CLOAC MASTER module](image)

Some CLOAC MASTER modules have been used in the SCT system and beam tests at CERN since 1998.

An additional number of CLOAC MASTER modules has been manufactured and made available to the SCT community for testing FE modules in combination with MuSTARD and SLOG modules [17].
Additionally, a number of CLOAC FANOUT modules has also been produced which provide 7 separate clock and data differential ECL outputs each (Fig. 6).

4. ACKNOWLEDGEMENTS

We would like to thank Professor Tegid W. Jones for his continuous support of our work in the ATLAS collaboration. We also wish to thank Janet Fraser who, at short notice and despite her own ATLAS-SCT work, helped to produce the diagrams and the overhead transparencies used in this paper.

5. REFERENCES

[15] CLOAC Module Description: http://www.hep.ucl.ac.uk/atlascct/CLOAC
[16] SCT Electronics: http://scipp.ucsc.edu/groups/atlascct/docs.html

6. FIGURES:

Fig. 1 SCT TIM Context and Essential Model: http://www.hep.ucl.ac.uk/~mp/TIM_figure.pdf
Fig. 2 TIM Functional Model: http://www.hep.ucl.ac.uk/~mp/TIM_Functional_model.ep
Fig. 3 Timing of TIM Output Signals: http://www.hep.ucl.ac.uk/~mp/TIM_Outputs_timing.ep
Fig. 4 Timing Flow of SCT-TTC signals: http://www.hep.ucl.ac.uk/~mp/TIM_Timing_flow.ep
Fig. 5 Picture of CLOAC MASTER module: http://www.hep.ucl.ac.uk/~tfj/bd2nov.jpg
Fig. 6 Picture of CLOAC FANOUT module: http://www.hep.ucl.ac.uk/~tfj/bd1nov.jpg

Fig. 6: Picture of CLOAC FANOUT module
Abstract

In the context of large data acquisition systems (DAQ) for LHC experiments, flexible and uniform interfaces between subsystems is a key feature to ensure best possible system integration/maintainability and a clear system upgrade policy. This approach is widely used in CMS at the border between sub-detectors front-end and the DAQ. Common requirements and reconfigurable hardware used in CMS DAQ are presented in this article.

1. Introduction

A basic block diagram of the CMS DAQ is shown figure 1. Its constitutive elements are the detector front-end, the trigger logic, the readout units (RU), the event builder, the event filter units (EFU), the computing services, and the event manager.

Fig. 1. CMS DAQ block diagram

The front-end electronic acquires data every bunch crossing and the trigger logic selects the data to be sent to the readout units. A readout unit is constituted of 1 DPM and several Detector Dependent Units (DDU). A DDU is controlling the associated front-end electronic and receives the trigger selected data. As a DDU is receiving data on several data links, a data packet is built locally (DDU event). The DDU event is kept available for the DPM. As a DPM is reading out several DDUs, a DPM event is also built. Then the DPM event (also called Event Fragment) is sent through the event builder to the requesting EFU. The association of the RU with an EFU is the task of the event manager.

2. Interfaces and standardization

The DAQ is the natural convergence point of the data produced by the sub-detectors. In the case of CMS, there will be about 12 different data sources providing data to the DAQ. Interfacing these sources with the DAQ is a critical point given the overall size and complexity of the final system (on-detector electronic, counting room electronic and DAQ). Reducing the diversity in the electronic devices is a valuable approach regarding the system integration (especially during the initial debug phase) and later the maintenance/upgrade operations.

Looking at hardware interfaces between heterogeneous systems, one can find a generic architecture often encountered in DAQ applications (see figure 2).

Fig. 2. Generic interface architecture

As soon as a "popular" hardware has to drive (or be driven by) a specialized one, this generic architecture is used (with some variations).

The DDU, part of the Readout Unit (see figure 3), can be seen as the interface between the DAQ and the sub-detector readout systems. Below the DDU, no sub-detector specific hardware is foreseen in the DAQ architecture. The task of the DDU is to deal with a given sub-detector with its specificities on one side and make available the data on the Front End Bus (FEB) according to its specification/protocol on the other side. More informations about the DDU functionalities are available in [1].

The principle of a common DDU for all sub-detectors in CMS is proposed for a long time now. A common functional specification document [1] is adopted by all CMS data producers. The next step is to study the feasibility
of a common hardware platform that can suit the sub-detectors needs. Architecturally speaking, the part of the DDU in touch with the FEB can be common for every sub-detectors both at the functional and physical level. Regarding the sub-detectors, two families can be distinguished: analog detectors and digital detectors. Concerning the analog detectors (Pixel, Silicon and MSGCs), a unique hardware development is underway and made by the Rutherford Appleton Laboratories [2]. The standardization is eased by the fact that the detectors are using the same data link and/or Front End chip [3]. About the digital detectors, the situation is not as easy due to the fundamental differences between detectors. However, the CMS DAQ group designed a versatile board that has been first used for specific DAQ applications. But during the design phase, special care have been taken to allow other applications outside the DAQ area to be implemented: especially DDU-type applications were considered.

In the next parts of the article, the generic block diagram of a DDU will be shown and compared to the block diagram of the versatile DAQ board. Then a quick overview of the different applications running on that board will be listed and finally, the next generation of versatile board, currently in the assembly/debug phase, will be presented.

3. Generic DDU

As reminded before, the DDU is in charge of interfacing a sub-detector environment with the central DAQ environment. One part of the DDU deals with the sub-detector specificities and the other part deals with the so-called FEB. This later part must be common for all sub-detectors on the functional level and can be common on the physical level. Architectural/functional flexibility is a major feature of the common part as the DAQ will follow the technological evolution of the telecommunication industry during its life time. Therefore, reconfigurable logic (FPGAs) and a layered approach are used wherever it is possible.

Generically speaking, the DDU must acquire the data of the FES, control/manage the FES and make available the data on the FEB after a specific processing (if any). The data encapsulation format and the communication protocol with the DAQ will be unique through CMS. The DDU generic block diagram is shown Fig. 3.

4. Generic DAQ platform

A DAQ hardware platform has been designed and developed last year in order to provide a prototyping facility for testing other DAQ boards (mainly the Dual Port Memory [4]) and evaluate architectural options within the CMS DAQ project.

4.1 Description

The architecture of the board features total reconfigurability thanks to the on-board FPGA (50Kgate-equivalent) 100% available to user-application. The FPGA [5] is linked on one hand to a commercial PCI interface [6] (initiator and target) and on the other hand to a 77 pins user port through bi-directional TTL drivers. The drivers are fully controlled from the FPGA allowing custom I/Os to be implemented. The FPGA has also access to 32 KBytes of nvRAM. Finally, the same access port to the TTC signals defined by RAL has been implemented on the board.

Fig. 3. Readout Unit Structure

Fig. 4. Generic DDU block diagram
This architecture allowed numerous applications to be developed. Detailed description and engineering documents are freely available on the WEB [7] to anyone interested by such hardware.

4.2 Applications

- **DPM exerciser**
  In the previous version of the DPM named P25++, the data input port was a custom development and the output port was a standard PCI. The generic board has been programmed to readout data through the output port (the generic board was initiator of the DMA) and to reinject these data into the input port. The data were cycling at 128 MB/sec. sustained (97% of the maximum possible performances of PCI 32bit/33MHz)

- **DDU emulator**
  Always with the P25++, the generic board has been configured to emulate a DDU. Under the control of the PCI bus, the FPGA was translating on the fly a PCI data stream (DMA) to the input format of the DPM. The throughput was again close to the maximum PCI speed.

- **FERA to PCI interface [8]**
  The generic board is in charge of transferring the data on the FERA bus (Fast Encoding and Readout ADC developed by Lecroy Corp.) to the PCI bus by means of DMA. The PCI destination address is controlled via a register in the FPGA.

- **Trigger interface for CMS Muon chamber [9]**
  For test beam applications, the board is used to interface the chamber readout system on PCI with the beam signals (spill, trigger). The busy and veto signals are controlled by the board.

- **Fast Messaging network based on IEEE-1394 [10]**
  Still under design, it is an extension of the previous application to several PCI based readout units. The network is Firewire at 400Mbit/sec. The triggers are tagged and broadcasted to all readout units to ensure the correct event fragments to be merged during the event building process. For that, a transition module has been developed to house the Firewire hardware: it plugs directly into the user connector.

  - **Myrinet protocol monitor [11]**
  For LHC DAQ systems, one major piece of equipment is the event builder. The most likely implementation of the event builder is based on a multi-stage switch fabric. If the behavior of an individual switch can be measured and simulated, the behavior of a switch fabric is much more difficult to study. In order to understand what is going on in the hardware, a protocol monitor is often needed. This device allows to measure the basic parameters of the device and allow to define the simulation constants needed to tune the software model. Moreover, it helps to interpret/explain some measurements when the architecture and the test setup is getting complex, and it is the case! For CMS, one candidate is a switch from Myricom [11]. A spy/monitor based on the generic board is under development. A pre-processor board is plugged on the user connector to allow the interfacing with the low-level layers of the switch protocol. The FPGA extracts the features of the messages (destination, length, status, flow-control, time tags...) and stores them into the nvRAM. A visualization software then acquires them and process them for display and statistics.

Given the comments of the different users and the technology improvements, the need for hardware flexibility (especially for the user connector), more storage capacity and faster FPGA/PCI interface triggered the development of a new generation.

5. New generation of the DAQ platform

Compared to the previous version, it features:

- **PCI 66MHz, 64 bits capability**
- **On-board 32 Mbytes SDRAM**
- **800MBytes/sec. internal bandwidth**
- **300Kgate-equivalent FPGA**
- **148 pins high performance port for custom hardware**
- **JTAG support for BSCAN and FPGA configuration**

The choice of the GT64120A from Galileo [12] as PCI interface enables the fastest speed on PCI (524 MBytes/sec. peak) and the usage of huge, inexpensive memory
chips (100 MHz SDRAMs). The FPGA is a Virtex 300 (the new family from Xilinx [13]) providing the equivalent of 300K logic gates.

Due to BGA technology used for the two previous chip, IEEE-1149.1 (JTAG) had to be implemented for test/debug purposes. The FPGA and its configuration EEPROM are compliant to IEEE-1149.1 and integrated in the JTAG chain as well. Finally the JTAG chain is available on the user connector to allow the test/debug of the application specific hardware extension. Each chip can be removed separately from the chain if the shifting time becomes “long”. This feature allows also individual debug if needed. The access to the JTAG chain is either local from an on-board tap or from the PMC connectors, hence allowing remote test/debug/reconfiguration.

To increase the flexibility at the hardware level, instead of providing a connector with fixed drivers and terminations (solution adopted in the first generation), all the remaining free pins of the FPGA are available on high performance/high density connectors (Matched Impedance Connector family from AMP [14]) where a specific extension board can be plugged. Hence, the platform can match exactly the requirements of the specific application by developing only an extension module.

The form factor of the core board is PMC. With its extension, the PMC specs. are violated but still allows the operation in a standard PMC slot. Mictor edge to edge connectors are available and would allow to match the PMC form factor but the cost and minimum quantities of such connectors are dissuasive for prototyping!

Again, the RAL TTC access port has been implemented but now, the FPGA has the capability to drive these lines if the application requires it: bidirectional LVDS drivers fully wired to the FPGA have been implemented on-board. This feature opens a full range of new applications that were not possible with the first generation of generic boards. As with the first generation, engineering files along with component specifications are freely available at [7]. When the board will be fully operational, access to CAD files under Cadence will be also given.

### 5.1 Foreseen and potential applications

- **The first application to be ported on that generic board will be a 200m-400MByte/sec. data link.** Such performances are required to implement the so-called “DAQ link” in CMS (this link goes from the DDUs located in the underground counting rooms up to the RUM located in surface buildings along with the switch and the filter farm).

- **Protocol analyser/monitor**
  A faster and more powerful Myrinet analyser may be ported on the new platform. In the near future, Myrinet will more than double the speed of their link and the first board will be saturated immediately with the high speed traffic.

- **Level 1 Accept generator/Control networks**
  As the DAQ test setup evolves towards the final architecture, trigger generation devices and fast control networks must be developed in order to exercise the setup under more realistic conditions. The versatility of the new generation enables these developments.

- **Front-End data fan-in/fan-out**
  For low/high occupancy detectors, data may need to be multiplexed/demultiplexed before/after the FEB. This is needed to use the FEB bandwidth in an efficient way or reduce the load to a small part of the switch: this can be done by such board, re-designing only the extension.

- **Finally, the board can be the core of a unique digital DDU (to reach the same situation as with analog detectors in CMS) or a general prototyping platform to get familiar with high speed PCI, to implement exotic interfaces to PCI... Whatever you can imagine!**

### 6. Summary

In a first part, steering principles for sub-detector/DAQ communication are presented. In order to ease system integration, the concept of a uniform interface for all sub-detectors has been adopted for CMS. A set of minimum requirements has been established and a common implementation for these minimum requirements is proposed. This standardized approach will ease the integration, the debug, the maintenance and the upgrade of the
system with minimal resources consumption (financial
and human).
In a second part, reconfigurable hardware platforms
developed by the CMS DAQ group are presented.
Thanks to the on-board programable logic, these plat-
forms are used by the sub-detectors but also by other
groups to develop their specific applications. An over-
view of these applications is given.
Finally, the latest generation of the platform is pre-
sented. The versatility of the platform has been
increased by using extension boards where application
specific hardware can be added. A 200m-400MB/s data
link based on this platform will be the first practical
application.

7. References

[1] CMS DDU design specifications
    CMS Note 1999/10
    A. RACZ CERN - EP/CMD

[2] CMS Tracker FED-PMC Page
    http://hepnts1.rl.ac.uk/CMS_fed/Default.htm

    ftp://ftp.te.rl.ac.uk/apv6/user_manual/
    apv6_user_manual_2.0.ps

[4] CMS Dual Port Memory
    see LEB99 Proceedings
    D. GIGI CERN - EP/CMD

    http://www.altera.com

[6] PLX WEB pages
    http://www.plxtech.com

[7] DDU Designers pages
    http://cmsdoc.cern.ch/~racz/DDU/

[8] A versatile F.E.R.A to PCI interface for the GASP
    experiment - M. Bellato, R. Ponchia - INFN internal
    report

[9] A reconfigurable trigger interface for small DAQ
    systems - M. Bellato - INFN internal report

[10] A readout control network for small DAQ systems
    based on IEEE-1394 standard - M. Bellato, R. Pon-  
    chia - INFN internal report

    http://www.myri.com

[12] Galileo Technology WEB pages
    http://www.galileot.com

[13] Xilinx WEB pages
    http://www.xilinx.com

[14] AMP MICTOR Family
    http://www.amp.com, then do a search on "mictor"!
In the acquisition system for CMS, the RDPM is a dual-port memory (up to 256Mbytes) used to buffer and filter events. The third prototype is currently under study and development. It will be a PCI board with three PCI busses: an input bus to receive data form the DDU, an output bus to send data to the computer through a switch and a control bus (each one with 64-bit @ 33-66MHz to reach the 400MB/s data bandwidth). The board will be built with FPGA components. This is an advantage to reprogram the board to be flexible and to test different events organizations. The third prototype will be integrated in the DAQ system demonstrator.

1. INTRODUCTION

The future experiments in the High Energy Physics, as Compact Muon Solenoid (CMS) at LHC in CERN needs complex Data Acquisition System (DAQ) [1]. Multilevel DAQ systems structures required fast buffer for intermediate storage of data before transferring between the levels. Usually as a data buffer is used fast dual-port memory, with possibility of collect a big amount of data, corresponding to the event size. Standard bus interfaces are used for designing of modules for such DAQ system. Most useful bus standard interface becomes Peripheral Component Interconnect (PCI)[2]. PCI Mezzanine Cards (PMC)[3] are intended to be used where slim, parallel board mounting is required for host modules with the logical and electrical layers based on the PCI.

2. CMS DAQ STRUCTURE

2.1 CMS DAQ Readout Column Description

Block diagram of the CMS DAQ Readout Column is shown on Fig.1. The RU is a major part of the Readout Column and it is placed between the Front-end Devices (FED) and Builder Data Network (BDN). This unit is used as an intermediate data buffer capable of receiving event data from FED at 400MB/s and sending at the same time requesting event data to the BDN at 200MB/s. Event organisation according to the Event-ID# is required to be implemented inside the RU. The same functionality and structure has the Builder Unit (BU) major part of the Filter Column.

3. READOUT UNIT

3.1 RU Functions and Requirements

RU functional diagram is shown on Fig.2. The RU has four ports and contains the following basic functional and structural components: Readout Unit Input (RUI) - input for event (up to 4KB) data size at 100KHz rate; Readout Unit Output (RUO) - output for sending data to the BDN; Readout Unit Memory (RUM) - dual-port memory up to 512MB size for storing the event data and Readout Unit Supervisor (RUS). Fast Interconnect is using between all components of the RU. Additional ports for Control and Monitoring are also available on the unit.

3.2 RU Block Diagram

All functions of the RU were possible by dividing the hardware implementation on two boards called RUM and
Readout Unit Input Output (RUIO). Those are long size 64bit at 33/66MHz PCI boards connected together. Block diagram of hardware implementation of RU is shown on Fig.3.

![Fig.3. RU Block Diagram](image)

In this hardware configuration from each side of the RUM is connected one RUIO board. All of them are configured via common (host) PCI bus. For internal connection between the boards we chose also 64bit PCI bus protocol running at 33/66MHz. Possible configurations for RU are using only RUM and mixed input/output port with control port, or using RUM and one only RUIO board.

### 3.2.1 RUM

RUM board is a general part of the RU. Readout Unit Memory is a PCI dual-port memory with third PCI bus for control. RUM receive the event header (Event-ID#, word-count, first memory block and status) and event data from the input. Event header is transferred to the Memory Management Unit (MMU) on board and is stored into the sequencer memory. Event data is stored into the data memory according to the memory block organisation. Four PCI Bridges (PBR) is using to connect the input, output, control and local bus. And fast local bus is using between MMU, Memory Controller (MC), PCI Interface Controllers and PBR. Block diagram of the RUM is shown on Fig.4. and contains the following general blocks: PBR; MMU; MC; PCI Interfaces; Memory; Local Bus controller (IOP or FPGA like unit) and PCI/PMC connectors. For all mention above general blocks we are using fast reprogrammable devices (as FLEX10K and APEX series from Altera) and for the local bus controller IOP480 from PLX Corp. Data memory is based on Synchronous DIMM modules with possibility of increasing the size up to 512MB.

![Fig.4. RUM Block Diagram](image)

### 3.2.2 RUIO

RUIO board shown on Fig.5. contains the following general blocks: Three PCI Bridges (PBR); PCI to Local bus IOP480 controller; Memory – Flash, SRAM and DIMM; Ethernet Controller and PCI/PMC connectors. Basic function of the RUIO is to extend the input and output bus of the RUM and provide more flexible control of the RU. Three PBR is implemented in FLEX10K200 component. Commercial available interface links board (as Myrinet, ATM, FC etc.) can be plugged into PCI/PMC connectors to connect RU to the BDN. The first five RUIO boards are produced and tested successfully.

![Fig.5. RUIO Block Diagram](image)

The IOP480 processor has 32bit 33MHz PCI bus interface and 32bit Local bus running at 60MHz, integrated memory SRAM/FLASH/SDRAM controller for up to 256MB of memory, DMA controllers, serial interface RS-232 and I2O Ready Messaging Unit. For Ethernet controller was chosen 21143 PCI 10/100Base-T LAN controller from Intel. The chip supports both 100-Mb/s and 10-Mb/s data rates and is optimized for low power based systems.
4. FPGA FLEXIBILITY

In order to implement all functions of the RU and its corresponding parts we decided to use reprogrammable logic devices as FLEX, APEX etc. This is based also on our experience from previous versions of the Readout Unit (RDPM see [4]). Flexible architecture of these devices is useful to reprogram and implement different functions and structures without changing the hardware.

4.1 PCI Bridge

High bandwidth of data transfer from FED to the BDN and complex control of the RU required using commercial available fast interface protocols as 64bit 33/66MHz PCI. Transferring the data and control from one to the other bus was possible by developing the multiple PCI Bridges as general part of the control port for the RUM and RUIO. There are two versions of the PCI Bridge – three and four bridges in one component, implemented respectively in RUIO and RUM. Basic structure of the four PCI Bridges is shown on Fig.6.

4.2 Memory Management Unit

Memory Management Unit is receiving the event header from input and output PCI interfaces. Each header contains Event-ID number, word-count, first memory block address and status. MMU is the device that keeps internal event data memory structure organised in blocks using event table and pointers. MMU also contains algorithm for freeing locations inside the data memory according to the transferred event out from the RUM. For these functions MMU is using SRAM and has a direct connection also to the Memory Controller on board. Block diagram of the MMU is shown on Fig.7.

4.3 Memory Controller

Memory Controller is device that control directly event data memory by generating the physical address to the memory according to the information receiving from MMU or PCI interface units. MC also contains internal arbiter for read/write access from the PCI ports, read and write address counters and control logic for the FIFO’s. Block diagram of MC is shown on Fig.8.

4.4 Readout Unit Control

Readout Unit Control is done basically by device after the fourth PCI bus in the RUM and RUIO designs. There are two different schemes of implementations. First of them is using commercial available I/O processor as IOP480 from PLX Corp. with supporting around the processor components. Second is to use programmable logic devices and replace with simple protocol the control of the RUM. The first solution is already successfully implemented in RUIO prototype. Experience with IOP and I2O protocol will be accumulated due to the prototype developing. Block diagram of the Readout Unit Control implementations is shown on Fig.9.
Fig.9. Readout Unit Control implementations

5. RU CONFIGURATIONS

As was written above the Readout unit is a set of two physical PCI devices RUM and RUIO connected together. Complexity of each of those devices provides the possibility of building RU by choosing one RUM and two RUIO, or one RUM and one RUIO devices. First configuration is shown on Fig.10, when the functions of RUI and RUO are implemented inside the RUM using IOP processor.

Fig.10. RUM and two RUIO

The second configuration is shown on Fig.11, where one RUM and only one RUIO are using. The functions of RUI and RUO are realised by RUIO devices. For control and data are using two different PCI busses.

Fig.11. RUM and one RUIO

6. CONCLUSIONS

The RU prototype follow more closely the needs of CMS Data Acquisition and can be considered as a stand alone firmware DAQ that can be used in test beam, in mini data acquisition systems and as a fundamental element for testing switched systems in realistic conditions. Using FPGA components latest generation is a flexible way to implement new and improve the existing functions of the RU unit. Future available on the market 64bit at 66MHz PCI machines (PC, Workstations, etc.) and PCI data link devices are base for implementing RU in real DAQ systems. The time scale for evaluation of the RU prototypes is about one year.

7. REFERENCES

1. CMS TriDAS Computing Controls, CMS Document 1997-090, CERN.
2. PCI Local Bus Specification Revision 2.0, April 30, 1993.
Readout Unit for the LHCb experiment

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Abstract
The Readout Unit (RU) for the LHCb data acquisition and trigger system is a programmable eventbuilder interface, taking input from up to four Gbit/s data link receivers, and outputting to single PCI nodes of a readout network. It has been conceived as a versatile and programmable prototype module that uses the CERN S-Link as link-receiver protocol [1], 9U- IEEE960 power and mechanics, and PCI bus protocols for the readout network. The FPGA-based receiver stage merges incoming event-fragments into subevent blocks that are stored in an intermediate subevent buffer. Subevents are forwarded by an FPGA-based eventbuilder interface logic that is directly connected via the PCI bus with the protocols of the readout network. An embedded I/O processor provides remote control over all input and output functionalities, via a 100Mbit/s LAN connection to the experiment control system.

1. PURPOSE OF THE READOUT UNIT
The Readout Unit (RU) is being developed to fulfil the functionality of the first stage of the LHCb data acquisition system [2] [Figure 1].

![Figure 1: LHCb DAQ system](image1)

The overview below [Figure 2] shows it's top level architecture between S-Link receiver inputs and PCI outputs. The role of the merger is to collect event-fragments from the input FiFos and store them in the subevent buffer. The subevent builder assembles these into subevent blocks. For complete event building, subevents are transferred via the subevent builder interface to a PCI bus compliant readout network.

![Figure 2: architecture of Readout Unit](image2)

1.1 Bandwidth requirements for LHCb
The nominal requirements for a Readout Unit are given by the LHCb level-1 trigger rate and event sizes per input link of the RU. The detector with the highest occupancy will generate max. 1 kByte per event including some formatting overhead. With four input links and a 40 kHz level-1 rate, this corresponds to a 160 Mbyte/s sustained throughput requirement for the RU. The requirements for the individual parts of the RU are summarised in [Table 1] below. Each link input requires 40 Mbyte/s input bandwidth, the output bandwidth is chosen 264 Mbyte/s by using 64-bit 33-MHz PCI (528 Mbytes/s for 66 MHz).

<table>
<thead>
<tr>
<th>PCI output</th>
<th>64bit@33MHz (66 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subevent Buffer</td>
<td>1 Mbyte</td>
</tr>
<tr>
<td>Peak input per link</td>
<td>40 Mbyte/s</td>
</tr>
<tr>
<td>Integral BW</td>
<td>160 Mbyte/s</td>
</tr>
</tbody>
</table>

Table 1: Bandwidth Requirements

2. THE RU MODULE
The Readout Unit is a 9U motherboard with modular I/O connections for data and control [Figure 3]. The input stage receives data fragments from front-end links via four S-Link receivers. Input FiFos are used to derandomize input data and to convert the output to a 64-bit format. The subevent merger (SEM) logic scans the FiFos, which share a 64 bit very high bandwidth bus, and writes their data to the subevent buffer (SEB), together with a directory entry. The output stage is the eventbuilder interface (EBI) which combines the data from the SEB into subevents which are then transmitted...
via the PCI bus to the readout network (RN). The monitoring and control unit (MCU) provides remote control and access to data via a LAN connection. An auxiliary PCI slot allows for extended applications of the RU, such as the use of a Timing and Controls (TTC) receiver card [3].

LHCb eventbuilding protocols can be implemented using PCI either for message passing or for memory-like access.

### 2.3 The Monitoring and Control Unit (MCU)

A commercial plug-in processor card [4] is used for remote monitoring and control via a LAN connection to the Experiment Control System (ECS). Tasks of the MCU include monitoring the SEB buffer status, error handling and reporting and remote control of the operating parameters of the RU. Apart from this, the MCU can also initialise the PCI bus, re-load FPGA configuration bitmaps, access status registers inside the FPGAs, implement high-level data transport protocols, or emulate RU functions before implementing them in FPGA hardware. The MCU firmware will be developed using a cross-compiler (for Intel i960) on host PCs with calls to low level monitor services.

### 2.4 The Front-end Link Receivers (FLR)

For the RU prototype we opted for the use of the 32 bit S-Link protocols of the ATLAS experiment at the link receiver side. The use of S-link mezzanine cards allows for a free choice of either using short (copper) or long (fiber) technologies for the input links. At the S-link connector the same 32 bit framing protocol is available for all link technologies.

### 2.5 Network Interface (NI)

This is a network-specific PCI card which adapts a given readout network technology to the PCI output bus of the RU. Since standard PCI cards are mechanically not compatible with 9U crate mechanics, a final version of the RU requires that this card is either available as PMC mezzanine or that its logic can be placed on the RU motherboard. An example of a PMC network interface can be found in [5]. For tests with standard PCI cards, a simple PCI-PMC adapter card may be used.

### 3. READOUT PROTOCOLS

The transfer of data between the RU’s and the 2/3rd level CPU farm computers requires a transfer protocol between the RU’s EBI logic and the 2nd/3rd level farm CPU’s [6].

The full readout protocol of LHCb is meant to be simple: a continuous, write-only data transfer is maintained from source to destinations. The phased readout protocol only transfers subevents which have been pre-selected by the 2nd level decision. This drastically reduces the amount of data to be transferred over the network, however its implementation, i.e. selective readout, is complex. Both readout protocols are to be studied with the Readout Unit prototypes.

---

1 Mbyte is the nominal SEB capacity for the RU prototype.
3.1 Full readout

Under the full readout protocol, the EBI output logic autonomously writes subevents via the PCI bus and the readout network (RN) to a destination CPU. The transmission via the RN can be either a memory mapped PCI-to-PCI transfer between sources and destinations (transparent), or a DMA between the SEB and a destination buffer (buffered I/O). The choice depends also on the possibilities of the RN.

Subevents are chained event-blocks in the SEB, with pointers stored in the SEB directory. Due to the use of circular buffers there is no need to implement a garbage collection mechanism. Buffer overflow in the SEB is prohibited via a Xon/Xoff return signal, generated by the input stage of the SEB logic.

3.2 Phased readout

Under this protocol, only small subsets of events are transmitted for making a 2nd level decision whilst the rest of the event is queued in the SEB. Since the remainder of the data is only transferred after a positive level-2 decision, the bandwidth across the RN network can be considerably reduced: non-accepted events are discarded from the SEB. For this protocol, the EBI logic needs to understand a set of messages like selective accept and reject from the RN.

4. SUBEVENT BUILDING

Subevents are built by the EBI output logic from the event-fragments stored in the subevent buffer. The event-data fragments stored in the SEB are identified by their event numbers which is used by the EBI output stage to build and frame subevents. The process of event building from a buffer is very tolerant for arrival spreads and allows in particular receiving several fragments of the same ID via the same link.

4.1 Input Data formats

A very simple input format convention is adopted for the Readout Unit prototype [Figure 4]. The framing overhead is minimal and consists of two 32-bit words in the header and one in the trailer. The start and end of the input block is identified via a hardware flag bit. In order to ease subevent building, the event identifier is contained in the header word.

The block size and the error status are contained in the trailer word. Four LSB bits are used by S-link.

3.2 Subevent framing

A recursive and simple way of generating subevent blocks has been adopted. The data blocks of event frames belonging to the same event number are concatenated behind the same header word as the input frames [Figure 5]. This requires that data blocks have their own consistent format which is transparent to the RU. The size and status fields for subevents are recalculated and appended as trailer word. An error block is inserted between the last data block and the trailer only in case of errors. The latter is indicated in the status word.

5. TECHNICAL IMPLEMENTATION

The RU module’s technical layout is shown is shown below [Figure 6].

5.1 Internal bus connections

At the input side, the 32 bit S-Link words are converted via interleaved 32 bit FiFos to a 64 bit SEB bus.
which is read out by the SEM FPGA with a clock rate of 50 MHz to provide a raw bandwidth of 400 Mbyte/s.

Input data are stored in a 64-bit-wide dual port memory interfaced between the SEM input and the EBI output stage. The latter consists of two parallel FPGAs (EBI and AUX) which share the 64-bit SEB bus at their inputs and the 64-bit PCI bus at their outputs. The reason for the parallel use of two FPGA's, apart from lower cost of the FPGAs is the increased PCI bandwidth which can be achieved with two tandem PCI masters. The MCU is connected to the 64-bit PCI bus and its 32-bit memory bus is connected to the EBI FPGA. The latter allows that the MCU can map the SEB into its local memory space. A dedicated, 8-bit-wide i960 bus interconnects all FPGAs with the MCU. This allows for FPGA configuration and access to status registers via the MCU, and further via a remotely connected server. The MCU provides a secondary, 32-bit PCI port which may be used for auxiliary PCI cards.

5.2 Motherboard layout

The RU prototype is implemented as 9U motherboard which only takes power from an IEEE-960 crate mechanics. All 6 mezzanines for data input (4) and for data output (2) are located on either front- or backpanel of the motherboard. A preview on the module (currently under design) is shown below [Figure 7].

5.3 Board design tools

The schematic capture was completed using Cadence Concept. The 12-layer board is designed using Cadence Allegro.

For critical buses design like for the 64 bit FiFo bus and the 66-MHz PCI bus, a signal integrity study using Cadence SpectraQuest and IBIS models from different vendors was carried out. The results of this study also influenced the placement of components in the PCB [Figure 8].

5.4 FPGA technology

Lucent Technologies’ ORCA 3TP12 device [7] has been chosen for both FPGAs (EBI and AUX) in the output stage. This device has a 64-bit 66-MHz embedded master/target PCI hard core interface, as well as an 8-bit embedded hard core interface to i960 processors. The latter interfaces directly to the MCU’s local bus and allows for remote configuration, program readback and access to internal FPGA. Approximately 35k equivalent logic gates are available for the EBI logic.

The SEM FPGA in the input stage (ORCA 3T55) is also a member of Lucent Technologies’ 3T family. The differences with the previous device are the available user logic size (up to 55k equivalent gates). This device has also an i960 interface but no PCI core [8].

5.5 FPGA development tools

Like for previous design projects we use a VHDL design methodology for ORCA FPGAs from Lucent Technologies. After a VHDL simulation with Cadence LEAPFROG, the VHDL output is synthesised by Exemplar’s LEONARDO to generate an EDIF output which is used by Lucent’s Foundry tools to place and route all required FPGA resources. The bitstream output is programmed into a Flash Eprom, which during power-up transfers its contents to all FPGAs in the Readout Unit.

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2 In a future RU version we expect that a single FPGA can be used.
6. STATUS AND OUTLOOK

The Readout Unit project is a joint activity of the CERN EP-ED electronics group and the LHCb experiment. A series of meetings [9] have led to the design decisions for the first prototypes to be built in 1999. Since technology choices for input links, readout network and control system are pending, we have opted for a modular approach using S-Link mezzanines for the link input, PCI for the readout network and T-base 100 LAN technology for the control system.

This module is meant to be reproduced in small quantity and serves mainly the purpose for developing the final RU concept. A second-generation module will be started when technology and protocol choices have been taken.

REFERENCES

1. For information on S-Link, see the Slink homepage http://www.cern.ch/HSI/S-Link/
2. LHCb collaboration, LHCb Technical Proposal, CERN/LHCC 98-4, Chapter 13
3. Estudio y Desarrollo de Nuevos Sistemas de Temporización, Trigger y Control para los Futuros Detectores de LHC del CERN, doctoral thesis on the TTCsr mezzanine Jorge Ferrer, CERN / Politechnical University of Valencia (to appear in English)
4. PXECORE embedded CPU mezzanine module from CompuLab. See http://www.compulab.co.il
9. For history and design documents, see the Readout Unit home page. http://nicewww.cern.ch/~hmuller/lhcb.htm
A PMC BASED ADC CARD FOR CMS TRACKER READOUT

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Abstract

The tracking system of the CMS detector at the LHC employs Front End Driver (FED) cards to digitise, buffer and sparsify analogue data arriving via optical links from on detector pipeline chips.

This paper describes a prototype version of the FED based upon the popular commercial PCI bus Mezzanine Card (PMC) form factor. The FED-PMC consists of an 8 channel, 9 bit ADC, card, providing a 1 MByte data buffer and operating at the LHC design frequency of 40 MHz. The core of the card is a re-programmable FPGA which allows the functionality of the card to be conveniently modified. The card is supplied with a comprehensive library of C routines.

The PMC form factor allows the card to be plugged onto a wide variety of processor carrier boards and even directly into PCI based PCs. The flexibility of the FPGA based design permits the card to be used in a variety of ADC based applications.

1. INTRODUCTION

The CMS experiment [1] is due to begin operating at CERN’s Large Hadron Collider facility (LHC) in 2005. A key component of the CMS detector is the tracker [2] which is designed to provide robust particle tracking and detailed vertex reconstruction within a strong magnetic field in the high luminosity environment of the LHC. The tracker is implemented using three technologies: Silicon Strips, Micro Strip Gas Chambers (MSGC) and a Pixel Vertex detector. The silicon and MSGC detectors are collectively known as the microstrip tracker.

The microstrip tracker readout system consists of approximately 1.2x10^7 detector channels and, at expected track occupancies, will generate over 70% of the final data volume at CMS. The tracker readout system is clocked at the LHC bunch crossing rate of 40 MHz and is designed to operate at Level 1 trigger rates of up to 100 kHz. Microstrips are read out using analogue electronics. A schematic of the proposed system is shown in Figure 1.

Microstrip signals are amplified and stored in analogue pipeline memory chips (APV) located on the detector [3], [4]. After some elementary signal processing and multiplexing the signals are transferred to the counting room via analogue optical links.

In the counting room the analogue optical data is converted back to electrical and digitised on Front End Driver (FED) cards. Each ADC channel processes data serially from a total of 256 microstrips (constituting an APV frame). The FEDs provide digital signal processing, including cluster finding, before storing the data in local memory buffers until required by the higher levels of the central data acquisition system. Each FED receives information from the central Timing and Trigger Controls system (TTC) via a TTCrx ASIC [5].

2. FED-PMC PROTOTYPE

2.1 Prototyping Requirements

The essential functions of the FED have been established using a 9U VME prototype [6]. However, as the card resides in the counting room and does not constrain the design of front-end components, the final implementation will be delayed until nearer to the LHC start up. Meanwhile, in order to fulfil the prototyping needs of the large and diversified tracker community, a FED prototype has been produced as a PCI Mezzanine Card (PMC) [7].

The prototype card (Figure 2) will also enable evaluation of the key components of the final FED such as commercial ADCs, digital signal processing elements and the higher level DAQ interface.

The choice of the PMC format, which interfaces via the popular PCI bus, allows the FED prototype to be

1 The microstrip tracker control system is outside the scope of this paper.
used on a wide variety of commercial off-the-shelf VME carrier boards. The FED-PMC is thereby able to benefit naturally from the constant improvement in carrier processing performance. With an appropriate interface card it can also be plugged directly on to the PCI bus of a PC or workstation.

The PMC implementation provides a cost effective solution for instrumenting detectors in test beam and laboratory setups. Software drivers are provided in order to hide the complexity of the card’s functionality and enable users to install and operate FED-PMC's in a “plug and play” fashion.

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Figure 2: Photograph showing both sides of the FED-PMC (Mk2 version).

### 2.2 Functionality

A diagram indicating the basic functional units of the FED-PMC is shown in Figure 3. The card has 8 electrical input channels which can be configured at assembly for either differential or single-ended inputs. Each channel utilises commercial ADCs [8] and is capable of digitising 9 bits at clock speeds from between 2 and 40 MHz.

The data is stored in contiguous blocks inside a Dual Ported Memory (DPM). The DPM is implemented as 4 x 64K x 18 bit synchronous memories [9] and is capable of buffering the raw data from approximately 250 APV frames. The data is read out (can be simultaneous with ADC capture) over the PCI bus via a 32 bit, 33 MHz commercial bridge interface [10]. A FIFO provides storage for event buffer pointers and event counter information.

A CPLD implements the clock and trigger control. Trigger and clock (LVDS) signals can be brought in via the front panel or optionally through the PCI backplane. The fine adjustment of the clock phase with respect to the data can be set under software control in order to obtain the optimum sampling point at the ADC. For testing purposes triggers can be generated internally by software and the card can run from the internal PCI clock (33 MHz).

Figure 3: Block diagram of the FED-PMC.

### 2.3 Firmware

At the heart of the FED-PMC design is an FPGA [11]. This permits a large fraction of the card’s functionality to be re-configurable in firmware and thereby maintains a flexible hardware architecture.

The basic firmware design configures the FED-PMC to provide raw data capture in a “digital scope” mode. VHDL blocks implement the following functions:

- Local data and address bus (slave)
- DPM interface
- Event buffer management
- FIFO and counters control
- Register interface
- Test functions

The flexibility of the FPGA based approach is demonstrated by the number of extensions to this core design which are in various stages of development for the microstrip tracker readout:

- APV Auto-Synchronisation mode : permits ADC data capture to be triggered on recognition of a header word which accompanies the APV data stream itself rather than on the external trigger.
- Data Generator mode : for exercising the interface to the higher levels of the DAQ using test patterns at high rate, (requires on-board DMA).
- Hit Finding mode : implementing pedestal and common mode subtraction with basic cluster finding.

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2 The ADCs are 10 bit, the LSB is not read out.

3 It should be noted that the original specification of the FED-PMC provided by the tracker detector groups did not require hit finding capabilities.
The precise algorithms employed depend on the type of microstrip detector being readout.

Core VHDL libraries are provided for those users wishing to develop their own FPGA designs.

During normal operation the FPGA is loaded on power up under software control from an on-board Flash memory. The memory can be reloaded with a new FPGA design via a local area network using the software tools provided. This permits FPGA design updates to be distributed from a central source and reloaded in situ. The FPGA can also be loaded directly from the network for testing of new designs without overwriting the Flash memory contents.

2.4 Software

The FPGA-based open hardware architecture, described in the previous section, is complemented by the design of the software architecture which forms an integral part of the delivered FED-PMC package. The software design follows a layered approach from the lowest-level drivers right up to a full graphical user interface.

A layered design (Figure 4) has several advantages for the end user:

- It abstracts the details of the hardware implementation. At the simplest level a handful of routine calls are required for card configuration and readout operation.
- It removes the need to rewrite code which has already been debugged in parallel with the hardware.
- It permits upgrades to the firmware to be transparently implemented. The firmware contains a version identifier permitting the software to recognise the design currently installed and operate accordingly.

![Layered Software Design](image)

Figure 4: Layered Software Design.

4 If the end user chooses to implement their own firmware design they must of course produce the necessary software to operate it.

The software is implemented by a comprehensive library of (open source) C routines. A high-level graphical user interface implemented using LabView [12] has also been developed for the test bench at RAL.

2.5 Operating Environments

The FED-PMC has so far been operated in the following environments:

- CES RIO2 PowerPC Single Board Computer (SBC) running with either LynxOS or VxWorks operating systems.
- Motorola MVME2604 PowerPC SBC running LynxOS.
- VMETRO MIDAS-20 PMC carrier.

By using appropriate extender cards up to 6 FED-PMCs, providing a total of 48 ADC channels, can be operated from one SBC.

Each FED-PMC occupies a total of just over 1 MByte of PCI memory space.

3. FED-PMC STATUS

3.1 CMS Tracker Beam Tests

The first FED-PMC's (Mk1) were produced during summer 1998 and commissioned during tracker test beam running at the CERN PS in October 1998. A second version (Mk2) of the card was used extensively during further beam tests at CERN during May and August 1999. Several FED-PMC's were integrated into the test beam DAQ system in a matter of a few hours and operated successfully, and without further expert intervention, throughout the data taking period.

A total of 20 Mk2 cards have recently been distributed to the CMS microstrip tracker community. The card will also be used for prototyping tests of the CMS Pixel Vertex detector.

3.2 Applications outside CMS

The CMS FED-PMC is also being employed by groups working on readout prototypes for the RICH and tracker detectors of the LHCb experiment [13].

The suitability of the FED-PMC for a medical imaging application is currently under study at Imperial College London, UK.

4. ADDITIONAL INFORMATION

The software tools and source libraries together with further information on the FED-PMC can be found at http://hepnts1.rl.ac.uk/CMS_fed/Default.htm.

5. CONCLUSIONS

The challenge of providing a flexible, cost effective and easy to use ADC card for the prototyping requirements of the CMS tracker community has been met by the employment of the following standards:
- Hardware: PMC (PCI bus) running on commercial carriers
- Firmware: FPGA with VHDL libraries
- Software: C drivers with high level user interface

The FED-PMC has been used successfully for CMS microstrip tracker detector evaluation studies during beam tests at CERN.

The versatility of the design has been demonstrated by the employment of the FED-PMC in applications outside of CMS.

6. ACKNOWLEDGMENTS

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7. REFERENCES

[12] LabView manufactured by National Instruments, Inc., 6504 Bridge Point Parkway, Austin, TX 78730-5039, USA.
TESTABILITY ISSUES IN THE CMS ECAL UPPER-LEVEL READOUT AND TRIGGER SYSTEM

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Abstract
This contribution describes the work carried out by the INESC team, in collaboration with LIP, in order to increase testability features on the CMS ECAL upper-level readout and trigger system. To accomplish this purpose, (1) extension of boundary scan test of electronic boards to system level, (2) introduction of self test in ASICs, (3) defect-oriented test effectiveness evaluation and (4) system-level modeling and simulation have been addressed and are reported. This work is consistent with the one carried out by Politecnico di Torino and CAEN in collaboration with CERN, in order to improve testability and reliability of the upper-level readout and trigger system.

1. INTRODUCTION
The CMS ECAL upper-level readout and trigger system [1] is composed of about one thousand boards installed in sixty 9-U VME crates. The complexity of the design and implementation of such a system requires the use of Design for Testability Techniques (DFT), in order to achieve a testable system during all the phases of its lifetime.

In collaboration with LIP, INESC has been evaluating the implementation of the ANSI IEEE 1149.1 Standard at different modelling levels (component, MCM, board, system), the inclusion of self-test techniques and in-system test procedures, as well as the specification of the system with a high level modelling technique.

Based on this study, a proposal of extending the use of the IEEE 1149.1 standard to system level emerged. To accomplish this goal, a boundary scan controller board is being designed. The architecture and the main features of this board are described in section 2.

The introduction of Built-In Self Test (BIST) in components, namely ASICs, and test effectiveness experiments are reported in section 3. A BISTed version of the synchronisation Tx/Rx IC, under development by TECMIC, is presented. Section 4 introduces the concepts behind a high level modelling technique used to specify the system. Finally, section 5 summarises the main conclusions.

2. APPLICATION OF BOUNDARY SCAN AT SYSTEM LEVEL
The upper-level readout and trigger system is controlled, during the normal operation of the acquisition system, by a controller board housed in each crate. The main objective of this task is to develop a VME based JTAG controller (hardware/software) enabling the application of a boundary scan test to the sub-system crate during idle time or when a maintenance operation is required.

This task has two components:
A. Development of a boundary scan test module – boundary scan controller board - being the interface between the sub-system controller and the VME dedicated lines to implement the IEEE 1149.1 test bus.
B. Development of the software for downloading the test and for getting back to the controller the test results.

2.1 Architecture of the Boundary Scan Test System
There are two main approaches to interconnect the test bus of a system composed by several IEEE 1149.1 compatible boards: the ring configuration and the star configuration. The ring configuration, figure 1a), uses the same control signals (TMS and TCK) for all boards and a single scan path in series with all the boards (TDI/TDO). The star configuration, figure 1b), uses also the same control signals for each board and a common TDI/TDO. Both configurations require the same amount of information to control and test the entire system. However, the ring configuration has a scan chain longer than the star configuration. This configuration has some advantages over the first one, requiring less test clock periods to get the test response. Moreover, if one board is removed or is faulty, the controller will still be able to
test the system. Hence, the star approach was selected for implementation.

Figure 1 – a) Ring configuration; b) Star configuration.

The star configuration requires the use of a special device, called *Scan Bridge* [2], to interface each board with the test bus. This device, developed by National Semiconductor, has one 1149.1 test port connected to the backplane test lines and three 1149.1 secondary test ports connected to a maximum of three local scan chains. Addressing one of these circuits in a system allows testing a particular board in the system. Unlike other approaches (for example, the MTM bus standard), the *Scan Bridge* provides an addressing scheme using a 1149.1 compatible protocol.

### 2.2 Boundary Scan Controller Board

The Boundary Scan Controller Board under design is a VME bus slave board with dimension 6U. This board will interface the VME bus using the P1/J1 and P2/J2 connectors, which include the test and maintenance signals [3], namely the MCLK (Module Clock) equivalent to the signal TCK of the IEEE 1149.1 standard, MCTL (Module Control) equivalent to TMS, MMD (Module Data) equivalent to the signal TDI, MSD (Module Slave Data) equivalent to the signal TDO and MPR - bus pause request (TRST#). These signals are used to apply the boundary scan test at system level. The boundary scan controller board receives VME bus commands, generated by the master VME board, to download and configure the test procedure, and drives the 1149.1 test signals in order to apply a boundary scan test to a single board inserted in the VME backplane.

As depicted in figure 2, the controller board contains the following functional blocks:

**VMEbus Interface Circuits** - These circuits, used to interface with the VME bus, implement the VME64 bus protocol to transfer data between the master board and the slave board. The loading of the local memory and the configuration of the local registers are done using the VME64 data transfer protocol.

**Local Test Controller (LTC)** - This circuit, implemented by a programmable logic device (PLD from ALTERA), is responsible for controlling the functionality of the test board. This circuit is divided in four sub-modules:

- **Test Control State Machine** - State machine that controls the state of the board and the execution of the tests.
- **VME Circuits Configuration** - Module responsible for configuring the operation mode of the VME bus interface circuits.
- **Data Transfer Controller** - Module that manages the data transfer between the local memory, the boundary-scan controller (PSC100F) and the LTC itself.
- **Status/Instruction/Configuration Registers** - Registers accessed by the VME bus master board, that allow to start and to stop the running test, and to monitor the current state of the test.

**Local Memory** - This memory is divided into two parts. One, stores the serial output test vectors (bit patterns for TDO and TMS) and the input vectors captured during the test execution (TDI bit patterns). The second part contains the state of the TRST# and other control data concerning the test flow.

Figure 2 – Block diagram of the boundary scan controller board.
**Boundary Scan Controller (PSC100F)** - This circuit, developed by National Semiconductor [4], is designed for interfacing a parallel processor bus with the serial boundary scan test bus. The circuit is divided in a serial interface, that includes a buffer for each of the test signals (TDO, TDI and TMS), and in a parallel interface accessed by the Local Test Controller.

**Test Clock Generator** - This programmable clock generates the test frequency applied to the TCK test signal. The generator is programmed by the LTC.

### 2.3 Boundary Scan Controller Software

Tests are generated for each board with the TERADYNE’s VICTORY software package [5]. This software is currently in use at CERN and will be re-used when generating the test for each board in the system level configuration. All VICTORY modules generate test vectors in SVF (Serial Vector Format), widely accepted by suppliers and users of boundary-scan test tools. The VICTORY software package includes a toolkit that allows the conversion of SVF code into a truth table containing the logic levels of the five test signals. Software to be developed will transform that truth table into a format suitable to download into the Boundary Scan Controller Board. The software is also responsible for configuring the board registers.

The VICTORY software package includes also a diagnostic tool (BSID) that uses the test results to diagnose eventual failures in the system. The Boundary Scan Controller Board software will convert the test results to a format suitable for the diagnostics tool.

### 3. ASIC BIST, QUALITY AND RELIABILITY

A second area of R&D includes the INESC support for test and reliability of key system components, namely a synchronization circuit, the Sync Tx/Rx [6]. A FPGA prototype of the circuit was under development by TECMIC, and must include testability features, namely BoundaryScan (BS) [7] and Built In Self Test (BIST). The final version of the IC is to be implemented using ASIC (Application-Specific IC) technologies; hence, the envisaged solution should apply to both layout styles. Here, we present some relevant aspects of the proposed solution [8] (Fig. 3).

BIST, combined with BoundaryScan, allows the IC self-test without the need to load complex data patterns and without the need to analyze individual circuit output. In BIST operation mode, the circuit automatically generates test patterns (through Linear Feedback Shift Registers (LFSRs)) and compresses its outputs. These compressed outputs, referred as signatures, are serially shifted out when the test ends and then compared with the fault-free circuit signature. BIST capability is relevant for production and lifetime testing, especially for complex, not easily accessible system modules, like the ones to be expected in the CMS electronics.

The proposed 1149.1 BS [7] architecture comprises:
- loop 0 - a boundary-scan register loop made of Boundary Scan Cells (BSCs),
- loop 1 - a test register (TR) loop with
  - two LFSRs and
  - the Sync Tx/Rx Status Register,
  - Data error counter,
  - Synchronization error counter;
- a TAP (Test Access Port) controller with
  - an instruction register (IR),
  - a bypass register (BP R) and
  - a controller (JTAG [7] state machine);
- a BIST controller
- a LFSR and EDC (Error Detecting Code) encoder

![](image.png)

**Fig. 3 - BISTed version of the Tx_Rx ASIC.**

LFSR1 (Fig. 3) generates the Input Data without the Hamming Code for the BIST session. The EDC Encoder generates the bits with the Hamming code. The Sync_Tx Input Data must be clocked and multiplexed by the BIST Controller, in order to allow normal (transparent) operation or LFSR stimuli injection. LFSR2 is used for signature analysis (SA) of the data stored in the Accumulator during each Read Accumulator cycle of the BIST session. LFSR3 is used for SA of the Sync_Rx Output Data. These LFSRs are transparent in circuit normal operation. Loop 1 must include also the Status Register, Data Error Counter and Sync. Error Counter as part of the signature of the circuit BIST operation.
An interesting feature of the proposed solution has to do with time requirements. The JTAG/IEEE1149.1 specification [2] requires that testing should be performed under control of a test clock TCK, independent of the main system clock. In general, system clocks (Tx and Rx_clock) should be interrupted and test clock TCK applied. However, for this synchronization ASIC, this clock gating has several disadvantages:

- introduction of delays in Tx and Rx_clock,
- important area overhead due to the required clock signal buffering and
- BIST speed limitation to the TCK rate (much smaller than “at speed” operation).

The proposed alternative (not fully compliant with 1149.1), is to fed system clock pins directly to the on chip system logic as they would be during non-test operation of the component. The deviation from the 1149.1 standard is due to BIST other than TCK clock requirements. However, all other BIST interface is kept 1149.1 compatible. Tx_clock must clock LFSR1 and 2; Rx_clock must clock LFSR3. Implementation details, namely for Xilinx™ XC4000 FPGA devices, are given elsewhere [9]. The FPGA prototype realization of the Tx_Rx synchronization IC is currently being carried out by TECMIC. The 40 MHz operation speed has been the main implementation problem in the FPGA technology; nevertheless, the problem can be easily solved in ASIC technologies, like GA (Gate Array) technologies. A standard cell design will be performed by INESC.

A complementary question to test generation and application is product quality and reliability. Product quality is usually measured by the Defect Level [10], defined as the percentage of defective devices that pass successfully the production test and thus are built into the numerous PCBs of the ECAL system. Reliability is a key factor of success for the CMS experiment, as long lifetime and low down-time are system specifications. Both issues are associated with the ability to predict and monitor the impact of physical defects, induced during IC manufacturing or lifetime operation, on IC behaviour.

The INESC QTHS Group [11] has developed a Defect-Oriented (DO) methodology and tools that allow layout dependent physical defect extraction, sampling and simulation, using lobs and VeriDOS tools [12,13]. In order to show the usefulness of the approach for the CMS electronic system, a preliminary experiment was carried out with CAEN using a module of the Level 1 (L1) filter.

The module is the filter tap, comprising a carry save multiplier and adder working at 40 MHz. It has 79 PIs, 54 POs (with registers), and was laid out using a commercial 0.8 µm CMOS technology. The module has 1368 logic gates and uses 21 library cells. A standard ATPG (Automatic Test Pattern Generation) tool generated 108 test vectors that cover 100% single Line Stuck-At (LSA) faults. However, BRI (bridging) and LOP (line-open) realistic fault extraction reveal 14,624 physical defects, likely to occur (the lobs tool computes their probability of occurrence, based on critical area evaluation and defects statistics data). Fault simulation results are shown in Fig. 4. Here, DC stands for Defects Coverage, which is the weighted percentage of defects uncovered by the LSA test set.

<table>
<thead>
<tr>
<th>Fault class</th>
<th>FI (%)</th>
<th>DC (v) (%)</th>
<th>DC (l) (%)</th>
<th>DC (v+l) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRI Y-Y</td>
<td>54.55</td>
<td>98.05</td>
<td>0.93</td>
<td>98.98</td>
</tr>
<tr>
<td>BRI A-B</td>
<td>17.02</td>
<td>98.40</td>
<td>11.60</td>
<td>100.00</td>
</tr>
<tr>
<td>BRI A-Y</td>
<td>7.83</td>
<td>97.22</td>
<td>2.77</td>
<td>100.00</td>
</tr>
<tr>
<td>BRI x-Vdd</td>
<td>4.35</td>
<td>95.22</td>
<td>14.78</td>
<td>100.00</td>
</tr>
<tr>
<td>LOP A-Y</td>
<td>9.65</td>
<td>99.24</td>
<td>0.00</td>
<td>99.24</td>
</tr>
<tr>
<td>LOP Y-Vdd</td>
<td>0.92</td>
<td>100.00</td>
<td>0.00</td>
<td>100.00</td>
</tr>
<tr>
<td>LOP x-Vdd</td>
<td>3.34</td>
<td>97.23</td>
<td>0.00</td>
<td>97.23</td>
</tr>
<tr>
<td>total</td>
<td>100.00</td>
<td>96.57</td>
<td>3.69</td>
<td>96.29</td>
</tr>
</tbody>
</table>

Results clearly show that 100% coverage of LSA faults does not guarantee 100% DC. In fact, using logic (voltage) detection only, DC(v)=95.57%. For certain classes, v-detection is quite low, as it is the case of BRI A-B (between logic gate inputs) and BRI x-Vdd (between gates internal nodes and power supply nodes). Fortunately, the Fault Incidence (FI) of some defects, like BRI x-Vdd, is low. Additionally, current (I_DDQ) detection is shown to be very important, if high DC is required. Additional test effectiveness evaluations will be carried out for the ECAL electronic system.

4. SYSTEM-LEVEL MODELING AND SIMULATION

Another aspect of INESC collaboration on CMS experience is related with the need to assess the coherence and completeness of technical specification against system requirements [1]. To achieve this goal, high level specification models have been used, that not only allow that assessment but also are a vehicle to test communication protocols under different possible architectures [14]. For accomplishing this purpose, a high-level model of the ECAL Front - End and Trigger Primitives Generators has been developed [15]. Beyond functionality, this model has focused on timing constraints and communication requirements among the different modules that constitute the system under consideration. CASE tools, Rational Rose [16] and Objectime [17], have been used for model development.
Objectime allows the animation and simulation of different aspects of system behavior. Additionally, it automatically generates sequence diagrams corresponding to envisioned scenarios of execution. These diagrams are, in fact, graphic representations of protocol dialogs among the different components (objects) that model the system. It is possible to assign time (real or virtual time) to those dialogs, and consequently, to test the correctness of a given protocol against timing requirements. If timing requirements are not fulfilled, the modification of either the protocol or the architecture and the evaluation of the impact of those modifications in system behavior are straightforward.

The use of these models may save considerable development time and efforts since, in most cases, there is not a need to use (and develop) physical prototypes to test different solutions. Models are independent of the implementation; therefore, architecture components or modules can be finally implemented in hardware, software or both.

5. CONCLUSIONS
A Boundary Scan Test Board Controller providing an hierarchical test application compatible with IEEE 1149.1 standard was proposed. It was shown that product quality and reliability, as well as monitoring through its lifetime, can be enhanced by combining 1149.1 (BS) and BIST at component level, and by evaluating, in the IC design environment, test effectiveness. This was carried out with a BISTed version of the Sync Tx/Rx ASIC, under development by TECMIC, and with the evaluation of the ability of a LSA test to uncover physical defects likely to occur in the L1 filter IC, being developed by CAEN.

The complexity of the hardware/software system, under development by a large design team located in different sites, and with very different backgrounds, clearly points out the usefulness of using system level modeling techniques and simulation to monitor the coherence and completeness of the technical specification and to validate its implementation. This has been shown through the development of models of the ECAL Front-End and Trigger Primitives Generators.

6. ACKNOWLEDGEMENTS
The authors would like to thank José Carlos da Silva for his help during the development of the boundary scan controller board.

7. REFERENCES
READOUT DRIVER FOR THE ATLAS LIQUID ARGON CALORIMETERS

W. E. Cleland, for the ATLAS Collaboration

Abstract

The Readout Drive (ROD) for the Liquid Argon calorimeter front-end electronics of the ATLAS detector is described. The ROD receives triggered data from 256 calorimeter cells. It must derive the precise energy and timing of calorimeter signals from discrete samplings of the pulse. In addition, it performs monitoring and formats the digital stream for the succeeding element in the readout chain. Data arrive over two 1.28 Gbit/s fiber optics links at a 100 kHz event rate (25Kbit/event). Principals of the design are discussed, along with simulations of data processing.

1. INTRODUCTION

In ATLAS [1] there are three basic types of liquid argon calorimeters: the em calorimeters (barrel and end-cap), the hadronic end-cap calorimeter and the forward calorimeters. The front-end electronics for all of these calorimeters is essentially identical, the differences being confined to the amplification stage upstream of the shaping amplifier. After shaping, the signals are stored in a switched capacitor array (SCA), and upon receipt of a Level 1 trigger, the samples relevant to the event are digitized on the front-end board (FEB). These digitizations are transmitted to the Readout Driver (ROD) module, whose function is to extract the parameters of interest for each calorimeter cell and pass these data to the Readout Buffer (ROB) module, the first element in the data acquisition chain. A simplified diagram of this part of the readout chain is shown in Figure 1.

![Figure 1: Simplified diagram of the portion of the readout chain involving the ROD.](image)

In the ATLAS FEB, which treats 128 calorimeter channels, the signals are amplified, shaped and then stored as analog levels in the SCA. Upon receipt of a Level 1 trigger signal, a 12-bit ADC digitises the appropriate samples. Three gain scales are employed, requiring three shaper channels and three SCA channels for each calorimeter cell. All samples are digitized on a common gain scale, which is chosen event-by-event by examining the amplitude of the sample closest to the peak of the signal. Each ADC digitises the signals from 8 calorimeter channels, and the results are sent over an optical fiber to the ROD module. The fiber contains data from all 16 ADCs in the FEB; 32 bits (2 bits/ADC) are sent every 25 ns, giving a transmission rate of 1.28 Gbit/s.

2. THE ROD MODULE

2.1 Overview

A single ROD module receives data from two front-end boards, consisting of (typically) 5 samples from 256 channels. The processors in the module calculate energy and timing information from these data, and in most cases, discard the raw data. The ROD also performs monitoring tasks, and during calibration runs, it executes a signal averaging task and sends averaged data to a local processor, which then calculates calibration constants for the channels belonging to that module. The ROD modules will be housed in a Readout Crate, which will in all likelihood will be a 9U VME crate with a dedicated host processor. The ROD system will be a highly specialized distributed computing resource for the ATLAS detector. It will consist of about 800 modules, each of which services up to 256 calorimeter channels. The total computing power of this resource will be approximately $4 \times 10^{15}$ arithmetic operations per second.

2.2 The Basic Algorithm

The most important function of the ROD is to determine the energy $E$ and time $T$ (relative to the nominal bunch crossing timing) from the digitized samples, along with a parameter $Q$ (such as chi-square), which indicates how closely the samples follow the known waveform. Secondary functions include updating histograms of these quantities and performing certain monitoring functions for some small fraction of the events.

A typical waveform of the shaped liquid argon waveform is shown in Figure 2, along with samples spaced by 25 ns. A general technique to estimate $E$ and $T$ in an accurate and computationally efficient manner is that of optimal filtering [2], in which the desired quantity is expressed as a sum of the samples multiplied by predetermined weights. The weights are found by requiring that the standard deviation of the
quantity be minimized while satisfying certain constraints. In our case, where there are two quantities to be determined, the procedure involves simultaneously minimising the uncertainty in both quantities. The expressions are:

\[ E = \sum a_i S_i \]
\[ E \cdot T = \sum b_i S_i, \]

where the sum extends over all of the samples \( S_i \), and where \( a_i \) and \( b_i \) are the weights. From the structure of these formulae, one sees that the error in the amplitude is amplitude independent, whereas the error in the time varies inversely with the amplitude. For this reason it only makes sense to calculate \( T \) only for those channels with \( E \) above some threshold value \( E_{th} \). The quality-of-fit parameter will most likely be a simplified expression for chi-square (i.e., one that ignores correlations between the different terms):

\[ Q = \sum (S_i - E(g_i + \bar{g}, T))^2, \]

in which \( g_i \) is the expected waveform normalized to unity. Since this calculation involves knowing both \( E \) and \( T \), it will also be performed only for the case where \( E \) is above the threshold value. Once \( E, T, \) and \( Q \) are found, the corresponding bins for general histograms of these quantities are calculated and incremented. In addition, if special histograms are required for specific calorimeter cells, which are being monitored, these histograms are also incremented.

Thus the basic algorithm is as follows:

- calculate \( E \) for all channels
- if \( E > E_{th} \), calculate \( T \) and \( Q \)
- update general histograms
- calculate quantities for monitoring specific channels

In simulation, these steps have been implemented for the C6202 DSP, and execution times for each stage of the algorithm are given in Section 5 below.

2.3 Design Considerations

The maximum Level 1 trigger rate for ATLAS is currently specified as 75 kHz, but an upgrade to 100 KHz is considered a strong possibility, and hence we use the latter figure as a design parameter for the ROD. Since the processing time per event depends on the fraction of cells with energy above the threshold, there can be considerable fluctuations from module to module. For this reason, a derandomizing buffer will be required to reduce the system dead time. One model of the process indicates that in order to keep the dead time below 0.5%, it is necessary to buffer 7 events [3]. We plan for each ROD to serve two FEBs, or 256 calorimeter channels. With a Level 1 trigger rate of 100 KHz, the average processing time per event cannot exceed 10 microseconds. Fortunately only a small fraction of the cells contain significant energy deposits in each event, which reduces considerably the computing power required. As mentioned above, the energy is calculated for each channel, but the time value is computed only for events with energy significantly above the noise, since it is only for these channels that the measurement is meaningful.

Given the design criteria listed above, there are several possible approaches to the ROD design. One could imagine using a multiply-accumulate chip, which is optimized to perform the calculation we require. Or one can even imagine designing and building a special-purpose ASIC to carry out the task. Our preference, however, is to evaluate solutions using programmable, commercially available processors which can perform our algorithm efficiently but have limited general computing capability. A natural choice is the Digital Signal Processor (DSP), a device whose technology is advancing at a rapid pace. We plan to study such devices in detail to ascertain if they are able to perform the task in the required time before examining more ambitious solutions. Likewise, we plan to use off-the-shelf components for all ancillary elements in the ROD, in order to minimise design effort.

2.4 Integer vs. Floating Point DSP

Since we are dealing with quantities which cover many orders of magnitude in size (\( E \), for example can range from tens of MeV to several TeV), it is both natural and convenient to use floating point DSPs. However, a
detailed investigation of the system of digitization we plan to use (12 bit ADC operating on 3 gain scales) indicate that integer DSPs, which are in general both faster and cheaper, are also adequate in this case. As long as 16-bit constants are used in the calculation, the effects of rounding in the determination of both the \( E \) and \( T \) are completely dominated by ADC quantization. The division of \( E \times T \) by \( E \) to obtain \( T \) is an inconvenience of course, but this can be handled to adequate accuracy by table lookup. Thus we plan to investigate both integer and floating point DSPs for possible use in the ROD.

3. ROD DEMONSTRATOR PROJECT

3.1 Purpose and Scope

In order to demonstrate the capability of candidate DSPs and to understand more clearly the design problems of the ROD, ATLAS has decided to pursue a ROD Demonstrator Project. The project involves the construction of a motherboard in the 9U VME64x format, into which can be plugged up to four daughterboard processing units (PUs). These processing units will contain one or more DSPs and will be used to process calorimeter data, either fed in from an artificial source or from a calorimeter module running in the test beam. The plan calls for implementing the FEB-ROD-ROB chain, so that all of the required functionality can be tested.

3.2 Hardware

The ROD Demonstrator Board is a VME64x 9U board with a custom P3 backplane. It accepts up to four Programming Units, which may be of different types. Input data may be supplied to the board from up to two FEBs or through the VME backplane. An input is also provided for the timing and trigger information (TTC) in the format that will be used in ATLAS. Output can be to a ROB module or through the VME backplane. In Figure 3 a schematic diagram of the board is shown.

The Processing Unit (PU) is a small (85x185 mm) daughterboard containing one or more DSPs plus any external memory required, input and output buffers, and an interface to the motherboard. The tasks performed by the PUs are expected to be very similar to the tasks required of the ROD in ATLAS. Currently, two PUs are being designed, one based on a floating point DSP (the SHARC of Analog Devices) and the other based on an integer DSP (the C6202 of Texas Instruments). As newer DSPs, which look promising, become available, we expect to add them to the project.

---

**Figure 3:** Schematic diagram of the ROD Demonstrator board.
4. A DESIGN EXAMPLE

4.1 Motivation

In order to illustrate the type of studies that are needed to qualify a DSP for adoption for the ROD, we discuss a concrete example in some detail. For this we choose the design of the PU based on the Texas Instruments C6202 DSP. It is not unlikely that another DSP will eventually be used, given the time scale for the ATLAS experiment, which begins in 2005.

4.2 The TI C6202 DSP

The C6202 is an integer processor with many of the features that are required by the ATLAS ROD. It can operate at clock speeds up to 250 MHz and has eight independent functional units (6 ALUs and 2 16-bit multipliers), permitting it to execute eight 32-bit instructions per cycle. The internal 128 Kilobyte data memory is somewhat limited for our purposes, since we need to (a) buffer the input data, (b) carry out calculations, and (c) store histograms, so we plan to augment it with an external dual-port memory. The unit has both an external memory interface and an expansion bus, which offers a convenient interface to an FPGA.

4.3 Design Sketch of the Processing Unit

![Simplified schematic diagram of the Processing Unit based on the Texas Instruments C6202 DSP. The items shown in dashed boxes are external to the Processing Unit. The interface to the VME system is not shown.](image)

In Fig. 3 we show a block diagram of the processing unit. The data from the FEB and the TTC are brought in on the left, where they enter an FPGA. This device performs certain routine checks on the input data and transfers them into a fast dual-port memory, which is connected to the external memory bus of the DSP. This configuration permits the data to be processed in the DSP without performing a transfer to its internal memory.

4.4 Ancillary Circuitry

There are four logical units in the Processing Unit in addition to the DSP: (1) Input FPGA, (2) Dual-port Memory, (3) Output FPGA, and (4) FIFO. The Input FPGA receives input data from both the FEB and the TTC (Trigger, Timing and Control) modules. The former contains the digitized data from the calorimeter whereas the latter contains information about the trigger (bunch crossing, trigger type, etc.). The two types of data are combined into one record by the FPGA, which also performs parity checks, and stored in the dual-port memory (the input buffer) until it is processed by the DSP. Once the DSP finishes the processing of the event, the results are written to the output FPGA, which formats the output data stream and puts it into the FIFO, which is the output buffer memory for the ROD. Because this unit will be used in a test situation, where there may be large fluctuations in event size, the input and output buffers are larger (corresponding to about 100 events of average size) than will probably be required for ATLAS.

5. QUANTITATIVE STUDIES

5.1 Benchmark Code

We have developed a set of tasks which each of the DSPs should perform in order to be able to make comparisons between them and also establish their viability as candidates for the final ROD system. This code does not include all of the tasks that will be performed by the DSPs in ATLAS, only the most time-critical ones. First, the event header is checked for errors in data format or parity. Then the basic operations performed are:

- check event header
- read five input samples and gain scale
- fetch weights
- calculate $E$
- if $E > E_{th}$, calculate $T$ and $Q$

The above steps are performed for each channel assigned to the DSP. In our current model of the ROD, four DSPs are used in each module, so 64 calorimeter channels are assigned to each DSP.

5.2 Timing Studies for TI C6202

The benchmark code described above has been implemented for the TI C6202 processor, using the simulator provided by Texas Instruments. To improve the calculation time, it was found necessary to break the code into small loops, minimising branching and conditional statements. Hand coding was used to optimise the parallelism available in the processor. Let
$N_e$ represent the number of cells which have $E > E_n$ (for this study $E_n$ was chosen to be twice the noise of the calorimeter cell, or about 100 MeV). In Table 1 are given the number of DSP cycles taken for each section of the algorithm, as a function of $N_e$, and in Table 2 we give an estimate of how this translates into execution times for events with different numbers of cells above threshold. Here we see that even if one-third of the cells are above threshold (a rare occurrence), the execution time is equal to the average spacing between events at the design trigger rate. This indicates that the TI C6202 would in fact meet the requirements for the ROD. More recent results, arising from further optimisation of the algorithm, show that the execution times given here are overestimates, which strengthen this conclusion.

**Table 1: Number of cycles required by TI C6202 for each stage of the algorithm.**

<table>
<thead>
<tr>
<th>Calculation</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preliminary (determine $N_e$)</td>
<td>311</td>
</tr>
<tr>
<td>Energy</td>
<td>$26+22*N_e$</td>
</tr>
<tr>
<td>Time</td>
<td>$27+22*N_e$</td>
</tr>
<tr>
<td>Chi-square</td>
<td>$89+15*N_e$</td>
</tr>
<tr>
<td>General histograms</td>
<td>$39+16*N_e$</td>
</tr>
<tr>
<td>Monitoring selected cells</td>
<td>$48+13*N_e$</td>
</tr>
</tbody>
</table>

**Table 2: Execution times of the TI C6202 DSP (in microseconds) as a function of number of cells above threshold, out of a total of 64 cells, and whether or not monitoring functions are being performed.**

<table>
<thead>
<tr>
<th>$N_e$</th>
<th>Monitoring?</th>
<th>Execution time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>no</td>
<td>1.6</td>
</tr>
<tr>
<td>1</td>
<td>no</td>
<td>2.8</td>
</tr>
<tr>
<td>10</td>
<td>no</td>
<td>6.2</td>
</tr>
<tr>
<td>20</td>
<td>no</td>
<td>10.0</td>
</tr>
<tr>
<td>64</td>
<td>no</td>
<td>26.4</td>
</tr>
<tr>
<td>1</td>
<td>yes</td>
<td>9.7</td>
</tr>
<tr>
<td>10</td>
<td>yes</td>
<td>13.7</td>
</tr>
<tr>
<td>64</td>
<td>yes</td>
<td>37.0</td>
</tr>
</tbody>
</table>

5.3 **Monte Carlo Studies**

The ATLAS Monte Carlo chain is used to produce artificial output data for the FEB, and this output has been fed to the benchmark code for the ROD described above. The first case to be studied is for the shower of a 50 GeV electron, for the case of only thermal noise (zero luminosity) and for pileup noise at low and high luminosity. It was found that the energy and width of the reconstructed distribution are consistent with the expected values for each case, and that the introduction of integer arithmetic has no measurable effect on the results. We expect to use this program for a variety of purposes, such as checking the algorithm in the reconstruction of different types of showers, estimating with more precision the parameters, which enter into the execution time of the algorithm, and to understand how these parameters depend upon event type.

6. **SUMMARY**

We have described the technical requirements for the Readout Driver for the liquid argon calorimeters in ATLAS. From our studies to date, it appears that commercial DSPs can meet the needs for this device. We are carrying out a demonstration project in which several DSPs, both integer and floating point will be evaluated for their suitability in ATLAS. We give an example of the conceptual design and the simulation results for one of the processing units being built for this project, which is based on the Texas Instruments C6202 DSP. Simulation of benchmark code indicates that the speed of this processor is close to meeting our requirements, and initial Monte Carlo results indicate that the algorithm used produces acceptable results for the case studied.

7. **REFERENCES**

3. ATLAS LAr TDR, *ibid*, p. 425
The Detector Control System for ALICE  
Architecture and Implementation

D. Swoboda for the ALICE collaboration, CERN, Geneva, Switzerland  
(email: detlef.swoboda@mail.cern.ch)

Abstract

The ALICE experiment will include more than 10 individual detectors of different technologies and with specific operating conditions. The instrumentation required to run and control the operation of each sub-detector will include commercial and custom hardware of various standards.

The detector control system (DCS) for the ALICE experiment will allow a hierarchical consolidation of the participating systems to obtain a fully integrated detector operation. This goal will be achieved by clearly defined interfaces between system layers. In addition, sub-detectors will continue to be able to access their equipment independently from other sub-detectors for maintenance, upgrading and debugging. The architecture will, therefore, be based on partitioning into self-contained sub-systems, which can be separately developed, maintained and operated. Horizontal communication between sub-systems will consequently be avoided.

The DCS will use, where possible, commercial hardware components and software.

The clear vertical separation and hierarchical structure of the system should also allow implementing of a single user interface to the experiment, which can access the DAQ control and the DCS.

The technologies which will be used for the controller level hardware and the software options are explained. Also described are the current development status and the experience to date with the small-scale prototypes that are used to verify design choices.

1. JUSTIFICATION

The detectors for the LHC experiments will be installed in underground caverns. The location of the equipment in the underground caverns removes the possibility of intervention during the operation of the LHC accelerator. Consequently, remote access becomes a primary condition.

The operational conditions of each detector have to be controlled and known permanently and with limited delay.

The detectors will be operated in a hostile environment. They will be constructed to very advanced specifications and contain sophisticated and complex apparatus which requires the maintaining of precise and stable operating conditions. Consequently, manual operation would be very difficult or impossible and remote monitoring and control become prerequisites.

All detectors of an experiment must be operated simultaneously in a coherent and compatible way. More than 10 sub-detectors will have to co-operate in the ALICE experiment. Some, like the Inner Tracking System are mechanically and geographically very tightly coupled. All detectors are correlated for physics data taking. Consequently, the operation of the experiment must be centralised and all participating detectors synchronised in a common control system.

Data exchange with other systems like DAQ, Trigger and external sources must be guaranteed. The physics data is strongly dependent on the operational conditions of the sub-detectors. Consequently, status and other data from the detector operation must be available to the DAQ and Trigger. This will require an automated data exchange between the systems. In addition information from external systems must be accessed by the detector control system.

The ALICE experiment has no static configuration. It will evolve during the life of the experiment and undergo rather frequent modifications and upgrades. Nor is there a single operation mode. Detectors will be operated in several modes and the experiment itself will be set up in different configurations. Consequently, it must be possible remotely to remove or insert detectors in the current experiment set-up without physical intervention.

Different groups in a number of institutes in several countries are developing the sub-detectors in ALICE.

Before the installation in the experiment they need to be completely tested. Consequently, the control of the detectors will be developed in various places. But it must be possible to integrate the individual control applications in one global and coherent system.

Each of these global requirements in it self justifies the implementation of a state of the art control system.

2. ARCHITECTURE

The ALICE detector control system (DCS) is characterised in ref. [1].

The DCS will have to operate in two major modes:

- In normal operation during physics data taking controlled start, operation and shutdown of the different sub-detectors will have to be guaranteed.
- Standard operator commands will be available for this purpose through the global experiment control system. Malfunctioning will be signalled through centralised alarms. Defined variables will be made accessible by other systems like DAQ and archived for later retrieval and analysis.
During other periods, the detectors will be operated in a less coherent manner. It will be necessary to run a detector or sub-systems separately for maintenance or upgrade. Nevertheless, interference to the operation of other equipment or external services must be prevented.

The architecture to satisfy the preceding requirements and constraints will be based on distributed intelligence. A set of generic requirements has been defined and described in the URD [2]. The essential features are scalability and modularity since the system configuration will undergo modifications and extensions throughout the life of the experiment. The general structure of the DCS will be based on a client/server model.

The ALICE DCS will be structured in several well-distinguished layers (table 1).

At the level of the experiment networked general-purpose workstations will be dedicated to the management of the configuration data for all detectors and equipment, alarms, logging, archiving and data communication.

Dedicated controller stations will control the individual detectors. In this context, a controller station is not necessarily a single computer but can be clustered if a high channel count or the heterogeneity of the equipment leads to this requirement.

The communication links at the controller level will be based on general CERN fieldbus recommendations [3].

Remote sensing and actuator equipment at the detector level and in the electronic crates and ancillary equipment, such as safety and general electricity, will be connected directly to one of the proposed standard buses or via suitable interface modules. The field buses will be interfaced to the dedicated controller stations.

Access to the DCS will also be required from remote locations. However, it is planned to introduce access restrictions depending on the client location.

A supervisory and configuration software system shall provide a uniform and coherent user interface to all detectors [4].

2.1. Process Layer

Field instrumentation like sensor heads and actuators will be of various types and in different locations.

The instrumentation at the process level will be tributary to the requirements for the detector hardware. Some of the items, like power-supplies, will be bought as commercial units.

Most of the systems, however, differ from detector to detector and are assembled from a variety of more or less complex instruments, i.e. temperature control including sensors, valves and switches. However, the interfaces to the control equipment will follow well-established electrical standards like 0 – 10 V for voltage interfaces or 4 – 20 mA for current loop interfaces. Where this is not possible for technical reasons, signal-conditioning interfaces will have to be added for the connection to the controller stations. This is for example the case for pneumatic valves or switches. Complex instruments generally feature already defined communication interfaces and protocols, i.e. gas analysers, voltimeters.

The ALICE detectors are in principle, with the exception of the inner tracker system, fairly accessible. Nevertheless, the amount of material due to sensors and cabling has to be restricted. Mechanical and electrical requirements for the detectors necessitate in addition in many cases the use of custom designed hardware or the adaptation to these constraints. In the case of the ITS special front-end chips have been designed which include already the electronics for detector control. A specific feature of the ITS detectors is the use of the JTAG/BS protocol [5] for access of detector control parameters.

Hardware interlocks of components will be implemented wherever possible. This is the case, for example, for automatic switch off of front-end chips in presence of possible latch-up conditions, or for automatic ramp-down of high voltages in presence of over-currents.

2.2. Control Layer

The process equipment will be interfaced to multipurpose control computer equipment of PLC (Programmable Logic Controller) type, in compliance with the relevant recommendation [6].

However, wherever convenient, like in case of large number of field instrumentation channels to be controlled, VME based controllers may be used. It is foreseen to use a dedicated control computer for each detector. Depending on the complexity of the sub-detectors, it is

<table>
<thead>
<tr>
<th>SCADA (Supervision &amp; Control)</th>
<th>Workstations (PCs)</th>
<th>Server Stations</th>
<th>External Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controllers &amp; Network (Device Control &amp; Data Acquisition)</td>
<td>PCs, VME, PLCs</td>
<td>Power supplies</td>
<td>Gas Control Instruments Magnet Control</td>
</tr>
<tr>
<td>Detector (Process parameters)</td>
<td>Custom HW (FEE)</td>
<td>Sensors (T, B, F, P,)</td>
<td>Actuators (Vvs,Sws)</td>
</tr>
</tbody>
</table>
envisaged to introduce a further grouping at the level of the controller stations. Self-contained instruments like gas-analysers and high- and low-voltage power supplies will also be integrated at this level.

The controller stations will be connected by one of the proposed standard field bus systems or a dedicated general purpose LAN, i.e. Ethernet and TCP/IP.

2.3. Supervisory Layer

The equipment of this layer consists of general-purpose workstations, which will be linked to the control layer through a LAN providing TCP/IP communication.

The workstations will be set up as supervisory stations to act as Man Machine Interface (MMI) to the detector control system and will be configured as server stations for detector monitoring and data logging. In addition, access from remote locations will also be possible provided that a proper network connection and access authorisation can be established.

A global experiment control system (ECS) will provide a unified view of the whole experiment to the operator and manage the data exchange between the DCS and external systems like DAQ. Trigger control, magnet control and general alarm and safety system (fig. 1).

![Figure 1 Experiment control system](image)

During normal operation the DCS will be accessed through this Supervisory Control layer and no peer-to-peer connection between DCS sub-systems and other systems is envisaged. The ECS will only provide a limited set of macroscopic actions to generate the sequence of operations necessary to bring the experiment to a given working condition. However, the detailed actions will be executed by the sub-systems, i.e. DCS, DAQ, etc..

In addition the ECS will monitor the operation of the sub-systems, generate alarms and provide the interlock logic where necessary.

This control layer is also responsible for the dynamic splitting of the experiment into independent partitions and the possibility of concurrent data taking from the partitions. Nevertheless, the direct access to each sub-system in order to gain detailed information and control will always be possible through the dedicated MMI.

2.4. Communication

The data transmission links can be categorised in layers equivalent to the hardware architecture (table 2).

<table>
<thead>
<tr>
<th><strong>SCADA (Supervision &amp; Control)</strong></th>
<th><strong>Internet</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Controllers &amp; Network (Device Control &amp; Data Acquisition)</strong></td>
<td><strong>LAN (TCP/ IP)</strong></td>
</tr>
<tr>
<td><strong>Detector (Process parameters)</strong></td>
<td><strong>Fieldbuses (Profibus, CAN)</strong></td>
</tr>
<tr>
<td></td>
<td><strong>GPIB, RSxxx</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Custom (JTAG)</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Wired ptp</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Fieldbus</strong></td>
</tr>
</tbody>
</table>

As the DCS also involves safety aspects the hardware links used are independent from the DAQ. At the field instrumentation level, point to point links for voltage or current signals will be the general case. An exception will be necessary for some of the ITS components. The severe constraints for the cabling and connection volume led to the adoption of the JTAG/BS protocol for many control data. Each ITS detector will have its own DCS JTAG channels, independent from the DAQ JTAG channels which are used for down-loading individual detector configuration data.

Where feasible, intelligent probe heads and/or actuators will be used; these devices will be connected to the controller level via one of the proposed standard field buses. This does not change the hardware architecture since the bus system will be seen as an extension of the controller station.

A field-bus or a dedicated LAN, which is also connected to the supervisory level, will establish the connection between different sub-systems.

Access to the equipment will be allowed from remote locations. However access restrictions are planned depending on the locations to avoid conflicts.

2.5. Software

The controller level software, which will reside in the control computers that are directly linked to the process, will be configured individually for each sub-detector. For development and maintenance of the detectors each group will also configure a personalised MMI.

This software will be based on the same product(s) as for the general ALICE DCS system and allow, consequently, the integration in the overall system during experiment operation and alternatively separate access and control of each sub-system during other periods.

It is planned that the driver software for the controller stations to interface the field instrumentation to the
ALICE DCS architecture will be based on the OLE (Object Linking and Embedding) [7] for Process Control (OPC) [8] standard.

The objective of OPC is to provide an industry-standard mechanism to communicate and exchange data between clients and servers by using OLE technology from Microsoft. It should allow a standardised access method and unified interface between the field level and a SCADA (Supervisory Control And Data Acquisition) system or office applications, i.e. Excel, running under Windows.

The goal of OPC is to provide interoperability between multiple vendors’ products. In the past, each product or instrument required a dedicated suite of servers / drivers to meet the end-users needs. OPC shall allow to develop generic servers, independent of location and number of clients.

The OPC interface standard is defined and developed by the OPC Foundation which includes the major companies in the automation sector (Siemens, Fisher-Rosemount, National Instruments, Rockwell software, etc.).

The OPC Foundation and the OPC Foundation member companies will focus on making sure that products are interoperable together, and by definition, vendors push the OPC Foundation to make sure that performance and throughput expectations are not compromised to achieve interoperability. Therefore, the Objects, Interfaces and functionality defined by OPC will continue to evolve and change as the technology continues to grow.

A wide range of OPC servers and applications is already available now and additional companies have announced their adherence.

3. DEVELOPMENTS AND VALIDATION

The CERN JCOP project [9] has been set up in 1997 to work on a common solution for the DCS of all LHC experiments. One activity concerns the study and evaluation of SCADA. An important number of other activities have also started, i.e. system architecture, data interchange with external systems [10], communication drivers.

However, these developments are mainly concerned with the upper layers of the system. Hardware related aspects, like power supply control, gas distribution, and fieldbuses, have also been addressed in this context but they are treated in a rather generic approach, since all experiments are concerned.

In ALICE some key aspects are being looked at in a complimentary way. They can be classified in three fields:

a) Hardware architecture
b) Communication systems
c) Software architecture

3.1. Hardware architecture

A partial control system for the ALICE HMPID detector has been implemented in 1998 [11], [12]. The purpose was to gain first experience to validate the use of PLC, communication through TCP/IP and a small-scale SCADA system. The development includes all layers of the planned ALICE DCS.

The prototype includes one circulator module (fig. 2), controlled by a PLC. The supervisory level has been implemented with Bridgeview, which was chosen as interim solution by the JCOP in order to provide a common migration level towards the final SCADA system. Despite the use of a mock-up hardware system, the implementation of the liquid circulator is based on real operating conditions. A second version has now been configured which will be used in the Cherenkov detector of the Star experiment at RHIC.

3.2. Communication systems

Important effort is put by the major automation system manufacturers in the promotion of the OPC standard.

The use of compliant communication drivers in the DCS system is believed to take advantage from this development. In order to validate the efficiency and suitability of the communication mechanism, several implementations for the control of high voltage power supplies have been developed. A first development uses the proprietary CAENnet to access a power supply from this manufacturer [13]. A second development has been completed for a Lecroy power supply using the default serial interface connection [14]. The aim of the latter implementation was to provide a complete remote access application which can use the basic communication
interface of any PC and is independent from the location where the power supply is installed, provided it can be connected to a networked PC (fig. 3).

Figure 3 High Voltage power supply control

A later upgrade to a communication via TCP/IP will simply require replacing the medium access object. This allows to preserve an identical user interface independent from the communication system.

3.3. Software architecture

A number of heterogeneous control systems will have to interchange data in the ALICE environment. Like for the control systems of the sub-detectors, they will be developed separately by different groups. Similar to the detectors they will, however, be operated closely coupled during ALICE data-taking. It is, therefore, proposed to implement a high-level experiment run control system [15]. This project involves three major parts.

3.3.1. DCS control

The current supervisory system for the ALICE HMPID liquid circulator prototype (based on BridgeView) will be re-engineered using a SCADA system.

One aspect of the planned development consists, therefore, in the evaluation of the necessary migration effort.

An extended system is currently being configured for use in a HEP experiment. This could provide the opportunity to test features like replication and scaling.

3.3.2. DATE control

The current DAQ control (DAQC) through DATE [16] (the ALICE DAQ prototype) will be re-engineered using a SCADA system. The new run control will access the processors involved in the DAQ via the present interface, based on an exchange of messages over TCP/IP sockets. No other interface is required, in particular no sharing of a database is foreseen.

The operator interface will emulate the facilities provided now by a Tcl/Tk program. The implementation will require writing an OPC driver to access the remote machines under control in the same way as a PLC.

Problems to be tackled include the formatting of presentation windows according to a configuration file and the possibility of cloning complex objects without re-defining all the tags and procedures.

3.3.3. Supervisory control

An experiment supervisory control (ECS) will be configured using a SCADA system. This part will provide the main control window for the operator. The first phase will be the connection of the DAQC and the DCS to a common SCADA. This work includes the design of an organisation of the control system based on layers, corresponding to different levels of visibility and access rights (fig. 4).

Figure 4 Run control prototype

The higher layer will provide a global view, and will be only allowed to make a reduced set of actions. Lower layer, i.e. DAQC and DCS, will have access to detailed information and control attached to each system.

The communication between layers will be based on a message-passing client-server model, with no sharing of memory structures (including databases). Systems on the same layer can only communicate via the layer above.

In a subsequent phase, the problem of splitting the entire system into independent partitions will be addressed. It should be possible to develop and operate sub-systems independently from the ECS. But it must also be possible to easily integrate the sub-systems in the ECS. The ECS control may also be split into different control domains that may operate independently and concurrently.

4. CONCLUSIONS

Major benefits of common hardware choices are well-supported controls- and communication interfaces. A reduction of the development and maintenance effort is also expected through the use of commercial software and strong recommendations of hardware standards. This can be enhanced by the commitment to adopt wherever reasonable common solutions for all LHC experiment.

During a first phase, the requirements seen from an operational point of view have been collected and analysed. However, this needs to be matched with the process level hardware.

Consequently, with the development of a better knowledge of the final detector implementation a second iteration starting bottom-up from the inventory of the
parameters to be monitored and controlled, the connection to the operation requirements must be established. This has now been started and should be completed during the next year.

A number of technical choices, described in the DCS architecture have been tested successfully with small-scale prototypes. We are entering now the phase where implementation of complete sub-system controls has to be started. The layered architecture of the ALICE DCS and the independence from the DAQ control system will allow the separate development and later integration of partitions into a global experiment control system. The adoption of standard and unique interfaces furthermore guarantees that technical progress can be easily accommodated by exchanging obsolete system parts by future developments.

It must be emphasised that most of the ALICE control systems are conceived on Unix platforms. The possibility to integrate these systems with the required functionality in the planned Experiment Control System is therefore of high importance.

REFERENCES

1. Data Acquisition, Control and Trigger, ALICE Internal Note/98-23
2. Detector Control System for an LHC Experiment User Requirement Document, ALICE/98-03
3. Recommendation for the use of Fieldbuses at CERN in the LHC era, proc. 1997 ICALEPS, Beijing, China
5. IEEE std. 1149.1a, 1993
6. Recommendations for the Use of PLCs at CERN, PLCWG, SL98-007 (CO)
10. LdiWG, LHC data interchange Working group
11. Test and Evaluation Station (TEST), ALICE Internal Note/99-13
12. First experience with PLC, OPC and Bridgeview in the context of the HMPID liquid distribution prototype, ALICE Internal Note/99-14
15. Supervisory Experiment Control, D. Swoboda, A. Vascotto, private communication, CERN 8/6/99
Study of the ALICE Time of Flight Readout System - AFRO

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Abstract

The ALICE Time of Flight Detector system comprises about 176,000 channels and covers an area of more than 100 m². The timing resolution has to be better than 150 ps. The readout system is based on a modular architecture. Detector cells are combined to modules of 2880 channels. A VHDL model of the readout system has been developed. Results of prototype electronics used in test beams are presented.

INTRODUCTION

The ALICE experiment at the Large Hadron Collider heavy ion program at CERN will include a large area Time of Flight (TOF) system, spanning over a hundred square meters with more than 170,000 individual read-out channels. Up to 10,000 charged particles are detected per unit of rapidity per event at midrapidity by this detector; particle identification of most of these particles is covered by the time of flight technique.

The design of the detector is not fixed yet. However, the readout model is as flexible as to allow adaptations to modularity and data flow easily.

In the present design it is planned to divide the ALICE Time of Flight Detector into 18 20° φ-segments and 4 1.74 m long z-segments. As a result the maximum number of TOF modules is 72. Each module is 1.74 m long and 1.3 m wide. It is equipped by 2880 chamber cells (60 cells x 48 cells) [1].

One option for the implementation of the detector cell is a glass-RPC detector cell [2]. The cells are constituted by a pair of identical double-gap chambers, each consisting of an aluminium anode and cathode and a central resistive plate at a floating potential. The different elements are assembled in a plastic box that provides electrical insulation and mechanical rigidity. This box has holes for wires connected to the metallic electrodes, for gas circulation and for insertion of spacers that define the gaps [3].

READOUT SYSTEM

Timing measurements are performed using an 8 channel TDC (time to digital converter) chip which requires a 40 MHz reference clock signal. The chip is being developed by the CERN microelectronics group [5]. The TDC chip has multi hit capability and generates a time tag for each hit onto a parallel bus. It allows hit data to be stored in an internal buffer until the level1 (L1) trigger decision has been reached. A trigger feature supports readout of only those data which are located within a programmable time window before and after the triggered event.

In order to perform slew correction the ‘time over threshold method’ is used to measure the amplitude of the signal. The advantage of the scheme is that no parallel ADC channels are needed. The amplifier produces a fast leading edge (~1-2 ns) and a slow trailing edge (~100 ns). The pulse width of the amplifier is proportional to the input charge. A slew correction can be undertaken using the over threshold time pulse duration. The TDC chips allows to measure both the time of the leading and the trailing edge with the same TDC channel.

The readout system is based on a modular architecture, detector cells are combined to modules of 2880 channels. Each of these modules can be read out and calibrated independently from each other. By distributing a reference signal, a timing relationship between the modules is established.

The readout architecture is divided into three stages; the TDC chip and its TDC controller, the module controller and the detector data link interface. The TDC controller programs the TDC. Upon arrival of a L1 trigger accept, 5.5 μs after the corresponding event, the TDC controller transfers hit data from the internal TDC memories to the memory of the module controller. In case of L1 trigger reject, the corresponding data are either discarded in the TDC buffers or transferred to the module controller for monitoring purposes.

The module controller prepares the data for transmission to the data acquisition system. In case a level2 (L2) trigger accept is issued, the module controller sends the corresponding data to the detector data link interface [4]. The maximum L2 trigger latency will not exceed 100 μs [7]. An detector data link interface acts as a data collector and as interface to the ALICE data acquisition system.

Fig. 1 shows a block diagram of the full system. 12 TDC chips (= 96 channels) are connected to one TDC controller. 30 TDC controllers are supervised by one module controller. 4 module controllers are read out by one detector data link.

On average, 10⁴ minimum bias events per second are expected. The L1 trigger rate will not exceed 2800 Hz. The maximum L2 trigger rate will not exceed 660 Hz.

A model of the readout system has been developed and an optimization process was performed using the hardware description language VHDL. It is planned to complete a FPGA based prototype of the TDC readout by the end of 1999.

For the estimation of the system data rate a maximum average cell occupancy of 30 % has been assumed unless stated otherwise. This number is grossly overestimated [8].

TDC CONTROLLER

The purpose of the TDC controller is to program the TDC and to read out and transfer data from the TDC to the module controller. One TDC controller processes 96 channels (12 TDC
The TDC controller passes the L1 trigger decision to the TDC chips. The trigger feature of the TDC chips [5] allows readout of only those hit data from the internal buffer memories which have occurred within a programmable time window before and after the triggered event. The TDC controller passes the data flow directly to the module controller without additional stages of buffering.

The TDC controller has been implemented using a commercial FPGA (XCS20, [6]) which works in a synchronous mode. Data may be transmitted at a 10 MHz rate. Although the overall occupancy will not exceed 30 %, the local occupancy used to design the system may be much higher. Considering the worst case of 100 % occupancy the resulting data flow from one TDC via the TDC controller to the module controller yields: 96 channels * 100 % * 2800 Hz * 64 bit = 1.7 * 10^7 bit/s.

A 10 MHz data transmission rate between the TDC controllers and the module controller for all TDC controllers yields a maximum average transfer time of: 2880 cells * 30 % occupancy * 100 ns * 2 words = 172.8 µs. That means that within 172.8 µs after the L1 trigger accept signal all data have been transferred from the TDC controllers to the module controller where the maximum average L1 trigger rate is 2800 Hz [7] (or 357 µs time period).

MODULE CONTROLLER

The purpose of the module controller is to collect the hit data from the TDC buffers after the arrival of a L1 trigger accept signal and to prepare the transmission to the ALICE DAQ via the detector data link DDL. Data are stored in a RAM which is controlled by the module controller until a L2 trigger decision has been issued. The use of a dual port memory allows the start of the transfer to the detector data link interface before the data transmission from the TDCs has terminated. However, a L2 reject signal might have been issued even before the end of the transmission of the hit data from the TDC buffers to the module controller. In this case the transmission is aborted, the external module controller memory is cleared and a command to the TDC controllers is issued to clear the corresponding remaining data in the internal TDC memories.

The average data rate at the input of the module controller can be calculated as follows: 2880 chamber cells * 30 % occupancy * 2800 kHz maximum average L1 trigger rate * 64 bit = 2.4 MHz * 64 bit = 1.5 * 10^8 bit/s. Given modern FPGA technologies this requirement allows the implementation of the module controller by means of commercial FPGAs (XCS40, [6]).

DETECTOR DATA LINK INTERFACE

The detector data link interface acts as data concentrator. It collects data from four module controllers and transfers it to the ALICE DAQ using the detector data links - DDL. 18 detector data link interfaces are employed. Each 4 module controllers are connected to a detector data link interface.

PHYSICAL IMPLEMENTATION

The physical implementation of the electronic system is divided into three building blocks: signal pickup cards, module reader cards, and detector data link (interface).

SIGNAL PICKUP CARD

Signal pickup cards contain shaping amplifiers, discriminators and TDCs for 16 channels. These cards are attached to the chamber PCB vertically. The chamber signals and the high voltage ground signals are connected to the bottom whilst the low voltage, clock signal, test signal input and digital data bus are connected to the top.

Fig. 1: ALICE time of flight detector data flow.

Fig. 2 illustrates the physical implementation of a signal pickup card. It contains four 4 channel analog chips and two 8 channel TDC chips. Fig. 3 illustrates the layout of the signal pickup cards on the chamber PCB. 6 TDCs, located on 3 signal pickup cards, are connected onto the same parallel data bus.
The signal pickup cards are able to send test pulses to all connected channels at the same time. This feature is used to test the time sensitive part of the electronic chain. The signal path from the chamber to the amplifier is kept as short as possible. The amplifiers are located directly on top of the chambers.

**MODULE READER**

The module reader unit has three module reader cards. Each module reader card contains 10 TDC controllers, the module controller, one clock receiver unit and one clock distribution unit. 12 TDCs are connected to a TDC controller. The module reader cards plug directly onto the digital data bus connectors of the signal pickup cards. The layout of all three cards is identical. All three module reader cards are plugged onto the same 32 bit wide module bus (see fig. 4). However, only one out of the three, the main module reader card, contains also the clock receiver unit, which distributes the clock to the three clock distribution circuits on the module readers, and a module controller FPGA. The main module reader card of a module plugs in the middle. This ensures a minimum propagation delay of the clock signal on the module.

The module reader card contains additional TDC chips for calibration purposes. They are used to measure the time when test pulses are sent to test inputs of the analog amplifiers. The time difference between the time of transmission and the reception of the signal is measured permanently in order to monitor time drifts of the electronics.

The TDC chips require a 40 MHz clock signal as a reference signal. Independent chamber modules must be referenced to each other in order to be able to compare time measurements of independent modules. Several options are possible. One option is to distribute a unique clock signal to each module where it is again distributed to each TDC chip. The timing reference between modules is established by the clock signal. Another possibility is to foresee independent clock generators on each module. The local clock generators must be calibrated on board by means of constant (cable) delays. Additionally the so called \( t_0 \)-signal, which is generated by a dedicated detector at the time an event occurs, is distributed to each module. In this case the timing reference is established by the \( t_0 \)-signal. Further studies will reveal the most practical solution.

**DETECTOR DATA LINK INTERFACE**

For practical reasons the detector data link interface merges the data from four modules mounted on the same detector \( \phi \)-segment. One DDL unit is foreseen for each detector \( \phi \)-segment. Fig. 5 illustrates how 4 modules in a detector \( \phi \)-segment are connected to each other and read out via a DDL unit. The maximum length of the data bus which connects the four modules does not exceed the length of three modules (< 6 m). The DDL interface is directly connected to the main module reader of the module closer to the readout side of ALICE.
A prototype of the frontend electronics and readout chain has been developed. The concept was validated during the test beam phases in 1999 using a 32 cell detector module constructed by the TOF collaboration [3]. An important issue for the design of the prototype electronics was to implement a system which is as close as possible to the ALICE implementation scheme [10]. Independent systems of high voltage distribution, low voltage distribution, and signal distribution are kept separated from each other. Also the number of chamber cells contained by a modular unit is low. However, for a large scale implementation this does not imply geometrically small units. A large mechanical structure can carry a high number of electrically separated modules.

The physical implementation of the prototype system consists of three parts: the chamber printed circuit board holding chamber cells, and the high voltage circuitry [12]; the signal pickup cards, holding amplifiers, discriminators and edge detecting circuitry, and the time measurement system. The time measurement system for the test beam measurements was built up using standard LeCroy 2228A TDCs. The signal charge of each channel was measured using standard LeCroy 2249 ADC modules. It is planned to upgrade the prototype signal pickup cards with 4 channel prototype TDC chips [11] and read out the data using prototype module reader cards.

The 4 x 8 individual detector cells are arranged in a chessboard pattern in two layers, providing a geometrical coverage of 97%. Mechanical support for the cells is provided by plastic spacers glued onto the detector PCB, which carries the high voltage circuitry, signal feed-throughs to the readout electronics, and closes the gas volume. The physical layout (fig. 6) of the high voltage distribution is carefully optimized to minimize crosstalk between neighboring channels across the electrical connections to a level of 1/2500. In particular the signal ground is separated from the HV ground for optimum picked-up noise and crosstalk rejection. All metallic parts on both sides of the PCB which are at HV potential are concentrated in the center of a 8-cell unit and covered by protective glue (Araldite) to avoid surface currents and discharges. The ground loop surrounding this HV area is only 6 x 12 cm wide and therefore rather insensitive to external high frequency noise. Four of the 8-cell units are connected to a common HV supply.

The detector PCB with the array of 32 cells is mounted on a metallic box which closes the gas volume, carries gas connections and allows to fix the module to a moving table. All six faces of the box are covered by a thin PCB with a copper layer connected to the HV ground for electrical shielding, leaving...
only small holes for the connectors to the readout electronics [3].

The signal pickup cards are attached to the detector PCB vertically. From the bottom the chamber signals and the high voltage ground signals connect to the signal pickup card. At the top side low voltage, the test input signal and the digital signals are connected. Fig. 7 shows a picture of the card.

The amplifiers are plugged directly onto the signal pickup card. These amplifiers have been built by the Institute of Theoretical and Experimental Physics (ITEP), Moscow, using discrete components. The rise time of the output signal is less than 1.8 ns. The fall time of the output signal corresponds to the input charge and lies within the range of 15 to 50 ns.

A commercial ECL discriminator (AD96685BR) is used to build up a fixed threshold discriminator scheme. A hysteresis of 14 mV is applied. The chip drives a trigger circuit for detection of positive and negative edges using components from the Motorola 10EL family.

The positive edge of the discriminated amplifier signal gives the timing information. The negative edge of the signal gives the amplitude information. The location of the amplifiers has been chosen to provide a minimum signal path length from chamber to amplifier. Discriminators are located directly behind the amplifier maintaining a signal path length between amplifier and discriminator of only 1.5 cm. The low voltage supply of the card is distributed by external cables and not by the chamber printed circuit board. The card has its own voltage regulators. A test pulse signal can be sent to each amplifier. The analog output signal of the amplifier is buffered and can be measured independently from the digital output. Fig. 8 shows the 32 cell module with 2 signal pickup cards.

In the test setup the cable length from the ECL drivers on the signal pickup card to the TDC electronics was about 15 m. This layout was necessary for the test setup, nevertheless an electronics time resolution of 45 ps (9 July 1999).

The overall system performance is very much dependent by the optimum modularity and careful location of the electronics.

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REFERENCE


“http://home.cern.ch/~akluge/alice/alice.html”.


[12] M. Spegel, The Chamber PCB for a glass RPC time of flight array with 90 ps time resolution,
“http://www.cern.ch/ALICE/Projects/TOF_PPC/”.

Abstract
A new TDC chip has been developed for the COMPASS experiment at CERN. The resulting ASIC offers an unprecedented degree of flexibility and functionality. Its capability to handle highest hit and trigger input rates as well as its low power consumption makes it an ideal tool for future collider and fixed target experiments. First front-end boards equipped with the F1 chip have been used recently at testbeam experiments at CERN. A functional description and specification for this new TDC chip is presented.

INTRODUCTION
The COMPASS experiment at CERN was proposed to and approved by the CERN authorities to investigate the complex hadron structure. One central issue of the experimental effort will be the measurement of the contribution of gluons to the nucleon spin. Previous experiments at CERN, DESY and SLAC made decisive advances towards the understanding of the nucleon spin in terms of its quark constituents, but the role of the gluon still needs more clarification. To reach this objective a demanding state-of-the-art double-stage spectrometer with large geometrical and dynamical acceptance will be set-up and commissioned through 2000.

The low cross sections of the studied interactions which will provide insight to the physics objectives of COMPASS necessitate high beam rates. The central detector has to be capable to digest the high particle flux from the traversing beam at intensities of $2\times10^8$ particles/spill. This leads consequently to the requirement of negligible dead time for the digitization units in the data acquisition system of the experiment. The anticipated amount of data on the order of several Gigabytes per spill (2.4 seconds) is at the edge of today's digitisation and bandwidth technologies.

Wherever applicable in COMPASS measurements are digitized at the detector by ‘intelligent’ front-end electronics [1]. The advantages of this scheme are obvious: besides the enormous cost savings due to obsolete data transfer and delay cables the fact of lower noise, higher bandwidth and the possibilities for data pre-processing open up new prospects for efficient data digitisation. In case of analog readout a pedestal subtraction and zero suppression is performed by the front-end devices at the COMPASS detector. To suppress background in time measurement components only those hits are read out which are time correlated to the trigger time. The distributed readout architecture of the COMPASS experiment is summarized in Figure 1.

Figure 1: The architecture of the COMPASS detector readout.

The digitized data are transmitted via CAT 5+ patch cables [2] at rates of up to 40 MByte/s from the front-end to FPGA based CATCH modules (CATCH = COMPASS Accumulate, Transfer and Control Hardware) which serve as readout drivers. The transmission between the front-end and CATCH modules is based on the serial protocol generated by the HOTLink chip [3]. The CATCH func-
tions as a data concentrator and a pre-event builder as well as a control unit of data integrity of events sent from the front-end devices. Furthermore, the CATCH takes over automatic front-end initialisation and calibration tasks. The same module serves also as a remote fan-out for the COM-PASS trigger distribution and time synchronisation system (TCS).

In the next hierarchical step of the data acquisition system the data are transmitted from the CATCH to large readout buffers (ROB) via S-link [4] connections. The ROBs are capable to store at least all data which have been collected during one spill. Again pre-event building and checks for data consistency are performed before the sub-events are transmitted via Gigabit Ethernet to filter computers. Here the final event-building is performed and complete events may be rejected based on physics constraints. Finally, the events will be transferred at a continuous rate of up to 35 MByte/s to the central data recording facilities at CERN where they are stored in object oriented federated databases for later off-line analysis.

**THE F1 TIME CONVERTER CORE**

Handling extremely high hit and data rates are the key feature of the COMPASS detector. Hitherto existing time converter chips were not designed to digitise six million or more hits per second with a precision of better then 100 ps. In addition, this demanding task even has to be performed without any dead time during time conversion. Given the complexity of the task to design a new TDC chip which fulfils all COMPASS requirements the most evident approach was to develop the F1 chip as ASIC together with an industrial partner of outstanding experience and knowledge. The outcome of the fruitful collaboration with acamesselektro electronic gmbh [5] is a state-of-the-art multi-purpose TDC chip with many different modes of operation in terms of functionality and resolution. To guide the reader through the technical description a schematic block diagram of the chip is given in Fig. 2. The technical specifications for the TDC are summarized in Table 1. The logic structure of the TDC architecture can be divided into the time measurement unit, the arithmetic logic executing the trigger correlated hit selection as well as the readout buffer and output interface.

The clockwork of the F1 is an asynchronous ring oscillator consisting of 19 identical voltage controlled delay elements (see Fig. 3). The dynamic range of the delay chain is extended to 16 bits by a coarse counter. A time measurement with the F1 contains the combination of the status from the array of the delay chain and the coarse time counter. The leading and/or trailing edges of hits and the leading edges of trigger signals are sampled by this device without any dead time.

The process technology of 0.6 μm sea-of-gates has a typical gate delay on the order of 100 to 150 ps depending on the batch of the production run, the ambient temperature and the supply voltage of the delay elements. To maintain stable gate propagation delays over extended periods a phase locked loop (PLL) is used to control the ring oscillator frequency. Thus the time measurement circuit maintains a constant time resolution and is tolerant to very large variations in temperature (±75 °C). The frequency of the ring oscillator and the time resolution of the F1, respectively, can be selected with two pre-scalers M and N (see Fig. 3). The ratio between the pre-scalers for the reference clock N and the ring oscillator M determines the cycle time of the asynchronous ring oscillator, which is 152 times the propagation time through a single delay element. Therefore, the user can chose the external reference clock freely between 500 kHz and 40 MHz.

Unlike a delay locked loop (DLL), a PLL filters any jitter of the reference clock signal. Therefore, no special precaution for the clock distribution system is necessary to provide the uncompromised high resolution of the TDC even in distributed applications. A carefully chosen floor plan together with the introduction of several separate power and ground supplies for the pad ring, high current output

![Figure 2: Block diagram for the F1 TDC chip. Components which are displayed as shaded boxes are implemented for each channel, whereas non-shaded boxes are unique and shared by all eight channels.](image-url)
Figure 3: An asynchronous ring oscillator, stabilised by a phase locked loop, is used in combination with a coarse counter to form the time measurement unit of the circuit.

The signal propagation of each input stage can be delayed by approximately 1 LSB divided in 64 individual steps. This feature can be used to improve the resolution of the TDC by a factor of two. In case the \( F \) is operated in the high resolution mode two neighboured input channels are connected internally and hence the original signal is split into two channels. The delay of one of the two signals is chosen such that it is half a LSB relative to its sister channel. This way additional phase information on the signal can be derived and be used to improve the time measurement to a resolution of 30 ps RMS. In this mode the dynamic range of the TDC is reduced by a factor of two.

THE \( F \) AS LATCH DEVICE

Another mode how to operate the \( F \)-chip is the latch or hit mode. This mode is suitable for the readout of detectors which do not require precise time information for event pattern reconstruction but only time stamps for event building in a pipelined data acquisition system or for background suppression. Therefore it matches the requirements for MWPC readout or standard latch units and can be regarded as a cost efficient replacement of existing commercial products.

In the latch mode the number of input channels of the \( F \) is increased to 32. Each group of four of the 32 channels is connected to a fourfold input register and a logic OR which is linked to one of the eight time measurement channels of the \( F \) (see Fig. 2). When a hit arrives on one of four combined channels the next clock cycle of the asymmetric ring oscillator starts a 6 bit counter. This counter, which defines the strobe length during which the registers accept input signals, is synchronous to the coarse counter, thus running with a period of \( F_{LSB} \times 38 \approx 5.7 \) ns, where \( F_{LSB} = 150 \) ps refers to a typical digitisation bin size of the \( F \) in the standard resolution mode. After a pre-set time of 5.7 ns < \( t_{clock} \times 364.8 \) ns (64 \times 5.7 ns) the four inputs are switched to a second hit input register and a time stamp is taken with the full accuracy of the standard mode. The 12 most significant bits of the time stamp are placed in front of the four bits from the input register and transferred to the hit buffer. To ensure that no hits are lost while the input to the hit registers are switched both hit registers will accept signals during an overlap of about 2 ns. Although it is desirable to have the overlap as short as possible small variations in production processes and the danger of efficiency gaps may require a longer overlap.

DATA SPARSIFICATION

Digitized time stamps from hits are stored in dual port buffers. Each \( F \) channel has its individual buffer which can store up to 16 hits before it blocks further data input. The hit buffers are addressed in random access mode such that the trigger matching unit can search for data which belong to a coincident trigger. In the high resolution mode the hits are stored alternately in both hit buffers of the two channels. The procedure to store the data alternately permits higher data rates or longer trigger latencies because it is equivalent to double a single hit buffer to 32 words. A second advantage is the improved performance of the trigger matching unit since two units work in parallel on the data set in the hit buffers.

An arriving trigger signal is digitized by the same time measurement unit as the hit-signals. A programmable trigger latency time is subtracted from the measured trigger time to account for the time needed to form and to distribute the trigger to the distant front-ends. Trigger time-stamps are stored in a common four word deep FIFO until the arithmetic logic units are available to start with the trigger matching process. A programmable trigger window defined by the maximum time spread of a detector, e.g. drift time in wire chambers or time of flight, is loaded at the initialisation of the chip. A hit is considered to coincide with a trigger if its time stamp is within the latency corrected trigger time and the upper limit of the trigger window (see Fig. 4). Local bookkeeping of all triggers arriving at the \( F \) trigger input is handled by a six bit counter. In the case of a trigger buffer overflow the number of missed trigger signals can be reconstructed from a comparison of the trigger counter and from the trigger time stamps.

The search mechanism which is used in the trigger matching unit uses two independent pointers. The read pointer specifies the memory address currently being accessed to look for a hit which matches the trigger time. The start-search pointer marks the address where the search
Figure 4: Example for the trigger matching procedure.

is supposed to start when the next trigger is loaded from the trigger FIFO. The start-search pointer is set to the read pointer position at the location of the first hit which matches the trigger time. All hits previous to this particular hit are deleted because they are outside of the future regions of interest. The selected hits are copied to the readout buffer. The search for further hits which belong to the same event is continued until either no more hits are stored or the next found time stamp in the hit buffer is younger than the region of the trigger window allows. Regions of interest for a sequence of triggers can overlap for those detectors which require long trigger windows. Therefore, selected hits are not deleted from the hit buffer when copied to the readout buffer.

When no triggers arrive for longer periods the write pointer may catch up with the start-search pointer. In this case no new hits would not be accepted by the hit buffer anymore and the time stamps would be lost until the next trigger starts the clean-up process of the hit buffer. To avoid this, an artificial fake trigger is generated internally at regular intervals as soon as the trigger FIFO is empty. The fake trigger is handled like any real trigger except that no data are copied to the readout buffer. The generation of fake triggers helps to clean-up the hit buffer from old hits and guarantees unambiguous time measurements.

**READOUT**

The introduction of dedicated readout buffers permits fast data readout while hits belonging to the next trigger are already selected in parallel by the trigger matching units. When the trigger matching process for a particular event is completed on all channels of a $F_1$ the data ready signal is set and the output interface is prepared for readout. In case several chips are connected to a single front-end data bus the readout is controlled by a circulating token. The token control in the $F_1$ has been optimised to avoid wait states when a token is handed over to the next chip.

The high speed readout interface of the $F_1$ can be clocked with a frequency of up to 50MHz. Two different modes for data readout are supported by the $F_1$: 8 bit and 24 bit readout. The eight bit readout is used in the COMPASS experiment for applications where serial data interfaces and serial data links are used. The eight bit readout mode accords with the timing specifications of the HOTLink parallel to serial converter chip [3]. For a safe timing the $F_1$ provides a bus-write-enable and a delayed bus clock with an adjustable skew for the HOTLink.

The 24 bit parallel readout can be used where highest data rates are anticipated and no data serializer is used. In this mode the user can exploit the full data throughput capabilities of the TDC chips.

**TDC INITIALISATION**

All data communications between the CATCH boards and the TDC front-end boards are exclusively serial. For the setup procedure, the TDC has a TTL serial data input which can be operated at a sustained rate of 10 MBit/s. The TDC serial interface is designed as a fourfold oversampling device. For different applications either the PLL reference clock or an optional dedicated setup clock can be used. The format for the setup data is characterised by two start and two stop bits, three bits for the chip address, a common address bit and four bits for register addresses followed by 16 bits for setup data. Since some data may be common for all chips on a board, these can be loaded in parallel by making use of the common address bit. In case of errors in the start or stop bits, the data reception is refused by the $F_1$.

**DAC INTERFACE**

In the COMPASS experiment the AD8842 octal 8-Bit digital-to-analog converter (DAC) [6] is used to control the thresholds of discriminators of some detectors. The AD8842 provides eight general purpose digitally controlled voltage converters with separate voltage inputs. Each AD8842 has its own register that holds the output state. The registers are updated from a 3-wire serial input digital interface.

The $F_1$ is used to interface the serial setup lines from the CATCH to the DAC and to store the threshold values for multiple downloads. The $F_1$ contains eight registers of 1 Byte which may hold all register values for one AD8842. The data can be formatted and send via the 3-wire output interface to the AD8842. This operation does not interfere with normal TDC time conversion.
Table 1: Technical description of the F1.

**Number of channels:**
- 4 for high resolution mode
- 8 for standard resolution mode
- 32 for latch mode

**Digitisation bin size:**
- 75 ps for high resolution mode
- 150 ps for standard operation mode
- 5700 ps for latch mode
  (typical values)

**Reference-clock frequency:**
- Between 500 kHz and 40 MHz
  (Clock is used for self calibration only)

**Differential non-linearity:**
- Less than 0.3 LSB

**Integral non-linearity:**
- Less than one time bin

**Variation with temperature or supply voltage:**
- Less than one time bin

**Dynamic range:**
- 16 bits

**Double pulse resolution:**
- Typical 22 ns

**Digitisation and readout dead time:**
- None

**Hit buffer size:**
- 32 measurements for high resolution mode
- 16 measurements for standard mode
- 16 measurements for latch mode

**Output buffer size:**
- 8 measurements

**Common readout interface:**
- 16 measurements

**Trigger buffer size:**
- 4

**Trigger latency:**
- up to full dynamic range of digitisation unit
  (typical values: 9.8 μs, 4.9 μs, standard, high resolution mode, respectively)

**Power supply:**
- 5.0 V

**Power consumption:**
- 80 mA

**Temperature range:**
- -40 to +85 degree centigrade

**Hit input:**
- LVDS, LVPECL or TTL

**Package:**
- 160 PQFP

Figure 5: This picture shows a 32 channel TDC board. The board dimensions and board interface connectors are according to the CMC standard [7].

**ACKNOWLEDGEMENT**

Our grateful appreciation goes to the local electronic workshop and engineer team, whose support during the development and production phase of the electronic components was essential. We also recognise the endeavours of our collaborators from the COMPASS collaboration and by the staffs of the collaborating institutions during several test periods at CERN. In particular we deeply appreciate the many stimulating discussions of our colleagues involved in front-end electronics development. The developments described in this report are supported by the German Bundesministerium für Bildung, Wissenschaft, Forschung und Technologie.

**REFERENCES**


[6] Analog Devices, Norwood, MA 02062-9106 *Datasheet: AD8842, an 8-Bit Octal CMOS TrimDAC.*

Assessment of EMC Parameters of LHC Front End Electronics

by Fritz Szoncsó CERN TIS

1) Introduction

EMC parameters are an issue for LHC detector electronics because package density and man made noise interfere strongly with the susceptibility that is a by-product of the dynamic range required by many detector systems. The parameters include relevant noise emissions by switch mode power supplies, noise transfer by linear power supplies, noise behaviour and emission by the electronics itself. It will be shown that radiation of noise is generally small and, in case this turns out to be a problem, may easily be screened. However, conducted noise may affect electronics via all connections and stray capacitances. Conducted noise handling will depend on system grounding, powering, cabling, connector quality. Screening efforts may interfere with conducted noise when screens become major stray paths. Knowledge about system immunity and the levels of conducted noise to be expected, all over the entire frequency range of the electronics, will enable designers to react early in the system design stage.

EMC parameters allow for sound system choices whilst avoiding over engineering of power systems. Common mode current load also determines the layout of the grounding scheme. The ground configuration may then be chosen such that inevitable common mode currents may enter and leave the system where they do no harm.

2) Measurement of common mode noise of switch mode power supplies

Switch mode power supplies (SMPS) generate differential mode noise that in general is called ripple. Ripple may easily be filtered to reach any value desired. However, SMPS also generate common mode noise. Pollution of the ground system becomes inevitable if this part of the noise is allowed to stray. Figure 1 shows how the SMPS couples to the mains and to the output lines.

fig. 1 Interference paths of a switch mode power supply
Large voltage swings occur in the primary winding of the power transformer T5. Connections to the switching transistors share part of the problem. Power supply designers will try to have capacitive currents circulate as much as possible inside the power supply. It is, however, impossible to decouple the power stage entirely from the case. Output rectification adds on to the problem because of diode noise and imperfect screening of the cabling and the transformer. Thus, in addition to the ripple that remains after the smoothing filter L1/C106, plus C110 and C109, the radio frequency potential of the entire output section varies somewhat with respect to ground. Due to the inherent asymmetry of the output section the radio frequency potential will not be the same when comparing positive and negative line. If one output line is grounded the resulting ground current will not be equal for positive and negative polarity grounding.

Standardised EMC measurements are done using 150 Ω terminations (valid for the standardised conducted noise spectrum) which is supposed to simulate the mains impedance. The result is not particularly relevant for physics detectors. Firstly, mains impedances at CERN are one to two orders of magnitude smaller because of the abundant presence of other power circuits and the close vicinity of large power transformers. Secondly, there is a widely spread tendency to ground the connected loads, i.e. the detector electronics, at the detector side. Both boundary conditions require entirely different impedances for measuring the actual common mode current.

Measurements in this paper were done using the configuration drawn up in fig. 2.

---

**fig. 2 Measurement configuration for SMPS noise assessment**
The mains impedance is simply neglected which reflects the conditions in the caverns to a large extent. One output polarity is grounded at the supply output, be it directly or via a resistor. This is, in terms of noise current, a worst case assumption. Low impedance grounding of the input circuitry will largely limit or even make impossible the development of any sizeable common mode voltage between mains input and ground. This effect "pushes" the common mode towards the load. For the common mode noise measurements a wide range current clamp is used to have access to the spectrum of the ground current under various conditions.

Measurements shown in fig. 3 show a slight common mode dependence on the polarity and some dependence on the load. The aim of the measurement is to determine whether or not a particular SMPS will be compatible with the immunity level of the electronics or system supplied. Measurements 4 and 5 (see fig. 3) detect the common mode noise when the SMPS is idling. The output asymmetry is visible but not dramatic. Bad quality SMPS would show much larger differences. Under load (measurement 8 and 9 in fig. 3) there is a broadening of the SMPS power pulses, a resulting different switching waveform and a more saturated operation of the magnetic elements. As a consequence the lower part of the spectrum, say, between 10 kHz and a few MHz, shows much higher noise generation. Whilst remaining within standards dictated by European Community decrees common mode noise now increases considerably. Common mode noise is conducted the better the lower the frequency becomes. It is this part of the spectrum that needs to be taken care of when treating the common mode problem. In particular, matching between the immunity spectrum (see section 4) and common mode generation would be advisable.

fig. 3 Conducted common mode noise of 5V 100 A SMPS grounded via a short lead. horizontal 5 MHz/div, vertical 10 dB/div a top line with reference level of –58 dBm (calibration: –60 dBm correspond to 0.45 mA)
The higher elements of the common mode noise spectrum do not show apparent differences between idling and loaded operation of the SMPS. A small difference for positive and negative grounding remains, however, visible even under load. This is the proof that, when this SMPS was designed, the output asymmetry has been thought of thoroughly.

SMPS of different manufacturers will have very distinct patterns of common mode generation. A second series of measurements, not shown in detail in this paper, indicated a strong polarity dependence of the noise spectrum. This second type of SMPS was evidently designed for negative grounding via short leads.

3) Measurement of common mode of switch mode power supplies followed by linear regulators

SMPS followed by linear regulators or long cables "see" a radio frequency impedance to ground that may be as high as a few kΩ. The resulting common mode currents now depend mainly on the impedance to ground seen by the non-regulated lead. This lead could have, for the radio frequency range, impedances in the kΩ-range. If used in an intelligent way the linear regulator following an SMPS may well be used for reducing common mode currents as much at it may reduce differential mode. Small common mode voltages may then develop without provoking currents above the immunity level of the front end to be supplied.

![fig. 4](image-url) Conducted common mode noise of 5V 100 A SMPS grounded via 5 kΩ horizontal 5 MHz/div, vertical 10 dB/div with a top line reference of –58 dBm (calibration: –60 dBm correspond to 0.45 mA)
Again there are four measurements, 10 and 11 (fig. 4) when idling, 12 and 13 (fig. 4) for two thirds of the nominal load. Grounding is done by connecting a 5 kΩ resistor between the negative lead and ground (measurements 10 and 12 in fig. 4) or between the positive lead and ground (measurements 11 and 13 in fig. 4). Common mode generation is the same as in chapter 2 but no common mode currents are allowed to develop. Any load supplied by a long cable may easily be kept free of SMPS-generated common mode noise if the asymmetric impedance (impedance to ground) is kept high according to common mode requirements established by a system policy or by immunity measurements.

It is stressed again that noise voltages have little effect provided they are not allowed to drive any noise currents over large loops. Noise and stray currents are easily accessible for precise measurement.

4) Common mode immunity

measurement of an electronics device

Front end boards are part of a system and need to reply to many boundary conditions. Grounding is necessary for many reasons. Grounding serves at the same time for safety equipotential, high level system reference, screen connection. It should, if ever possible, not be used for any power return.

The radio frequency potential difference between metallic enclosures and the board will be one of the ingredients for common mode. However, the largest “user” of the common mode budget, i.e. the ground connection(s), is the power supply system because of its inherent galvanic connection throughout the caverns and counting rooms. Some common mode on power supply lines inevitably strays everywhere, including on to the screens of signal input cables. Board analogue inputs and threshold lines are the most sensitive points.

Fig. 5 shows the sensitivity of a board's test pulse input to common mode noise. It does not matter where this common mode comes from. Measurements 1, 2, 3, 4 give the noise suppression capability of the board. The board's analogue output is connected directly to a spectrum analyser. Common mode is introduced on the test pulse line with a level of 0.1 V, 0.4 V, 2.5 V and 5 V respectively, over the frequency range of 0 - 100 MHz, on the current probe now used as a broad band signal transformer. A distinct pattern of noise sensitivity in the range of a few dozens of megahertz is clearly visible.

Fig. 5 Common mode immunity of front end test pulse input.

frequency 0 - 100 MHz, 20 dB/unit, top line reference level –88 dBm
Using the same method the noise sensitivity of the board was tested on all other connections leading to or from the board, such as analogue power return, digital supply lines, threshold input line. All other lines were found to have higher immunity to common mode. The weakest point remains at the board input where common mode must be kept below a level that may be derived from the dynamic range and the measured board immunity. The level of common mode noise present after final installation inside a detector depends on the ground impedances present at the connections of the board. Ground impedances are often to be considered like parallel impedances, hence the large confusion once the grounding system needs to be modified in order to achieve better noise performance. Stray ground currents originating outside the system under test usually are quickly found.

A radio frequency radiation test showed very little board radiation of max. 78 µA/m in the lower MHz-range. As a consequence the board would be immune up to even higher field levels due to reciprocity. Radio frequency irradiation over large frequency ranges may only be tested in screened rooms. This test was not performed.

5) Conclusion

The paper intends to establish a direct relationship between the noise generation by power supplies and the noise immunity of front end systems.
Both noise generation and immunity parameters may easily be determined using slightly modified EMC-procedures that reflect the situation inside the physics experiments.
EMC parameters allow designers to use cost effective SMPS even in delicate environments. Matching of SMPS and delicate load must be done over the entire frequency range that falls into either bandwidth. In case common mode noise is allowed to drive currents some power line radiation will occur.
Linear power supplies also generate noise. The common mode part is generally small because linear power supplies actively generate very little common mode noise. However, quite close coupling to the mains is established by the capacitance of the windings of the mains transformer (≈ 2 nF). Electrostatic screens reduce this coupling by a few orders of magnitude. Electrostatic screens therefore are mandatory for common mode and mains noise decoupling. It may also be shown that linear power supplies with long distance remote sensing show systematic limitations on the achievable noise performance.
Low Voltage Supply System for the Very Front End Readout Electronics of the CMS Electromagnetic Calorimeter

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Abstract

We use a two stages low voltage power supply system with remote sensing. Linear low voltage power supplies outside the cavern feed local voltage regulators housed in water cooled boxes inside the detector with significant power losses over around 120 m of therefore cooled cables. All voltages are floating and provided independently to groups of 50 crystals, two trigger towers. They are grounded at the detector end. Controls, overvoltage and overcurrent protection and fuses are integrated into the power supplies. Radiation tests on the low voltage regulator components were performed. A low voltage regulator has been built and tested.

1 Introduction

The barrel part of the CMS [1] Electromagnetic Calorimeter (ECAL) is composed of 61200 lead-tungstate crystals arranged in 36 super modules (SM) housing 1700 crystals each [2]. There are two end caps composed of 16000 crystals. After the crystal’s scintillation light is converted into an electrical signal, the readout electronics in the barrel and the end cap region are identical. Throughout this article mainly the barrel region is considered supposing a low voltage system (LVS) for the end caps will be derived from the barrel one at a later stage.

Groups of $5 \times 2$ crystals in $\eta \times \phi$ form a submodule read out by a Very Front End (VFE) module. A trigger tower consists of $5 \times 5$ crystals. Their energy is summed to provide first level trigger information. The LVS will be subdivided into independent Low Voltage Channels (LVCH). Each of them will power groups of 50 crystals corresponding to 2 trigger towers, corresponding to 5 VFE modules.

1.1 Requirements for the Very Front End Electronics

The VFE electronics requires four independent low voltages, $+5\text{V}$ and $-2\text{V}$ for the analog part and $+5\text{V}$ and $+2\text{V}$ for the digital part. Their expected currents (I) and the resulting power consumptions (P) are summarized in the following table:

\begin{center}
\begin{tabular}{|l|cccc|}
\hline
Voltage [V] & +5 & -2 & +5 & +2 \\
\hline
$I_{LVCH}$ [A] & 7.8 & 1.3 & 1.5 & 3.3 \\
$I_{SM}$ [A] & 264 & 43 & 51 & 111 \\
$I_{Barrel}$ [A] & 9486 & 1530 & 1836 & 3978 \\

\hline
$P_{LVCH}$ [W] & 38.8 & 2.5 & 7.5 & 6.5 \\
$P_{SM}$ [W] & 1318 & 85 & 255 & 221 \\
$P_{Barrel}$ [W] & 47430 & 3060 & 9180 & 7956 \\
\hline
\end{tabular}
\end{center}

The VFE electronics will be very sensitive to noise, especially to correlated noise as introduced by the power supplies because the energy of 25 crystals is summed as the trigger towers energy. Therefore linear power supplies are proposed in order to avoid all potential problems arising from the use of switching mode ones.

1.2 Environmental Constraints

The ECAL barrel is located inside the 4 Tesla superconducting magnet [3]. Behind the crystals an integrated dose up to 2Mrad and up to $5 \times 10^{13}$ n/cm$^2$ are expected at an integrated luminosity of $5 \times 10^6$ pb$^{-1}$. In addition the available space inside the detector is very limited. There is no space for the low voltage power supplies inside the SM's and only about $(800 \times 500 \times 150)$ mm$^3$ per SM about 4 m away from
the SM’s but still in the CMS magnet. Outside the
detector radiation levels and the magnetic stray field are
strongly depending on the location. There is sufficient
space at the galleries but still in a radiation environ-
ment of 100 rad absorbed dose and in a moderate mag-
netic field of 0.05 T. An important point is also the
accessibility of the system. To access the electronics
inside the detector, the entire end caps have to be re-
moved. Also the access to the electronics in the cavern
is limited to the shutdown periods of the accelerator. In
contrary there is always access to the counting house,
where radiation and magnetic field are negligible.

2 Low Voltage System Layout

The LVS is very complex taking into account the large
number of channels, 1224 for the barrel, the total re-
quired power of ~74kW for the ECAL barrel only and
the problems of radiation and magnetic field. So any
chosen solution includes advantages and disadvantages.
In addition the final LVS performance strongly depends
on its behavior in the CMS environment including the
interference with other parts of the detector and not
only on single blocks specifications.

We propose a two stage power supply system with
floating voltages and remote sensing in both stages,
as sketched in Figure 1. In the first stage linear low
voltage power supplies (LVPS) located outside the caver-
ner feed low voltage regulators inside the detector over
~120 m long cables. The LVR’s regulate the voltage
at the load in a distance of ~7 m, constituting the sec-
ond stage. This configuration is identical for all four
voltages required by the VFE modules. The grounding
will be performed at the detector end.

The major disadvantage of this solution is the huge
power loss in the system. In order to minimize this loss
the cables cross sections are increased in three steps
from the load back to the LVPS. A minimal power loss
at the LVR is achieved by regulating its input voltage.
But still the power losses in the cables and the LVR’s
are significant.

In Table 1 the different cross sections (A) of the cop-
er cables and the resulting voltages (U) and power losses (ΔP) for a single LVCH are summarized, with
the variables as defined in Figure 1. With 34 LVCH’s
in a SM this leads to power losses of ~200 W in the
cables inside the SM, ~240 W between the SM patch
panel and the LVR box, ~700 W in the LVR box and
~1400 W from the LVR box to the LVPS. Assuming an
efficiency of 50% for the linear LVPS’s the total power
consumption of the ECAL barrel will be ~350 kW,
leading to an overall efficiency of ~25%.

It is obvious that the entire system, including the
cables and the LVR’s requires water cooling. The cool-
ing system of the SM’s will remove the additional en-
ergy lost in the cables inside the SM’s themselves. The
LVR’s will be housed in water cooled boxes and the
cables are placed into water cooled channels. We are
investigating the possibility to use the return flow of
the SM cooling system for this purpose.

3 The Low Voltage Regulators

3.1 Radiation Test

As the low voltage regulators will be located inside
the detector it is mandatory that they survive radiation
doses up to 1 Mrad. Therefore a set of commer-
cial components was tested using the PSI Optis beam
[4] with 1.25 x 10^{9} protons/(cm^{2}s) of 64 MeV. This
simulates at the same time ionizing and nonionizing
About 2 hours operation at Optis beam correspond to 10 years of the expected irradiation for the ECAL VFE electronics at LHC. In particular we tested a SGR117A three-terminal type, positive, adjustable voltage regulator from Linfinity, a TLE4270 fixed voltage regulator from Siemens, a MC1723CP type regulator from Motorola, a SIPMOS-SPP30N03L power transistor from Siemens, a BTS6405S2 [5] semiconductor smart switch from Siemens and a IRFZ24N-HEXFET transistor from International Rectifier.

The components were tested on experimental setups under working conditions equivalent to their future use. All of them but the BTS6408S2 switch survived a minimum of 2 hours of irradiation. In Figure 2 the behavior of the SPP30N03L during ~140 minutes of irradiation is drawn for an output current of $I_{out} = 8$ A and an output voltage of $+5$ V, for an input voltage voltage of $U_{in} = 6.28$ V. The shift of the gate-source voltage, $V_{gs}$, is tolerable as it enables always a safe operation of the pass transistor. The output voltage was constant at $(5.001 \pm 0.001)$ V. Figure 3 presents the results for the MC1723CP low voltage regulator from Motorola during ~120 minutes of irradiation. The output voltage decreased nearly linearly with the irradiation by about 50 mV. This change is clearly correlated with the change in the reference voltage $V_{ref}$.

### 3.2 Prototype Layout

The failure of the BTS640S2 switch, which also includes fault protection features, in the irradiation test lead to a very simple design of the LVR. All additional functionality like switching of the output voltages, overvoltage and overcurrent protection and output current measurement were moved into the LVPS. The LVR serves one LV channel with a single PCB of $104 \times 77$ mm$^2$ containing four independent voltage regulators based on the MC1723CP type regulator and the Siemens-SIPMOS SPP30N03L pass transistor. The schematic layout is given in Figure 4.

It is forseen to add some means to measure the sensed voltage at the load and the $V_{gs}$ and to transfer them to the LVPS rack controllers.

### 3.3 Prototype Test Results

The LVR's frequency response was studied at the prototype board and with a SPICE model. Therefore the input to output transfer functions, the $+15$ V to output transfer functions, the output dynamic impedances, the output noise and the cross talk between the different channels for all four independent voltages were measured.

The LVR unity gain cross over frequency is about a few kHz depending on the gain of the MOSFET. The input to output transfer functions showed two maxima one just above the unity cross over frequency and the second one around $(100 - 500)$ kHz due to the self resonance of the regulator. The output noise was found to be around a few $\mu$V/3 kHz. The cross talk increased with the frequency.

### 3.4 LVR housing

For one ECAL super module 34 of the above described LVR boards are needed. As they will be located inside the cryostat it is mandatory that they are water cooled in order to remove the energy of 800 W per SM. Therefore a special housing, the LVR box, is constructed. It
is based on two aluminum plates, sandwiching a cooling pipe. Two rows of up to 9 LVR boards can be mounted on each side of the cooling plate. The pass transistors are directly screwed onto it. The box has a size of 800 × 500 × 150 mm³ and the two smallest side panels serve as input and output patch panels.

4 Low Voltage Power Supplies

4.1 General Layout

The LVPS’s have to match the modularity of the LVCH’s, in order to enable an individual control of the voltages and a measurement of their output currents. Thus the LVPS has to provide 4 voltages corresponding to +5V, −2V, +5V and +2V at the load. One transformer is feeding 4 independent channels composed of rectifier, filter and low voltage regulator with a pass transistor. Four additional windings with following rectifiers and stabilizers provide four +15V auxiliary voltages for the LVR. The system performs overvoltage, undervoltage and overcurrent protection and reacts on the over-temperature and other emergency signals. A block diagram is sketched in Figure 5.

The current and voltage protection functionality is based on the BTS64052 smart power switch. It has ground referenced input for switch ON/OFF, a diagnostic feedback status output and a sense voltage output proportional to the output current.

4.2 Technical Specifications

Each LVCH as described above provides the following main voltages: (+8.0 ± 1.0)V, (−3.9 ± 0.5)V, (+7.5 ± 0.9)V and (+4.1 ± 0.5)V, with the following maximal currents respectively: 12.0 A, 20 A, 2.3 A and 5.0 A. The input is standard AC 220 V. The line regulation for +10% and −20% of the AC input voltage has to stay below 0.5% and the load regulation below 1% of the output voltage. A maximum ripple and noise of 3 mV RMS and 30 mV peak to peak at the power supply output is tolerable. The supply provides adjustable overvoltage and undervoltage protection, a thermal shutdown at 85°C, soft turn on 0.5 s, fast turn

Figure 5: Block diagram of the low voltage system for one LVCH.

Figure 6: LVR box with LVR modules and cooling plate.
4.3 LVPS housing

Each ECAL barrel SM requires 34 of the above specified LVPS’s. They will be mounted into a 19" rack together with the rack controller. Having in mind the sizes of the main transformers and of the electrolytic capacitors it is possible to house six LVPS’s in one 19" 4 to 5 units high crate. Hence 6 crates per rack allow the installation of 36 LVPS’s. Their total power loss will be below the admissible 8kW. Each crate consists of a mechanical support structure with a connector backplane and built in AC/DC conversion units for 6 LVCH’s in the back part. In the front up to 6 Regulator modules can be inserted, serving one LVCH each. The front panel of them provides a status information via LED’s and contains all necessary switches and buttons. In addition the rack will contain the required fan units. The rack controller will be housed in a 4 to 5 units high crate. It includes a front panel display with control buttons, a rack ON/OFF button, a rack reset button and power and reset switches for the auxiliary voltages and the controller itself. A possible layout of the LVPS rack and the regulator module front panel is given in Figure 7.

5 Conclusion

The system design of a linear low voltage system for the CMS ECAL has been shown. Active components for the LVR withstanding the radiation have been identified. A prototype of the LVR board has been built and tested. The LVPS specifications are basically known and its design is in progress. We conclude that a linear LV is feasible with the known disadvantages of large power losses and thus a huge amount of cables.

References

ARE SWITCHING POWER SUPPLIES ACCEPTABLE FOR THE LIQUID ARGON CALORIMETER FRONT-END ELECTRONICS?*

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Abstract
Using high power density DC-DC converters followed by linear ripple attenuators could satisfy the power requirements of the Liquid Argon (LAr) calorimeter front-end electronics. A solution based on resonant charging DC-DC converters is discussed in terms of noise characteristics, radiation and magnetic field tolerance, power efficiency and reliability.

1. INTRODUCTION
The Liquid Argon (LAr) calorimeter system to be used in the ATLAS experiment has complex readout architecture composed of almost 190,000 high precision, high dynamic and low noise electronic channels. The global layout of the detector is shown in Figure 1. The central cryostat contains the barrel electromagnetic calorimeter (EM Accordion). Each end-cap cryostat houses an electromagnetic calorimeter (EM Accordion), two hadronic end-cap calorimeters and one forward calorimeter.

Figure 1. Three dimensional view of the LAr calorimeter system and the location of the front-end electronics

The front-end electronics, which process and prepare the detector signal for the “off detector” data acquisition system, is basically composed of preamplifiers, shapers, pipeline memory, digitisation and digital filtering. Different front-end crates are used for the three-calorimeter types. The majority of the crates serve the EM calorimeters. A typical crate contains 3584 readout channels densely packed in various boards. The power supply requirements for an EM crate are summarised in Table 1.

The large power consumption per crate, about 2.8 kW, combined with the limited space available in the detector area for the distribution of multiple low voltage power lines, jeopardise the use of linear power supplies located in the control rooms, i.e. far away from the detector, in favour of a solution which employs compact switching power supplies located in proximity of the front-end crate.

Table 1: EM crate power requirements

<table>
<thead>
<tr>
<th>Pin,1,6,10</th>
<th>Voltage [V]</th>
<th>Current [A]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ground</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>+6</td>
<td>180</td>
</tr>
<tr>
<td>3</td>
<td>+11</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>+6</td>
<td>24</td>
</tr>
<tr>
<td>5</td>
<td>+6</td>
<td>90</td>
</tr>
<tr>
<td>7</td>
<td>+4</td>
<td>105</td>
</tr>
<tr>
<td>8</td>
<td>-4</td>
<td>150</td>
</tr>
<tr>
<td>9</td>
<td>-6</td>
<td>12</td>
</tr>
</tbody>
</table>

2. “ON-DETECTOR” POWER SUPPLIES
Linear power supplies, which have been the traditional power sources in high energy physics experiments due to their stability and low output noise characteristics, have been generally mounted remotely from the detector location, in areas with no physical space and radiation environment constraints. This solution is based on the assumption that low or medium power must be distributed and/or that enough space is available for the power cables in the experimental area. Both assumptions are false for the Atlas LAr calorimeter system. With remote power supplies, the high power and the low voltages needed by the LAr read-out electronics, will require the use of massive water-cooled power cables which will not fit in the service area available for the detector. A different power supply system must be envisioned for the detector.

*The U.S. Department of Energy supports this work: Contract No. DE-AC02-98CH10886.
The diameter of the power lines could be substantially reduced if high voltage lines are run from the control rooms down to the detector region, where the conversion from high to low voltage lines could take place. The power supply system could be indeed composed of two parts: a source of high voltage power to be located remotely and a source of low voltage power mounted “on-detector”, i.e. as close as possible to the front-end crates. In this solution each electronic crate will have a dedicated low voltage power supply properly dimensioned to fit into the space available.

The high voltage supply can be implemented by using standard commercial supplies, while the low voltage power source needs to be specifically designed for the Atlas LAr requirements. The “on-detector” supply will not be easily accessible during the experiment and consequently must be extremely reliable with built-in redundancy and provision for external monitor and controls. Moreover the supply should have low output noise, operate in magnetic field and be radiation tolerant. High power density and efficiency are also important. Table 2 summarises the power supply specification.

Commercially available low noise DC-DC converters can in principle satisfy most of the above requirements. Few converters are able to operate in magnetic and radiation environments.

DC-DC converter modules made by VICOR Corporation, Andover, MA 01810, USA, have been measured against specification and the results are summarised in the following section.

3.  CONVERTER CHARACTERISTICS

3.1  Zero-Current-Switching

VICOR switching power supply modules make use of a patented resonant charging mechanism, called zero-current-switching (ZCS) [1]. Current flows through the MOSFET switch as half sine wave loops. The current is virtually zero both when the switch is closed and when it is opened. This result in a much less high frequency electromagnetic interference (EMI) than with conventional, fixed frequency switching power supplies. Any residual differential high frequency interference is easily removed by passive filtering.

VICOR converters can operate at frequencies in excess of 1MHz, with efficiencies greater than 80% and power densities of up to 7.3 W/cm^3. Two different series of VICOR DC-DC converter modules, with nominal input voltage of 300V, have been tested: the VI-200 series, or 1st generation modules, and the VI-300 series also called “2nd generation”. Both converter families share some common features such as availability of various standard programmable output voltages, stable regulation, current limit, internal overvoltage and overtemperature protection. All modules are parallelable with N+M fault tolerance and current sharing, and are phased-array-control compatible.

The second-generation modules contain a complete redesign of the control, magnetic, switching and packaging elements. The modules have also one-third the number of parts of the previous series [2].

The tested modules have output voltages from 5 to 12 VDC, similar to the ones of interest for the LAr power supply. For the VI-200 series the maxi size modules were tested, for the VI-300 series the maxi and mini size modules were tested.

3.2  Noise Characteristics

The virtually loss-less energy transfer from input to output achieved with the zero-current-switching technology greatly reduces the conducted and the radiated noise. The typical peak-to-peak (p-p) ripple noise of the VICOR converters for the output voltages of interest is ~ 100 mV on a 20 MHz bandwidth.

A large fraction of this noise concentrates above 10 MHz [3]. If a filter, the RAM module made by VICOR or an equivalent one, is added to the output of the converter, the noise reduces to less than 3 mV p-p. However questions remain to be solved in term of coherent noise contribution to the front-end electronics (FEB) noise due to the power supply. The issues to be proved are:

- Can the common mode high frequency switching signal be diverted from the input cables and preamplifiers on the FEB?

- Can the differential modulation at the switching frequency be reduced to a level where its noise contribution is negligible?

Measurements made using a VI-200 switching power supply on the most sensitive FEB supply, have shown that the coherent noise is ~ 56 μV rms compared to a random noise of 2.1 mV. The dominant coherent noise is a low frequency, almost sinuoidal ripple.

The additional low-voltage dropout regulators, foreseen for the FEB on-board filters, will virtually eliminate the already small residual ripple. No increase in coherent noise was measured by replacing linear power supplies with VICOR VI-200 DC-DC converters mounted in a MEGAPAC unit and followed by output
A 0.5% noise degradation was measured with the ripple attenuators filter bypassed.

Similar results should be expected for the VI-300 converter family.

3.3 Magnetic Field Sensitivity

Units from the VI-200 and VI-300 series were operated at Brookhaven National Laboratory in a uniform magnetic field adjustable from zero to $10^3$ gauss.

The parameters under measurements were the output voltage and the switching frequency of the device under test. The temperature of operation of the module was kept constant at $\sim 50^\circ$C during the test through proper air-cooling. The results were identical for both families of converters and are illustrated in Figure 2 and 3 for a VI-300 module with 5V output.

The performance of the converter depends from the relative orientation between the magnetic field and the module under test. Figure 2 illustrates that, when the magnetic field is orthogonal to the width of the module, the converter operates with minor variation in output voltage and switching frequency, up to 520 gauss. At higher field the unit shuts off and does not restart until the magnetic field is decreased below the critical intensity. However the worst condition happens when the applied field is parallel to the width of the module.

As shown in Figure 3, the converter operates correctly up to approximately 180 gauss, when it suddenly stops functioning. The failure is irreversible. A failure analysis performed by VICOR engineers found that one of the reset transistors of the unit was damaged by an excessive current flowing in the transistor during the main switch’s off time, the increase in current was very likely caused by the saturation of the main transformer core. The relative orientation between the magnetic flux confined in the transformer core and the external magnetic field could also explain the observed not-isotropic behaviour of the converter. The magnetic field lines interfere with the operation of the transformers inside the VICOR module mostly when they are parallel to the transformer cores and if all cores are oriented in the same direction, such as in this case.

3.4 Radiation Tolerance to Neutrons

Converters from both VICOR families have been irradiated with 1 MeV neutrons at the University of Massachusetts, Lowell, USA. The parameters measured during the test were again the output voltage and the switching frequency of the converter. Through proper air-cooling, the module temperature was kept constant at $\sim 50^\circ$C during the test. The results were very different for the two families of converters.

The VI-200 devices showed degradation almost immediately and failed in approximately 3 hours, at a total fluence of $\sim 3 \times 10^{11}$ n/cm$^2$. A second unit was subsequently irradiated at ten time lower fluence to exclude a fluence-dependent behaviour. This second unit also failed at the same total fluence. The damage was in both cases irreversible.

Failure analysis made by VICOR on the irradiated unit found that only the opto-coupler circuit in the converters had failed. Replacing the damaged opto-coupler with a new one successfully repaired both units. The standard opto-couplers used in the VI-200 units are commercial circuits, with no special precautions taken to make them rad-tolerant.

Neutron irradiation results were very different for the “2nd generation” VI-300 converters. As illustrated in Figure 4, for a VI-300 module with 5V output, this family of devices were able to withstand up to $\sim 1.3 \times 10^{13}$ n/cm$^2$ without noticeable degradations. The
control units in these “new” modules are made of bipolar integrated circuits without an opto-coupler circuit [4].

The measurements also indicate the presence of annealing effects related to the fluence. The irradiated converters showed a partial recovery after few days from the end of the test. However, no load current effects were measured.

At higher doses the units are less efficient, the switching frequency and the output voltage decrease more and more. At 1.1x10^13 Gy (110 krad) both characteristics reduce to ~ 50% of their original value. No recovery was observed after the conclusion of the test.

Second generation converters stop functioning at ~ 200-250 Gy (20-25 krad). The failure happens rapidly with no annealing.

The different behaviour of the two families is still unexplained. VICOR has indicated that the 2nd gen units use a “proprietary” integrated power MOSFET (IPD), which differ from the one used in the 1st gen converters [4]. This MOSFET is an unpacked device bonded directly to the converter substrate. The VI-200 family uses a MOSFET device packaged in a TO-220 case. No layout compatibility exists between the two converter families. The different layout prevents from swapping the MOSFET transistors between families.

4. CHOICE OF THE CONVERTER

4.1 Second generation unit advantages

The VI-300 converter family has some advantages respect to the VI-200 family.

The 2nd-gen converters have higher power per unitary volume, have an improved transformer design which should reduce common mode noise [2], have on-third the number of part of their predecessors and meet the experimental magnetic field and radiation environment constraints. However some of the specification is barely met. The extremely high power-density of these units leaves some space to introduce some “shielding” in the full size power supply.

4.2 Reliability Issues

The main argument in term of reliability is the drastic reduction in number of components used in the VI-300 family (from ~ 200 components to ~ 35 components).

The improved quality screening of the components, the improved thermal management between the transformer and the baseplate, the reduced thermal impedance from the IPD junction to the baseplate have improved the unit mean-time-between-failure (MTBF) up to 2.5 million hours at 25°C.

Moreover the built-in protection and the current sharing capability allow N+M fault tolerance architecture.

The units will be anyway “components out of the shelf”, a quality assurance procedure need to be defined to avoid properties variation from batch to batch. The quality assurance should be mostly performed at full size prototype instead that at single element level.

More measurements are needed to study single event effects (SEE).
4.3 Toward a prototype

A “six-voltages six-currents” power supply for a full front-end crate could be made by using 24 VICOR 2nd-gen modules in a configuration which will guarantee 100% redundancy. Twelve converters will be active all the time while 12 units will be on stand-by and ready to start in case of a failure. The maximum deliverable current will exceed by 10% the maximum nominal crate current.

Each voltage will have an input section to regulate the 300V DC input and an output section to achieve the output ripple specification. All the components used in this IN/OUT circuit will be evaluated for radiation tolerance. The converters will be mounted on three cooling plates and each cooling plate will dissipate the same power.

The limited magnetic field and ionising radiation tolerances of the tested modules will require additional “shielding” in the full size prototype.

The location of these “on-detector” power units must be carefully estimated to minimise environmental specification.

The supply control and monitoring electronics will be compatible with the slow-monitor system accepted by the LAr collaboration.

5. CONCLUSIONS

The commercial VICOR 2nd gen DC-DC converters, family VI-300, meet all the power supply specification for the LAr calorimeter system. However VICOR provides only the bare DC-DC converters. The modules need to be properly “packaged”; IN/OUT and control circuits must still be designed. An industrial counterpart interested in this application has been identified and a full size supply has been proposed.

Preliminary coherent noise measurements indicate that a power supply based on these DC-DC converters should be indistinguishable from a linear power supply, provided proper output filtering.

6. ACKNOWLEDGMENTS

The authors wish to thank F. De Giso and K. Nardone of VICOR Corporation for the fruitful discussions and the help provided. F. Densing, D. De Simone and G. Kegel for the assistance during the tests of the converters.

7. REFERENCES

4. K. Nardone, private communication.
RADIATION HARDENED POWER ELECTRONICS
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ABSTRACT
Previous options for radiation-hardened power electronics have been mostly limited to expensive, bulky discrete designs or modules, typically built from up-screened commercial devices. The Intersil Rad-Hard Silicon Gate (RSG) process has been used to design the industry's first family of guaranteed Rad-Hard Power Management “building block” ICs for use in all forms of radiation environments. These devices are capable of providing highly reliable performance in critical power control circuits at reduced cost and size.

1. INTRODUCTION
A new family of devices is under development at Intersil that provides the basic functions needed for power switching, DC-DC conversion and motor control circuits[1]. Most are designed to be guaranteed Rad-Hard (300Krad (Si) minimum), enhanced performance replacements for their commercial equivalents, which are commonly used in many rad-hard applications. The last device that will be described, the HS-802805RH, combines several of these “building blocks” to provide a new solution for radiation-hardened power supply problems.

2. RSG PROCESS DESCRIPTION
The process that will be used for most of these products, RSG (Rad-Hard Silicon Gate), offers a large variety of MOS and bipolar devices suitable for medium to high voltage analog, mixed signal and power applications. RSG is a fully complementary BiCMOS-on-insulator process which uses Intersil's dielectric isolation (DI) starting material to produce high quality vertical complementary bipolar, medium voltage CMOS, high voltage bipolar and MOS devices and a variety of signal and reference diodes, thin film and diffused resistors and capacitors.

3. PRODUCT DESCRIPTIONS
This family of products, listed in Tables 1 and 2, and briefly described here, are intended to provide explicitly radiation hardened equivalents to industry standard IC types and provide new levels of combined hardness, integration and overall reliability. The 110V CMOS and DMOS transistors available on the RSG process enable the direct control of high voltage power MOSFETs. Dielectric Isolation, SOI technology provides Single Event Latch-Up (SEL) immunity, and vertical PNP and NPN geometries virtually eliminate the radiation effects common in many commercial, lateral PNP structures.

<table>
<thead>
<tr>
<th>Table 1: Available Intersil Rad-Hard Power Products</th>
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<tr>
<td>Device #</td>
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<tr>
<td>HS-1840ARH</td>
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<tr>
<td>HS-139RH</td>
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<tr>
<td>HS-3530ARH</td>
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<td>HS-4423RH</td>
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<td>HS-4424RH</td>
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<td>HS-1825ARH</td>
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<td>HS-2100RH</td>
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<td>HS-117RH</td>
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<td>HS-4080ARH</td>
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<th>Table 2: Intersil Rad-Hard Power Roadmap</th>
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<tr>
<td>Device #</td>
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<td>HS-705RH</td>
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<td>HS-201HSRH</td>
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<td>HS-1009RH</td>
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<td>HS-DG403RH</td>
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<td>HS-DG405RH</td>
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<td>HS-1715ARH</td>
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<td>HS-1845ARH</td>
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<tr>
<td>HS-2981RH</td>
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<td>HS-802805RH</td>
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The following descriptions are of the products that are currently available[2].

3.1 HS-1840ARH

The HS-1840ARH, a 16 channel analog multiplexer, is a redesign of the HS-1840RH with improved performance, including improved analog input overvoltage protection and input impedance during power loss. It is designed to provide a high input impedance to the analog source if device power fails (open), or the analog signal voltage inadvertently exceeds the supply by up to 35V, regardless of whether the device is powered on or off.

The HS-1840ARH is excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. The device is available in a 28 lead side-brazed DIP and a 28 lead ceramic Flatpack.

3.2 HS-139RH

The HS-139RH is a quad voltage comparator that is a pin for pin replacement for the industry standard 139. It consists of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply, and the low supply current (< 2mA) makes these comparators suitable for low power level shifting or analog to digital conversion applications. The HS-139RH is available in either a 14 lead side-brazed DIP or a 14 lead ceramic flatpack.

3.3 HS-3530ARH

The HS-3530ARH is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as 3V may be used with little degradation of AC performance.

A major advantage of the HS-3530ARH is that operating characteristics remain virtually constant over a wide supply range (3V to 15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters. This device is available in either an 8 lead CAN or a 10 lead ceramic flatpack.

3.4 HS-442xRH Family

The HS-4423RH and HS-4424RH are the base products of a family of dual FET Drivers. The HS-4423RH is a pin for pin replacement for the Micrel 4423, a dual inverting 3A FET Driver. However, the HS-4423RH is designed to convert TTL signals into high current output that can drive up to a 4300pF load from 0V to 18V in less than 50ns. The fast rise and fall times and high current outputs allow very quick control of high gate capacitance power MOSFETs, thus minimizing switching power losses. The HS-4424RH, a non-inverting dual FET driver with the same ac and dc specifications, is also available and, if there is sufficient customer demand, a complementary version, the HS-4425RH can be made available with a very short lead time.

The HS-442xRH family also features several Low Voltage Lock Out (LVLO) options that put the outputs into a tri-state mode if the power supply dips below a certain voltage, preventing the possibility of MOSFET burnout. These dual devices can also have their inputs and outputs paralleled in order to create a single 6A driver. The HS-442xRH family is available in a 16 pin ceramic flatpack that is outline compliant with the industry standard 16 pin SOIC.

3.5 HS-1825ARH

The HS-1825ARH Regulating Pulse Width Modulator (PWM) is an enhanced replacement for several industry standard types and is specially designed for switching power supply and servo applications. It can be used in either current-mode or voltage-mode operation, and is especially well suited for single-ended boost converter applications.

Device features include a precision voltage reference, low power start-up circuitry, a high frequency oscillator, a wide-band error amplifier, and a fast current-limit comparator. The BiCMOS design results in fast propagation delays times and high output current over a wide range of output voltages. The HS-1825ARH is available in a 16 lead ceramic flatpack.

3.6 HS-2100RH

The HS-2100RH is a high frequency, 100V Half Bridge Driver that is a rad-hard pin-for-pin version of the Intersil HIP2500 Half Bridge Driver and a replacement for the IR2110. Its targeted applications include PWM
amplifiers/servodrivers and synchronous rectified power converters. It also features 2A output drive and a high side output that can be offset to 120V. The low-side and high-side gate drivers are independently controlled, giving the user maximum flexibility in dead-time selection and driver protocol.

In addition, the HS-2100RH has on-chip error detection and correction circuitry which monitors the state of the high-side latch and compares it to the HIN signal. If they disagree, a SET or RESET pulse is generated to correct the high-side latch, thus protecting the high-side latch from single event upsets. This prevents both the high-side and low-side MOSFETs from being on at the same time. The HS-2100RH is available in a 16 lead ceramic flatpack.

3.7 HS-117RH

The HS-117RH Voltage Regulator, a radiation hardened equivalent to the industry standard LM-117, is an adjustable positive voltage linear regulator capable of operating up to 40VDC. The output voltage is adjustable from 1.2V to 50V with two external resistors. The device is capable of sourcing from 50mA to over 1.25A peak current. Protection is provided by the on-chip thermal shutdown and output current limiting circuitry. The HS-117RH is available in a 3 terminal TO-257 package.

3.8 HS-4080ARH

The HS-4080ARH is a rad-hard version of the Intersil HIP4080A Full Bridge Driver. It features 2A outputs that drive 4 external N-Channel MOSFETs in a full bridge configuration, with user programmable dead time to decrease switching power loss. An on-board charge-pump can maintain an upper supply maximum voltage of 95V while operating from a single 12V supply. Its targeted applications are PWM motion/motor control and dc-dc converters, but it can also drive medium voltage motors.

The HS-4080ARH includes a TTL-level input comparator with an output pin (OUT), which can be used to facilitate hysteresis and PWM modes of operation. The DIS pin disables gate drive to all outputs regardless of the command states of the input pins, IN+ and IN-. Its HEN input can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. To simultaneously modulate both upper and lower drivers, HEN is continuously held high while modulating the IN+ and IN- pins.

A combination of bootstrapping and internal charge pumps allow for use as drivers for simple N-Channel high-side switches. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs. There are two charge pump circuits in the HS-4080ARH, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 50uA to 75uA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp (<15V).

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected N-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V. The gate driver design allows for very short propagation delays while nearly eliminating all gate driver shoot-through which significantly reduces IC power dissipation.

The HS-4080ARH also incorporates a Low Voltage Lockout (LVLO) feature that disables the outputs if the supply voltage drops below 9V. The outputs are re-enabled when the supply voltage returns to above 9.5V. This device is packaged in a 20 lead ceramic flatpack.

The following devices are currently under development at Intersil and should all be available in the next few months.

3.9 HS-705RH

The HS-705RH Power Down Reset is pin for pin compatible with industry standard types will be available in a 14 lead ceramic flatpack. It monitors the power supply and battery voltages in microprocessor systems and provides a reset signal during power-up and power-down and features a “watchdog” circuit and a power fail threshold detector. The threshold detector input (PFI) may be used to monitor power supply failure or low battery conditions.

The HS-705RH will be built on a sub-micron CMOS process in order to achieve 3.3V operation, and is radiation-hardened by design to 300Krad (Si).

3.10 HS-201HSRH

The HS-201HSRH Quad SPST Switch is the first in a planned family of high-speed, rad-hard, analog switches with very low ON resistance. The fours switches are independently selectable and pin compatible with the industry standard HI-201HS switch. The part is designed to accept CMOS as well as TTL-level input signals while passing a wide analog signal range of +/-15V. Overvoltage protection/power down high impedance and ESD protection is also incorporated into the design.
Other planned switches for this family include a dual SPDT (HS-DG403RH) and a dual DPST (HS-DG405RH). These parts will be packaged in both a 16 lead side-brazed DIP and a 16 pin ceramic flatpack.

### 3.11 HS-1009RH

The HS-1009RH is a 2.5V shunt regulator diode designed to provide an exceptionally stable 2.5V reference over a wide current range and to maintain that stability over the full military temperature range and over time. A 0.2% reference tolerance is achieved by on-chip trimming. An adjustment terminal is provided to allow for the calibration of system errors. The use of this terminal to adjust the reference voltage does not affect the temperature coefficient. The HS-1009RH will be available in a TO-46 3-terminal package.

### 3.12 HS-1715ARH

The HS-1715ARH Complementary Switch FET Driver is an enhanced replacement for the UC1715. It generates true and complement signals from a single input that is PWM and TTL compatible, with user-programmable dead time between the outputs. The HS-1715ARH will also have 1A minimum output drive from both outputs, with both outputs also being tri-stateable.

The HS-1715ARH is designed to provide drive waveforms for complementary switches, which are commonly used in synchronous rectification circuits and active clamp/reset circuits. In order to facilitate zero-voltage switching, independently programmable delays between the two output waveforms are provided. This device will be packaged in a 16 pin ceramic flatpack.

### 3.13 HS-1845ARH

The HS-1845ARH, a current mode Pulse Width Modulator, is designed to be a radiation hardened pin for pin replacement for the UC1845. This PWM controller provides the necessary features to implement off-line or DC-DC fixed frequency current mode control schemes with a minimal external parts count. Features include Low Voltage Lock Out (LVLO) with a start up current of less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and an output stage designed to source or sink high peak current. The HS-1845ARH will be packaged in 14 lead ceramic flatpack.

### 3.14 HS-2981RH

The HS-2981RH, an 8-channel source driver replacement for the UDN2981, is recommended for high-side switching applications that benefit from separate logic and load grounds. This device, which is built on a high voltage bipolar process, and is only hard to 100Krad (Si), encompasses load supply voltages to 80V and output currents to -500mA. This 8-channel source driver is useful for interfacing between low-level logic and high-current loads, such as relays, solenoids, lamps, and stepper/servo motors. The HS-2981RH will be packaged in an 18 lead ceramic flatpack.

### 3.15 HS-802805RH

The HS-802805RH 80W DC-DC power converter is the first in a series of radiation-hardened, high reliability power supplies to be offered by Intersil[3]. These power supplies utilize several of the circuits previously discussed as part of a single transistor forward topology with synchronous rectification to obtain the highest possible efficiency (near 90%) and best dynamic performance.

The HS-802805RH utilizes two DC-DC converters to optimize power conversion efficiency and facilitate voltage sequencing necessary to protect other circuits during power-up and power-down. It has a supply range of 18 to 40 volts, and can generate an adjustable main output voltage of 4 to 6 volts, at up to 16A, and a nominal -5 volts and up to 500mA at the auxiliary terminal.

Also provided are output inhibit functions referenced to either input or output and synchronization capability that allow these units to be easily integrated into larger distributed power systems. These supplies are targeted to be approximately 6 in^3 and weigh less than 250 grams.

### SUMMARY

A new family of devices is under development at Intersil that provides the basic functions needed for power switching, DC-DC conversion and motor control circuits. They are designed to be guaranteed rad-hard, enhanced performance replacements for their commercial equivalents, which are commonly used in many rad-hard applications.


### REFERENCES

2. Intersil Data Sheets.
3. Intersil Rad Hard DC-DC Converter Brochure.
Preliminary test for radiation tolerant electronic components for the LHC cryogenic system.

J. A. Agapito¹, F. M. Cardeira², J. Casas¹, A. Duarte³, A. P. Fernandes², F. J. Franco³, M. J. Gil¹, P. Gomes¹, I. C. Gonçalves³, A. Hernández Cachero¹, U. Jordung¹, M. A. Martín³, J. G. Marques³, A. Paz³, A. J. G. Ramalho³, M. A. Rodríguez Ruiz¹ and J. P. Santos³.

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Abstract

The LHC accelerator will use about 1600 main superconducting magnets operating below 2K. The magnets temperature is a control parameter and its target accuracy imposes very severe constraints on both the sensing element and its signal conditioner. They will both be installed inside the tunnel, thus exposed to a relatively high neutron fluence and gamma dose. It is then crucial to understand the effects of radiation on the performance of the electronic components that will be selected for the signal conditioner. This paper presents data concerning the radiation effects on typical active and passive discrete electronic components. This is the first step toward building a radiation tolerant signal conditioner.

1. INTRODUCTION

The typical signal levels involved in the measurement of resistive type cryogenic temperature sensors are in the millivolt range, with measuring accuracy of about 0.5%, imposing the use of low-noise instrumentation amplifiers. These devices are usually fabricated in bipolar technolo-

gies that according to the literature may exhibit a significant degradation when exposed to the LHC tunnel environment. For 10 years of operation of the LHC machine the expected neutron fluence is $2 \times 10^{13}$ n·cm$^{-2}$ and the gamma dose is 500 Gy.

In order to evaluate and design radiation tolerant electronic systems, irradiation campaigns are being performed both at the Portuguese Research Reactor, RPI (at ITN, Portugal) and at CERN. The investigated components include passive and active devices under normal operating conditions.

2. IRRADIATIONS AT ITN

For these experiments, the reactor is operated at a reduced power of 2.5 kW, so that the fluence of $5 \times 10^{13}$ n·cm$^{-2}$ is reached in about 5 days, with 14h operation + 10h stand-by per day. The components under test were mounted on several PCBs, placed inside a hermetic Al cylindrical container, immersed in the reactor pool. The container is lined internally by 1mm of Cd (to cut thermal neutrons) and surrounded by a 20mm thick Pb shield (to reduce the fission gamma field). It is placed in front of the reactor core, with its longitudinal axis perpendicular to the reactor face.

The neutron fission fluxes were measured with Ni detectors placed at the centre of the boxes that contained the PCBs. They are based on the averaged neutron cross section for the reaction $^{58}$Ni + n $\rightarrow$ $^{58}$Co + p in a $^{235}$U fission spectrum. Figure 1 shows the measured flux distribution along the container’s axis, as a function of the distance from each box to the container’s inner face closest to the reactor core. A photodiode sensitive to neutrons was placed in one of the boards, so that the neutron fluence was monitored online.

Gamma radiation both from fission and background origin is present when the container is immersed in the pool. Integration dosimeters placed on the back of each PCB reveal, after the completion of the tests, a total gamma dose between 17kGy and 3.5kGy.

Three campaigns have been performed, measuring passive and active components. Precision and standard thin film resistors, different types of capacitors, discrete active components and operational amplifiers were tested in the different periods. On-line measurements were performed by UCM before, during and after irradiation and stand-by periods, to evaluate the neutron and gamma irradiation damages as well as annealing effects.

2.1 Amplifier models and test set-up

Online measurements have been made on the following types of Amplifiers: Bipolar (OP27E, OP27F, OP77), JFET (TLE2071, LF351, LF356), DIFET (OPA111,
OPA124), LinCMOS (TLC2201) and Instrumentation (AD620, AD621, AD624). Figure 2 shows the proposed amplifier model [1], where:

- \( V_+ \), \( V_- \) and \( \text{OUT} \) are, respectively, the non-inverting input, the inverting input and the output voltages.
- \( V_{os} \) is the input offset voltage
- \( I_b \) is the input bias current
- \( I_{os} \) is the input offset current.
- \( R_i, R_o \) are, respectively, the input and output resistances
- \( G_{ol} \) is the open loop gain, for operational amplifiers, or the externally controlled gain, for instrumentation amplifiers.
- CMRR is the common mode rejection ratio.

![](image)

Figure 2: Operational Amplifier model

To measure the amplifier characteristics a standard test set-up is used [2], Figure 3. It permits online measurements of \( V_{os}, I_b, I_{os} \) and \( A_{vl} \) (closed loop gain). A set of electromechanical, relays remotely controlled, selects the adequate configuration to measure each parameter.

![](image)

Figure: 3 Layout for Opamps parameters measurement

The PCBs inside the container are connected to the measuring system through a 20 m long shielded cable, with 50 twisted pairs of wires. Monitoring instrumentation incorporates an I-V source-measure unit, a digital voltmeter and a computer controlled switching system. A complete measurement cycle is performed every 20 minutes. The accuracy of measurements is 0.5% for \( A_{vl} \), 1% for \( V_{os} \) and 5% for \( I_b \) & \( I_{os} \).

### 2.2 Results

All the characteristics of the amplifiers changed with radiation. Their variation with neutron and gamma radiation depends on the fabrication technology. Moreover, some amplifiers are destroyed after ending the radiation exposure. There is a large reduction of open loop gain but adequate performance is observed for closed loop gains below 100.

Low frequency bipolar amplifiers (Table 1, Figure 4) show a linear growth of offset voltage up to a critical radiation dose, with an exponential annealing during stand-by periods. For higher doses, the offset voltage grows exponentially and the bias and offset currents degrade drastically.

<table>
<thead>
<tr>
<th>( n_{cm}^2 )</th>
<th>( 0 )</th>
<th>( 10^{10} )</th>
<th>( 2 \times 10^{11} )</th>
<th>( 5 \times 10^{11} )</th>
<th>( 10^{12} )</th>
<th>max</th>
</tr>
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<tbody>
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<td>1.15-26</td>
<td>22-48</td>
<td>53-125</td>
<td>1.1-4.0</td>
<td>3.2 – 4.9</td>
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<tr>
<td>( A_{vl} )</td>
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<td>100.3</td>
<td>100.3</td>
<td>100.5</td>
<td>100.8</td>
<td>100.9</td>
</tr>
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<td>100.7</td>
<td>100.6</td>
<td>100.6</td>
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</tr>
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<td>( V_{os} (\mu V) )</td>
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<td>101.2</td>
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<td>101.2</td>
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<td>-400</td>
<td>-290</td>
<td>-110</td>
<td>-110</td>
</tr>
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<td>1770</td>
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<tr>
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</tr>
<tr>
<td>&amp;</td>
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<td>80</td>
<td>430</td>
<td>1060</td>
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<td>&amp;</td>
<td>-10</td>
<td>130</td>
<td>230</td>
<td>140</td>
<td>160</td>
<td></td>
</tr>
</tbody>
</table>

| \( I_{lb} (nA) \) | -20 | 360 | 1680 | 4630 | 7670 |
| & | 0 | 90 | 320 | 1040 | 1580 |
| & | -15 | 120 | 340 | 820 | 1770 |
| & | -10 | 630 | 1500 | 4420 | 6980 |
| & | 10 | -20 | -20 | -30 | -30 |
| & | 0 | 60 | 230 | 730 | 1250 |

| \( I_{os} (nA) \) | 15 | 290 | 1380 | 3810 | 6290 |
| & | 0 | -1 | -1 | -1 | 0 |
| & | 0 | -11 | -16 | -14 | 6 |
| & | -10 | 540 | 1280 | 3710 | 6230 |
| & | 0 | 20 | 40 | 50 | 50 |
| & | 0 | 50 | 60 | 70 | 50 |

![](image)

Figure 4: Bipolar operational amplifier
JFET input bipolar amplifiers (Table 2, Figure 5) show a variation in offset voltage that depends on the sample and its behaviour is not understood. Bias current grows parabolically, due to the variation of the carriers recombination time with the accumulated radiation [3]:

\[ \tau_c = \tau_{0c} + K \cdot \Phi(t) \]

The input current is that of a reverse-biased pn junction, thus:

\[ I_i = I_{0i}(1 + k \cdot \Phi(t))^{1/2} \]

During reactor stand-by time, an exponential annealing is observed, reducing the bias current, that may be attributed to the partial vanishing of lattice defects. There is also a linear relationship between the bias current after annealing and the total accumulated dose.

Table 2: JFET TLE 2071 (Max. Tol. 3.5-10^{13} n-cm^-2)

<table>
<thead>
<tr>
<th>ncm^-2</th>
<th>0</th>
<th>10^{12}</th>
<th>2-10^{12}</th>
<th>5-10^{12}</th>
<th>10^{12}</th>
<th>35-10^{12}</th>
</tr>
</thead>
<tbody>
<tr>
<td>kGy</td>
<td>0</td>
<td>1.13</td>
<td>.22-48</td>
<td>.53-2.5</td>
<td>1.1-4.0</td>
<td>6.6-7.8</td>
</tr>
<tr>
<td>Aref</td>
<td>99.6</td>
<td>99.8</td>
<td>99.5</td>
<td>99.7</td>
<td>99.4</td>
<td></td>
</tr>
<tr>
<td>100.5</td>
<td>100.7</td>
<td>100.8</td>
<td>100.6</td>
<td>100.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.6</td>
<td>100</td>
<td>99.8</td>
<td>100</td>
<td>99.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100.3</td>
<td>100.1</td>
<td>100.2</td>
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<td></td>
</tr>
<tr>
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<td>101.5</td>
<td>101.4</td>
<td>101.5</td>
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</tr>
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<td>100</td>
<td>100.8</td>
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<td></td>
<td></td>
</tr>
<tr>
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<td>-760</td>
<td>-870</td>
<td>-820</td>
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<tr>
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<td>5850</td>
<td>4980</td>
<td>1780</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DiFET amplifiers (Table 3, Figure 6) show an increase in offset voltage with radiation, but the variation is sample dependent. Gamma radiation is probably the origin of a fast variation in offset and bias currents initially due to positive SiO2 trapping charge accumulation effects until they are compensated by the Si-SiO2 interface charge generation for higher doses.

Table 3: DiFET OPA111 (Max. Tol. 3.3-10^{13} n-cm^-2)

<table>
<thead>
<tr>
<th>ncm^-2</th>
<th>0</th>
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<th>2.10^{12}</th>
<th>2.10^{13}</th>
<th>5.10^{13}</th>
<th>10^{14}</th>
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<tbody>
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<td>kGy</td>
<td>0</td>
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<td>.27-79</td>
<td>.61-1.8</td>
<td>2.0-3.5</td>
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<td>100.5</td>
<td>100.6</td>
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</table>

![Figure 5: JFET Operational amplifier](image)

![Figure 6: DiFET Operational amplifier](image)

LinCMOS amplifiers (Table 4, Figure 7) increase their offset voltage with radiation. Offset current increases until reaching a fluence of 1.2·10^{14} n/cm^2; where the current variation is inverted. Four of the tested samples were destroyed above 1.68·10^{14} n/cm^2, probably due to the relatively high level of gamma radiation.
Table 4: LinCMOS TLC2201 (Max. Tol. 1.68·10¹¹ n·cm⁻²)

<table>
<thead>
<tr>
<th>n·cm⁻²</th>
<th>0</th>
<th>10¹⁰</th>
<th>2·10¹⁰</th>
<th>5·10¹⁰</th>
<th>10·10¹⁰</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>kGy</td>
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<td>13.26</td>
<td>22.48</td>
<td>53.25</td>
<td>1.1·10³</td>
<td>3.7·10³</td>
</tr>
<tr>
<td>Aᵥₒ</td>
<td>100.7</td>
<td>100.9</td>
<td>101.0</td>
<td>100.2</td>
<td>100.8</td>
<td></td>
</tr>
<tr>
<td>Vₒ(nV)</td>
<td>100.9</td>
<td>101.0</td>
<td>101.1</td>
<td>101.4</td>
<td>101.3</td>
<td></td>
</tr>
<tr>
<td>Vₒ(nA)</td>
<td>100.2</td>
<td>100.2</td>
<td>99.9</td>
<td>100.6</td>
<td>100.2</td>
<td></td>
</tr>
<tr>
<td>Iₒ(nA)</td>
<td>3·10¹³</td>
<td>3·10¹³</td>
<td>3·10¹³</td>
<td>3·10¹³</td>
<td>3·10¹³</td>
<td></td>
</tr>
</tbody>
</table>

Table 5: Instrument. AD624 (Max. Tol. 4·10¹³ n·cm⁻²)

<table>
<thead>
<tr>
<th>n·cm⁻²</th>
<th>0</th>
<th>10¹⁰</th>
<th>2·10¹⁰</th>
<th>5·10¹⁰</th>
<th>10·10¹⁰</th>
<th>max</th>
</tr>
</thead>
<tbody>
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<td>kGy</td>
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<td>18.32</td>
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<td>1.5·10³</td>
<td>4.7</td>
</tr>
<tr>
<td>Aᵥₒ</td>
<td>99.1</td>
<td>99.2</td>
<td>99.2</td>
<td>99.4</td>
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</tr>
<tr>
<td>Vₒ(nV)</td>
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<td>100.1</td>
<td>99.3</td>
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</tr>
<tr>
<td>Vₒ(nA)</td>
<td>-30</td>
<td>-180</td>
<td>-300</td>
<td>-90</td>
<td>-30</td>
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<tr>
<td>Iₒ(nA)</td>
<td>-30</td>
<td>-180</td>
<td>-300</td>
<td>-90</td>
<td>-30</td>
<td></td>
</tr>
</tbody>
</table>

Instrumentation amplifiers AD620 and AD621 were destroyed at low neutron fluences below 10¹² n·cm⁻². According to the literature much better hardness is obtained when using faster bipolar devices. This partially explains the good performance of AD624 (Table 5, Figure 8) that has better frequency characteristics. However one AD624 sample was destroyed at 10¹¹ n·cm⁻².

Thin film resistors, both high and ordinary precision types, are not affected by radiation and show a variation lower than 0.1%. Only some potentiometers exhibited a higher degradation, although below 0.7%.

DC-DC converters, loaded at 40%, changed the output voltage linearly with radiation. During the stand-by period after radiation there was an exponential annealing, without recovering their initial value. Figure 9 shows the voltage variation of a multiple output dc-dc source as a function of temperature and neutron fluence.
3.1 Test setup

The control and acquisition computer, measurement instrumentation and power supplies are installed in a control room 150m away from the irradiation area. The power input to each device under test is protected with a dedicated fuse, to avoid a general disruption of the supply in case of a latch-up.

In order to cope with the large number of readout channels, a multiplexing system was designed and installed near to the irradiated samples. It consists of 17 scanner cards, each sequentially selecting one out of ten 4-wire channels. Five cards are used to scan the passive components to be read from each board. Each of the remaining twelve cards is used to connect 1 out of 10 different resistors to each conditioner’s input.

The design of the multiplexing system took into account the TCC2 radiation level. Each card is made out of ten 4-contact relays, driven by high-frequency bipolar transistors and selected by a modulo-10 CMOS counter. They are still fully operational.

3.2 Results

All resistors (2x 10 high-precision and 2x 7 ordinary-precision) and (2x 3) potentiometers survive 650 Gy + 17·10^{11} n·cm^{-2} with no appreciable degradation (ΔR/R < 0.05%). Among 10 ceramic and electrolytic capacitors, some show a small initial drift and then stabilise at ΔC/C ≈ 1%; others degrade less than 0.5%.

Two samples of ISOR-80-C™ resistance to 4-20 mA signal conditioners, from Steiner Technik, show the gain increasing linearly with dose (600ppm/Gy), up to 200 Gy + 5·10^{11} n·cm^{-2}. Above 250 Gy the output derives fast to saturation and becomes unusable.

Four samples of IPAC-L™ resistance to 4-20 mA signal conditioners, from INOR show the output offset increasing linearly with dose (4μA/Gy), up to about 25-100 Gy + 0.7-2.6·10^{11} n·cm^{-2}. At this point, the gain drops to zero and the devices become unusable. However, one of the samples recovered but after a short irradiation period was definitely broken.

Two samples of IPAC-4L™ resistance to 4-20 mA signal conditioners, from INOR, show the output offset increasing linearly with dose (-0.4μA/Gy), up to about 40 Gy + 0.1·10^{11} n·cm^{-2}. At this point, the gain drops slightly and the offset maintains the same behaviour until 100 Gy + 2.6·10^{11} n·cm^{-2}, when the device is suddenly destroyed. Occasional ±6μA offset jumps suggest upsets in an 11.5bit ADC or DAC.

Two samples of LIN-multirange conditioners [5] are destroyed after 270 Gy + 7.1·10^{11} n·cm^{-2} where the output drops to 4mA. One of the samples has 2 range-indicator optocouplers, which voltage decreases exponentially reaching -50% at 50 Gy + 1·10^{11} n·cm^{-2}.

One sample of the T2F conditioner [5] show a degradation below 6%; the other sample had the output abruptly stopped at 40 Gy + 1·10^{11} n·cm^{-2}, while internally operational; it recovered after 3 weeks annealing.

Two samples of LOG conditioners [5] show a degradation below 2.5%, difficult to distinguish from ambient temperature induced drift.

REF02 (5V reference) from BURR-BROWN, shows a drift of ~6.3 ppm/Gy. REF02 (5V reference) from ANALOG DEVICES, shows a drift of +5.7 ppm/Gy. AD780 (2.5V reference) from ANALOG DEVICES, shows a drift of +2.5 ppm/Gy.

4. CONCLUSIONS

Instrumentation bipolar amplifiers like AD624 exhibit good radiation tolerance for neutron and gamma radiation levels expected in the LHC. DiFET and JFET amplifiers are in principle also good candidates; we believe that their relatively high degradation is produced by the gamma dose at ITN, that is significantly higher than for the LHC. Next experiments will be designed to discriminate between gamma and neutron radiation effects.

Also higher frequency bipolar devices will be tested, although a trade-off between radiation hardness and low frequency performance might be necessary. Fortunately, the high accuracy resistors have very good radiation hardness. It is thus possible to measure thermometric signals in a resistance comparison bridge, for reducing the effects of radiation on gain, offset and bias of the front-end analogue circuitry.

As could be expected, poor radiation performance is observed for industrial signal conditioners not intended to operate in a radiation environment. This is why we will continue with the evaluation of discrete components, to build all front-end electronics with parts fully qualified for the radiation levels expected in the LHC.

This work has been financed by the co-operation agreement K476/LHC between CERN & UCM and by the Spanish research agency CICYT (TIC98-0737), and partially supported by ITN.

5. REFERENCES

LIQUID COOLLING SYSTEMS (LCS2) FOR LHC DETECTORS.

P. Bonneau, M. Bosteels, CERN, 1211 Geneva 23, Switzerland

Abstract

This paper describes a number of projects involving the liquid cooling of electronics, undertaken by the SF section of the CERN/EST/SM group. These facilities have been specifically designed to cool LHC-type detectors, in collaboration with users and services of the ST/CV group. The liquid circuit operating conditions in large physics detectors can be summarised as follows:
- as the facilities are generally located in temporarily inaccessible areas, the filling, bleeding and draining operations must be automatic;
- the number of active components installed in these areas must be reduced to a minimum and be able to cope with the special conditions prevailing there – magnetic fields, radiation, restricted access;
- the risk of leaks must be reduced as far as possible. If the fluid used is water the consequences of leaks are obvious, while if fluorocarbons are used, the cost of leaks can quickly become prohibitive;
- all parameters must be controllable from the control rooms;
- the equipment, preferably tried-and-tested industrial plant, must be selected in collaboration with the future maintenance and operations services, for certain CERN facilities, for instance, with the ST/CV group.

1. LCS2 OPERATING PRINCIPLE

The liquid is held in a storage tank (3) maintained below atmospheric pressure by a vacuum pump (2). A check valve discharges any excess air in the event of drainage and prevents the pressure in the storage tank from rising above atmospheric pressure. The liquid is moved into the exchangers (1) incorporated through the electronic system by a circulator (4).

The pressure at the various points of the circuit depends on the head losses and hydrostatic pressures. The detailed operating principle can be found on the Web [1]. At start-up, if the pressure in the storage tank is not low enough the vacuum pump is activated. While the latter is in operation, in the event of an air intake for instance, the circulator cannot function. The pressure throughout the circuit still equals the pressure in the storage tank.

2. THE COOLING OF THE CERES TPC

2.1 Aims

TPC detectors require a precise operating temperature, 20°C for CERES, with +/- 0.2°C stability. The sources of temperature variation in CERES are:
- its proximity to the RICH detector, which can heat up to 50°C;
- the magnet,
- the detectors’ read-out electronics,
- the hall environment.

Three types of cooling system have been installed:
- an insulating screen between the magnet and the TPC,
- cold screens against the electronic cards,
- various CO₂ circuits.

2.2 Isolating screen

The screen consists of an aluminium cylinder attached by heat-transfer cement to copper pipes in which water circulates. The pipes are connected to two adjustable-temperature manifold assemblies. The aim is to set a constant temperature outside the TPC, by removing the heat deriving from the environment.

2.3 Cold screens

Attached to each electronic card is a copper plate with welded-on pipe. The plates are water-cooled. The temperature is maintained above dew-point and is the same on all the plates. The aim here is to remove the heat deriving from the electronics.

2.4 CO₂ circuits

A closed CO₂ circuit is used both to prevent air intake by diffusion into the TPC active drift gas and to maintain a uniform temperature. The circuit is divided into 6 sub-circuits, each with adjustable flow-rate and temperature.

2.5 Liquid supply

All the circuits are supplied with water via an LCS2 system. In all the CERES circuits, the pressure always remains below atmospheric pressure.

2.6 Controls

All the circuits are remote-controlled by a PLC. The temperatures are adjusted by individual PID controllers. This facility has been operating continuously for two years, with the only maintenance operation being the replacement of the filters once a year.
3. ATLAS LIQUIS ARGON CALORIMETER COOLING

3.1 Aims
The electronics of this detector gives off a total maximum power of 200 kW. The facility will be 25 m high.

3.2 Description of the facility (Fig. 2)
A 20 kW cooling facility for the calorimeter tests is currently in service at CERN. The chosen technique is to place a liquid-cooled screen between each card; the liquid currently used is demineralised water, circulating partially below atmospheric pressure, although tests with C6F14 were recently successfully carried out.

The water is held in a storage tank (1) maintained below atmospheric pressure by a vacuum pump. A variable-speed circulator (2) injects the water into the riser pipes via a chilled-water heat exchanger (3). Equal pressure is maintained in all the sub-circuits by an expansion valve (4). The pressure may be adjusted according to the head loss in the circuits, and in the case of the ATLAS calorimeter it will be set at 50 mbars below atmospheric pressure.

The water then flows into the screens and is returned by gravity to the storage tank. The pressure in the riser depends on the hydrostatic pressure and the head loss, and the pressure in the screens is equal to that of the storage tank plus their own head loss.

The facility can operate using other liquids, such as C6F18 or similar. The temperature gradients and flow-rates depend on the properties of the liquids used. We have built a similar system, operating with liquid C6F14, for the joint tests on the CMS micro-strip gas-chambers and the ATLAS transition radiation tracker. This system has also been used for tests on the ATLAS Tile Calorimeter and the ALICE tracker.

4. COOLING OF THE STAR FTPC

4.1 Aims
TPC-type detectors require extremely precise temperature with +/- 0.2°C stability. For this facility the temperature stability is also required when the detector is shut down.

The electronics dissipates 600 W.

4.2 Description of the facility (Fig. 3)

The cooling liquid is used is demineralised water, which is held in a storage tank (1) and maintained at 0.5 bar below atmospheric pressure by a vacuum pump (2). The water is moved by a circulator (3) into a plate heat exchanger (4), cooled by chilled water from the CERN network.

The temperature is adjusted by a proportional thermal valve controlled by a PID controller according to the exchanger output temperature. This controller has two set temperatures, according to whether the detector power is on or off, and can be modified remotely. The liquid flow is spread over the two circuits by two rotameters.

The system is controlled by a small PLC.

5. CMS PIXEL COOLING

5.1 Aims
This detector, containing silicon pixel detectors, must be kept below 0°C. Its electronics dissipates 16 kW (4). The small diameters of the pipes permissible in the detector impose high pressure drop.

5.2 Description of the system (Fig. 3)

A 7 kW facility capable of operating at –20°C has been built and tested for testing the SI prototypes for CMS. The liquid used is C6F14.

With the facilities mentioned previously, the liquid is held in a storage tank maintained below atmospheric pressure. To avoid losses of C6F14 vapours via the vacuum pump, a molecular sieve trap (28) is installed at the vacuum pump outlet. The liquid is moved into the circuits at an adjustable pressure of up to 10 bars by a variable-speed pump. The liquid then passes through two exchangers – an electric re-heater (10) and an evaporator (11) connected to a refrigerator unit using R404 refrigerant.

The cold liquid is then passed through a distribution manifold to supply the various circuits. The pressure at the pump outlet can reach 8 bars.

5.3 Controls
The whole facility is monitored by an Ethernet-connected PLC. The liquid loss protection operates as follows:

- the entire system is first maintained at 0.5 bar below atmospheric pressure for a certain period. If this pressure level remains stable, the circulator pump (9) is switched on and the circuits are filled. After bleeding, the level in the storage tank stabilises; this level is monitored by a controller (3). If suddenly the level in the storage tank falls sharply during operation, the pump is stopped and start-up recommences. Then the faulty circuit has to be identified by isolating the circuits in sequence.

All the drawings and photos of these various systems can be found on the Web [1]

6. CONCLUSIONS

The LCS2 liquid cooling system at controlled low pressure has now been used on most of the facilities for the LHC projects. Users have not encountered any problems and the friendly use is highly appreciated.

For the final facilities in the LHC experiments we propose using 20 to 50 kW capacity modules, spread across the experiments. These modules would include the liquid storage in the experimental area, together with the circulator pump, the chilled water exchanger and pneumatic regulating valve. All the other equipment would be installed in areas accessible while the detectors are in operation.

The use of similar modules in all the experiments will result in cost savings and will simplify the maintenance.

Fig. 2
CMS INNER TRACKER
Cooling system

Fig. 4
FLUOROCARBON EVAPORATIVE COOLING DEVELOPMENTS FOR THE ATLAS PIXEL AND SEMICONDUCTOR TRACKING DETECTORS


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ABSTRACT

We report on the development of evaporative fluorocarbon cooling for the ATLAS Pixel and Semiconductor Tracker (SCT) detectors. Data are presented from cooling studies on representative prototype Pixel and SCT detector thermo-structures, using perfluoro-n-propane (C₃F₈), -butane (C₄F₁₀), trifluoro-iodo-methane (CF₃I) and custom C₃F₈/C₄F₁₀ mixtures. Thermo-physical properties were calculated for custom mixtures. For most of the structures tested at full projected power dissipation, operation of silicon detector substrates at temperatures below –7ºC (required for 10 year lifetime in the radiation environment of LHC) should be possible, albeit in some cases with increases in inner diameter (I.D.) of the coolant tubes from those of the present series of prototypes.

Heat transfer coefficients in the range 2-5.10³ Wm⁻²K⁻¹ have been measured in a 3.6 mm I.D. heated tube dissipating 100 Watts - close to the full equivalent power (~110 W) of a barrel SCT detector “stave” - over a range of power dissipations and mass flows in the above fluids.

Aspects of full-scale evaporative cooling circuit design for the ATLAS experiment are discussed, together with plans for future development.

1. INTRODUCTION

The SCT detector [1] will have 4 cylinders around the collision point (barrel) and 9 forward disks at each end. Each cylinder consists of “staves” containing 12 silicon strip detector modules, while disks contain 132 modules. The total SCT dissipation will be around 41.3kW, with ~9.2W from each module, subdivided into ~2W (after 10 years of irradiation) from the silicon substrate, and ~7W from the readout electronics.

The pixel detector [2] has ten forward disks and three cylinders containing staves of 13 pixel detector modules. The total detector dissipation will be around 18.7 kW, with around 7.9W from each module (11W in the B-physics layer at a radius of ~4.5 cm from the beams).

Our studies [3],[4] have been directed to cooling systems contributing the minimal possible material, particularly important for the pixel B layer. Evaporative fluorocarbon cooling combines high heat transfer coefficients with very low circulating coolant mass (1–2 gram.s⁻¹/100W to evacuate). Liquid refrigerant can be delivered to the detector in capillaries with IDs as small as 0.6 mm. Furthermore, fluorocarbon refrigerants are non-flammable, non-toxic insulators with zero ozone depletion potential.

Table 1: Selected Refrigerant Properties (~15º C)

<table>
<thead>
<tr>
<th>Fluid</th>
<th>L [Jg⁻¹]</th>
<th>Vol_vap/ cm³(lq)</th>
<th>S.V.P (bar a) @ -15º C</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₃F₈ [5],[7]</td>
<td>97.0</td>
<td>71.4</td>
<td>2.46</td>
</tr>
<tr>
<td>C₄F₁₀ [5],[7]</td>
<td>101.1</td>
<td>242.6</td>
<td>0.58</td>
</tr>
<tr>
<td>CF₃I [7]</td>
<td>100.8</td>
<td>176.3</td>
<td>1.33</td>
</tr>
<tr>
<td>C₃F₈/C₄F₁₀ (50/50) [8],[9]</td>
<td>98.3</td>
<td>147.6</td>
<td>1.01PᵥS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.65PₛL</td>
</tr>
</tbody>
</table>

Latent heat data for the various refrigerants are shown in table 1, together with their saturated vapor pressures and the volume of vapor produced per cm³ liquid evaporated at ~15ºC (a temperature chosen to accommodate probable thermal impedances between the silicon substrate and the coolant). A target evaporation pressure of 1 bar (abs)
would allow the use of very low mass tube (~0.2 mm wall aluminum or composite) in a variety of aspect ratios.

2. TEST RESULTS ON SCT AND PIXEL PROTOTYPE THERMO-STRUCTURES

2.1 The Refrigerant Recirculator

A closed-loop evaporative recirculator (figure 1) has been built for testing thermo-structures using all the fluids of table 1. Structures are placed in a chamber purged with inert gas and maintained at −7°C, to simulate the environment of the SCT and pixels in the ATLAS inner detector.

![Figure 1: The Two-Stage Evaporative Recirculator](image)

The present circulator contains two compressor stages and a water-cooled condenser, also serving as a high-pressure liquid refrigerant reservoir. The first stage compressor is used only with low input pressure vapors as in the case of C\textsubscript{4}F\textsubscript{10} or C\textsubscript{3}F\textsubscript{8}/C\textsubscript{4}F\textsubscript{10}, since the pumping speed of the second stage compressor is insufficient at input pressures below 1 bar abs. These compressors will soon be replaced with a single stage dry scroll compressor (Atlas Copco SF4-8-120) with a measured flat pumping speed of ~20 m\textsuperscript{3} hr\textsuperscript{-1} for both C\textsubscript{4}F\textsubscript{10} (P\textsubscript{in} = 0.25, P\textsubscript{out} = 4 bar abs) and C\textsubscript{3}F\textsubscript{8} (P\textsubscript{in} = 1.4, P\textsubscript{out} = 8 bar abs).

Liquid refrigerant enters a four-channel supply manifold, whose pressure - defined by a regulator – determines the liquid mass flow. Fluid enters the test structures via capillaries with diameters varying between 0.6 and 1 mm, or via injectors made from synthetic ruby watch bearings with orifices varying between 210 and 300 μm.

The temperature of evaporation of fluid in the test structures depends on the pressure in a 4-channel vapor collection manifold tank, controlled via feedback from a pressure sensor\textsuperscript{2} to a variable orifice valve located between the tank and the compressor input. The circulating mass flow is metered after the tank.

2.2 Tests on a Forward SCT Thermo-Structure

Figure 2 shows a recent model for the on-detector cooling for a quarter disk of the ATLAS forward SCT, in which 18 similar disks will each support 132 silicon strip modules, and dissipate 1.2kW.

![Figure 2: Forward SCT Quadrant Thermal Model](image)

On the “front”, heat from two arcs of silicon micro-strip modules (simulated with resistive heaters) is conducted to the coolant via attachment blocks glued to the cooling tubes (figure 3). On the “rear” a third arc of modules will provide tacking hermeticity through overlap.

To accommodate thermal expansion effects, each quadrant has two serpentine circuits with 3.6 mm ID tubes, and lengths 2.5 & 3.5m ("A"&"B"), respectively cooling 14 and 19 modules. Each circuit first cools the inner front arc of modules, follows an arc at the outer radius, and then cools the modules on the rear of the panel.

Thermal connections to the cooling tube are of several types: some attachment blocks evacuate the simulated 7W power of the module readout electronics ("E"): those along the front outer arc evacuate only ~ 2W of substrate ("S") dissipation. The innermost front blocks traverse the support, and evacuate, in addition to the 9W (E+S) dissipation of the front inner modules, ~2W from the simulated substrates of the rear modules. Blocks are of

\textsuperscript{1} Edwards ECP 30 Dry Rotary Scroll Vacuum pump
(rated 30 m\textsuperscript{3} hr\textsuperscript{-1} air; P\textsubscript{in} = 1 bar abs, P\textsubscript{out} = 1.5 bar abs limit)

\textsuperscript{2} Haug SOGX 50-D4 Dry Piston Compressor
(rated 3.6 m\textsuperscript{3} hr\textsuperscript{-1} air, P\textsubscript{in} = 1 bar; P\textsubscript{out} = 9 bar abs limit)

\textsuperscript{3} MKS Baratron Model 122B Range 0-5000 Torr (abs)
several different heights, and some span a gap between joined tubes, presenting lower impedance for heat conduction into the fluid.

For C₃F₈, the results were significantly better. At full power (7W (E); 2W (S)) and a boiling pressure 2.3 bar, the temperature of all blocks, with the exception of the rear “S” side of the double block (now being redesigned), were below ~6°C, and the temperature gradient along the tube was only ~2°C. The temperature difference between the blocks and the tube was also less, probably due to a higher heat transfer coefficient for C₃F₈. By decreasing this boiling pressure, the temperature of the test structure could be further, uniformly, reduced.

2.3 Tests on SCT Barrel Structures

The present cooling circuit manifolding proposed for the SCT barrel is shown in figure 6. Coolant is injected through a capillary to a series pair of staves with a total tube length of 3.2m. A common exhaust is shared with a second series pair of staves mounted in parallel.

In the present thermo-structure, each stave carries 12 heater plates attached with thermally conductive glue to one 7.2mm side of a flat-walled oval tube having an equivalent I.D. of 2.7mm. A total of 64 temperature sensors are attached to the plates and on the tubes between them. Plates are laminated from two (60 x 20 mm) pieces of aluminum with thermally conductive glue, to investigate the layering of the detector module, in which the hybrid supporting the readout electronics (“E”) is mounted on top of the silicon substrate (“S”), which has closer attachment to the cooling tube. Temperature sensors are mounted on the E and S sides of the blocks.

Figure 7 shows sample data taken with C₃F₈ at ~9W/block. The temperature (pressure) gradient between the input of the first series stave and the output of the second is ~7°C (1.1 bar). Block temperatures vary between -2°C and -13°C, and the target (S) temperature of -7°C is not met at the beginning of the first stave. The (60 x 7mm) film of thermal glue fastening the blocks to the tube causes an average temperature difference of ~7°C between the tube and the S sides of the blocks. The E sides are ~2°C warmer. It was concluded that the 2.7 mm ID of the cooling tubes in the present thermo-structure was insufficient to evacuate the
vapor produced from ~220W dissipation of two staves in series.

![Figure 7: Barrel SCT Manifold Test with C₃F₈: 10 Watts per block, two staves in series](image)

Figure 7: Barrel SCT Manifold Test with C₃F₈:
10 Watts per block, two staves in series

Figure 8 is an example of test data with the manifold rebuilt for a “single pass” of refrigerant. The temperature (pressure) profile along the 1.6m stave with the 2.7mm ID tube is ~2°C (0.3 bar). Block temperatures (E) vary between ~8°C and ~11°C, and the target (S) temperature of ~7°C was met everywhere along the stave.

Figure 8: Forward SCT Manifold Test with C₃F₈:

10 Watts per block, single stave

Two-phase flow pressure drop calculations indicate a total pressure drop of 350 mbar in a series pair of SCT staves each dissipating ~110W, if a tube hydraulic ID of ~ 4mm is used: the next iteration of the SCT stave will study a tube of this dimension.

2.4 Tests on Pixel Forward Structures

Thermal measurements have been made on a developmental series of forward pixel disk sector thermo-structures [2], in which cooling tubes bent in “W” or “WV” shapes are sandwiched between skins of Carbon-Carbon (C-C). In some structures, an aluminum tube with slightly flattened faces was used, while in others, a glassy carbon tube, “flocked” with grown-on carbon fibers is bonded to the C-C plates. Figure 9 shows the thermal profile on a prototype sector with a 3.2 mm ID carbon tube and C₄F₁₀ coolant at a boiling pressure of 345mbar. This sector dissipated a total of 38W. More recent structures have higher dissipation and a shorter cooling tube with increased diameter. The temperature profile on the sector was found to be invariant with orientation [2].

Figure 9: C Pixel Disk Sector Test Data (C- tube: C₄F₁₀)

2.5 Tests on Pixel Barrel Structures

Thermal measurements have been made on an 80cm pixel barrel stave thermo-structure (figure 10) with a 3.4 mm equivalent ID cooling channel made from a carbon fiber U channel glued to a sealed C-C support plate, onto which 13 dummy pixel modules are glued. In the pixel cooling layout, pairs of staves in the 2 outer (r = 10, 13 cm) pixel layers dissipate ~100W and share a common exhaust tube. In the B-layer the higher occupancy closer to the beams, stave dissipation is ~143W.

![Figure 10: Pixel Stave Carbon-Carbon thermo-structure](image)
Figures 11a & b show the temperature profile along the stave for CF$_3$I and C$_4$F$_{10}$ for power loads varying between 78W and 143W, for C$_3$F$_8$ at a power of 100W and for a 50/50 (molar) C$_4$F$_{10}$/C$_3$F$_8$ mixture at 55W. The average silicon temperatures at the different boiling pressures are given in table 2.

![Figure 11a: Temperature Profiles along the Pixel C-C stave: CF$_3$I and C$_4$F$_{10}$](image)

![Figure 11b: Temperature Profiles along the Pixel C-C stave: C$_3$F$_8$ and 50%C$_4$F$_{10}$/50%C$_3$F$_8$ molar mixture.](image)

Table 2: Temperature Profile Summary for different fluids: pixel stave thermo-structure

<table>
<thead>
<tr>
<th>Fluid</th>
<th>Power on pixel stave (W)</th>
<th>Boiling Pressure (bar abs)</th>
<th>Average Silicon Temp</th>
</tr>
</thead>
<tbody>
<tr>
<td>CF$_3$I</td>
<td>78</td>
<td>1.10</td>
<td>-8.0</td>
</tr>
<tr>
<td>C$<em>4$F$</em>{10}$</td>
<td>78</td>
<td>1.08</td>
<td>-7.0</td>
</tr>
<tr>
<td>C$_3$F$_8$</td>
<td>100</td>
<td>0.35</td>
<td>-7.0</td>
</tr>
<tr>
<td>C$_3$F$_8$/ C$<em>4$F$</em>{10}$ (50/50)</td>
<td>55</td>
<td>0.83</td>
<td>-11.0</td>
</tr>
</tbody>
</table>

It was found that the ID of the present pixel stave tube is insufficient to maintain the -7°C silicon temperature with C$_4$F$_{10}$ at dissipations exceeding ~80W, and with the 50/50 C$_4$F$_{10}$/C$_3$F$_8$ mixture at dissipations exceeding ~60W, but that cooling to the target temperature was possible, both with CF$_3$I and C$_3$F$_8$ at the highest envisaged dissipation (figure 11b). The next version of the pixel stave will use a 4.6 mm equivalent ID tube, which should be large enough to allow pairs of pixel staves to be connected in series.

3. MEASUREMENT OF HEAT TRANSFER COEFFICIENT

A second refrigerant recirculator was constructed to allow simultaneous measurements of heat transfer coefficient (HTC) while full size thermo-structure prototypes were measured in the main circulator. Heat transfer coefficients were measured on a 1.6m long simplified SCT stave with 12 copper blocks soft-soldered onto a 1.6 m long cupronickel tube with 3.6mm ID. On each block were a ceramic heater and a PT100 sensor. PT100’s were fitted to the coolant tube in 13 positions between the blocks and at each end. Another sensor measured the liquid temperature upstream of the capillary or injector. In this tube, HTCs were measured at 12 points along the tube from the (block-tube) temperature difference, and knowledge of the dissipation at each block and its contact area with the tube. Typical HTC measurements for the different fluids in this tube are shown in figure 12, and varied in the range 2-5.10$^3$ Wm$^{-2}$K$^{-1}$ depending on power dissipation. The highest HTCs were seen in the case of C$_3$F$_8$, and the lowest with 50/50 C$_4$F$_{10}$/C$_3$F$_8$. Reduced HTCs for mixtures have been reported elsewhere[10].

![Figure 12: Heat Transfer Coefficients in a 3.6mm ID tube: C$_4$F$_{10}$, CF$_3$I, C$_3$F$_8$ & 50%C$_4$F$_{10}$/50%C$_3$F$_8$ mixture at similar power and flow rate.](image)

4 REFRIGERANT IRRADIATION STUDY

4.1 Effects of Neutron Irradiation

Small, static liquid samples of perfluoro-n-hexane (C$_6$F$_{14}$), CF$_3$I, solid Teflon and iodine (I$_2$) were irradiated up to 3x10$^{13}$ fast neutrons.cm$^{-2}$ to simulate the expected environment at LHC. Studies showed the main longest-lived radioisotopes to be $^{15}$F (106 min: 511 KeV...
4.2 Radiation-Induced Chemical Modifications

Small, static liquid samples of \( \text{C}_6\text{F}_{14} \) and \( \text{CF}_3\text{I} \) were exposed to 60°C gamma irradiation. After an absorbed dose of 3 Mrad, about 1% by weight of \( \text{C}_6\text{F}_{14} \) liquid had been radio-chemically modified: there was chemical evidence of the production of reactive HF, due to impurities containing C-H groups. Scanning electron microscopy and Auger electron spectroscopy were used to characterize the morphologies and elemental compositions of C, F and O-containing polymeric deposits formed on stainless steel and aluminum samples immersed in liquid during irradiation. After 6 Mrad, surfaces were almost uniformly covered to a depth of ~0.4 μm. Degradation and plate-out were greater in a sample of \( \text{C}_6\text{F}_{14} \) to which 3% (vol.) n-heptane had been added to act as a H-source.

Since saturated fluorocarbons (\( \text{C}_n\text{F}_{(2n+2)} \)), are synthesized from alkane precursors, batch testing for residual H contamination (using the characteristic Fourier Transform Infra-Red signature of C-H bonds) is advisable. Techniques for the catalytic removal of \( \text{C}_n\text{F}_x\text{H}_{(2n-x)} \) contamination were developed [11] for the DELPHI RICH detector, where high fluid purity is needed for good UV transparency: similar techniques could be used in the present application.

After irradiation to 2 Mrad, liquid \( \text{CF}_3\text{I} \) had become opaque, and breakdown of \( \text{CF}_3\text{I} \) into \( \text{I}_2 \) and HI was seen. This was not a complete surprise, since \( \text{CF}_3\text{I} \) is a refrigerant with a short (~24 hr) atmospheric half-life. Oily residues (pre-polymers) were observed after the evaporation of the irradiated \( \text{CF}_3\text{I} \), and thick deposits, including crystalline \( \text{I}_2 \) were observed on aluminum and stainless steel immersion samples. Although it was possible to clean the \( \text{CF}_3\text{I} \) to remove \( \text{I}_2 \) and re-establish the transparency, \( \text{CF}_3\text{I} \) was finally abandoned as a coolant owing to its chemical aggressivity, even in the un-irradiated state, to elastomer seal materials.

5 CONCLUSION

Evaporative cooling has been demonstrated at the full power dissipation of the ATLAS SCT and pixel detectors. Studies with engineering prototypes and measurements of heat transfer coefficient indicate that \( \text{C}_3\text{F}_8 \) is presently the best candidate refrigerant. The low boiling pressure of \( \text{C}_4\text{F}_{10} \) (~350 mbar abs @ ~–25°C) allows a small pressure head to drive vapor back to the compressor input. Of the fluids with “ideal” thermodynamics (saturated vapor pressure ~ 1 bar (abs) at ~–25°C), \( \text{C}_3\text{F}_8/\text{C}_4\text{F}_{10} \) custom mixtures are less favored due to lower heat transfer coefficient, while \( \text{CF}_3\text{I} \) has been rejected due to its chemical aggressivity, poor chemical stability under ionizing radiation, and radio-activation concerns.

REFERENCES

CERN/LHCC/97-16/17, 30 April 1997
CERN/LHCC/98-13, 31 May 1998
R. Budinsky, G. Hallewell, G. Lenzen, J. Thadome & V. Vacek; Proc. ATLAS Cooling Review, 
CERN (18-19 September, 1997)
[5] Mfr: 3-M Corp. Specialty Chemicals Division, 
St. Paul, MN55133-3223, USA
Powder Springs, GA, 30127-0127, USA
M. Lísal, R. Budinsky & V. Vacek 
Fluid Phase Equilibria, 135 (1997), 193
[9] Custom mixture: properties with “REFPROP”: 
Database of thermodynamic and transport properties of refrigerants and refrigerant mixtures: Version 6.01 
National Institute of Standards and Technology, Gaithersburg MD 20899 USA (1998): \( \text{C}_4\text{F}_{10} \), \( \text{C}_3\text{F}_8 \), mix & \( \text{CF}_3\text{I} \) extensions by V. Vacek.
T. Inoue, N. Kawae & M. Monde: 
Heat & Mass Transfer 33 (1998), 337
[11] “Per-fluorocarbon Liquid: Specific Chemical Aspects for use within the DELPHI RICH” 
S. Ilie & G. Lenzen: 
DELPHI 93-33 RICH54, 30 March 1993.
Custom HV and LV Supplies for LHC Experiments

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Abstract

CAEN has strongly invested its resources, in the last three years, in the development of a Power Supply system (SY1527) totally dedicated to LHC applications. The first applications of this system, currently under test at CERN Electronics Pool, include both standard boards and custom supplies. The standard boards technology, acquired by CAEN in 20 years of experience, is now employed in the development of custom systems that allow to power up both the various detectors and the relevant front end electronics. The radiation and magnetic field levels impose on all the remote distributed systems several design criteria, including safe and reliable operation. Existing custom supplies and new architectures, based on the new SY1527 system, both for high and low voltage generation and distribution in presence of moderated radiation and magnetic fields levels, will be presented. Power dissipation issues in the experimental halls are critical. New solutions for a more efficient energy transfer are under study, in particular for what concerns low voltage supplies.
THE GASSIPLEX0.7-2 INTEGRATED FRONT-END ANALOG PROCESSOR FOR THE HMPID AND THE DIMUON SPECTROMETER OF ALICE

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ABSTRACT

The most recent member of the Gasplex family of ASICs has been designed in a 0.7 µm n-well CMOS process to meet specifications for the ALICE applications: 500 fC linear dynamic range and a peaking time of 1.2 µs. Its internal circuitry is optimized for the readout of gaseous detectors. A dedicated filter compensates the long hyperbolic signal tail produced by the slow drift of the ions and allows the shaper to achieve perfect return to the base line after 5 µs. Measurement of fabricated chips showed a noise performance of 530 e⁻ rms at 0 pF external input capacitance and 1.2 µs peaking-time, with a noise slope of 11.2 e⁻ rms/pF. The gain is 3.6 mv/fC over a linear dynamic range of 560 fC.

1. INTRODUCTION

Since the AMPLEX[1], the benefit of using multiplexed analog integrated circuits as front-end for the readout of gaseous detectors, has been widely proved. Its main feature was to use the peaking time of the shaped signal as a delay, allowing an external trigger to memorise the information by a Track-and-Hold circuit. Based on the same technique, the GASPLEX[2] was the first monolithic circuit for which the pulse shaping was adapted to the special signal of gaseous detectors. A simplified version of the GASPLEX, the GASSIPLEX1.5, manufactured with a volume production of 60 wafers, has a simpler logic I/O levels with the same functionality and internal shaping. The more recent version presented in this paper, the GASSIPLEX0.7-2, has been designed in a 0.7 µm n-well CMOS technology with a peaking time of 1.2µs and an extended dynamic range of 500 fC. The analog circuitry follows the same principle as the GASPLEX: a Charge Sensitive Amplifier (CSA) with a long decay-time in order to collect the largest part of the detector signal.

After the CSA, a deconvolution filter compensates the logarithmic shape of the charge signal and provides the shaper with a quasi-step function with one pole given by the RC time constant of the CSA. The shaper provides a Semi-Gaussian signal with a 1.2µs peaking-time and a return to the baseline better than 1% after 5µs. A track-and-hold circuit stores the analog information at the peaking time and finally the 16 channels are multiplexed to one output. The Gassiplex0.7-2 also provides an individual channel calibration with a precision better than 1.5%.

2. CIRCUIT DESCRIPTION

The Gassiplex0.7-2 is a 16-channel low noise signal processor. It has been developed to fit the requirements of two ALICE detectors: the HMPID[3] which uses the Ring Imaging Cerenkov (RICH) technique and the dimuon spectrometer[4]. Both detectors utilise Multivwire Proportional Chambers with cathode pad or cathode strip readout. In gaseous detectors, the ion cloud released by the avalanche around the anode wires induces current as long as it drifts in the electric field from the anode to the cathode. The charge close to the anode can be approximated by the expression q(t) = Q₀ Aln(1+t/t₀) and the current by i(t) = I₀B/(1+t/t₀), where Q₀ is the total ionic charge and A, B and t₀ are constants depending on the detector geometry and the electric field.

The following diagrams show the different blocks of the channel circuitry: CSA, deconvolver and shaper. The CSA is made of two main parts: a folded cascode stage and an active feedback resistor. The input transistor is a p-channel with a W/L of 400; coupled with the folded transistor it allows to work with a large range of detector capacitance, and exhibits good performances at relatively low power budget. The feedback resistor has been implemented with a 50kΩ high ohmic silicon layer, followed by a current divider of 400; coupled with the feedback capacitance, it results in a decay-time constant of 20µs.

After the CSA, a deconvolution filter has been implemented to compensate the long tail resulting from the ions drift. The detector can be modelled as a linear system with an impulse response h(t) = U(t)/(t₀+t) stimulated by a Dirac pulse δ(t) = Q₀δ(t), U(t) being a step function. To perform the deconvolution, the transfer function of the deconvolver G(s) should be the exact inverse of the transfer function of the detector H(s), namely G(s) = H(s)⁻¹, where H(s) is the Laplace transform of h(t).

The charge given by the detector is approximated by the sum of three weighted exponentials [5]. Each exponential is modelled by a pole (OTA1, OTA2)
placed in the feedback of a summing amplifier (SUM_OTA) to implement the inverse transformation:

\[ G(s) = \frac{V_{out}}{V_{in}} = \frac{A}{1 + \beta A} \]

and \( \beta = K_1/(1+sT_1) + K_2/(1+sT_2) + K_3/(1+sT_3) \). Notice that the third exponential is internal at SUM_OTA. After deconvolution the filter output looks like a step function with one pole given by the Rf.Cf decay-time constant of the CSA. It allows the shaper to maintain a stable and precise return to the base line.

After deconvolution the filter output looks like a step function with one pole given by the Rf.Cf decay-time constant of the CSA. It allows the shaper to maintain a stable and precise return to the base line.

Fig 1: CSA and Filter blocks

The shaper circuit shown in fig. 2 has an original feature: from the output of the filter two different integrating paths are compared at the inputs of an amplifier (OTA4); it results in a Semi-Gaussian shape and thereby eliminates the usual differentiation capacitor.

Owing to the pole given by the time-constant of the CSA (Rf.Cf), it is necessary to introduce a zero in the transfer function of the shaper. This is done on the output of OTA5 with an active resistor Rp/z. The cancellation occurs when the two time-constants are equal; thus, \( Rp/z = Rf.Cf/C5 \), C5 being 9 pF gives Rp/z = 2.22 MΩ. This resistor is equivalent to the feedback resistor of the CSA and shares the same biasing.

Fig 2: Shaper block

In addition, the Gassiplex07-2 provides individual channel calibration. Each channel has a 1pF-injection capacitor coupled to an analog switch activated by a shift register. The accuracy of the calibration circuit reflects the fact that capacitances are the most accurate elements in a CMOS process.

This calibration input multiplexer as well as the output multiplexer provide a Clock-out output which can be used to daisy-chain several chips (four in the Alice case), the analog output being common. The Clock-out of a chip is equal to the Clock-in minus the 16 clocks that perform the readout of the chip.

Finally another important feature is the possibility to switch-off the deconvolution filter in case of using a Silicon detector. Notice that if the detector leakage current is bigger than 1nA, a coupling capacitor is needed between the inputs of the Gassiplex07-2 and the detector.

3. MEASUREMENTS RESULTS

Measurements have been done on several chips coming from two wafers; the results were slightly different, but not distinguished in the measurements presented here.

3.1 Noise versus input capacitance

The noise measurements (fig. 4) have been performed at a power consumption of 8mW/channel.
with 350 μA drawn by the input transistor and a peaking time of 1.2 μs. It resulted in a noise slope of 11.2 e⁻rms and a residual noise of 470 e⁻rms.

For a maximum output voltage of 2 V, the aim has been to achieve at the same time the low noise and the largest dynamic range. The target characteristics correspond to the use of a 12-bit ADC.

### 3.2 Gain non-uniformity

The sensitivity (fig. 5) has been measured on 10 chips coming from 2 wafers; for these 160 channels, the gain has showed a rms spread of 0.05 mV/fC, which is 1.36% of the mean value (3.675 mV/fC).

### 3.3 Dynamic range and linearity

The HMPID detector and the muon spectrometer need different characteristics of electronic circuitry amplification. The first one needs low noise and high sensitivity to be able to detect single photon emission; the second one requires low noise and large dynamic range to achieve precise measurements, for the localisation of the muon track.

For a maximum output voltage of 2 V, the channel spread of the 16 channels in a chip and between chip. On 10 chips (fig. 7), coming from 2 wafers, we have measured a difference of 6 mV between the average values of pedestals; while the rms value of the pedestal spread on 160 channels is 13.5 mV.
3.5 Calibration

An analog multiplexer allows calibration of the chip channel per channel, through analog switches and individual 1 pF capacitors. However a parasitic injection, coming from the external circuitry, is added to the calibration signal. Figure 9 shows this parasitic effect with a 40 mV calibration input signal. Channel 1 and 2 are affected by this effect, while channel 14 reflects a layout defect.

After having measured this effect, it is possible to know the relative accuracy of the gain. Figure 10 shows the results: the diamond points are the measured gain for a direct channel to channel injection through an external capacitance, the triangle points are the gain measured through the calibration input including the parasitic effect and the square points are the gain when the parasitic is deducted. One can see the good reproducibility of the internal 1 pF capacitors. The difference between direct signal injection and calibration signal injection is due to the discrepancy in the values of the external and internal capacitors.

3.6 Peaking time adjustment

The peaking time can be adjusted from 1.1 $\mu$s to 1.3 $\mu$s by modifying the bias current of the shaper. With a value of 34 $\mu$A, the peaking time is 1.2 $\mu$s.

3.7 Silicon mode

An external DC level can switch off the deconvolution filter. In this case the Gassiplex07-2 can be connected directly to a Silicon detector if its leakage current is smaller than 1 nA, or through a capacitor if the current is bigger. The gain is reduced to 2.2 mV/fC and the dynamic range increased to 900 fC. Noise and linearity are not affected.

3.8 Radiation tolerance

An irradiation test has been made on one chip, using a Xray beam. The exposure was by step of 10 Krad up to 50 Krad; after each step measurements of pedestals, noise and power consumption have been made. All parameters increase by few %. A last step of 50 Krad caused a jump of 800 mV on the output DC level, but the chip was still working. After one week at 100 $^0$C in a oven, all the parameters were recovered. Further tests on several samples are planned.

3.8 Pulse shaping on Gas Detector

The circuit has been tested on a Muon cathode pad gas detector using a $^{55}$Fe Xray source. One can see on fig. 11 that the return to the base line is almost perfect.
3.9 Low power application

Depending on the application, the power consumption can be decreased by limiting the current bias in the CSA and in the buffers; at the cost of reduced noise performance and readout speed. At 4 mW/channel, the noise slope becomes 15 e\(^{-}\)rms/pF and the maximum readout speed will be 4 MHz.

3.10 Table of performances

<table>
<thead>
<tr>
<th>Technology</th>
<th>Alcatel-Mietec-0.7(\mu)m</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon area</td>
<td>3.63 (\times) 4 = 14.5 mm(^2)</td>
</tr>
</tbody>
</table>

Gaseous detector mode

| Peaking time | 1.2 \(\mu\)s |
| Peaking time adjust. | 1.1 to 1.3 \(\mu\)s |
| Noise at 0 pF | 530 e\(^{-}\) rms |
| Noise slope | 11.2 e\(^{-}\)rms/pF |
| Dynamic range ( + ) | 560 IC (0 to 2 V) |
| Dynamic range ( - ) | 300 IC (0 to –1.1 V) |
| Gain | 3.6 mV/IC |
| Non linearity | ± 2 IC |
| Baseline recovery | ± .5% after 5 \(\mu\)s |
| Analog readout speed | 10MHz (50 pF load) |
| Power consumption | 8mW/chan. at 10 MHz |
| Output Temp Coeff. | 0.05 mV/\(\circ\)C |

Silicon detector mode

| Gain | 2.2 mV/IC |
| Dynamic range ( + ) | 900 IC (0 to 2 V) |
| Dynamic range ( - ) | 500 IC (0 to –1.1 V) |
| Non linearity | ± 3 IC |
| Noise at 0 pF | 600 e\(^{-}\) rms |
| Noise slope | 12 e\(^{-}\)rms/pF |

Low power mode

| Power consumption | 4mW/chan. at 4 MHz |
| Noise at 0 pF | 600 e\(^{-}\) rms |
| Noise slope | 15 e\(^{-}\)rms/pF |

4. CONCLUSIONS

The Gassiplex07-2 is a very flexible ASIC for a very wide range of detector readout applications. A 12-bit ADC has to be used to benefit from its low noise as well as its dynamic range. Analog multiplexing requires effective zero suppression and pedestal subtraction to retrieve information of channels hit by events. A companion ASIC, Dilogic-2, performs these operations; it can process 16, 32, 48 or 64 channels and can store up to 512 x 18-bit words in a on-chip asynchronous read-write FIFO. Samples will be available in October 99.

Several packages can be used: ceramic LCC 48, QFP 44L plastic (10x10mm) and TQFP 48L (7x7mm). Concerning the ALICE detectors, the application being well defined, a new design iteration will be made in the coming months to make the logic levels compatible with the low level CMOS logic and also to reduce the number of biasing pins.

5. ACKNOWLEDGEMENTS

We would like to acknowledge Lambertus Van Koningsveld for his fruitful help in the use of different software.

6. REFERENCES

[4] "The forward muon spectrometer. Addendum to the ALICE Technical Proposal" CERN/LHCC 96-32, LHCC/P3-Addendum 1
DEVELOPMENT OF AN OCTAL CMOS ASD FOR THE ATLAS MUON DETECTOR

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Abstract

Development of a CMOS amplifier/shaper/discriminator for the ATLAS Muon detector is presented. The first phase of this work has resulted in a simplified 4-channel device (ASD-lite) fabricated in HP 0.5µm n-well CMOS operating at 3.3 volts. Highly accurate DC models resulted in performance which closely matches SPICE predictions. On-chip crosstalk, a parameter not easily simulated, is measured to be below 0.5%. Results of chip measurements and on-chamber tests will be presented. This device will be used for early testing of ATLAS MDT (Monitored Drift Tube) modules. Further work on the final octal MDT-ASD, which will be fully programmable and include Wilkinson leading edge charge measurement, will be presented.

Front End Requirements

The Muon spectrometer aims for a $P_T$ resolution of 10% for 1TeV muons. This translates into a single wire resolution requirement of <80µm. The average drift velocity is about 20µm/ns, which implies a systematic timing error for an individual tube of about 500ps.

The planned gas gain is low, about $2 \cdot 10^4$, to avoid aging problems. The expected signal (collected charge) is roughly 1500 electrons (0.25fC) per primary electron, so good position resolution requires a low noise front-end.

A specified preamp peaking time of 15ns is a good compromise in terms of resolution and stability 1. The channel to channel crosstalk is specified to be less than 1%. The high count rates of up to 400kHz/wire together with the long electron drift times require either a bipolar shaping scheme or active baseline restoration to avoid resolution deterioration due to baseline fluctuations.

At the time of the TDR2 the baseline MDT gas was Ar/N$_2$/CH$_4$ 91/4/5 (3 bars absolute) which is very linear and has a maximum drift time of 500ns. The choice for the ASD shaping scheme was unipolar shaping with active baseline restoration3 for the following two reasons. First, it allows the measurement of the signal trailing edge4,5, which has a fixed latency with respect to the bunch crossing, with an accuracy of about 20ns. Second, it avoids multiple threshold crossings per muon track, which would increase the hit rate and therefore the readout occupancy.

Aging problems with all MDT gases containing hydrocarbons caused a change of the baseline gas to Ar/CO$_2$ 93/7 (3 bars absolute) which has a maximum drift time of 800ns and is very nonlinear6. The long drift time and the non-linearity degrade the trailing edge resolution to about 80ns and cause multiple threshold crossings even for a unipolar shaping scheme7. We therefore have adopted a bipolar shaping scheme since it does not require an active BLR and also does not require programmable filter time constants. To avoid multiple hits from multiple threshold crossings for a single signal we introduce a fixed dead time equal to the maximum drift time. It was shown that the overall increase in dead time does not cause a degradation of the pattern recognition efficiency8.

An ADC will measure the signal charge in a 20ns gate following the threshold crossing time. The charge is then encoded into a pulse width in the usual Wilkinson technique. This information allows a resolution improvement by performing a time slewing correction. Additionally, it is useful for diagnostics and monitoring purposes and might also be used for dE/dx identification of slow moving heavy particles like heavy muon SUSY partners.

Two modes of operation will be provided. In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge and is considered the default operating mode.

Readout System Packaging

The ATLAS MDT system consists of about 350,000 pressurized drift tubes of 3cm diameter, with lengths from 1.5 to 6m. The MDTs are read out by an ASD at one end, and the other end is terminated in the characteristic impedance of the tube (380Ω). The preamp input impedance is a relatively low ~100Ω to maximize collected charge. To minimize cost, the MDT signals are carried on two-layer "hedgehog boards" to a mezzanine board, which contains 24 readout channels: 3 Octal ASDs, a single 24-channel TDC, and associated control circuitry.

A single MDT chamber may have as many as 432 drift tubes or 18 hedgehog/mezzanine board
sets. Data are read out of each TDC individually via a 40Mbit/sec serial link to a single CSM (Chamber Service Module) which multiplexes the (up to) 18 serial links into a single optical fiber for transmission to the ATLAS DAQ. A daisy-chain JTAG bus permits downloading of parameters to ASDs and TDCs and triggering of test/calibration pulse injection.

Each superlayer (3 or 4 layers of individual tubes) is entirely enclosed in a faraday cage shield at both ends. All AC signals entering or leaving the shield are low-level differential signals (LVDS). All DC signals are filtered at the shield entry point.

Each complete MDT chamber is electrically isolated from the support structure, and all services (gas, electrical, etc) are also electrically isolated or floating at the source. The MDT chambers will be individually grounded in a controlled way to a single common ground point.

ASD Overview

The chip is fabricated in HP 0.5µm CMOS operating at 3.3V. The analog structure of each channel of the ASD is shown in Figure 1.

![ASD block diagram](image)

Figure 1: ASD block diagram

It is a fully differential structure with a pair of identical preamplifiers at the input, a shaper stage, followed by a discriminator leading edge charge integrator to be described later. The second preamp provides DC balance, common mode pickup rejection and improved power supply rejection.

Some important specifications are:

- Input impedance: \(Z_{\text{IN}} = 120\Omega\)
- ENC = 5000e rms or ~3.5 primary electrons
- Shaper peaking time = 15ns
- Sensitivity at shaper output: 3mV/primary electron (gas gain \(2 \times 10^4\)) or 12mV/IC referred to delta function into terminated MDT
- Linear range ~1.5V or 500 primary electrons
- Nominal threshold setting: ~60mV or 20 primary electrons (~ 6 \(\sigma_{\text{noise}}\))

SPICE simulation using bsim3V3 models supplied by MOSIS closely match the measured chip parameters.

Preamp

Each preamp is an unfolded n-channel cascode structure, shown in Figure 2, with large input FET M1 of W/L = 2400µm/0.9µm running at 1mA drain current. Current is determined by the p-channel cascode current source, M3/M4. Impedance at the hi-Z node is set by R1. Bias voltages are provided by a bias network (not shown) which is common to all preamps on the chip, but bypassed externally to ground with large capacitors. This insures minimal crosstalk through the bias network (<0.25% measured).

![Figure 2: Cascode n-channel preamp](image)

Input impedance at low frequencies is determined by open loop gain (\(g_{\text{m1}}R1\)) and feedback resistor R2. At high frequencies, it is determined by \(g_{\text{m1}}\) and feedback and stray capacitance. Resistors and capacitors are chosen so that both are equal to 120Ω in spice simulation. Owing to the accuracy of the bsim3V3 models, measured DC and dynamic pulse input impedance are very close to this value.

Since the MDT is terminated at its far end, the termination dominates the noise\(^{10}\) with an additional 30% coming from the preamp.

Shaper

The shaper consists of three near identical differential amplifiers. The first serves only to provide gain and make the signal completely complementary. The basic differential amplifier is shown below in Figure 3.

![Figure 3: Basic differential amplifier](image)
The basic transconductance element is the transistor pair M3/M3a with transfer function given approximately by the product of the drain impedance $Z$, and the source admittance $Y$ (modified somewhat by M3/M3a source impedance). Thus the network can be configured for a variety of desired transfer functions including gain in which both $Z$ and $Y$ are resistive elements, and bipolar shaping stages in which $Z$ is resistive and $Y$ is a series R-C. Bandwidth of each stage is dominated by the product of $Z$ and the load capacitance, typically the gate capacitance of the subsequent stage as well as drain capacitance of M3, M3a, M4, M4a. Typically each stage adds approximately 3–4ns to the total peaking time and is consistent through multiple chip submissions.

The DC operating point is constrained by common mode feedback. This is formed by the upper and lower transistor pairs M5/M5a and M1/M1a operating in their diode region as voltage controlled resistors. Typically these pairs operate with $V_{DS}$ of order 50mV and so very little of the 3.3V supply is given up to their operation. The value of the DC operating point is set by a simple bias network (not shown) controlling the B1/B2 nodes to be $V_{DD}/2$ or 1.65V. Both Monte Carlo simulations and chip measurements indicate that this value is quite process independent and is thus quite accurate, typically ±25mV. The common mode and differential bandwidths of this circuit are approximately the same. This insures, for example, that the output of the first differential amp after the preamp is almost completely complementary with very little common mode component. The stage has very low common mode gain and thus good rejection to substrate induced noise pickup throughout the shaper stage. Probe station measurements indicate that substrate noise coupling from the digital circuits after the discriminator, into the preamp shaper stages is at the few mV level at the shaper output and is considered negligible.

**Wilkinson ADC**

The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of approximately 20ns width at the leading edge of the signal, integrating charge onto a holding capacitor during the gate, and then running down the hold capacitor at constant current. The rundown current is chosen so that maximum rundown time is of order 100ns. The simplified circuit is shown below (Figure 4).

The Wilkinson cell is fully differential and uses the same differential transconductor as the shaper stage as floating current sources, both for the integration current source, as well as the rundown current sink.

![Figure 4: Wilkinson ADC](image)

A simplified diagram of the logic for this cell, the gate generator, is shown in Figure 5.

![Figure 5: Wilkinson gate generator](image)

Both flip-flops are D-type with asynchronous reset. Disc1 and Disc2 refer to the main (timing) discriminator and a second discriminator, which is placed across the hold capacitor of the Wilkinson cell. The input flip-flop, FF1 is configured as a one-shot via the delay element marked DEL. On firing of Disc1, a fixed pulse is thus generated which gates current into the hold capacitor and causing Disc2 to go above threshold. At the trailing edge of the Gate, flip flop FF2 fires enabling the rundown. When the hold capacitor goes below threshold, FF2 resets and the Output pulse is terminated. The box labeled “Dead Time” contains delay elements and logic to preclude re-firing of FF1 both during the current cycle and for a fixed delay afterward. In the final version of the chip, this delay will be programmable over the entire drift time of the MDT, or up to ~1µs.

Unlike the logic for configuring the ASD, the gate generator logic runs during normal MDT operation and so must not induce substrate noise or crosstalk into the analog sections. To insure this, the logic sub-circuits are all fully differential and are bypassed on chip with respect to the power rails. Each logic transition is accompanied by a complement in very close proximity. The logic cells are therefore individually designed and are not standard cell logic.

Preliminary test results of the Wilkinson integrator (just received as of this writing) closely match SPICE predictions. Pulse width dependence on leading edge charge is as expected and substrate coupling from the logic cells is minimal.
Timing Discriminator

The Discriminator is implemented as a differential amplifier with gain of about 5 driving a comparator with hysteresis, as shown in Figure 6. The shaper output is AC-coupled to the diff-amp input, and the discriminator threshold is applied there as an external DC voltage. The diff-amp is very similar to those used in the shaper and described above. The comparator will be described in more detail here.

Figure 6: Timing discriminator block diagram

The comparator is a high-gain differential amplifier with symmetrical current-mirror loads. The main differential pair (M1, M2) is biased at 400µA. Two current-mirror loops provide a differential output. The voltage gain is about 500 with no hysteresis. A simplified schematic is shown in Figure 7.

Hysteresis is provided by (M1A, M2A) which unbalance the static current through the main differential pair by a variable external current, shifting the effective discriminator threshold by up to 100mV. Positive feedback from two inverters reverses the threshold offset polarity when the discriminator fires.

The bias currents for the main differential pair and the hysteresis pair are provided via current mirrors. The main bias current is set at about 400µA using a poly resistor; the hysteresis is controled by an external current.

Figure 7: Comparator schematic

LVDS Output

This cell\textsuperscript{11}, shown in Figure 8, provides a low-level logic output with a nominal swing of 200mV differential into 100Ω centered at 1.2V. This corresponds to the "reduced range link" described in IEEE 1596.3 (the LVDS standard). The circuit is designed to be compatible with a specific receiver (the AMT TDC) and should also be compatible with commercial LVDS receivers. No claim is made that it complies fully with the standard for an LVDS transmitter.

Differential drive is provided directly from the discriminator outputs to two moderately sized inverters. These inverters drive the output stage, which is essentially a pair of current-starved inverters (M1/M2) and M3/M4), with their output current limited by transistor pairs operating in their resistive region (M5-M8). Common-mode feedback from the outputs to the current-limiting FETs sets the common-mode output voltage.

The DC characteristics are set entirely by transistor sizes and are thus subject to process variations. Observations on a small number of fabricated devices largely agree with Monte Carlo SPICE simulations and are compatible with the intended TDC receivers.

Figure 8: LVDS output schematic

Crosstalk and Substrate Noise

Early prototype multi-channel ASD chips showed significant crosstalk of a few percent. This crosstalk was diagnosed as caused by noise coupled to the chip substrate, and subsequently "broadcast" throughout the device. Several remedial measures were taken in subsequent prototypes, and the crosstalk is now below measurable levels (less than 0.5%).

Two distinct types of crosstalk were observed: "Analog" crosstalk – differentiated, proportional to input charge, affecting only neighboring channels and "Digital" crosstalk –in response to discriminator firing, essentially independent of distance from source. A chip fabricated with HP 0.5µm process consists of a heavily-doped silicon substrate about 500µm thick with resistance of about 1Ω, overlaid by a lightly-doped epitaxial layer about 6 µm thick with a much higher resistance of 33kΩ, with the active circuitry
above this. According to the literature the substrate in this type of device can be treated as a single circuit node for analysis purposes, and can couple signals between widely separated subcircuits. In our original prototypes no particular care was taken to prevent this.

Remedial measures included the following: A balanced, differential circuit topology was adopted throughout the design, both to reduce susceptibility of sensitive subcircuits and to reduce radiated noise. The LVDS output driver switches by far the largest currents in the device, and was found to radiate substantial noise. Series resistors were added to degenerate the power supply connections to this subcircuit. Diffused guard rings (with closely spaced contacts) were added around all circuits (digital and analog). For the digital circuits, the guard rings were always placed within 8µm (the thickness of the epitaxial layer) of active transistor area. Guard ring connections were brought out to separate bonding pads, though it was not found necessary to isolate them outside the IC package. Separate bonding pads were provided for digital power, analog power and bias circuit bypass capacitors.

Many remedial measures were taken and the measured crosstalk was consequently minimized. It was not practical to measure the effectiveness of each modification individually.

**Programmability**

Many features of the MDT-ASD will be programmable. They fall into three broad categories and are summarized in Table 1. The adjustments are sent to the ASD as a serial bit-stream using JTAG or a similar protocol.

<table>
<thead>
<tr>
<th>Operating Point</th>
<th>Testing, Cal.</th>
<th>Failure/ Malfunc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing Disc.</td>
<td>Pulse Injection (8 levels)</td>
<td>Dead Time Adjustment</td>
</tr>
<tr>
<td>Timing Disc.</td>
<td>Output Boundary Scan</td>
<td>TOT output mode</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>Channel disable</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. ASD programmable features

The data are converted to physical quantities by custom Digital-to-Analog Converter cells (DACs). According to the requirements, two types of DACs are used: Resistor chain voltage output converters (VDAC) and switchable scaled-transistor current mirrors (CDAC). Figure 9 shows the schematic of an 8-bit VDAC. The converter is implemented using a two-stage scheme (2×16-resistor chains). The range is applied to the RN (negative) and RP (positive) terminals. The 4 MSBs [b7:b4] switch the specified segment of the total range to the second chain, which puts out the selected voltage to the DACOUT terminal according to the LSBs [b3:b0]. Resistor chain DACs are inherently monotonic and exhibit good linearity, depending mainly on transistor and resistor matching of the fabrication process. For the used 0.5µm minimum feature size process, the final layout of the cell has the dimensions 280µm × 250µm. A DAC of this type is used to set the threshold of the main timing discriminator within a range of 0 to 4 times the nominal value (60mV) with a resolution of 1mV.

![Figure 9. 8-bit Voltage DAC schematic](image)

The CDACs supply their output currents directly to current mirrors in the respective cells. In order to meet the stringent requirements for the gate voltages of the mirror transistors, “bootstrap” references are used. With the use of this reference circuit, a variation of less than ¼ LSB at full count for the output current of a 4-bit CDAC at a power supply change of 10% in both directions was achieved (Figure 10). The reference current varies −0.4% (for VDD − 10%) and +1.4% (for VDD + 10%).

![Figure 10. Simulation of a 4-bit CDAC at VDD nominal and ± 10%](image)
Converters of this type control the hysteresis of the main discriminator as well as gate width, run-down current and dead time of the Wilkinson ADC cell.

**Test Results**

The ASD Lite chip was extensively tested on an 8×3 tubes chamber prototype in a cosmic ray setup. The chip proved to be unconditionally stable on this setup.

Figure 11 and Figure 12 show the analog output signal and the discriminator signal for a cosmic muon (ASD lite). Note that this is a signal from a single muon track. The 'spiky' structure is due to charge deposit fluctuations along the track.

![Figure 11: Analog signal from a cosmic ray muon (ASD Lite)](image1)

![Figure 12: Discriminator output for the above signal](image2)

A prime issue is chip protection against high voltage discharges close to the preamp input. It was verified that, with an appropriate input protection circuit on the Mezzanine card, the chip could survive multiple full chamber discharges.

The overall channel to channel crosstalk was measured to be <0.7%.

Figure 13 and Figure 14 show a TDC spectrum from cosmic muons and an ADC spectrum from a radioactive source, which was obtained by integrating the analog output pulse from the scope trace (DSO).

![Figure 13: ADC spectrum from a radioactive source](image3)

![Figure 14: TDC spectrum from cosmic muons](image4)

**Conclusions and Future Plans**

A four-channel all-CMOS ASD has been designed, fabricated and tested extensively on ATLAS MDT detectors. A fully-programmable eight-channel ASD is under development. Roughly 50,000 packaged ASDs will be produced, starting in 2001, for the ATLAS experiment.
References

1 W. Riegler, "MDT resolution simulation, Fronted electronics requirements" ATLAS note ATL-MUON-97-137 (1997) CERN


6 M. Aleksa, W. Riegler "Non-Linear MDT Drift Gases like Ar/CO2 as MDT drift gases” ATLAS note ATL-MUON-98-268 1998 CERN

7 W. Riegler, M. Aleksa "Bipolar versus unipolar shaping of MDT signals” ATLAS note ATL-MUON-99-003 (1999) CERN

8 M. Virchaux, J.F. Laporte, Reconstruction Efficiency and Dead Time” Unpublished internal Muon document


11 The authors gratefully acknowledge conversations with O. Milgrome who suggested this topology.


ASD for the Thin Gap Chambers in the LHC Atlas Experiment

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Abstract

An amplifier-shaper-discriminator (ASD) IC and 16-ch ASD board were designed and built for Thin Gap Chambers in the forward muon trigger system of the LHC Atlas experiment. The ASD IC uses SONY Analog Master Slice bipolar technology. The IC contains 4 channels in a QFP48 package. The gain of its first stage (preamplifier) is approximately 0.8V/pC and the output from the preamplifier is received by a shaper (main-amplifier) with a gain of 7. The baseline restoration circuit is incorporated in the main-amplifier. The threshold voltage for discriminator section is common to the 4 channels and their digital output level is LVDS-compatible. The IC also has an analog output of the preamplifier. The equivalent noise charge at input capacitance of 150 pF is around 7500 electrons. The power dissipation with LDVS outputs (100 \( \Omega \) load) is 59 mW/ch. Beam tests of the ASD boards were made and showed good performance. The results of the irradiation tests by gamma ray and neutrons proved that the circuits retains the properties required for the TGC readout after 10 years of LHC running.

I. INTRODUCTION

The Atlas experiment in the LHC uses Thin Gap Chambers (TGC) \cite{1,2} as its forward muon trigger detectors \cite{3,4}. The total number of TGCs are 3600 and we will be dealing with TGC signals from their anodes (several wires are ganged together) and strips, totaling nearly 330k channels. The capacitance of the TGC as a signal source is a few hundred pF, which comes from the thin gap structure of the chamber and is rather large capacitance when compared with that of an ordinary chamber. The requirement of fast signal processing and the characteristic of large detector capacitance contradict each other when we design a low-noise preamplifier. Much attention was paid to the process choice and circuit design for the TGC application. The ASD as TGC front-end electronics must have a good time resolution for bunch-crossing identification and a high rate capability to cope with high background rate (100 kHz /channel) and must be robust for the longtime operation without maintenance.

II. CIRCUIT DESIGN

Because the signal source has relatively large capacitance and because fast signal shaping as well as low noise are the requirements on the amplifiers, transistors with large \( g_m \) are preferred. Hence we chose to base the amplifiers on bipolar transistors \cite{5,6}. The chip has been developed in collaboration with SONY Corporation, using their bipolar ‘Analog Master Slice Process’. This semi-custom process provides prefabricated NPN and PNP transistors, resistors and capacitors, so that a designer has to design using these elements that are predetermined beforehand for the silicon wafer. The base-structure we used contains 850 NPN transistors, 3834 PNP transistors, 1738 resistors and 42 capacitors, totaling approximately 1000 usable elements. There are five kinds of NPN transistors on the chip including low noise transistors and power transistors. The standard transistor has \( f_T = 3.2 \) GHz. The low noise transistor has \( f_T = 950 \) MHz and base-spread resistance \( r_{bb'} = 17.5 \) \( \Omega \). Availability of the low-noise transistors with very low \( r_{bb'} \) was one of the motivation to use the process. There also are two kinds of PNP transistors of which the standard one has \( f_T = 300 \) MHz. Capacitors are of 2 pF and 20 pF value totaling 408 pF (Metal Insulator Semiconductor, MIS capacitor) in total. resistors are of either 8 k\( \Omega \) or 2.5 k\( \Omega \) (poly-silicon), 297 \( \Omega \) (diffused) and 129 \( \Omega \) (diffused).

Figure 1 : Block diagram of the ASD chip.
A block diagram of the ASD chip is shown in Figure 1, with schematics in Figure 2 and 3. Its first stage is a common-emitter cascade charge amplifier. The input stage of the preamplifier is implemented with the low-noise NPN transistor with $r_{bb}'$ of 17.5 $\Omega$. The relatively large capacitance (higher than 10 pF between the collector and substrate) of the transistor disfavors the use of the transistor in common-base configuration which is usually employed in preamplifiers for chambers [7]. The collector current of the head transistor is set high (0.9 mA) to achieve large $g_m$, which have advantage to achieve lower noise at large detector capacitance. The integration constant is set to 16 ns. The gain of the preamplifier stage is approximately 0.8 V/pC. An emitter follower output of this preamplifier stage is provided for monitoring.

The second stage consists of a main-amplifier with a baseline restorer and differential outputs. The main-amplifier section has a gain of 7. Depending upon the output differential signal level seen by the switch control section, the switch connects to the “A” side or to the “B” side of Figure 1. When the switch is connected to the “A” side, the capacitor $C_b$ will be charged from the current source by the amount of $i$. When the switch is connected to the “B” side,
the capacitor will be discharged by the amount ‘i’, resulting in stabilized DC output levels, or a baseline restoration. In other words, the circuit makes the baseline level of the differential outputs from the main-amplifier to be equal.

Following the main-amplifier is an offset setting which transforms the main-amplifier outputs to the levels required at the inputs to the comparator, where offset voltage is controlled by DC voltage (Vth) supplied from outside of the chip. The comparator is shown in Figure 3. Its outputs conform to the Low Voltage Differential Signalling standard, LVDS, to assure drivability and immunity against noise and minimizing power.

By design, this circuit can be used for both wire and strip signals by setting an appropriate threshold level. Table 1 is a summary of this chip’s characteristics.

Figure 4 shows the result of a PSPICE simulation of the preamplifier output, the main-amplifier differential outputs and the comparator LVDS outputs against impulse inputs of -0.1 ~ -0.5 pC charge. Dynamic range (non-saturated range) of the preamplifier is negative / positive impulse charge input of from -1.2 to +2.0 pC. The slewing rate of the preamplifier also limits the linearity for large positive charge inputs. The dynamic range and the gain of the preamplifier observed at the buffered direct output depends on the external load and is less than the internal one. The circuit can successfully accept signals of 5 MHz or higher frequency.

4 channels of ASDs was fabricated on a 3.1mm X 3.1mm die. The threshold voltage is common to 4 channels. In the layout work of the IC, we paid much attention to reduce interference between analog and digital signals and cross-talk among channels. Both ground and power patterns and I/O pads for the analog part are separated from those for the digital part. The chip is housed in a QFP48 package. For the protection from static charge, diodes are attached between all I/O pads and the most positive / negative voltage excepting those for ground and DC powers.

III. PERFORMANCE

The analog and digital signals from the ASD chip for impulse inputs from -0.1 to -0.5 pC are shown in Figure 5. The overall time walk of the comparator outputs due to the input charge variation of between -0.1 pC to -2 pC is less than 2 ns, when the threshold is set at 0.01 pC equivalent, as shown in Figure 6.

We also tested the performance of the main-amplifier and comparator using prototype chips where the preamplifier, the main-amplifier and the comparator were fabricated separately for independent study. In order to check comparator characteristics, we measured propagation delay

![Figure 5](image-url) Analog and digital signals from the ASD for impulse inputs from -0.1 to -0.5 pC.

![Figure 6](image-url) Overall time walk of the ASD outputs due to the input charge variation.

![Figure 7](image-url) Measured the ENC (closed circle) and calculated ENC (open circle) using design parameters of the preamplifier and measured impulse response of the evaluation system.
while changing conditions such as: varying over-the-threshold-voltage of the input pulse that has fixed rise time / varying over-the-threshold-voltage of the input pulse that has fixed slope / varying rise time while input pulse height was kept constant. The result show that the time walk of the comparator was within less than 2 ns under these conditions. These results agree with predictions by the PSPICE. Temperature dependence of the preamplifier gain was approximately -0.08 %/°C. The feedback capacitor of the preamplifier is supposed to be the major contributor to temperature dependence. The ENC was measured as a function of the input capacitance as shown in Figure 7. We calculated the ENC using design parameters of the preamplifier and measured impulse response of the evaluation system. The calculation reproduces the measured data with the \( r_m \) of 15 Ω and the \( h_{fe} \) of 90. Cross-talk among channels were less than 0.5 % when analog output pins are left open. If the open-emitter buffer for the analog output drives 50 Ω load, the cross-talk became 3 times larger. Influence of the digital part on the analog part was much less than the cross-talk between channels.

**IV. ASD BOARD**

The 16-ch ASD board was designed for wire signals and strip signals from the TGC. Each board contains 4 ASD ICs with protection circuits and a test pulse circuit that receives a test pulse and distributes a charge impulse to each channel. The board design is common for all TGC chambers. LVDS logic signals from the ASD board are transmitted through a 20-pair twisted-pair cable and a preamplifier output through a LEMO type connector. DC power, ground, threshold voltage (common over a channel) and test pulse are supplied back to the ASD board via the same twisted-pair cable. In order to reduce the production cost, the board was designed as a 2-layer PCB. Devices are surface mounted except for connectors on only one side.

**V. BEAM TEST**

We tested TGCs with the ASD ICs at KEK and CERN in 1998. We used pion beams with essentially no background hits at KEK. Whereas at CERN the chamber was tested using muon beams under gamma irradiation. The time jitters and the efficiencies were measured varying the high voltage to the TGC and the gamma irradiation rate. The threshold voltage was set at 5 times of the ENC of the ASD. The time jitters measured are consistent with the ones using hybrid ASD circuits tested before. The rate dependence of the efficiency at applied voltage of 3.0kV is shown in Figure 8. The efficiency is high enough even at five times the predicted background rate (150 Hz/cm²) at the inner station (the worst place). The ASD boards together with the Module-0 TGC chambers perform as expected in the real ATLAS environment. During the beam tests, we could operate the ASD boards very stably and enough performance was proved.

**VI. IRRADIATION TEST**

According to the simulation of the expected radiation environment in ATLAS [8], radiation levels at the TGC wheels are an ionization dose of 0.62 Gy/yr and 1.0 x 10¹⁰ 1MeV equivalent neutron/cm²/yr. Taking into account the uncertainty in the estimation, a safety factor of four is required [8]. The bipolar transistors, which have a higher sensitivity to radiation damage, require an additional factor of 1.5 for the neutron flux and a factor of five for the ionizing dose. The radiation tolerance criteria at the worst location of the TGC trigger station for 10 years running is an ionization dose of 130 Gy and 1.2 x 10¹² 1MeV equivalent neutrons/cm².
Figure 10: Normalized $h_{fe}$ values as a function of $I_c$ for NPN transistors for various neutron fluences.

Figure 11: Gain of the ASD chips versus neutron fluence.

The gamma irradiation tests were performed using $^{60}$Co and $^{137}$Cs gamma ray sources at the rates of 6.7 kGy/hour and 5 Gy/hour. The $h_{fe}$ parameters of the transistors, and the gain and the ENC of the ASD ICs were measured. The result showed that the degradation in $h_{fe}$ at the dose of 100 Gy is within 10%. The gain change of the preamplifier part of the ASD chip were measured up to the total dose of 30 kGy, as shown in Figure 9. Changes in both the gain and the ENC after 100 Gy irradiation are within the range of the piece-to-piece variation.

The neutron irradiation tests were performed using 12GeV Proton Synchrotron at KEK and the Prospero facility in France. Figure 10 shows the $h_{fe}$ values normalized to the ones before the irradiation as a function of $I_c$. After the irradiation of $1.1 \times 10^{12}$ 1MeV equivalent neutrons/cm$^2$, the decrease of the $h_{fe}$ at the nominal value of $I_c$ was found to be less than 10%. Figure 11 shows the gain difference after the irradiation of $1.2 \times 10^{12}$ 1MeV equivalent neutrons/cm$^2$ is within 5%. There was no apparent difference in the ENC up to $1.7 \times 10^{13}$ 1MeV equivalent neutrons/cm$^2$.

It was proved that the ASD chips and the components of the ASD board retain the properties required for the TGC readout after 10 years of LHC running even at the location of the worst background condition.

V. SUMMARY

We have designed and built a chip containing 4 channels of ASDs for the TGCs of the Atlas LHC experiment using SONY semi-custom Analog Master Slice bipolar process. We also developed 16-channel ASD boards and performed beam tests with real TGCs at both KEK and CERN. Irradiation test using gamma ray and neutrons were performed and then radiation tolerance of the chip has been assured. The mass-production (100k pieces) of the chips has been done in summer of 1999 and the assembling of the ASD boards (23k) is scheduled in the first quarter of 2000.

VIII. REFERENCES


Data Flow Simulations through the ATLAS Muon Front-End Electronics

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Abstract
A VerilogHDL simulation of the data flow along the readout chain of the ATLAS MDT front-end is presented. The input rates for this simulation are taken from the chamber occupancies as provided by the ATLAS physics Monte Carlo. The chamber hit-rates include backgrounds as well as hits for collisions of interest. The program has been used to study various trigger tower groupings and to examine the buffer occupancies at a range of luminosities.

1. INTRODUCTION
The ATLAS muon precision chambers are instrumented with Amplifier Shaper Discriminator circuits (ASD) and Time to Digital Converters (TDC) mounted directly on the chamber ends. The ASD units convert the track ionization signals to digital form and the TDC units digitize, store, and transmit time data along serial lines in LVDS form to the readout system. This study begins with this digital information and examines the performance of various designs up through the final on-chamber module called the CSM. Future studies will examine the data flow up to the readout buffers, called ROBs.

Since the performance of the ATLAS muon TDC has previously been examined in simulation[1], the first step in this simulation is to verify that the TDC is appropriately modeled for the hit rates of interest. This is done by matching the output buffer occupancies seen in the full TDC simulation to that modeled for this work. A simple model of the TDC is needed here since this simulation requires the emulation of 18 TDC units and full TDC simulation would be prohibitively slow. Eventually this simulation is expected to be extended to a full ROB group for which 108 TDC models would have to be simultaneously run.

With a suitable TDC model for emulation of the trigger and data rates complete and tested, a design for the next module along the readout chain, the CSM was undertaken. This unit is required to accept serial data from 18 TDC chips, buffer them to avoid data loss, multiplex them into a single output path that is also buffered awaiting transmission to the next unit located in a Tower Summary Crate (TSC) and called the Muon ReadOut Driver (MROD). To date this simulation has been completed up through the CSM module.

A preliminary version of the CSM is also to be fabricated for chamber testing. This version of the CSM, called the CSM-0, is being designed in VME format and will not be chamber mounted as in the final design. It will also not rely on the MROD units for event assembly. The simulations described in this note are for the CSM-0 which does contain event assembly logic. The VME card implementation will also be discussed briefly.

2. DATA RATES AND TDC MODELING
2.1 Predicted Rates in the MDT Chambers
Data from the MDT tubes flows along a data path as indicated schematically in Figure 1. The individual tube sense wires attach to ASD inputs within a Faraday cage covering the tube ends. The mezzanine card that holds three 8 channel ASD chips also contains a 24 channel TDC. The single tube shown in Figure 1 is thus 1 of 24 input to the TDC. Data from all 24 channels is directed to the output upon receipt of a trigger signal to the TDC.

Figure 1 also shows the TDC serial data entering the next module, the CSM. This connection is one of 18 such serial links from 18 distinct TDC chips. The CSM must process each of these 18 sources into a single line to the TSC based MROD. The data path to the MROD is expected to be a fibre link running at 640Mb/s or greater. The MROD is required to handle six CSM outputs and must therefore deal with the data from 108 TDC chips or 2592 tube channels.

The MROD is designed to accept data from a full trigger group, which in the ATLAS MDT requires it to accept up to 6 chamber units or 6 CSM outputs. A preliminary grouping of chambers into towers has been used for this study. Although this grouping is not final it is representative of the choices that are likely. In order to examine the data rates from the MDT up to the ROB a preliminary choice has been made for the chamber groups feeding each MROD. The rates expressed in the Table 1 are for this preliminary grouping. The table has been truncated to a section of the barrel for simplification.

The physics Monte Carlo designated TP43 was used to calculate the hit rates given in Table 1 for each chamber of the MDT. This Monte Carlo contains hits from events of interest and hits from background processes. All backgrounds are included except halo muons, which are expected to be negligible compared to those included. All hits estimated by the physics Monte Carlo must be handled by the ASD and stored within the TDC. All edges, however, are not transmitted by the TDC to the CSM. Only those found
to be within the drift time window are processed and sent to the output FIFO within the TDC upon receipt of an external trigger signal. These hits are serialized and sent along the data path to the CSM. Table 1 shows the number of tubes for each chamber (#Chn), the average tube rates (KHz/Chn), the composite rate of all channel hits accepted by the TDC within the drift interval (MHz), the number of mega-bits sent from the TDC each second (Mb/s/TDC), the number of mega-bits sent from the CSM each second (Mb/s/CSM), the number of CSM units attached to each MROD (CSM/TSC), and the number of giga-bits sent each second (Gb/s/ROB) from each MROD. Clearly, handling these rates will be a challenge. The rates from Table 1 represent the range of values the CSM and MROD designs must accept.

Figure 1 A block diagram of the units through which data flow from the MDT tubes up to the ROB.

![TDC Output FIFO - Full Sim - 9x](image1)

**Figure 2a** The TDC output FIFO occupancy from the full TDC simulation.

![TDC FIFO Occupancy](image2)

**Figure 2b** The output FIFO occupancy for the simplified TDC model for various rates from 1x to 9x.

### Table 1: Average Data Rates

<table>
<thead>
<tr>
<th>Group</th>
<th>#Chn</th>
<th>KHz/Chn</th>
<th>MHz</th>
<th>Mb/s/TDC</th>
<th>Mb/s/CSM</th>
<th>Mb/s/ROB</th>
<th>CSM/TSC</th>
<th>Gb/s/ROB</th>
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<td>36</td>
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<td>22.7</td>
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<td>1.0</td>
<td>2.5</td>
<td>29.9</td>
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<td>29.9</td>
</tr>
<tr>
<td></td>
<td>BIL 6</td>
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<td>41</td>
<td>1.0</td>
<td>2.5</td>
<td>29.9</td>
<td>1</td>
<td>29.9</td>
</tr>
<tr>
<td></td>
<td>BML 5</td>
<td>288</td>
<td>107</td>
<td>2.6</td>
<td>6.0</td>
<td>72.5</td>
<td>1</td>
<td>72.5</td>
</tr>
<tr>
<td></td>
<td>BML 6</td>
<td>288</td>
<td>107</td>
<td>2.6</td>
<td>6.0</td>
<td>72.5</td>
<td>1</td>
<td>72.5</td>
</tr>
</tbody>
</table>

### 2.2 TDC Modeling

The TDC design was formulated in VerilogHDL and a full simulation of its performance exists. Since the character of the simulation is most critical at high rates, a comparison of the full TDC simulation at the highest rate with the simplified version used in this data-flow simulation has been made. Also since the serialization unit of the TDC processes data from the output FIFO only, this particular unit has been simulated only. Thus, for each trigger, the number of hits for each TDC is generated and injected into the output FIFO. The process begins with a trigger, defined to occur a randomly selected time (exponential distribution) after the previous with the appropriate average to produce the desired rate. For each trigger a number of hits is selected randomly from a Poisson distribution with the appropriate mean for the average hit rate.

Figures 2a and 2b show the TDC output buffer occupancy for the full TDC simulation at 9 times the TP43 value, 2a, and for the simplified simulation for values from 1x to 9x. The occupancies match well for the 9x situation. One difference is clearly observed. The TDC has 32 locations in its output FIFO where the
simplified simulation has 64. Since the TDC has a other
internal buffers for data, the final position of its output
FIFO is seen to be occupied for cases when the data in
the simplified simulation extends beyond 32. This
difference is not important since when the FIFO is
highly occupied the serial unit operates continuously
unloading the output FIFO. The simplified version
must have 64 positions in order to avoid loosing data
since it has no other place to hold the hits.

3. THE DATA FLOW SIMULATION

3.1 The Components

That part of the simulation concerned with modeling
the TDC has already been described. It is shown in
bubble of Figure 3 labelled “Emulate 18 TDCs”. For
the results shown the simulation was performed at 5
Hits/TDC and a trigger rate of 75KHz. Other rates have
also been studied.

![Figure 3 The components of the VerilogHDL
simulation including those that provide the input
specification, module definition, and performance
monitoring.]

A second bubble labelled Storage and VME I/O has
also been represented. This part of the simulation is
used for initialization of the TDC and CSM but is not
described since it does not function during data flow
and is not timing critical.

A third bubble labelled TTCem represents the
simulation code for emulating the trigger, timing, and
control in accordance with the LHC design. This code
is needed for development of the control signals to the
TDC and CSM modules but is not specific to the MDT
system and is not described further. The actual
VerilogHDL code for the TTCem is synthesized so that
the CSM-0 module performs the appropriate trigger,
timing, and control.

The primary unit studied in this report is the CSM
module. It contains the core of the data flow functions.
It deserializes the data from the 18 TDC chips and
FIFO buffers them awaiting acceptance by a scanning
multiplexer. Data from the multiplexer is accepted if it
represents input for the current event being sought. The

CSM-0 must therefore have an event FIFO that is
loaded from the TTCem event stream and unloaded in
turn as events are sought from the multiplexer. The
CSM includes an output FIFO that accumulates data for
the event. The final CSM will send data from its output
FIFO to the MROD within the TSC. The CSM-0,
however, sends it output FIFO data to a deep FIFO on
the VME card. It also sends a word count for each
event along with the event ID to a second FIFO. For
the CSM-0 the readout sequence includes a VME read of
the word count followed by a block transfer of the
complete event from the data FIFO.

A final bubble in Figure 3 represents the
performance monitoring code of the simulation. This
code forms histograms of the FIFO occupancies, word
counts/event, and processing time/event.

4. THE RESULTS

A representative simulation is shown in Figure 4a
through 4d. The TDC output FIFO is shown in Figure
4a for the 5 Hits/TDC at a 75KHz trigger rate.

![Figure 4a The TDC output FIFO occupancy at 5
Hits/TDC and 75kHz trigger rate.]

![Figure 4b shows the CSM input FIFO occupancy.]

Figure 4b displays the occupancy of the input FIFO buffer of the CSM module. This is the buffer that holds TDC data awaiting acceptance by the multiplexer. Although the multiplexer scans the incoming data rapidly, this buffer holds appreciable data while the CSM-0 builds an event. The event assembly logic holds off processing data for the next event awaiting data from the last TDC for a given event. During this time the other TDC chips that have continued to send new data.

Figure 4c exhibits the word count per event. For events with 5 Hits/TDC plus headers and trailers, one expects 128 words on the average. The slightly smaller peak in the distribution remains to be investigated. It may be due to round-down of the Poisson generation since the number generation is integer based.

The final plot of Figure 4d shows the processing time (latency) of the CSM-0. The longest time comes from events caught behind a burst of data from previous events. The shortest time represents the minimum transmission time of events with few hits and without contention from previous events. The largest latency is about 50 $\mu$s.

**SUMMARY**

Modeling of hardware with VerilogHDL offers the advantage of performance determination for critical designs. It also provides the source for the development of actual components. If the synthesis of the HDL code into either FPGA or ASIC devices can be shown to meet the clocking specifications, the simulated performance can be delivered by the actual hardware. We expect to commit the CSM-0 code to a Xilinx FPGA and construct the module within weeks.

**REFERENCES**

[1] Requirements and Specifications of the TDC for ATLAS Precision Muon Tracker, Yasuo Arai and Jorgen Christensen, ATLAS Internal Note, MUON-NO-179, 14 May 1997
READOUT ELECTRONICS FOR A HIGH-RATE CSC DETECTOR

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Abstract

A readout system for a high-rate muon Cathode Strip Chamber (CSC) is described. The system, planned for use in the forward region of the ATLAS muon spectrometer, uses two custom CMOS integrated circuits to achieve good position resolution at a flux of up to 2500 tracks/cm$^2$/s.

1. THE ATLAS CSC SYSTEM

The CSC system forms the forward section of the muon spectrometer of ATLAS. It consists of 64 four-layer chambers of 768 x- and 96 y-strips. Interpolation is performed on the x-strips to achieve a resolution of about 50 μm in the precision coordinate. Front end electronics cards are located around the perimeter of each chamber and enclosed by a Faraday shield. With 32 chambers per endcap the total channel count is 55,000. Fiber optic links transfer digital data, clock, and control signals to and from each chamber.

The acceptance of the CSC system is from 2.1 < |η| < 2.7, resulting in an expected flux as shown in Fig. 2 (rates incorporate a standard “safety factor” of 5). Strips in the high-η region will experience an average rate of about 600 kHz, taking into account the spread of charge on the cathode plane. Monte Carlo simulation shows that pileup effects can be tolerated if a bipolar pulse shape with a width less than about 1/5 of the average interpulse time is used.

Signals from each strip are amplified, filtered, and sampled at 40 Msa/s. Sampled data are stored on-chamber for the duration of the Level 1 trigger latency. To minimize the cost and power of the on-detector electronics, a switched-capacitor array (SCA) performs the sampling and storage in the analog domain. Upon receipt of a valid Level 1 trigger, the appropriate samples are read out, digitized, zero suppressed, and transmitted over fiber optic links to the read out drivers (RODs). At a trigger rate of 100 kHz, and assuming ten 10-bit time samples to be read out per channel, per trigger, the gross digitization rate for the CSC system is 6s-10$^6$ chan. /10$^3$Hz> 10b > 10 samples = 6s-10$^7$ bits/s.

Since chamber occupancy is of order 10%, simple zero suppression alone is not sufficient to reduce the data volume to a manageable level. It will also be necessary to suppress data belonging to out-of-time events, and to track segments which do not project back towards the interaction point. Overall, a reduction of about 80 -- 200 is expected. The remaining data, about 1 Gbit/s per chamber, will be transmitted on optical fiber to the RODs, where space points will be extracted by interpolation.

2. SIGNAL PROCESSING

2.1 Pulse Shaping

Because we require a high SNR at high data rates, the signal processing is a tradeoff of rate-handling ability versus noise. By Monte Carlo analysis, it is found that the pileup effects can be avoided if the width of the pulse at the 1% level (FW1%M) is less than 430 ns.

Conventional pulse shaping filters, which use cascaded real poles, produce an asymmetric quasi-Gaussian pulse which becomes more symmetric as the filter order is increased. By using a pulse shaper with complex poles, more symmetric pulses can be obtained with a lower filter order. Hence, we can obtain lower series noise for the same filter order, or lower number of filter stages (thus lower power consumption) for the same noise. A bipolar pulse shape was selected, as its ability to reject low frequency noise, drift, and ion tails was deemed to compensate for the small increase in series noise.

2.2 Signal to Noise

In an interpolating system the fractional position resolution is related to signal to noise ratio (SNR) as

\[ \sigma_x / x = k \sigma / Q \]

where \( \sigma_x / x \) is the position resolution as a fraction of the interstrip spacing, \( Q/\sigma \) is the signal to equivalent noise charge ratio, and \( k \) is a constant of order 1. To achieve the desired fractional resolution of 1% the SNR must be of order 200. The ionization produced in these chambers by a normal incidence track is 90 ion pairs, leading to an induced charge signal on the cathode strip of around 70 fC. Hence to achieve the desired position resolution all sources of electronic noise must amount to less than about 2500 r.m.s. electrons.

3. ELECTRONICS ORGANIZATION

Each chamber has eight 96-channel Amplifier-Storage Module (ASM) boards mounted around the chamber periphery. These boards pick up the 768 x-strips from the four precision cathode planes. The charge signals are
amplified and filtered by preamp/shaper (P/S) ASICs (12 channels per chip) and the amplified pulses are then sampled and stored in the SCA. The ASM board contains eight P/S, SCA, and ADC chips, along with control logic in a 12 x 24 x 0.5 cm volume. The raw data from the ASM at a rate of about 1 Gbit/s is sent to the data concentrator on LVDS links.

A possible layout of the ASM board is shown in Figure 1.

Figure 2 shows a diagram of the ASM board mounting on the chambers.

In Figure 3, the organization of the readout of one endcap is shown.
4. PREAMP/SHAPER ASIC

4.1 Preamp input transistor optimization

The input device is chosen to be an NMOS transistor with minimum channel length. Then, the width is selected to give minimum noise for the allotted power budget. Using the standard analysis the device width that minimizes series white noise is the one that gives a FET capacitance of CDet/3. However, with 0.5μm CMOS and input capacitance of 50 pF the device would be biased in the weak inversion region where the standard analysis is no longer valid. We reduce the device width to put it near the border of weak-strong inversion to achieve a lower capacitance at the same gm. Finally, a behavioral model in MathCAD is used to select the input device dimensions. The current source and cascode devices in the preamp are also chosen for low noise using this mode.

4.2 DC feedback and compensation

For our expected strip capacitance of 20 – 50 pF we choose a preamplifier feedback capacitance of 1.2 pF. A NMOS FET biased in the triode region is used for DC feedback with an equivalent resistance of about 1.2 MΩ, which gives negligible parallel noise and keeps the reset time short enough to prevent the preamp from saturating under the highest expected rate. The bias is provided by a replica circuit which sets the feedback FET’s gate potential with reference to the input/output potential of the amplifier; it is essential to use such a scheme which tracks temperature and process variation to prevent excessive variation of the effective R_F.

The compensation circuit is a nonlinear version of the standard pole-zero compensation used in discrete designs. The compensation FET sees the same gate, source, and drain voltage as the feedback FET and so the two devices maintain a constant resistance ratio even as the preamp output swings in response to a large transient signal. In practice the feedback FET nonlinearity is well-compensated by this system.

4.3 Shaper

The method of Ohkawa [1] is used to design a 7th order shaper which is the best approximation to a true Gaussian waveform. The shaper has a single real pole and three second-order sections in cascade. Each second-order section is made with a multiple feedback topology. This arrangement uses a high-gain inverting amplifier whose input serves as a virtual ground, and has low sensitivity to component tolerances.

The amplifier stages used in the shaper are NMOS-input folded cascodes with a gain-bandwidth product of about 200 MHz. The amplifiers dissipate about 3 mW each. Small current sources at the inputs of each amplifiers allow the input and output DC levels to differ, where necessary to maintain high dynamic range.

The final stage is a symmetric OTA with rail-to-rail class AB output. Dissipating only 5 mW, this circuit can drive up to 400 pF capacitive loads to within 0.1V of either supply rail at slew rates of over 50 V/μsec.

A block diagram of the P/S is shown in Figure 4.
5. SCA

The SCA developed for the ATLAS Liquid Argon calorimeter [2] is well-suited for use in the CSC system. It is organized as 4 groups of (3 + 1 reference) channels, and is capable of simultaneous read and write at 40 MHz with 12 bit resolution. The readout logic of the LAr SCA is internally set to multiplex the outputs of two chips into a single ADC; a modification to the IC has been implemented to allow each SCA to be read out into its own ADC for higher throughput. Otherwise the architecture and pinout of the chip is unchanged.

6. P/S RESULTS

The first prototype of the CSC P/S was received from the foundry in early September 1999 and was found to function in very close agreement to simulations. Figure 5 shows the simulated (solid line) and measured (dotted) waveforms.

Noise and linearity results are shown in Figure 6 and Figure 7 respectively.

To simulate the effect of high rates, double-pulse signals at varying separations were injected. As shown in Figure 8, the interpulse spacing can be below 300 nsec without any pileup.
The Class AB output driver was able to drive low impedance loads with low distortion. Figure 9 shows the output waveform of the P/S unloaded, and loaded by 470 pF and 100.

The performance of the P/S chip is summarized in Table I.

**Table I**

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5 µm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>16</td>
</tr>
<tr>
<td>Die size</td>
<td>2.78 x 3.96 mm</td>
</tr>
<tr>
<td>Architecture</td>
<td>Single-ended</td>
</tr>
<tr>
<td>Intended Cdet</td>
<td>20 – 100 pF</td>
</tr>
<tr>
<td>Input device</td>
<td>NMOS W/L = 5000/0.6 µm, Id = 4mA</td>
</tr>
<tr>
<td>Noise</td>
<td>1140 + 17.6 e-/pF</td>
</tr>
<tr>
<td>Gain</td>
<td>3.8 mV/fC</td>
</tr>
<tr>
<td>Max. linear charge</td>
<td>450 fC</td>
</tr>
<tr>
<td>Class AB Output swing</td>
<td>To power supply - 250 mV</td>
</tr>
<tr>
<td>Pulse shape</td>
<td>7th order complex Gaussian, bipolar</td>
</tr>
<tr>
<td>Pulse peaking time, 5% - 100%</td>
<td>73 ns</td>
</tr>
<tr>
<td>FW1%M</td>
<td>340 ns</td>
</tr>
<tr>
<td>Max. output loading (3% distortion)</td>
<td>500 Ω, 500 pF</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>0.8% adjacent, 0.5% non-adjacent channel</td>
</tr>
<tr>
<td>Power supply</td>
<td>Single +3.3V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>32.5 mW/chan</td>
</tr>
</tbody>
</table>

7. Conclusions and Future Work

The front end electronics of the ATLAS CSC system is in development. The custom ASICs, typically the longest lead-time items in such a project, have completed one prototyping cycle and perform in accordance with specifications. Future efforts in design will concentrate on data selection/compression algorithms, controller hardware design, mechanics, interconnect, and cooling of the on-chamber components, and design of the fiber links and RODs. The first performance test of a complete front end prototype chain will take place this year in a test beam with high background simulation. Qualification testing for radiation tolerance, both of the custom and COTs components, will begin in 2000. Production is slated for 2001 - 2003.

REFERENCES


Abstract
A new front-end amplifier-discriminator-monostable integrated circuit for the CMS Resistive Plate Chambers is presented.

The aim of the circuit is to amplify current signals, ranging from 20 fC to 20 pC and generate output pulses having rise time as fast as possible for timing purposes.

The full custom ASIC was designed and manufactured in the 0.8 µm BiCMOS technology by Austria Mikro Systeme.

1. INTRODUCTION
The Resistive Plate Chambers are gaseous parallel-plate detectors that will be used in the CMS experiment for the muon trigger system [1]. In fact they combine good spatial resolution with an excellent time resolution and make the muon trigger capable of identifying muon track, measure its transverse momentum and relate it to the correct bunch crossing.

The RPC proposed for CMS consists of two 2-mm gaps with common pick-up readout strips in the middle and will be operated in the so-called avalanche mode, for sustaining event rates up to 1000 Hz/cm². The shape of the current signal, induced by a single cluster, is described by the function \( I(t) = I_0 \exp(t/\tau) \), \( 0 \leq t \leq 15 \text{ ns} \), for freon-based gas mixtures having electron drift speed in the order of 130 µm/ns and \( \tau \) (gas time constant) \( \sim 1 \text{ ns} \) at the nominal working point of the detector. This can also be considered a good approximation of the real signal, since almost the whole-induced current originates from the first two clusters.

2. DESIGN CONSTRAINTS
In the barrel RPC, the readout strips are 1.3 m long, with a propagation delay \( \sim 5.5 \text{ ns/m} \) while their width ranges between 2 and 4 cm, according to RPC position in the apparatus. The characteristic resistance of the strip ranges from 40 to 15 Ohm respectively, while their capacitance ranges between \( \sim 160 \text{ pF} \) and \( \sim 420 \text{ pF} \). The induced signal has a rise time \( \sim 1 \text{ ns} \) shorter than propagation delay of the strip, therefore this one behaves like a transmission line and must be properly terminated at both ends. In fact, reflected signals increase occupancy and, if the termination resistance is larger than the characteristic resistance of the strip, a fraction of input charge is reflected and lost. The strip is terminated on one end by the input resistance of preamplifier, on the other end by a resistor.

Simulations and past experience show that, setting the threshold around 20 fC, the detector is fully efficient. This means that a \( \sigma_{\text{noise}} < 4 \text{ fC} \) could be tolerated.

3. CIRCUIT DESCRIPTION
The circuit is made of eight identical channels, each one consisting of amplifier, zero-crossing discriminator, monostable and differential line driver. A single channel block diagram is shown in Fig.1. Since the termination resistor has a small and variable value, an AC coupling between strip and amplifier is required. The requested power supplies are +5V and GND; the overall power consumption is about 45 mW/channel.

3.1 The Amplifier
The preamplifier (Fig. 2) is a cascaded common emitter transresistance stage, with input impedance of 15 Ohm at the signal frequencies (between 100 MHz and 200 MHz), in order to match the characteristic impedance of the strip in the worst case of 4-cm wide strips. In the other cases, the matching will be obtained adding an external series resistor at board level. The current in the input transistor \( Q_e \) is about 700 µA (for noise reason, as shown in §3.2) and, in order to reduce the supply voltage value [2], a resistor \( R_{\text{casc}} \) is added between the emitter and the base of the cascode transistor \( Q_{\text{casc}} \). The value of \( R_{\text{casc}} \) is about 4.5
that is much higher than the input impedance of \( Q_{\text{in}} \) and only a small fraction of the signal current is lost into \( R_{\text{casc}} \). The open loop gain is about 100, while the dominant pole is about 116 MHz and the charge sensitivity is 0.5 mV/fC. A “dummy” input preamplifier was required to balance the DC output variations of the real input first stage.

In
\[ V_{\text{test}} \]
\[ C_{\text{test}} \]
\[ Q_{\text{test}} \]

\[ R_{\text{feed}} \]
\[ C_{\text{feed}} \]

\[ V_{\text{out}} \]
\[ Q_{\text{in}} \]

\[ Y(s) = \frac{sC_{\text{in}} + \frac{1}{R_{\text{feed}}} + sC_{\text{feed}}}{\left( 1 + \frac{g_{m}R_{\text{load}}}{1 + sR_{\text{load}}C_{\text{load}}} \right)} \]  \hspace{1cm} (1)

where \( C_{\text{in}} \) is the input capacitance of \( Q_{\text{in}} \); \( R_{\text{feed}} \) and \( C_{\text{feed}} \) are, respectively, the feedback resistance and capacitance; \( g_{m} \approx 27 \text{mA/V} \) is the transconductance; the parallel of \( R_{\text{load}} \) and \( C_{\text{load}} \) is the internal load across which the voltage gain is produced.

If we set \( R_{\text{load}}C_{\text{load}} = R_{\text{feed}}C_{\text{feed}} \) and define \( C_{\text{tot}} = C_{\text{in}} + C_{\text{feed}} \) then

\[ Y(s) = \frac{g_{m}R_{\text{load}}}{R_{\text{feed}}} \] \hspace{1cm} (2)

If we impose \( R_{\text{in}} = \frac{R_{\text{load}}}{g_{m}R_{\text{load}}} = 15 \Omega \), then

\[ Z_{i}(s) = \frac{R_{\text{in}}}{1 + sR_{\text{in}}C_{\text{tot}}} \] \hspace{1cm} (3)

Being \( C_{\text{tot}} < 3 \text{pF} \), the pole of the above expression is > 1 GHz and

\[ Z_{i} \sim R_{\text{in}} \approx 15 \text{ Ohm} \] \hspace{1cm} (4)

up to the signal frequencies (between 100 MHz and 200 MHz), as required by the matching condition.

The expression of the input admittance is:

The preamplifier is DC-coupled to a gain stage, whose schematic is shown in Fig. 3. It is designed to provide non-saturated response on the dynamic range and to fully exploit the zero-crossing timing, as shown in §3.3. The circuit must ensure a linear behaviour only in the threshold range (\( Q_{\text{in}} < 100 \text{ fC} \)), while for larger inputs non-linearity is not a problem. A simple way to meet these requirements is to design a two-step piecewise-linear function fitting, which is accomplished by summing the output currents of two gain segments. The preamplifier output is sent to two differential amplifiers having different gains but common output nodes. The external amplifier (\( Q_{1H}, Q_{2H}, R_{L} \)) has a DC voltage gain ~ 7 and is used to amplify small signals (\( Q_{\text{in}} < 200 \text{ fC} \)) while the internal one (\( Q_{1L}, Q_{2L}, R_{L} \)) has a voltage gain ~ 0.25 and amplifies signals above 200 fC never saturating in the dynamic range. The overall charge sensitivity is 2 mV/fC for input charges < 100 fC and the power consumption of the amplifier, including the “dummy stage”, is 15 mW.

The transfer characteristics of the amplifier are shown in Fig.4, while a typical transient response is shown in Fig.5.
3.2 Noise calculation

The equivalent circuit of RPC and amplifier for noise analysis is shown in Fig.6 [3]. The parallel noise is dominated by the thermal noise of the terminating resistor $R_0$ at the far end of the strip and can be represented by an equivalent noise current generator with power density $i^2_n$ ($A^2$/Hz) in parallel to $R_0$:

$$i^2_n = 4KT/R_0 \approx 1.1 \times 10^{-21} \text{ A}^2/\text{Hz} \quad (T = 300 \text{ K}) \quad (5)$$

The series noise is represented by an equivalent noise current generator with power density $e^2_n$ ($V^2$/Hz) in series with the input:

$$e^2_n = 4KT (0.5/g_m + R_{bb}) \approx 4.9 \times 10^{-19} \text{ V}^2/\text{Hz} \quad (6)$$

being $R_{bb} \approx 11$ Ohm the base spread resistance of $Q_m$.

Fig. 6. Equivalent circuit of RPC and amplifier for noise analysis.

The preamplifier is current sensitive, so it is convenient to transform the noise voltage generator into an equivalent current noise generator with power spectrum

$$i^2_{ns} = \frac{e^2_n}{|R_i + Z|^2} \quad (7)$$

where $Z = \frac{R_0}{1 + sR_0 C_{tot}} = R_0$ is the impedance shown in Fig.6, assuming the strip impedance matched at the far end. For simplicity, assuming $R_m \approx R_0 = 15$ Ohm, as shown in the expression (4), we obtain:

$$i^2_{ns} = \frac{e^2_n}{4R_0^2} = 5.5 \times 10^{-22} \text{ A}^2/\text{Hz} \quad (8)$$

The rms noise at the output is found by integration of the noise current through $R_m$ multiplied by the square of the magnitude of the amplifier transfer function $H(j\omega)$:

$$V_m = \sqrt{\int \left( i^2_{ns} \left| H(j\omega) \right|^2 \right) df} \approx 2.1 \text{ mV rms} \quad (9)$$

where $H(s) = \frac{V_{out}(s)}{I_m(s)} = \frac{A}{1 + s\tau_L}$ \quad (10)

being $\tau_L$ the time constant of the dominant pole and $A$ the gain. Assuming the line to be ideal, the impedance seen at the far end is:

$$Z_i(s) = R_0 + \frac{Z(s) + R_0 \tanh(st_h)}{R_0 + Z(s) \tanh(st_h)} \quad (11)$$

being $t_0 \approx 7$ ns is the propagation delay and $Z_i$ the expression (3). Then, the parallel noise current flowing into the preamplifier is:

$$i^2_{np} = i^2_{ns} \left| \frac{R_0}{R_0 + Z_i} \right|^2 \quad (12)$$

If we assume again $Z_i = R_m = R_0$, then $Z_i = R_0$ and

$$i^2_{np} = \frac{i^2_{ns}}{4} = 2.8 \times 10^{-22} \text{ A}^2/\text{Hz} \quad (13)$$

The rms parallel noise at the output is:

$$V_{np} = \sqrt{\int i^2_{np} \left| H(j\omega) \right|^2 df} \approx 1.5 \text{ mV rms} \quad (14)$$

Finally, the total output noise is:

$$V_v = \sqrt{V_m^2 + V_{np}^2} \approx 2.6 \text{ mV rms} \quad (15)$$

Simulations of the circuit, including all the noise sources, shows a total output noise ~ 3.4 mV, corresponding to an ENC ~ 1.7 fC, fully satisfying the noise limit of 4 fC.

3.3 Zero-Crossing Discriminator

Accurate timing information from the RPC is crucial for unambiguous assignment of the event to the related bunch crossing. The simplest method to provide trigger pulse is the leading edge timing, which can be performed by a threshold discriminator. Though its simplicity, this method is affected by the amplitude time-walk. In the case of RPC signals, with a 1000:1 dynamic range ($20\text{fC}$ to $20\text{pC}$), the time walk is ~ 10 ns [4].

An amplitude-independent timing response can be approximated by the technique of zero-crossing: a C-R network differentiates the input signal and produces a bipolar pulse crossing the zero in correspondence of the peak of the input signal [5]. In the hypothesis that input signals have the same peaking time, the zero-crossing time is independent of signal amplitude and can be used as time reference. This solution can be easily integrated into ICs. In Fig. 7, the block diagram of the implemented discriminator is shown. The differential outputs of the amplifier are strongly differentiated through a CR network having 4 ns time constant. This grants the fast recovery time of the baseline (< 50 ns) as shown in Fig. 8.
The threshold (arming) discriminator provides charge selection capability and consists of a double stage differential amplifier, with a threshold range between 5 fC and 500 fC.

\[ Q_{in} = 20 \text{ fC} \]
\[ Q_{in} = 600 \text{ fC} \]
\[ Q_{in} = 20 \text{ pC} \]

Time (s)

**Fig. 8 Differentiated amplifier output in the dynamic range.**

A one-shot circuit follows the arming discriminator. It shapes the arming pulse typically at 20 ns, in order to ensure its coincidence with the ZCD output. The zero-crossing discriminator is another double stage differential amplifier, having no threshold. Combining the output of the one-shot and that of the ZCD, we obtain the output of the discriminator, as shown in Fig. 9.

The power consumption of the discriminator is about 8 mW.

### 3.4 The monostable and the Output Driver

In an RPC working in avalanche mode, an after-pulse often accompanies the avalanche pulse with a delay ranging from 0 to some tens of ns. Therefore, a monostable circuit follows the discriminator and gives a pulse shaped typically at 100 ns, in order to mask the possible second trigger and to prevent the zero-crossing discriminator from triggering on the noise. The choice of the pulse length comes from the trade-off between the possible second trigger and the dead time. Being the expected maximum rate less then 400 kHz/channel, a length of 100 ns, giving a dead time of 4%, has been considered a good compromise. In any case, there is the possibility to tune it in the range 50 ns ± 300 ns. The dead time introduced by the monostable is ~ 10 ns and its power consumption is ~ 2 mW.

The Output Differential Driver is capable to feed a twisted pair cable with a signal level of 250 mV on 100 Ω, as required by LVDS receivers. The power consumption is ~ 18 mW but the driver output current can be tuned in order to compensate process variations.

#### 4. TEST RESULTS

14 untested prototypes were received and tested in April 99. They were mounted on a test board housing 2 chips.

##### 4.1 Analog performances

In the first phase, we set the gain of the amplifiers to the nominal value of 2 mV/fC. In the chip, four channels share the same gain control input so we measured the gain uniformity inside each group of four channels. The maximum spread measured was less then ±7%, for input charges < 80 fC. Being the amplifier AC-coupled to the discriminator, this spread represents also a measure of the threshold uniformity and, for our application, it is fully satisfying. For instance, setting the threshold to the nominal value of 20 fC, the maximum expected error is only ±1.5 fC.

The noise was measured using the following technique [6]: an input charge \( Q_{in} \) at the frequency \( f_{in} \) is sent to the circuit. With the superposition of the noise, the signal amplitude has gaussian distribution; we set two different thresholds \( V_{th1} \) and \( V_{th2} \) in order to have the output signal with frequency \( f_{out1} = 0.117 f_{in} \) and \( f_{out2} = 0.883 f_{in} \). Then, \( V_{th1} = V_{th2} = 2.35 \sigma_g = 8.5 \text{ mV} \), corresponding to an ENC ~ 1.8 fC.

##### 4.2 Timing performances

Timing performances were measured using an oscilloscope HP54542C. The threshold was set to 30 fC and charge pulses ranging between 35 fC and 20 pC were injected by means of a pulse generator LeCroy 9210. For all the prototypes, the maximum input to output propagation delay dispersion among the eight channels was measured as shown in Fig. 10. The maximum \( \Delta T \) resulted to be 0.9 ns.
Fig. 11 shows the average delay time: for $Q_{in} < 2$ pC, the time walk is less than 1.5 ns. For higher charges (up to 20 pC) it rises up to 2.5 ns.

Fig. 10. In-chip delay dispersion.

Fig. 11. Average delay time.

5. CONCLUSIONS
A BiCMOS front-end chip for the CMS-RPC detectors has been designed and prototyped. Measurements on 14 prototypes agree with the simulation results and fulfill all the design constraints.

6. ACKNOWLEDGEMENTS
We would like to thank Mr. Raffaele Liuzzi for the definition of the test-board design, Mr. Michele Papagni and Mr. Carlo Pinto for their useful support in the electronic set-up.

7. REFERENCES
PERFORMANCE AND IRRADIATION TESTS OF THE 0.3 μm CMOS TDC FOR THE ATLAS MDT

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Abstract

ATLAS Muon TDC test-element group chip (AMT-TEG) was developed and tested to confirm the performance of critical circuits of the TDC and measure radiation tolerance of the process. The chip was fabricated in a 0.3 μm CMOS Gate-Array technology.

Measurements of critical elements of the chip such as the PLL, and data buffering circuits demonstrated adequate performance.

The effect of gamma-ray irradiation, using a Co60 source, and neutron irradiation, using PROSPERO reactor in France, were also examined. The test results revealed radiation tolerance adequate for the operation of the circuits in the environment of the ATLAS MDT.

1. INTRODUCTION

High-resolution, low-power and low-cost VLSI TDC’s are required in the ATLAS precision muon tracker (MDT: Monitored Drift Tubes). The MDT requires about 370 k channels of sub-nano second TDC to realize the high resolution of the MDT.

Although we have developed several TDCs which fulfill some of the basic requirements, the ATLAS MDT TDC has more demanding requirements especially in data handling. Thus we have began a project to develop a new TDC chip called the AMT (ATLAS Muon TDC) [1] in collaboration with the CERN microelectronics group. To study the chip architecture, intensive Verilog simulations were done [2]. In addition, a quick test chip was developed in a 0.7 μm CMOS process [3] for a medium scale test (10 k channels) of muon front-end electronics.

Since the mass production of the chip is scheduled for year 2001, we have selected a relatively advanced process, 0.3 μm CMOS Gate-Array technology (Toshiba TC220G), for the final TDC chip. This new process provides a lower per channel cost and higher performance. In addition, we can expect a longer lifetime for the process, and, in turn, easier maintenance.

To measure the basic performance of the design and confirm the radiation tolerance of the process, we have developed a test element group chip (AMT-TEG) using the 0.3 μm process.

The chip contains bare NMOS and PMOS transistors, a ring oscillator for radiation tests. Gamma-ray irradiation was performed with a Co60 source at Tokyo Metropolitan University. Neutron irradiation was performed at the PROSPERO reactor in France.

Photograph of the chip is shown in Fig. 1, and a block diagram of the AMT-TEG chip is shown in Fig. 2. There are 24 input channels in the chip. These inputs are connected to three 8 ch ASD chips [4] in the MDT design. To reduce number of input pins, only 16 hit input pins are implemented and selectively connected to internal circuitry in this AMT-TEG chip.

The AMT-TEG chip contains most of circuits used in the final AMT chip. Only the trigger interface and trigger matching circuit are excluded. In addition some circuits were simplified and error checking was minimized.

Fig. 1. Photograph of the AMT-TEG chip. The size of the chip is 5.2 mm by 5.2 mm. Total number of gates used is about 70 k gates. The large block in the left side is the 24-ch channel buffer.
Since the detailed operation of the chip is described in other documents [1, 2], only brief explanation is presented here.

The hit signal is used to store the fine time and coarse time measurement in individual channel buffers. The fine time measurement is obtained from taps along an asymmetric ring oscillator. The time of both leading and trailing edge of the hit signal can be stored.

Each channel has a 4 word buffer where measurements are stored until they can be written into the common first level buffer.

To achieve a high-resolution time measurement with sufficient stability, Phase Locked Loop (PLL) is used. The PLL circuit produces a double frequency clock of 80 MHz from the LHC clock (40 MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained.

2. PERFORMANCE TEST

2.1 PLL and Ring Oscillator

Although the chip is designed in a gate-array technology, layout of the time critical parts such as PLL and the asymmetric ring oscillator were designed manually to achieve high resolution.

We determined the jitter of the PLL circuit by measuring the oscillation period of each cycle. RMS values of the measurements versus frequency and power supply voltage are plotted in Fig. 3 (a) and (b) respectively. The jitter of the PLL is small (< 140 ps) and stable for the 40-120 MHz frequency range and for supply voltages between 2.8 - 3.8 V (normal operating condition is 80 MHz and 3.3V respectively).

The jitter shows a small structure around 90 MHz and the value is a little worse than that of the previous chip [5] which was fabricated in a 0.5 μm process. However the jitter is still small enough for the MDT detector which requires 500 ps resolution. Additional attention will be directed to the layout around the PLL in next chip to achieve better stability.

![PLL Oscillation Stability vs Freq](image1)

![PLL Stability vs Vdd](image2)

![Simulation and measurement results for the oscillation frequency of the asymmetric ring oscillator versus control voltage Vg.](image3)
Fig. 4 shows the control voltage (Vg) dependence of the asymmetric ring oscillator. Results from simulations for worst, typical and best conditions are also indicated. In the present chip, maximum frequency of the oscillator is 130 MHz, and well beyond that required for the 80 MHz operation.

2.2 Two Edge Separation

Recording speed of the channel buffer is important to have a good double pulse resolution or edge separation. Minimum edge separation was determined by reducing pulse width and pulse separation until the hit information is lost.

Fig. 5 shows an example of minimum pulses. Two leading and two trailing edge timing are successfully recorded in the 4 word channel buffer. Since the test instruments cannot generate pulses shorter than 5 ns, actual performance of the chip may be better than 5 ns, which is already far better than the MDT requirement.

2.3 Data Buffering Speed

The data transfer speed from the channel buffer to the first level buffer is an essential part of this TDC architecture. If the channel buffer becomes full, further hit information will be lost. In a Verilog simulation, the probability of hit loss is very low (< 10^-6) for 300 kHz input rate in all channels.

The transfer speed is measured by changing the number of simultaneous hit channels and determining the minimum hit interval where all hits are accepted.

In Fig. 6 we plot minimum hit interval for N channel simultaneous inputs. Above the data point all hit information is recorded, but if the hit interval is reduced less than the data point, a part of the hit information become lost due to the lack of the transfer capability. The line in the figure shows expected speed from the circuit. We see the overhead for arbitration is only 2 cycle and successive data transfer occurs at each cycle.

2.4 Time Resolution

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The result is shown in Fig. 7. The RMS value of 305 ps is obtained. This value is worse than that of previous TDC chip [5] which achieved 250 ps resolution, but still has adequate resolution for our purpose.
2.5 Non-Linearity

Non-linearity of the time measurement was measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. The Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are shown in Fig. 8 (a) and (b) respectively. Both are small enough (RMS < 70 ps) for our purpose.

![DNL and INL graphs]

Fig. 8. (a) Differential non-linearity, and (b) Integral non-linearity measurement.

3. IRRADIATION TEST

3.1 Gamma-ray Irradiation

Gamma-ray irradiation test was done at Tokyo Metropolitan University with a Co\textsuperscript{60} source. The irradiation rate was about 90 rad(Si)/sec, and total dose irradiated was 100 krad(Si). During the irradiation so called worst bias conditions for MOS transistors (3.3 V is applied to NMOS gate, and no voltage is applied to PMOS gate), were used. To study post-radiation effects, parametric measurements were also done after annealing (1 week at 100 degree C) following the MIL-STD-883 method [6].

Total dose expected for worst location of the MDT electronics is 11 krad(Si) for 10 years LHC operation (including a factor 4 safety factor) [7].

In a sub-micron process, most severe damage from the ionization process is an increase of leakage current. Fig. 9 shows drain leak current for NMOS and PMOS transistors. An increase of NMOS drain leak current above 25 krad(Si) was seen while no increase is seen in PMOS. Recovery of the pre-radiation condition is seen after the annealing in NMOS.

Threshold voltage shifts of transistors are shown in Fig. 10. There is no shift seen in PMOS transistors and a NMOS transistor while small shifts (~100 mV) are seen in two NMOS transistors. Since these transistors do not have any protection circuit, the transistors are susceptible to damage. More samples are needed to confirm whether the shift is due to the irradiation or not.

Fig. 11 shows variation of oscillating frequency of a ring oscillator and supply current. The ring oscillator is composed of 33 NAND gates. The oscillating frequency becomes lower above 50 krad(Si). The total chip current was also increased above 50 krad(Si).

Considering low dose rate in the LHC environment, we think the chip can be used safely up to 50 krad(Si), thus the chip has enough margin to be used in the MDT environment.

![Drain leakage and supply current graphs]

Fig. 9. Drain leakage current of (a)NMOS and (b)PMOS transistors. Left-most and right-most points show the value before irradiation and after 1 week at 100°C annealing respectively.

![Threshold voltage shifts graphs]

Fig. 10. Threshold voltage shifts of (a)NMOS and (b)PMOS transistors.
Table 1. Summary of the measurements and the requirements.

<table>
<thead>
<tr>
<th>Measurements</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL frequency</td>
<td>40 - 120 MHz</td>
</tr>
<tr>
<td>PLL operating voltage</td>
<td>2.8 - 3.8 V</td>
</tr>
<tr>
<td>Coarse time counter speed</td>
<td>120 MHz</td>
</tr>
<tr>
<td>LVDS interface</td>
<td>&gt; 100 MHz</td>
</tr>
<tr>
<td>Multiple edge resolution</td>
<td>&lt; 5 ns</td>
</tr>
<tr>
<td>L1B transfer speed</td>
<td>(2+N) cycle</td>
</tr>
<tr>
<td>Time resolution</td>
<td>305 ps RMS</td>
</tr>
<tr>
<td>Diff./Int. Non-Linearity</td>
<td>&lt; 70 ps</td>
</tr>
</tbody>
</table>

4. SUMMARY

A test-element group chip (AMT-TEG) for the ATLAS Muon TDC was developed for circuit performance test. Radiation tolerance was also measured for gamma-ray irradiation and neutron exposure.

Table 1 summarize the results of the present measurements and requirements of the TDC. The AMT-TEG chip demonstrated adequate circuit performance for the MDT TDC. In addition, the 0.3 μm process showed adequate radiation tolerance for both gamma ray and neutrons at the radiation level of MDT front-end electronics.

Acknowledgements

We are grateful to J. Christiansen and CERN microelectronics group for their help on the chip architecture study. Authors would also like to thank, R. Richter for help on the neutron exposure, and R. Hamatsu for help on the gamma-ray irradiation.

5. REFERENCES


3.2 Neutron Irradiation

Neutron irradiation was done at the PROSPERO reactor facility in France. Eight chips were exposed to neutron flux of $1.0 \times 10^{13}$ and 4 chips were exposed to $1.6 \times 10^{13}$ n/cm$^2$ (1 MeV neutron equivalent). During the neutron exposure, chips are placed in a conductive plastic case. The expected neutron flux at MDT front-end electronics for 10 years of LHC operation is less than $1.2 \times 10^{13}$ n/cm$^2$ (including safety factor 4) [7].

After cooling of the radioactivity (~ 2 months), we measured transistor parameters and ring oscillator frequency. We have not observed any apparent change in all sample chips.
A 40 MHz clock and trigger recovery circuit for the CMS tracker fabricated in a 0.25 \( \mu \)m CMOS technology and using a self calibration technique

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**ABSTRACT**

In the CMS central tracker, the LHC clock and the first level trigger decisions are distributed encoded as a single signal. This paper describes an ASIC for clock recovery and first level trigger decoding to be used in the tracker data acquisition and slow control systems. The IC was implemented in a 0.25 \( \mu \)m CMOS technology using a rad-tolerant layout. It recovers the clock and trigger signals meeting the CMS tracker power budget and radiation hardness constraints. In the design of this ASIC a self-calibration techniques was adopted to accommodate for process parameters spread and device parameter changes due to radiation induced damage.

1 INTRODUCTION

The CMS central tracker electronics operates synchronously to the 40.08 MHz LHC master clock. In this system, the clock and the first level trigger decisions are encoded and distributed as a single signal as shown in Figure 1.

![Figure 1 Clock coding scheme](image)

This signaling scheme minimizes the bandwidth and the power requirements of the transmission system. However, a dedicated circuit is required to recover the clock and the trigger signal in the front-end and control modules (Figure 2). The recovered clock is used in the front-end APV ASIC for data sampling and therefore jitter less than 0.5 ns is required to maintain the precision of the analog measurements. As the circuit has to be used in an environment close to the sensitive analogue front-end electronics, it is necessary to reduce the switching noise generated by the IC. Moreover, this circuit has to operate in an environment where, due to the large number of readout channels, the power consumption has to be minimal. Finally, the central tracker is a detector region that exhibits severe radiation conditions \([1, 2]\). It is thus required to guarantee a total dose tolerance that can be as high as 10 Mrad over a period of 10 years.

To meet the requirements described before and the tracker radiation constraints, the IC has been implemented using radiation tolerant layout techniques \([3]\) in a 0.25 \( \mu \)m CMOS technology.

2 PLL-DELAY CHIP ARCHITECTURE

Besides the clock recovery and trigger decoding functions, mention before, the developed ASIC (PLL-Delay IC) implements phase deskewing for the clock and trigger signals. The clock phase can be adjusted in steps of 1.04 ns (fine deskew) up to a maximum delay of 25 ns, while the trigger signal phase can be delayed up to a maximum of 16 clock cycles also with 1.04 ns resolution.

The major blocks of the ASIC are shown in Figure 3, they consist of: a 40 MHz Phase-Locked Loop (PLL), a trigger decoder, a programmable delay line, a calibration

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state machine and an I\textsuperscript{2}C interface that allows programming various parameters in the IC internal registers.

**Figure 3** PLL block diagram

The core of this ASIC is the PLL [1,3, 4]; it consists of the following major blocks:
- a double mode digital phase detector, working, during the lock acquisition, as a 3-state Phase Frequency Detector (PFD) and, once lock is achieved, as a 2-state Phase Detector (PD);
- a charge-pump circuit, converting the signals from the PFD/PD into a control current. The charge pump circuit consists of two 10 μA current sources and four switches controlled by the phase detector outputs;
- a loop filter integrating the charge-pump current and controlling the loop dynamics.
- a 12 stage differential Voltage Controlled Oscillator (VCO). To ensure proper power supply noise rejection and also to minimize the generated noise, a differential constant amplitude VCO, similar to the one described in [3], was used. Each stage is a current-controlled differential delay cell. To optimize the jitter behavior of the VCO, a linear relationship between the VCO control voltage and the VCO frequency was implemented. The signal amplitude of the VCO cell is held constant by means of a replica bias circuit and a power supply independent reference generator.

As shown in **Figure 4**, clock phase shifting is implemented by selecting the output of one of the twelve VCO stages using a multiplexer.

Two conflicting requirements exist in the design of a low jitter PLL. On one hand the smallest possible PLL gain is desirable to ensure the lowest possible jitter in the presence of input noise and of suppressed clock cycles. On the other hand, to cover the whole range of process and temperature variations a high loop gain is necessary to ensure locking. Phase noise filtering is one of the major goals of this design and, consequently, a low loop gain PLL was implemented. In the IC process chosen and with the required low loop gain, it is not possible to guarantee phase locking under all conditions. To circumnavigate this problem a digital circuit implementing an auto-calibration procedure was implemented. This calibration process (to be described later) compensates also for process parameter spreads and device parameter changes due to radiation damages.

**Figure 4** Representation of the clock delay selection

2.1 **SYSTEM STABILITY**

The loop filter consists of a series, resistor/capacitor in parallel with a smaller capacitor. This last capacitor, is added to mitigate the frequency ripple of a second order loop. It introduces an additional pole in the PLL open loop transfer function

\[
G_f(s) = \frac{w_c (1 + sT_2)}{T_2 s^2 (1 + sT_2/b)}
\]

where, \(w_c = K_{\text{VCO}} I_p R(b-1)/2\pi b\), \(K_{\text{VCO}}\) is the VCO gain, \(b=(1+C_2/C_1)\), \(I_p\) the charge pump current and \(T_2=R C_1\).

**Figure 5** Phase margin of the loop as a function of \(b\) parameter. The gray area delimits the variation region of the parameters.

The location of this additional pole must be chosen in such a way that the steady state and the dynamic response should stay practically unchanged. In addition, the presence of this pole has to be chosen to guarantee stability. By inspection of the Bode diagram it was verified that for the chosen design parameters the stability of the system is maintained over the entire range of process parameters, power supply voltages and temperature.

In **Figure 5** the phase margin as a function of \(b\) with \(w_c T_2\) as parameter is shown. For small values of \(b\) the phase margin becomes small indicating a poorly damped system with a conjugate pole pair close to the imaginary axis.
2.2 NUMERICAL MODEL

Phase Locked Loop circuits are difficult to simulate at the circuit level. The complexity of the complete ASIC and the long time required for the PLL to achieve lock (several microseconds of real time) typically demands prohibitively long computing time (> 24 hours) with tools such as Spice. Therefore, a behavioural discrete time model of the PLL has been implemented allowing quick study of the system design space and optimization of the critical circuit components. A model has been developed and coded in C.

![Image of Simulated PLL Jitter](image)

*Figure 6* Simulated PLL jitter when a trigger pulse occurs

The system stimulus can be chosen clean or noisy to study the low frequency noise filtering properties of the PLL. Random triggers, i.e. missing clock pulses, can also be programmed in the clock sequence to simulate real LHC conditions. The simulated response to a missing clock pulse is shown in *Figure 6* when filter parameters corresponding to the actual implementation are used in the simulation model.

2.3 AUTO-CALIBRATION PROCEDURE

To accommodate for process variations and devices parameters changes due to radiation damage an auto-calibration procedure has been implemented. In *Figure 7* (a) it is represented a typical relation between the VCO frequency range and the loop filter voltage. In *Figure 7* (b) it is represented the type of transfer characteristics implemented in this design. The VCO has a small gain ($K_{VCO}$) and its operation frequency is a function of the PLL control voltage ($V_c$) and of an offset current ($I_p$) such that

$$f_{VCO} = K_{VCO} V_c + f(I_p).$$

As can be seen in the picture only some of the curves will allow the PLL to lock at the required 40.08 MHz frequency. Therefore at the start-up (or each time a reset is received) it is necessary to select the suitable locking range. To do this the calibration procedure shown in *Figure 8* is executed.

![State Transition Graph for Autocalibration Procedure](image)

*Figure 8* State transition graph for the autocalibration procedure

The offset current ($I_p$) of the VCO delay cell is initially set to a minimum value ($I_p^0$) and the PLL is allowed enough time to lock.

If the lock is not achieved this means that the VCO is in one of its characteristics curve (*Figure 7*-b) that does not cross the operation frequency and, consequently lock might not be possible. In this case the offset current is increased and the whole process repeated until the circuit is able to acquire lock at the right frequency.

In the case the offset current is set to the maximum value ($I_p^{max}$) and the lock is not achieved, the PLL gain is increased (High Gain mode) and the calibration sequence is started again.

Once the lock is achieved the phase detector - which up to now has been operating in the phase-frequency mode - is switched to the phase detector only mode.

The auto-calibration process is stopped and all the ASIC functions are enabled.
3 IMPLEMENTATION

The IC has been submitted for fabrication using a 0.25 μm CMOS technology (Table 1) and implemented using rad-tolerant layout techniques [5, 6].

Radiation tolerance of integrated circuits is a primary concern in future high-energy physics experiments.

<table>
<thead>
<tr>
<th>Prototype version in 0.8 μm</th>
<th>Prototype version in 0.25 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCMOS, 2 level of metal, 2 poly</td>
<td>CMOS, 3 level of metal, 1 poly</td>
</tr>
<tr>
<td>Power supply=4 V</td>
<td>Power supply=2.5 V</td>
</tr>
<tr>
<td>Area Chip core = 1.6x1.3 mm²</td>
<td>Area Chip core = 0.9x0.8 mm²</td>
</tr>
<tr>
<td>Area Standard Cell = A</td>
<td>Area Standard Cell = A/8</td>
</tr>
<tr>
<td>Area Full custom part = Ac</td>
<td>Area Full custom part = Ac/2</td>
</tr>
<tr>
<td>Available</td>
<td>Submitted for fabrication</td>
</tr>
</tbody>
</table>

Table 1 Technology features

Although radiation hard technology exists, they do not always provide:
- adequate density;
- high volume, high yield and low cost per wafer.

In addition, in a deep submicron technology just because the power supply scales down the power consumption decreases.

On the other hand the ultra thin oxide of deep submicron technologies is inherently tolerant to total dose effects reducing significantly the radiation-induced changes of transistors parameters. Moreover, by employing enclosed geometry and P+ guard-rings around N-channel devices the radiation-induced leakage paths along the edge of the devices and between devices are eliminated.

Recent results have confirmed the potential of this approach, and have demonstrated design solutions in deep submicron technology that minimize total dose effects and the risk of Single Event Upset (SEU).

A previous prototype version of this IC was fabricated in a commercial 0.8 μm BiCMOS technology [8], resulted in an area of 2.6x2.1 mm², where roughly half of the area was used by digital standard cells. In this new version (Figure 9) the area occupied by the digital standard cells has been reduced by a factor of 8 while the full custom part is reduced by a factor of 2. Moreover, due to the reduction of power supply voltage the power consumption has been reduced by about 40 %.

4 CONCLUSIONS

A PLL-Delay ASIC for clock recovery and first level trigger decoding in the CMS tracker has been designed. The IC has been submitted for fabrication using a standard 0.25 μm CMOS technology with a rad-tolerant layout. The ASIC provides a clock signal with adjustable phase in steps of 1.04 ns and a trigger signal with phase programmable in multiples of the clock period. An auto-calibration circuit is used to obtain low jitter avoiding dependency on process and radiation induced damages. A numerical PLL model was implemented to study the dynamic behaviour of the PLL and to allow optimization of the loop parameters.

5 REFERENCES

[6] G. Anelli et al., Total Dose behavior of submicron and deep submicron CMOS technologies,
CANBUS AND MICROCONTROLLER USE IN THE
BABAR DETECTOR AT SLAC

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Abstract

The BaBar collaboration has chosen the Controller Area Network (CAN) [1] bus for its controls and monitoring field bus. In addition, the Motorola MC68HC705X32 [2] microcontroller, which has a CAN interface, was chosen for the standard intelligent device for monitoring boards. This paper describes the CAN system used by BaBar and the embedded software that supports it, using the General Monitoring Board (GMB) as a specific example. The GMB is a CAN module that digitizes 32 differential analog signals and has eight bits of bi-directional I/O.

1. INTRODUCTION

The BaBar detector at the Stanford Linear Accelerator Center's PEP-II collider is designed to study CP violation by accumulating a large number of pairs of neutral mesons containing a b quark. The key to obtaining a large number of these events is efficient operation for a long time, and a critical element in this "factory mode" of operation is reliable monitoring of the entire detector. Early detection of out-of-range conditions can prevent costly down time due to hardware failures.

The heart of the monitoring system is the Experimental Physics and Industrial Control System (EPICS) [3]. This suite of tools uses a VME single board computer both to interface to the monitoring hardware and to serve the data to client processes running on a TCP/IP network. Clients can be such processes as operator displays, data archivers, and alarm handlers.

The BaBar field bus between the sensors and the control system is CAN. This bus follows an open standard that was developed for use in the automobile industry and enjoys widespread use, making parts easily available and inexpensive. Reliability was a primary consideration in its design. EPICS-supported VME hardware exists in the form of an industry pack (IP) carrier board from Greenspring Corporation [4] and a CAN driver IP module from TEWS [5].

Many microcontrollers with a built-in CAN interface exist and it is also possible to use an external CAN interface with most other microcontrollers. The BaBar collaboration chose to standardize on the Motorola MC68HC705X32 microcontroller, which has an embedded CAN interface.

In terms of the OSI reference model for communications, CAN defines the lowest two layers, the physical and datalink layers. EPICS provides the higher layers, although the middle layers are very thin; EPICS appears to CANbus mostly as an application layer. Figure 1 illustrates this structure.

![Figure 1: The OSI Reference Model for CAN](image)

BaBar monitors over 50,000 quantities, distributed among six detector subsystems and a general infrastructure system. Monitored quantities include temperatures, radiation levels, power supply parameters, humidities, gas systems, and front-end electronics.

2. BABAR CANBUS STANDARDS

2.1 CANbus description

CANbus has international recognition as standards ISO 11898:1993 and ISO 11519-1:1994. It is a daisy-chained bus in which two wires carry the signal information. Other wires in the bus carry a ground reference, an optional +5 V line for driving interface circuitry, and a current return for the +5 V line. While other physical implementations are possible, BaBar uses cables of twisted pairs of copper wire.

The two signal lines are labeled CAN_H and CAN_L. In the quiescent mode, both lines are at the midpoint of their range, about 2.5 V. During data transmission these signals go above or below their dormant state by at least 700 mV. When active, the bus is in either a dominant state or a recessive state. The dominant state has CAN_H high and CAN_L low. If multiple modules on the same
bus are trying simultaneously to assert dominant and recessive states, the bus will be in the dominant state. The dominant state represents the value "0" and the recessive state the value "1". Because CAN_H and CAN_L independently carry the information, the bus can function if one of the signal lines is broken, albeit with lower noise rejection.

In general, CAN modules do not need identifiers. Instead, each message carries a message identifier, which also sets the priority, and modules look for messages that they have been told to accept. Thus multiple modules may read a message from the bus and the sending module does not know or care how many modules are reading it. A lower message ID takes priority over a higher one. The CAN standard supports both 11-bit and 29-bit message IDs; BaBar has chosen to use 11 bits.

If a module wishes to use the bus, it begins by sending the message ID while simultaneously monitoring the bus. If at any point, it asserts a recessive state and sees the bus in a dominant state it knows that another module is trying to send a higher priority message and it aborts the transmission. Because the bus is always in the correct state for the highest priority message there is no inefficiency in bus arbitration. At the end of the message, modules that have pending transmissions try again.

Error detection using a 15-bit cyclic redundancy check is built into the CAN hardware, as is a standard error response protocol.

In general, CANbus modules are all equal; there is no intrinsic master/slave relationship.

2.2 BaBar CANbus Usage

BaBar has chosen to restrict the generality of the CAN standard in two ways. First, because we use EPICS and the VME CANbus interface to collect the data, we have what is essentially a master/slave structure. Second, we assign station numbers to each module on the bus and embed it into the message ID. Each module is then told to accept only messages with its own number in the appropriate bits of the identifier.

The BaBar standard CAN message identifier has the following structure:

Bit 10: A priority bit. It exists to allow users to force messages to a higher priority, if needed. In practice, this has been rarely done.

Bit 9: A direction bit. If this bit is zero, the message is from EPICS to the module specified in the module field. If it is one, it is a reply from the module to EPICS.

Bits 8-4 (5 bits): The module field. In general, up to 32 modules can exist on one bus, but for compatibility with a commercial standard used elsewhere in BaBar, we usually drop five of the possible values, leaving a maximum of 27 modules on the bus.

Bits 3-0 (4 bits): The command field. Together with the priority bit this field allows each module to accept up to 32 commands. Eight of the commands are BaBar-wide standards and the remaining 24 are available to users. By restricting eight commands for standard use we were able to develop tools that work on all boards following the BaBar standard. These tools are described in section 4.

2.3 Microcontroller Description

Each standard module has a Motorola MC68HC705X32 microcontroller (MCU) on it. This MCU has a CAN interface, four eight-bit bi-directional data ports, an internal watchdog circuit, and has EPROM, EEPROM, and RAM memory. The EEPROM memory is particularly useful for storing nonvolatile data such as station numbers and CAN register settings.

2.4 Interface Circuit

A standard circuit permits all BaBar modules to have a common interface between CAN and the MCU. A key feature of the circuit is the use of optical isolation to decouple the ground on the CANbus from the ground on the module. This prevents ground loops, which can interfere with monitoring and control.

Figure 2 shows a schematic diagram of this interface circuit. The PCA82C250 is a CAN interface chip and the HCPL710 is an optical isolator.
3. MONITORING BOARDS

3.1 General Description

A variety of monitoring boards has been developed to meet the needs of BaBar. Each of the six detector subsystems has developed at least one to meet its special needs and several boards exist which are used by more than one subsystem.

As the most widely used example of a BaBar monitoring board, we present a description of the General Monitoring Board (GMB). BaBar uses more than one hundred of these, and they are used by all six subsystems.

3.2 General Monitoring Board - Purpose

The GMB is used to monitor voltages, currents, and temperatures. A block diagram is shown in figure 3.

Up to 32 differential analog signals can be read by the GMB and digitized by a 12-bit ADC which covers the range of 0 V to +4 V in 1 mV steps. A passive network conditions the input signals and feeds them to an analog multiplexer (AMUX). The ADC is read by the MCU in a continuous background scan. When the MCU receives a CAN message requesting data, it sends the stored values from the most recent scan.

In addition, the eight signals from MCU I/O port C are brought to a 10-pin connector for such uses as driving relays, setting alarms, and reading valve positions. Care must be taken when using these signals because there is no buffering to protect the MCU and to prevent ground loops from the external connection.

An on-board DC-to-DC converter provides +9 V and -9 V bias voltages for the analog multiplexer and for biasing solid state temperature sensors as described below.

3.3 General Monitoring Board - Description

The module measures 120 mm by 100 mm. The CAN signals arrive on a DB-9M connector which is daisy-chained to a DB-9F connector for the CAN output. The 32 analog signals arrive on a 2x32 DIN connector. The port C signals are connected to a 10-pin low profile Amp connector.

A two-pin connector provides the power. Originally, the board used +5 V power but a later modification added a regulator to allow us to distribute +12 V power and reduce it to +5 V on the board. This eliminated problems associated with voltage drops over long power cables.

Front mounted LEDs display a steady green signal when power is on and an amber flash when a CANbus message is sent or received. Figure 4 shows a photograph of the GMB.

![GMB Photograph](image)

Figure 4: GMB Photograph

A passive input circuit on each channel conditions the input signal. This circuit can convert a current source into a voltage, it can scale an input voltage via a voltage divider, and it can provide a bias voltage for solid state temperature sensors and convert their returned current to a voltage. These are shown in figure 5. The first diagram in the figure shows the general circuit, which consists of two resistors, two jumpers and one optional filter capacitor to reduce high frequency noise.

The second circuit shows the configuration for use with AD592 temperature sensors from Analog Devices [6]. J1 is set to provide a nominal +9 V bias to the sensor, which produces 1 µA of current per degree Kelvin. This current flows across a 10 K resistor to convert it into a voltage with 10 mV per degree Kelvin.

The third circuit uses Rs and Rl to form a voltage divider to scale the input appropriately. Note that Sense_lo is not necessarily connected to the board’s ground via J2.

3.4 General Monitoring Board - Serial Port Version

A modified version of the GMB brings out the serial port from the MCU to permit communication with RS-232 and RS-485 devices. The input signals have active filtering which permits a zero-offset adjustment on each
Figure 5: Input Networks

3.5 General Monitoring Board, Version 2

A revised version of the GMB, called the GMB-2, is being designed. In addition to the capabilities already described, this board will contain a serial interface, allowing it to be read from standard serial ports. In addition, more display indicators are provided and more protection has been included to increase reliability. This version will be marketed by BiRa Systems of Albuquerque, NM [7].

4. SOFTWARE

4.1 Core Microcontroller Software

The MCU software is designed to have a set of core routines common to all BaBar boards. These routines call standard user routines for user-specific code. In the standard software distribution, the user routines are simple stubs.

Core routines are used for such tasks as reading the CAN interface and MCU registers, accessing RAM and EEPROM, and reporting the board status,

4.2 User Microcontroller Software

User-supplied software responds to CANbus commands not included in the set of eight reserved core commands. This software performs user-specified tasks in the background mode, and responds to all interrupts not handled by the core CAN interrupt service routine. This is where users install the unique functionality of their boards.

4.3 VxWorks Software

Utility software exists on the EPICS VME single board computer, which runs the VxWorks operating system from Wind River Systems [8]. Routines exist to scan an entire CAN bus for boards responding to the BaBar standards and to list their serial number and operating parameters. Other routines allow users to change a board's station number and to enable and disable the watchdog circuit on individual boards or all boards on a bus.

4.4 EPICS Applications

Several general tools exist at the EPICS level. These are client applications that provide graphical displays. The most important of them is called canProbe. It allows users to compose and receive arbitrary CAN messages, and it works on any CAN module, not just those following the BaBar standard. Other tools are board specific. Most notable is an application to retrieve and display all 32 channels from a GMB.

5. PERFORMANCE

After an extensive commissioning period using cosmic rays, the BaBar detector is now collecting data. CANbus modules are working in all subsystems and operate reliably. The use of common tools and common hardware has greatly reduced the work in building the monitoring and control system, and allows for a greater pool of expertise in running the detector.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

[1] CAN was invented by Robert Bosch GmbH, Postfach 50, D-7000, Stuttgart, Germany. Additional information can be obtained from CAN in Automation (CiA) at Am Weichselgarten 26, D-91058 Erlangen, Germany.
[2] The MC68HC705X32 is manufactured by Motorola Corporation. Literature is available at Motorola Literature Distribution, P.O. Box 20912, Phoenix, AZ 85036 or at http://motorserv.indirect.com.
[3] EPICS was originally developed at Los Alamos National Laboratory and Argonne National Laboratory.
Much support and development continues to come from its user community. More information can be found at the following web sites:


The ATLAS Level-1  
Calorimeter Trigger Pre-Processor

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Abstract

At the input to the calorimeter part of the Level-1 Trigger a Pre-Processor system performs the preprocessing of about 7200 analogue trigger-tower signals. The preprocessing includes digitisation, identification of the corresponding bunch-crossing in time (BCID), calibration of the transverse energy, rate monitoring, readout of raw trigger data, and high-speed data transmission to the following processors. The preprocessing of a large number of analogue signals requires a compact Pre-Processor system with fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs). In this paper we present the tasks of the Pre-Processor, measurement results, and advanced technologies used for the preprocessing of about 7200 analogue signals.

1 Introduction

The ATLAS Level-1 Trigger is a fast pipelined system for the selection of rare physics processes. Its selectivity achieves an event rate reduction from the 40 MHz LHC bunch-crossing rate down to the first level accept rate of 75 kHz. The Level-1 Trigger searches for isolated electrons and photons, hadrons, jets of particles, muons, and it calculates calorimeter global energy sums within 2.0 μs latency. Hence, fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) are required. For that reason the Level-1 Trigger is also referred to as ‘hardware’ trigger.

The Level-1 Trigger is divided into three subsystems, the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor (CTP). The Calorimeter Trigger gets analogue input signals from the electromagnetic and the hadronic calorimeters. These signals are summed separately in order to form trigger tower signals with a granularity of 0.1 x 0.1 in the η and φ directions. All in all the Calorimeter Trigger has about 7200 analogue input signals, which are transmitted electrically via twisted-pair cables from the detector to the Level-1 Trigger electronics, located in the trigger cavern. The maximum cable length for trigger input signals is 60 m. Based on these input signals the Calorimeter Trigger performs the following tasks:

- preprocessing of input signals;  
- an electron/photon trigger algorithm;  
- a hadron/tau trigger algorithm;  
- a jet trigger algorithm;  
- calculation of global trigger quantities ($E_T$-miss and sum-$E_T$).

The results from the Calorimeter Trigger are the multiplicity of showers passing transverse-energy thresholds, and the coordinates of regions of interest (RoI). The multiplicity information is sent to the Central Trigger Processor (CTP) and the RoI data is sent
to the Level-2 Trigger. See Figure 1 for the overall architecture of the Atlas Level-1 Calorimeter Trigger.

A Pre-Processor Module (PPM) has 64 analogue line receivers to receive the trigger tower signals from the calorimeter. The signals are processed by commercial integrated circuits (ICs) and application specific ICs (ASICs), most of which are located on 16 Multi-Chip Modules (MCMs). A MCM combines different IC technologies, e.g. analogue and digital components to increase the die to package-area ratio. Inside each MCM, four ADCs digitise the analogue signals to 10-bits. Two Pre-Processor ASICs (PPrAsics) perform the BCID algorithm, the transverse-energy calibration to 8-bits in a look-up table, and the pre-summing of jet elements. It also contains pipeline memories to store trigger data up to 2 μs, until a level-1 accept signal arrives from the CTP initiating the readout. Codes for the detection of transmission errors are generated before trigger tower data are serialised to 800 Mbit/s using gigabit links manufactured by Hewlett Packard (G-links). LVDS links from National Semiconductor may be used instead. A bunch-crossing multiplexing scheme, which doubles the effective bandwidth of the high-speed serial link, is used for the transmission of preprocessed trigger towers to the CP. Pre-summed jet elements are serialised on the MCM and linked to the JEP with 9-bit resolution. The φ-duplication of links at quadrant boundaries is fanned out to cable drivers. The readout data from all PPrAsics are collected by one Readout Merger ASIC (RemAsic). This ASIC interfaces to a custom ring-like bus on the backplane (PipelineBus), which shifts readout data via a readout driver board to the readout buffers. Slow control is used to set up the configuration and to load test data.

2 Tasks of the Pre-Processor

The Pre-Processor is of importance for the running of the ATLAS experiment, because all the Level-1 Calorimeter Trigger input data have to pass through it. The tasks that the Pre-Processor system has to perform, based on its input signals can be summarised as follows:

- **Preprocessing**: Provide the trigger processors downstream with digital data containing the transverse energy deposited, identified with the corresponding bunch-crossing. For the Cluster Processor (CP) the granularity is 0.1×0.1 for $|\eta| < 2.5$ and for the Jet/Energy-Sum Processor (JEP) the granularity is 0.2×0.2 for $|\eta| < 4.9$. In both cases the input data are separate for the electromagnetic and the hadronic calorimeters.

- **Readout of event data**: Raw trigger data from the Pre-Processor are needed to tell what has caused a trigger and to allow monitoring of the performance of the trigger system.

2.1 Preprocessing tasks

The preprocessing tasks are illustrated in Figure 2 for the processing of one trigger tower signal. The prepro-
Figure 2: Preprocessing of one trigger tower signal by the Pre-Processor [TDR98].

processing steps are marked as A to H and are described as follows:

A: Reception of analogue trigger tower signals: The differential analogue trigger tower signals are received by a differential line receiver circuit. The input voltage range is linearly mapped, with 0–2.5 V representing 0–250 GeV. A programmable DAC with 10-bit resolution is used to adjust the zero baseline for each input signal.

B: Digitisation and phase adjustment: Each analogue input signal will be digitised by a flash analogue-to-digital converter (FADC) with 10-bit resolution. The time position of the sampling strobe with respect to the analogue input signal can be adjusted in steps of 1 ns within a range of 25 ns. This is required to perform the fine synchronisation of each trigger tower signal and to sample each pulse at its maximum. An ASIC (Phos4) developed by the CERN Microelectronics group will be used for this time adjustment.

C: Synchronisation: The digitised data needs to be synchronised to the same bunch-crossing, because of different time-of-flight for particles from the interaction point to the calorimeter and the different cable lengths from the calorimeter to the trigger cavern (USA15). Synchronisation is done in steps of 25 ns by a FIFO with a programmable depth of 16 bunch-crossings. Assuming a cable propagation delay of 5 ns/m, this corresponds to the delay of an 80 m long cable. This includes enough contingency because the actual cables are not going to be longer than 60 m.

D: Bunch-crossing identification (BCID): This circuit consists of two algorithms to identify the transverse energy deposition represented by a trigger tower signal, and the corresponding bunch-crossing in time. One algorithm is applied to non-saturated signals and one is applied to saturated signals.

E: Lookup table: A lookup table is used to fine-calibrate the digitised data to the deposited transverse energy $E_T$. It maps the 10-bit data after BCID to 8-bit, with a least significant bit (LSB) of 1 GeV. In addition, it can be used to subtract a pedestal and it can apply a minimum threshold to suppress noise.

F: Formation of jet elements: The Pre-Processor pre-sums four 8-bit trigger towers to coarser jet elements with a size of 0.2×0.2. The summing is done separately for the electromagnetic and the hadronic calorimetry, leaving the option to apply separate jet thresholds for electromagnetic and hadronic clusters in the Jet/Energy-Sum Processor. The summing tree in the Pre-Processor requires all four inputs for a jet element to be in adjacent trigger tower channels. The resolution
for the jet elements is reduced to 9-bit accuracy, with a least count of 1 GeV, before transmission.

**G: Bunch-crossing multiplexing:** This transmission scheme (BC-mux) doubles the effective bandwidth of the serial links to the Cluster Processor. In case of a G-link transmitter/receiver chip-set the number of links is only 2166 instead of 4332, with each G-link carrying four trigger-tower signals. This BC-mux scheme can not be used for the transmission of jet elements to the Jet/Energy-Sum Processor because the presumming removes empty bunch-crossings.

**H: Serial data transmission:** Preprocessing results are sent to the downstream processors via high-speed serial links. A high-speed serial transmission is required to keep the number of data links to an acceptable value. The feasibility of a serial data rate of 800 MBd was demonstrated using the G-link chip-set. Because of the high power dissipation of G-links, LVDS links will probably be used for the final system.

### 2.2 Readout tasks

The Pre-Processor provides pipelined readout of raw trigger input data as well as $E_T$ values after the lookup table in order to tell what has caused a trigger and to provide diagnostic information. It allows the monitoring of the performance of the trigger system and the injection of test data for trigger system tests. These tasks are marked as I to K in Figure 2 and are described as follows:

**I: Pipelined readout:** The function of the readout pipelines in the Pre-Processor is equivalent, but independent of those of the detector readout. The Level-1 Trigger captures its own event data as soon as it has triggered. Two sets of pipeline memories capture event data in the Pre-Processor. One records the raw FADC data at the Pre-Processor input and one records after the lookup table and BCID. The number of time slices around an accepted event can be preset to read up to 128 time slices. Without introducing deadtime to the readout, the identified bunch-crossing and two time slices around can be read out.

**J: Data playback:** The Pre-Processor, comprising 7296 input channels, can inject data for technical tests of the Level-1 Trigger system. This allows testing the functioning of the trigger processors and the relative timing of the processors and the input channels.

**K: Histogramming:** This is a useful feature for monitoring of the trigger performance. Two modes of ‘online’ trigger monitoring are foreseen for each trigger tower input at the Pre-Processor. The first mode is rate monitoring, where entries in a histogram above a programable threshold are counted for a given time duration. The second mode is used for monitoring of the transverse energy spectrum of either the raw FADC data or the energy calibrated output after the lookup table and BCID. The latter mode allows the monitoring of a ‘bunch window’ out of the 2961 LHC bunches in one turn.

### 3 Measurement results

This section describes measurement results as part of a modular Pre-Processor test system. The aim was to demonstrate the functioning of the demonstrator MCM, with all its real time preprocessing and its high-speed serial data transmission of trigger tower data. The MCM test set-up consists of two VME motherboards, each equipped with a CMC daughter card. One Motherboard carries a Pre-Processor CMC card and the other one carries a G-link receiver CMC card. As input to the Pre-Processor card, a liquid argon-shaped calorimeter signal was generated by an Arbitrary Function Generator (AFG).

![Figure 3: Correlation of the analogue input signal with the high-speed serial bit-stream (G-link signal).](image)

The input signal is processed by MCM components in the following way: first it is digitised to 8-bit pre-
cision, next, a Pre-Processor ASIC prototype (FeAsic) performs BCID for non-saturated trigger-tower signals, and then a Finco ASIC converts logic levels from TTL to PECL before the data are serialised at 800 MBd by the G-link transmitter chip. The G-link output signals from the Pre-Processor CMC card were connected via a 1 m long coax cable to the G-link receiver CMC card. The G-link receiver decodes the serial bit-stream and provides the parallel output data to a motherboard FPGA. The FPGA latches the G-link data from two G-links (2×16 bits) and writes the data to the motherboard dual-port memory. This is done at a speed of 40 MHz.

Figure 3 shows the correlation of the analogue input signal with the high-speed serial bit-stream. The bunch-crossing-identified data occurs after a latency of 9 bunch-crossings (225 ns) in one G-link bit-stream. This latency attributed as follows: one tick from the FADC, seven ticks from the FeAsic, and one tick from the G-link.

4 Multi-Chip Module technology

A demonstrator Multi-Chip Module (PPrD-MCM) was successfully designed and built (See Figure 4 for a picture). It includes most of the final preprocessing and the readout of the Calorimeter Trigger, for four trigger tower signals. The preprocessing includes digitisation to 8-bit precision, identification of the corresponding bunch-crossing in time (BCID), calibration of the transverse energy, readout of raw trigger data, and high-speed serial data transmission to the Calorimeter Trigger processors.

The MCM has a size of $4.3 \times 3.7 \text{ cm}^2$ and it consists of 9 dies. The MCM was designed with a smallest feature size of 100 µm and it was fabricated in a laminated MCM-L process. It was tested as part of a modular Pre-Processor test system, where transmission and readout tests have shown the feasibility of building a compact Pre-Processor system. Reliability and temperature aspects have been investigated. The clocked MCM temperature is about 42.5 °C, with variations from chip to chip. The un-clocked MCM mean temperature is $34.6 \pm 1.5 \text{ °C}$ (See Figure 5).

Figure 5: Infrared picture used for temperature measurements.

5 Conclusions

The measurement results described here have demonstrated the functioning of the demonstrator MCM. For one analogue trigger-tower signal, most of the preprocessing has been shown. This includes all the preprocessing from the analogue line receiver circuit up to the reception of high-speed serial data at 800 MBd. The established MCM design technique and experience will now be used for the final Pre-Processor Multi-Chip Module. All Details about the final MCM will be specified and then the MCM size can be optimised to fit 16 PPr-MCMs on a VME board aimed to process 64 trigger tower signals.

References

[TDR98] ATLAS Level-1 Trigger Group

*ATLAS First-Level Trigger Technical Design Report*

ATLAS TDR-12, CERN/LHCC/98-14, CERN, Geniva 24 June 1998
OPTIMIZATION OF A READOUT ARCHITECTURE FOR PIXEL DETECTORS

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Abstract

This paper analyzes in detail some theoretical aspects in the modeling of a readout architecture for pixel detectors. In fact, these problems are common to the design of data acquisition systems and other processes containing buffers and where the input and output signals can be expressed by probability density functions. It is the purpose of this paper to point out that the same type of analysis can be extended to other systems with the benefit of saving time in long Montecarlo simulations and prototype design. The example case in which this paper is based on is the readout architecture of a column-based pixel detector amplifier and discriminator chip containing more than 3000 pixels of 50µ x 400µ. Several readout strategies are compared searching for an optimal design, which minimizes data loss and maximizes throughput. In particular, the probability of losing pixel hits by overflowing the readout system is minimized studying the behavior of the stochastic Markov process. Also, the communication channel bandwidths and local buffering are optimized.

I. INTRODUCTION

Pixels Detectors are the future for most of the inner tracker and vertex detector systems in high energy physic experiments. They provide position information in the µm range and a very good signal to noise ratio. The current work has been done at Fermilab, as part of the specification and design of a pixel device to meet BTeV experiment requirements [1]. Since BTeV plans to use the pixel detector as part of the trigger system the most important requirement is readout speed [2]. The primary goal is to achieve a readout rate to cope with the number of hits generated by a luminosity of \(2 \times 10^{32} \text{p/cm}^2\) and a bunch crossing (BCO) time of 132 ns at Fermilb’s Tevatron. The current paper is organized as follows. Section II describes the pixel readout architecture. Section III analyses the problem of the buffers used to Time Stamp the pixel hits. Section IV describes the problem of using FIFOs for data equalization and optimization of the data output channel. Section V discusses the Output Data Channel optimization. Finally, Section V summarizes the results.

II. READOUT ARCHITECTURE

Pixel detectors must provide spatial and temporal information of a particle going through. The particle’s trajectory is calculated based on the information provided by the hit pixels. If the pixel provides only a binary output, the spatial resolution is directly proportional to the pixel size. Instead, if the energy collected in the group of pixels turned on by a single particle is also measured, the hit can be calculated based on the center of mass of that measurement. The later method improves the pixel’s spatial resolution. The current example assumes a chip of 18 columns by 160 pixels. The pixel cell size is kept constant at 50µ x 400µ. The pixel cell provides a digitized value of the collected charge.

As said, the purpose of the current paper is to find a general framework to design a pixel readout architecture subject to the imposed requirements: maximum readout speed and minimum data loss. Data loss is caused by overflows of the internal resources (i.e. registers and buffers available). An optimization of those resources is mandatory since they increase the so-called “dead area” of the chip, the area that cannot be covered by pixel detectors [3].

Figure 1 shows one possible readout architecture. This architecture is not guaranteed to be optimal but depicts component blocks and points of analysis. The Pixel Array readout is organized in columns. Each column has its own End of Column Logic (EOC) at the bottom. The pixel cells store hit location, a 2 or 3 bit value of the input, and a pointer to the Time

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III. ONE BUFFER OR MULTIPLE BUFFERS?

The readout architecture showed in Figure 1 has one TSR buffer and EOC logic per column. However, any number of TSR and EOC sets can be implemented. The columns can be grouped to Time Stamp and to be readout using any number of TSR and EOC sets. The first part of this section considers the case of a single TSR buffer for the entire chip. The second part considers multiple TSR buffers.

II.1 One buffer

The TSR buffers contribute to the chip’s dead area. Hence, its number must be minimized. However, the random nature of the pixel hit rate will make the number of required TSRs to fluctuate in time. If all the TSRs are being used, the incoming hits are lost until a TSR becomes available. This stochastic process can be modeled as a Markov process. A single TSR buffer can be modeled as a birth-death process as shown in Figure 2. The TSR buffer’s input and output are stochastic variables with Poisson distributions with parameters \( \lambda \) and \( \mu \) respectively [4]. The TSR registers form a M/M/1 queue.

Figure 2: Markovian birth-death model for a single TSR buffer

The state equation of an M/M/1 queue must satisfy the Chapman-Kolmogorov equation of state transition. This leads to a complex differential-difference equation. However, the most important system characteristics can be obtained analyzing the steady state of the queue. The balance equations are:

\[
\begin{align*}
\lambda \cdot p_k &= \lambda \cdot p_{k-1} + \mu \cdot p_{k+1} \\
\mu \cdot p_0 &= \mu \cdot p_1
\end{align*}
\]  

Substituting (2) in (1):

\[
p_k = p_0 \cdot \left( \frac{\lambda}{\mu} \right)^k = p_0 \cdot \rho^k \quad \rho = \frac{\lambda}{\mu}
\]

\[
p_0 = 1 - \rho
\]

It is clear that the system is stable for values of \( \rho < 1 \). That is, when the average input rate is smaller than the average output rate, otherwise the buffer size grows unbounded. \( \rho \) also represents the utilization factor, that is the proportion of time the output is busy. The M/M/1 first and second moments can be easily derived:

\[
E[N] = \frac{\rho}{1 - \rho} \quad \text{Var}[N] = \frac{\rho}{(1 - \rho)^2}
\]

Where \( E[N] \) is the expectation and \( \text{Var}[N] \) the variance of the process. According to Little’s formula[4]. The average response time can be expressed as:

\[
E[R] = \frac{E[N]}{\lambda} = \left[ \mu \left( 1 - \rho \right) \right]^{-1}
\]

II.2 Multiple buffers

On the other hand, a multiple buffer TSR set can be analyzed as follows. Figure 3 shows the state transition diagram of a 2 buffer system. The solution can be generalized for m-buffers.

Figure 3 State transition diagram of a 2 buffer system

The balance equations can be inferred from the transition diagram:

\[
(\lambda_1 + \lambda_2 + \mu) \cdot p(k_1, k_2) = \\
= \lambda_1 \cdot p(k_1,1, k_2) + \lambda_2 \cdot p(k_1, k_2,1) + \mu \cdot \left[ p(k_1,1, k_2) + p(k_1, k_2,1) \right]
\]

\[
(\lambda_1 + \lambda_2 + \mu) \cdot p(k_1,0) = \\
= \lambda_1 \cdot p(k_1,1,0) + \mu \cdot \left[ p(k_1,1,0) + p(k_1,1,1) \right]
\]

\[
(\lambda_1 + \lambda_2 + \mu) \cdot p(0, k_2) = \\
= \lambda_2 \cdot p(0, k_2,1) + \mu \cdot \left[ p(0, k_2,1) + p(1, k_2) \right]
\]

\[
(\lambda_i + \lambda_j) \cdot p(0,0) = \mu \cdot \left[ p(0,1) + p(1,0) \right]
\]

And the normalization factor is:

\[
\sum_{k_0, k_1} p(k_0, k_1) = 1
\]

The solution of this system can be found by direct substitution (see [5]) and is expressed as:
\[ p(k_1, k_2) = (1 - \rho_1) \rho_1^{k_1} (1 - \rho_2) \rho_2^{k_2} \]  
\[ \text{Where,} \quad \rho_1 = \frac{\lambda_1}{\mu} \quad \text{and} \quad \rho_2 = \frac{\lambda_2}{\mu} \]

Since \( k_1 \) and \( k_2 \) are independent, this system of two buffers can be generalized to an m-buffer system in the following way:

\[ p(k_1, k_2, \ldots, k_m) = \prod_{j=1}^{m} (1 - \rho_j)^{k_j} \rho_j^{k_j} \]  
\[ \text{(12)} \]

Then, the Poisson random variables describing the TSR buffer input and output are statistically independent. The expectation and variance for each TSR buffer can be calculated as:

\[ E_r[N] = \frac{\rho_i}{1 - \rho_i} \quad \text{where} \quad \rho_i = \frac{\lambda_i}{\mu} \]  
\[ \text{(13)} \]

\[ \text{Var}_r[N] = \frac{\rho_i}{(1 - \rho_i)} \]  
\[ \text{(14)} \]

Several important conclusions can be drawn from the comparison of (4) and (5) with (13) and (14). First, we are interested in the average number of occupied TSR buffers. If a system is designed with only one TSR buffer common to all the columns, then the average number of occupied buffers is given by equation (4). The values of \( \lambda \) and \( \mu \) can be calculated based on the average number of hits and the average number of TSR released every cycle, \( \lambda = \text{p.h/T} \) where \( \text{p} \) is the probability of having a hit during a certain time interval \( \Delta T \), and \( \text{h} \) is the number of \( \Delta T \) intervals in \( T \). In the current example, \( \lambda \) depends on the pixel hit rate which for a fixed pixel chip is directly proportional to the luminosity of the accelerator’s beam generating the events. The maximum value that \( \lambda \) can reach in the single TSR buffer architecture is given by the use of one TSR every cycle of the accelerator’s beam (BCO). A system demanding one TSR every BCO has a \( \lambda \) equal to 7.57. Accordingly, \( \mu \) is calculated based on the pixel-hit distributions along the pixel chip. These distributions are obtained from simulations. In our case \( \mu = 20.41 \) 

Then, \( E[N] = 0.58 \)

In the multibuffer approach, the expectation values can be calculated based on the input’s probability distribution function (pdf). For instance, let’s assume one TSR buffer per pixel column as shown in Figure 1. According to [6][7], the hit rate distribution in the pixel detector planes follows an inverse quadratic law respect to the proximity of the pixel to the center of the beam:

\[ p(r) = \frac{1}{r^2} \quad \text{or} \quad p(x, y) = \frac{1}{x^2 + y^2} \]

Where \( r \), \( x \), and \( y \) are the coordinates from a pixel to the center of the beam. Since the pixels are handled by column readout, we are interested in all the hits affecting an entire column. Hence integrating along the y-axis:

\[ p(x) = \int_{-\infty}^{+\infty} \frac{1}{6} \frac{1}{x^2 + y^2} dy = \frac{1}{x} \left[ \text{erf}^{-1} \left( \frac{13.68}{x} \right) - \text{erf}^{-1} \left( \frac{6}{x} \right) \right] \]

The resulting pdf is shown in Figure 4.

![Figure 4 Probability density function of an 18-column pixel chip](image)

It is clear that the total number of TSR buffers used in the multibuffer approach is the sum of the expectation in every column. That is:

\[ E_{tot}[N] = \sum_{i=0}^{N} E_i[N] = \sum_{i=0}^{N} \frac{\rho_i}{1 - \rho_i} \quad \text{where} \quad \rho_i = \frac{\lambda_i}{\mu} \]  
\[ \text{(15)} \]

The total expectation is calculated based on the \( \lambda_i \) values obtained from the column pdfs functions (Figure 4) and the already calculated \( \mu \).

\[ E_{tot}[N] = 2.08 \]

It is easy to see that in the case of the pixel detector chip, if every column is assigned to its own TSR set, when a beam event hits more than one column, the same Time Stamp will be stored in as many registers as columns are hit. In average, the \( E_{tot}[N]/E[N] \) ratio equals the average column hit rate per bunch crossing of the accelerator. In other words it is a function of the accelerator’s luminosity. This ratio can easily reach 5 for the expected luminosity of the Tevatron at Fermilab (2 * 10^{11} p/cm^2).

As important as the average number of occupied buffers is its dynamic fluctuation. It was said that if the number of TSR registers is overflowed all new data is lost until the readout system releases a TSR. A good measure to this problem is provided by the Variance of the process. The number of required TSR buffers can be calculated based on the 1st and 2nd moments and the maximum data loss allowed in the system. Let’s allow a maximum data loss of 10\text{exp}(-5). This is equivalent to an entry of 3.12 in the Gaussian error function. In other words the buffer must be at least 3.12*\sigma+E[N] deep. Where \( \sigma \) is the standard deviation. This value can be used to calculate the maximum \( \rho \) value (\( \rho = \lambda/\mu \)) allowed. In the current example, since the \( \rho \) values are already given, we can calculate the minimum buffer size to keep the data loss less than a certain value (p.e. 10\text{exp}(-5)). In the single TSR buffer approach the minimum buffer depth (MBD) is:

\[ \text{MBD}[N] = \text{inv}_-\text{erf}(\text{mx}_-\text{error}) \times \sigma + E[N] = 3.12 \times \sigma + 0.58 = 3.4 \]  
\[ \text{(16)} \]
In the multiple TSR approach, the buffers must be considered individually since they may overflow separately. However, since the hit distribution is monotonic decreasing with the distance to the beam it suffices to analyze the busiest column (i.e. column 1). Then, 
\[ MBP[N] = \text{inv}_\text{erf}(mx._\text{error}) \ast \sigma_1 + E[N] = 3.12 \ast \sigma_1 + 0.15 = 1.4 \] (17)

IV. THE FIFO BUFFERS:

The pixel data is readout off chip using a single high-speed synchronous communication channel, the Output Data Controller (ODC). In order to optimize the overall pixel readout system’s throughput the ODC utilization must be as close to 100% as possible. This can be achieved having one or more FIFO buffers inside the pixel chips to equalize the random pixel hit data flowing from the pixel array. Different schemes can be analyzed based on the two-buffer tandem system. The simplest system contains one TSR buffer and a FIFO buffer. Other systems with multiple TSRs and FIFOs can be calculated using the corresponding \( \lambda_i \) and \( \mu_i \).

The two-stage tandem network is shown in Figure 5a. The state diagram is shown in Figure 5b. The system has some similarities with the one described by (11). This system has 2 buffers in series instead of parallel.

The balance equations can be inferred from the transition diagram:
\[
(\mu_i + \lambda) p(k_1, k_2) = \\
= \mu_i p(k_1 + 1, k_2 - 1) + \mu_i p(k_1, k_2 + 1) + \lambda p(k_1, k_2 + 1) \\
(\mu_i + \lambda) p(k_1, 0) = \mu_i p(k_1 + 1, 0) + \lambda p(k_1, -1) \\
(\mu_i + \lambda) p(0, k_2) = \mu_i p(1, k_2 - 1) + \lambda p(0, k_2 + 1) \\
\lambda p(0, 0) = \mu_i p(0, 0)
\]

And the normalization factor is 
\[
\sum_{k_1, k_2} p(k_0, k_1) = 1.
\]

The solution of this system can be expressed as:
\[
p(k_1, k_2) = (1 - \rho_1), \rho_1^k (1 - \rho_2), \rho_2^{k_1}
\]

where \( \rho_1 = \frac{\lambda}{\mu_1}, \rho_2 = \frac{\lambda}{\mu_2} \) (18)

Again, we find that \( \rho_1 \) and \( \rho_2 \) are independent in the steady state. The expected number of registers occupied in each buffer can be obtained analyzing the marginal probability
\[
P(N_1 = k_1) = p(k_1) = (1 - \rho_1), \rho_1^k.
\]

The last equation does not reflect the overflow problem in the TSR buffers since the state diagram was not bounded. It is worth to mention that no overflow occurs in the FIFO buffers since the data can be held in the pixels until the FIFO full condition goes away. The overflow can be calculated limiting the size of the buffers. Let’s assume that the sizes of the TSR and FIFO buffers are \( n \) and \( m \) respectively. Then the overflow is:
\[
P_{ov} = P(k_1 > n) = \sum_{k_2 = 0}^n \sum_{k_1 = 0}^m p(k_1, k_2)
\]

\[
= \lambda, p(n, 1) + \lambda, p(n, 2) + \ldots + \lambda, p(n, m)
\]

\[
= \lambda, \sum_{k_2 = 1}^m (1 - \rho_2), (1 - \rho_1) \rho_1^{k_2}
\]

\[
= \lambda, (1 - \rho_2), (1 - \rho_1) \sum_{k_2 = 1}^m \rho_2^{k_2}
\]

\[
= \lambda, (1 - \rho_2), (1 - \rho_1) \frac{1 - \rho_2^{m+1}}{1 - \rho_2}
\]

\[
P_{ov} = \lambda, (1 - \rho_1), (1 - \rho_2)^{m+1}
\] (19)

Figure 6 shows the probability of overflowing the TSR buffer as a function of the number of registers in that buffer. The number of registers in the FIFO buffer is used as a parameter. The plots show that the Pov decreases when the number of registers in either buffer is increased.
p(k1, k2, ..., kn) does not have an analytical expression and must be represented by its transition matrix:

\[
P = \begin{bmatrix}
p_{00} & p_{01} & \cdots & p_{0n} \\
\vdots & \ddots & \ddots & \vdots \\
0 & \cdots & \cdots & 0 \\
p_{m0} & p_{m1} & \cdots & p_{mn}
\end{bmatrix}
\]

then, the probability distribution function of the steady state can be found taking

\[v = \lim_{n \to \infty} P(n)\]

Where \(v\) represents the steady state of the system and \(P(n)\) is the n-iterated transition matrix. It evident that for \(n \to \infty\) the solution to this system must accomplish:

\[v = P.v \Rightarrow (I - P).v = 0\]

The last equation can be solved analytically or numerically. Then, the overflow can then be obtained computing:

\[P_n = \lambda \sum_{k=1}^{\infty} P_{kn}\]

V. MAXIMIZATION OF THE OUTPUT CHANNEL UTILIZATION

The last point in the analysis of this architecture concerns the output data channel (ODC). It is clear, that from the system’s performance point of view the utilization of the output channel must be maximized. The utilization is maximized by reading-out data from the pixels, as soon as possible and keeping the FIFO(s) not empty, unless the pixel array is empty. The analysis of this system is similar to the one of Section III. The system can be designed with one or more FIFOs. The equations describing the probability distribution function, and moments are the same as (3), (4) and (5) for the single buffer and (12), (13), and (14) for the multi FIFO approach. It is obvious that in order to maximize the utilization of the output channel, the speed of the data input to the buffers must be higher than the speed of the output. Then, the output is the bottleneck of the system and the FIFOs are loaded unless the pixel array is empty. This condition makes the data output work close to 100% of utilization. The Utilization (U) of a single FIFO system (M/M/1 queue) is equal to \(\rho\). If \(U = \rho \geq 1\) (i.e. \(\lambda \geq \mu\)) the system becomes marginally stable or unstable. Since the FIFOs do not loose data, as is the case with the TSR buffers, this is not an undesired condition.

The output data channel is usually designed based on system constrains such as data path width and data output clock rate. This parameters are imposed by the mechanical and electrical characteristics of the inter-connective system, and they define the \(\mu\) of the Poisson distribution of the output channel. The \(\lambda\) will depend on the input’s architecture. That is the number of FIFO buffers. The convenience of having one or more FIFO buffers has a similar analysis to the one in Section III. A single buffer system with a data input rate \(\lambda\) equivalent to the sum of the individual input rates \(\lambda_k\) of the multi-buffer system, will minimize the buffer size and, hence, the dead area.

In practice, a high speed and small size (i.e. 8-bits, 100MHz clock) data output is preferred due to system integration issues. A single buffer can keep \(\rho < 1\) by having an internal wider data bus, transferring all the information corresponding to one pixel, or a group of pixels, at once (i.e. pixel coordinates, Time Stamp, and digitized input value).

VI. CONCLUSIONS

This paper analyzed some theoretical aspects in the modeling of a readout architecture for pixel detectors. Most of this analysis can be extended to data acquisition systems where buffers are used to equalize data flows coming from different sources. The analysis of systems as random processes can be very advantageous, avoiding long Monte Carlo simulations and costly prototype designs. The particular case study in which this paper is based on, the readout architecture of a column-based pixel detector amplifier and discriminator chip, has shown that a single TSR buffer will minimize the dead area, minimizing the total number or buffer registers, while providing the same performance. A measure of relative buffer size can be defined as:

\[
BSR = \frac{\sum MB_D[N]}{MBD[N]},
\]

where \([MBD]\) and \([MBD]\) are integer numbers representing the minimum buffer size needed. The BSR of one TSR buffer per column versus a single TSR buffer is 9. Section IV showed how to design a system to minimize overflow and what is the influence of TSR and FIFO buffer size in the overflow measure. It was also shown that a single FIFO system can keep very small overflow rates with small size buffers. Finally, Section V showed that a saturated system is convenient to maximize the output channel utilization.

REFERENCES:


Abstract

We have developed a prototype data link board in order to test Single Event Upset mitigation techniques in a programmable logic device and to investigate the adequacy of the selected devices for the ATLAS Front-End links. We used only commercial off the shelf (COTS) devices on which radiation tolerance data was available. Different digital design methods for transient error elimination in an FPGA will be compared and radiation tolerance of the serialiser and media interface will be tested. Our card can also be used as a simplex S-LINK Link Source Card using G-LINK as physical layer with optical or electrical media.

1. INTRODUCTION

In recent years great advances have been made in the field of programmable logic technology. While once Programmable Devices (PLD) were mostly applied to prototyping, logic emulation systems and extremely low volume applications, they now are used in a number of high volume devices, and in exotic applications in hostile environments like radiation or high temperature.

Front-end links are used to transfer data from electronics systems placed on detector to off-detector read-out drivers. Some functions, like high speed serialising can not be implemented in PLDs due to speed limitations. It is probable that the detectors will use commercially available or ASIC devices for such functions. Calorimeters and Muon Detector could use programmable devices as glue logic devices which interface between standard components and detector specific interfaces.

Some programmable logic devices, like most antifuse based FPGAs, are tolerant to the low or moderate radiation dose rates which are present at calorimeters and Muon Detector ATLAS Front-End link locations. However, these chips may have transient errors termed Single Event Upsets (SEU) caused by energetic particles.

2. SEU IN DIGITAL LOGIC CIRCUITS

A Single Event Effect (SEE) is defined as any measurable effect to a circuit due to a nuclear particle strike. A Single Event Upset corresponds to a soft error (data corruption) appearing in a device due to the energy deposited in silicon by an ionising particle. High energy protons and neutrons are also known to produce ionisation effects indirectly through nuclear reactions within the silicon [1].

SEU is a non-destructive phenomenon, which concerns in general every memory element temporarily storing a logic state. Typical examples of circuits affected by SEU are random access memories, registers, microprocessors, programmable logic devices, digital signal processors, etc (Figure 1).

![An SRAM configuration element (switch) in a programmable device](image)

Figure 1: An SRAM configuration element (switch) in a programmable device

3. SEU MITIGATION METHODS

System-level SEE requirements based on functional impact may be fulfilled through a variety of mitigation techniques, including the use of hardware, software and device tolerance requirements. All of the potential SEE mitigation methods may require that either additional hardware or software be added to the system design.

Hardware or software design may serve as effective mitigation, but design complexity may present a problem. The most cost efficient approach of meeting a SEE requirement may be an appropriate combination of SEE-hard devices and other mitigation.

It is convenient to classify system level SEE effects into two general categories: those that affect data responses of a device, and those that affect control of a device or system. When using programmable or semi-custom circuits it is not evident how to divide devices into categories like data or control related units. Today’s complex FPGAs allow a whole system to be implemented within a single chip, including data related
subcircuits like RAM, FIFO, encoding or decoding circuits and control related functions like signal processors, state machines or counters. This means that different mitigation technologies have to be used within the same device.

3.1 SEE Propagation Analysis

A SEE may propagate through a circuit, subsystem and system, thus making system-level impacts an important consideration. SEE propagation analysis is the science of determining the effect and potential risk that the occurrence of a SEE has on the device where the event occurs, on its associated circuitry and subsystem. For example, a SEU occurs in a serialiser of a data link causing a single flip in a data bit. This "invalid" data sample may provide a false observation of an event, which may significantly modify the results of the data analysis.

3.2 Mitigation of Memories and Data-Related Devices

Error detection and correction (EDAC) offers a method for trading bandwidth for error rate. Incorporating EDAC in a link adds logical complexity and a certain amount of latency to the system. Replacement of failed memory parts with scrubbing is an other emerging technique.

The simplest, but "detect only" EDAC method is the use of parity checks. Another common error detection method is called cyclic redundancy check (CRC). CRC detects if one or more errors are occurred in a given data structure. Hamming code is a simple block encoding that will detect the position of a single error and the existence of more than one error in a data structure. Reed-Solomon codes are capable of correcting consecutive and multiple erroneous bytes. Convolutional codes can correct isolated burst noise in a data stream [2].

3.3 Mitigation of Control-related Devices

The techniques described in the previous section are useful for data SEUs. They may also be applicable to some types of control SEUs. A memory that stores program or configuration data for a microprocessor can be an example.

Watchdog timers may be implemented in both hardware and software and are used to indicate the health of the devices by sending a message from one system location to another. If the message is not received by the next location within a set time period, a time-out occurs and an action is launched to repair or replace the faulty block.

Redundancy between circuits or subsystems is an effective method on both flip-flop and system level. Switching between redundant subcircuits can be done by voting or by a higher level intervention. In some reprogrammable FPGAs a redundant system may be implemented with a very low overhead by reserving free resources. A place and route tool would be invoked to search for a new placement for the failed parts [3].

4. A PROTOTYPE DATALINK CARD

Our card (Figures 2, 4) can be used as a Test Data Generator for on-line radiation testing or as a simplex S-LINK [4] Link Source Card using the HP G-Link [5] as physical layer. The circuit’s actual function depends on the configuration of the FPGA. The aim of this project was to develop a circuit board in order to test a candidate programmable logic device (PLD) for implementing a radiation tolerant digital datalink.

4.1 Test Data Generator Mode

If the FPGA is configured as test data generator (Figure 3), two independent data paths can be used to check the correct functioning of the card. With this configuration the card requires three control signals on its differential (RS-422) inputs which select test patterns or reset the card.

![Figure 2: Block diagram of the test card](image-url)

![Figure 3: Test Data Generator Configuration](image-url)
Four different test patterns can be generated by the loadable circular shift registers. To test the internal functioning of the PLD, four shift registers are implemented. Two of them are made from triple modular redundant (TMR) flip-flops to reduce SEU probability. We chose this mitigation method because TMR is an effective mitigation method on flip-flop level, the circuit operation does not stop temporarily in case of an error which is important in a data link application and this method is supported by some design tools. One data path is sent to and fed-back from device pins to test the I/O circuits as well. The data patterns at the outputs of the shift registers are compared in each clock cycle. If no errors have occurred, the comparison result will be true. If a SEU occurs in one of the shift registers, in the I/O feedback path or in the comparator, the result of the comparison will be false.

Since the signalling speed is limited on the twisted pairs going to the control room, multiple words are compared in one "test period" and a latch is toggled if one or more comparison errors occur during this time. The length of a test period is 6.4 µs. At the end of each test period a "control pulse" is sent from a counter on one twisted pair. Similar, "test" pulses are generated on the three other twisted pairs in case no comparison errors occurred during the test period. The theoretical error probability (the probability that the pulse is missing at the end of a test period) is different on each line. This method ensures a slow signalling rate on the twisted pairs and full speed operation of the internal logic circuits. The clock frequency is 40MHz, which is the read-out frequency of most ATLAS Front-End links.

The second data path serves for monitoring the joint functioning of the FPGA, serialiser and media interface. The test pattern generated by the FPGA is framed into 224 word packets, which start and terminate with a control word and are sent to the G-Link serialiser with four parity bits. The serialised data is transmitted using optical (standard 9-pin transceiver) or electrical media (Lemo connector) to the receiver.

4.2 S-Link Source Card Operation Mode

In case the FPGA is configured for S-LINK Source, the card serialises the data on its FIFO-like 16- or 32-bit parallel interface and transmits it via electrical or optical media. The simplex G-LINK LDC can be used to receive the data.

This simplex S-LINK is capable of transferring 16-bit serial data continuously at a 40 MHz clock frequency using four parity bits and the G-Link coding scheme for error detection.

5. RADIATION TEST SETUP

The irradiation started on the 1st of June, 1999. The test zone is settled along a secondary beam line of the CERN Super Proton Synchrotron (SPS) accelerator, downstream of a particle-conversion target [6]. The radiation field is typical of a proton accelerator; it includes mainly gammas and neutrons, plus some high-energy particles.

5.1 FPGA Test Signals

The test signals are processed in the remote control room by a PC with a National Instruments PCI-DIO-32-HS high speed digital I/O module. Data acquisition and error detection is controlled from Labview. The error detection can detect if one or more (control or test) pulses are missing or if none of the pulses are received, as control pulses show up periodically. If the control pulse is missing, it is due to an error occurred in the pulse generator circuit. In case no pulses are received for
a longer period, permanent damage of the circuit is probable.

5.2 G-Link Test Signals

The G-LINK serialiser (HDMP-1022) sends serial data to the optical media interface. At the receiving side the simplex G-LINK LDC is used. The FPGA of this card includes an automatic data checker, which checks the data pattern, parity and packet length of the received packets. If an error occurs, an error code is generated and the erroneous data with the error code will be written into a log file on the host computer (PC, Linux).

6. RADIATION TEST RESULTS

On the first two weeks of the irradiation period the card was powered from the power supply of a VME Crate. A power MOSFET transistor was found to be extremely sensitive to radiation in the VME's power supply and three power supply units have died in a very short period, after a few Grays of radiation. The power supply was changed to an external one, which is placed to an area where the dose rate is relatively low.

The total accumulated dose between during the first two months was ~20Krad. The card stopped functioning after 9 weeks of operation. The problem was the degradation of the LM117H Linear Regulator chip which generates 3.3V supply voltage for the Actel chip from 5V. Its output voltage has dropped to 25% of its value measured before irradiation. The chip was replaced 3 weeks later.

The upset rate was in correlation with the dose rate (gamma). As on-line neutron fluence detection was not available we could not make a direct relation between radiation intensity and error rate. The error rate in the first month of irradiation was 2-15 bit flips and 1-4 synchronisation errors per day.

No errors were observed on the A54SX16 FPGA.

7. CONCLUSIONS

We did not observe single event errors on the A54SX16 FPGA. Tests at NASA [7] show that this chip does not latch-up and its supply current is not increasing significantly until more than 50Krad. This makes this chip suitable for use in low dose rate environment. We are planning to test this chip in heavy ion radiation in order to investigate the effectiveness of the used SEU mitigation methods.

The LM117H voltage regulator chip proved to be rather sensitive to radiation. We are planning to test the HS-117RH radiation hardened voltage regulator.

It is necessary to find a radiation tolerant serialiser which does not loose synchronisation in radiation since it can take up to 600 microseconds while the link regains synchronisation and 48 Kbytes of data is lost during this time.

It would be essential to establish a reference radiation environment where neutron energy spectra is known and similar to that of the future LHC application in order to estimate the error rate in the real application.

Future investigations are necessary to prove the radiation tolerance of the laser transceiver.

REFERENCES

7. NASA-GSFC radiation test results: http://rk.gsfc.nasa.gov/fpgas.htm#Some Radiation Test Results - SX Series Radiation Data
The ALICE Detector Data Link

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Abstract

The ALICE detector data link has been designed to cover all the needs for data transfer between the detector and the data-acquisition system. It is a 1 Gbit/s, full-duplex, multi-purpose fibre optic link that can be used as a medium for the bi-directional transmission of data blocks between the front-end electronics and the data-acquisition system and also for the remote control and test of the front-end electronics. In this paper the concept, the protocol, the specific test tools, the prototypes of the detector data link and the read-out receiver card, their application in the ALICE-TPC test system and the integration with the DATE software are presented. The test results on the performance are also shown.

Introduction

During the preparation of the ALICE Technical Proposal [1] the need emerged for a common interface between the front-end electronics (FEE) of the different detectors and the data acquisition system (DAQ). A dedicated working group was formed to collect in a document [2] the needs of the detectors and the DAQ. The following main requirements have been identified:

- only one standard link, named detector data link, for the information transfer between the FEEs of all the sub-detectors and the DAQ;
- standard protocol;
- point-to-point full-duplex optical connection;
- high-speed transmission of event data;
- remote control and test of the FEEs from the DAQ;
- bi-directional data block transfer between the DAQ and the FEEs.

Concept

The detector data link (DDL) and the read-out receiver card (RORC) constitute together the detector read-out chain. The DDL transfers the event fragments from the experimental pit to the computing room and stores them in the input buffer of the RORC. The RORC interfaces the DDL to the front-end digital crate (FEDC). The DDL consists of the following components:

- source interface unit (SIU), connected to the FEE;
- destination interface unit (DIU), connected RORC;
- physical medium (two fibre optic cables).

The FEDC is responsible for the sub-event building. The RORCs, plugged-in the FEDC, are controlled by a SBC. The local data concentrator (LDC) reads-out the event fragments from the RORCs and assembling them into sub-events. Then the sub-events are sent to the central event building switch. If it is reveals to be needed, separate I/O busses could be used for the control and the read-out functions in this crate, because of the speed limitation of the available standard backplanes. We hope, however, that in a few years high-performance channel-based I/O busses (e.g. System I/O) or really fast standard backplanes (e.g. VME320 or VME1000) will be available. In this case the two I/O busses will be merged and the final version of the FEDC will have only a single I/O bus.

Figure 1 shows a part of the ALICE DAQ, consisting of a detector read-out chain and a sub-event building system.
In most applications, the SIU will be connected directly to the FEE (see Figure 2).

**Figure 2** Direct connection to the FEE

In some of the applications (for example, where the level of the radiation is too high for the SIU), the SIU will be placed outside of the detector with a distance of several meters. In this configuration a radiation hard medium-speed transceiver shall be used inside the FEE. The DDL is connected to the FEE through a DDL. This configuration is foreseen for the Si-Pixel detector.

**Figure 3** Indirect connection to the FEE

Figure 4 shows another possibility for the indirect connection. In this case the DDL concentrator is implemented as a VME interface, and the information is transmitted between the two VME crates by using two DIUs and two RORCs. This configuration is foreseen for the trigger detector, because the trigger unit will be placed in a VME crate. Dedicated software will emulate the behavior of the SIU and the FEE, so from the DAQ point of view this configuration will be identical to the basic configuration.

**Figure 4** Indirect connection through VME bus

The DDL is connected to two external systems (e.g. FEE and RORC). The RORC-DIU interface consists of 2 uni-directional busses for the full-duplex information transfer (see Figure 5). It is, for example, possible to send commands to the FEE or the interface units, while event data are transmitted from the FEE to the DAQ.

**Figure 5** The DDL interfaces

The FEE-SIU interface consists of a bi-directional bus and a JTAG controller port [3], which can be used for the remote testing and control of the FEE via the TAP.

**Main technical parameters**

The main data flow will take place from the FEE to the RORC. The DDLs will be able to read-out the complete ALICE events (40 MB) within less than 2 ms, transmitting event data from the FEE to the RORC with a detected bit error rate of $\leq 10^{-15}$. Each DDL will be able to transmit data at a rate of 100 MB/s. As the zero suppression algorithm requires downloading big blocks of data into the FEE, a throughput of 10 MB/s is needed in the opposite direction. Both the FEE and the SIU will be remotely controlled from the FEDC through the DDL, since their placement inside the detector will not allow using any other cabling apart from the DDL physical medium. Therefore, commands and status information will also be transmitted between the FEE and the RORC. Since the SIU is located inside the detector, the requirements for the lifetime ($\geq 10$ years), the power consumption ($\leq 5$ W) and the footprint ($\leq 50$ cm$^2$) of this unit are key issues. More strict requirements have been identified for the ITS [2] sub-detectors where radiation tolerant electronics is needed and the footprint of the SIU shall be less than 20 cm$^2$. To achieve the high reliability of the experimental apparatus, efficient test of all the sub-systems will be provided. The DDL will allow testing the FEE remotely by using JTAG controller port of the SIU. The DDL itself will also have a powerful self-test mode.

**DDL protocol**

1. **Protocol layers**

The DDL protocol consists of four layers: the DDL interface layer (most upper), the signaling and framing layer, the coding layer and the physical layer.

The DDL interface layer is described in the Interface Control Document (ICD) [4]. It includes the physical and electrical description of the interface units. The ICD defines also the interface signals, the information structures, the transactions and the timing.

The signaling and framing layer is described in the Physical and Signaling Interface Specification [5]. It is...
a mixture of the FC(2) layer of the Fibre Channel Standard [6] and DDL specific solutions.

The coding layer is compatible with FC(1) layer of the Fibre Channel Standard (FCS), where the well known 8B/10 coding scheme is used [7].

The physical layer is compatible with FC(0) layer of the FCS. For the DDL prototype the 100-M5-SL-I nomenclature is used, having the following main parameters: 100 Mb/s transmission speed, 50 µm multi-mode optical fibre, 850 nm laser transmitter, data transmission up to 500 m distance.

2. Transactions

The information transfer on the DDL is organised in control-status transactions and block transfer transactions. The control-status transactions are simple, while the block transfer transactions are complex, consisting of several control-status transactions. All the transactions are started by a command and terminated by a command transmission status word. It indicates, if any errors have occurred during the transaction.

The following control-status transactions are defined:
- front-end electronics control;
- front-end electronics status read-out;
- interface unit control;
- interface unit status read-out.

Figure 6 shows the FEE status read-out transaction, as an example of the control-status transactions.

The following block transfer transactions are defined:
- event data transmission;
- data block downloading;
- data block read-back;
- self-test.

Figure 7 shows the event data transmission transaction, as an example of the block transfer transactions.

Prototype project

The main goals of prototype development project are:
1. build a prototype of the complete read-out chain;
2. develop hardware and software tools for the test;
3. integrate the read-out chain with DATE [8] software;
4. try out the system in normal working conditions.

1. Components of the read-out chain

The following tasks are included in this project:
- experimental media interface (MI) design and test;
- DIU development;
- RORC development;
- SIU development.

Within the MI test sub-project, the design and the test of an 1.06 Gbit/s MI circuits and an experimental PCB layout and stack-up have been accomplished and the main functional components have been selected and tested. The results of these tests allow us to safely integrate the high-speed serial MI directly on the DDL cards.

Within the DIU development sub-project a first prototype version and an improved prototype version have been designed, built and tested. The DIU photos can be found on the WEB [10]. The DIU consists of two main functional parts: the protocol engine and the media interface (see Figure 8). In the protocol engine the three upper layers of the DDL protocol are implemented. The MI interfaces the protocol engine to the physical medium. It realises only the lower protocol layer. It is able simultaneously to send and receive serial data stream with a transmission speed of 1.06 Gbit/s, so some
signals in this sub-system can have harmonics up to 7 GHz. The PCB layout design is quite critical here, this is the explanation why a MI test project was necessary. The main technical features of the DIU are:

- multi-volt system (+5V and +3.3V supply voltages);
- 48 cm² footprint;
- 9x1 OT² with duplex SC fibre optic connector;
- FC³ electrical transceiver (53 MHz reference clock);
- protocol engine is in two FLEX10K50A PLDs:
  - 4 clock signals are used
  - single port FIFO is available only
  - +3.3V core logic;
- two EPC1 configuration PROM;
- passive serial configuration.

Within the RORC development project, a first prototype and an improved prototype version have been designed, built and tested [11]. The photos can be found on the WEB [10]. The main task of the RORC is to receive and store temporary the event fragments, coming from the FEEs through the DDL [1]. When the LDC is free, the event fragments are read out from the RORC by the LDC for the sub-event building. The RORC is also able to transmit data blocks and commands to the FEEs and receive status information from them through the DDL.

The prototype SIU now is under development. The components have been selected, the mechanical, the PCB layout and the digital designs are ready. The SIU has similar architecture as the DIU. The main technical features of the SIU are:

- single +3.3V system;
- 27 cm² footprint;
- 5x2 SSF⁴ OT with VF45-RJ fibre optic connector;
- serial backplane electrical transceiver:
  - 53 MHz reference clock
  - built-in elastic buffer
  - 106 MHz reference clock
  - built-in 8B/10B encoder/decoder
- protocol engine is in one FLEX10K100E PLD:
  - 2 clock signals are used
  - dual port FIFO is available
  - 256-pin FineLine BGA package
  - +2.5V core logic;
- single EPC2 configuration EPROM;
- ISP configuration via JTAG chain.

Figure 8 The architecture of the DIU

The prototype SIU now is under development. The components have been selected, the mechanical, the PCB layout and the digital designs are ready. The SIU has similar architecture as the DIU. The main technical features of the SIU are:

- single +3.3V system;
- 27 cm² footprint;
- 5x2 SSF⁴ OT with VF45-RJ fibre optic connector;
- serial backplane electrical transceiver:
  - 53 MHz reference clock
  - built-in elastic buffer
  - 106 MHz reference clock
  - built-in 8B/10B encoder/decoder
- protocol engine is in one FLEX10K100E PLD:
  - 2 clock signals are used
  - dual port FIFO is available
  - 256-pin FineLine BGA package
  - +2.5V core logic;
- single EPC2 configuration EPROM;
- ISP configuration via JTAG chain.

Figure 9 The architecture of the prototype RORC

The RORC consists of two memory buffers for the high-speed transmission of the incoming and the outgoing data blocks and a FIFO for the incoming status information. For the testability, a loop-back multiplexer and a DDL test multiplexer are used, supporting the RORC and the DDL self-test working modes. Figure 9 shows the architecture of the prototype RORC. The main technical features of prototype RORC are:

- normal, RORC and DDL self-test modes;
- two DDL channels;
- up to 3M x 32 bit input buffer;
- 512k x 32 bit output buffer;
- 64 x 32 bit status FIFO;
- VME64x (VITA 1.1-199x) module and connectors;
- 6U board height;
- A32, D8-32, D32_BLT, D64_BLT transfer types;
- 50 MB/s block transfer rate;
- slave and interrupter building blocks;
- programmable base address;
- interrupt event: status FIFO is not empty.

2. Hardware and software tools for the test

For testing and monitoring of the DDL and the RORC, the following hardware tools have been developed:

- DIU extender (DIUEXT);
- SIU extender (SIUEXT);
- SIU simulator (SIMU);
- FEE emulator (FEMU).

---

² optical transceiver
³ fibre channel
⁴ small form factor
The DIUEXT is an extender board, having the same footprint as the DIU. It can be inserted between the DIU and the RORC. There are five connectors on this board, providing connection for logic analyzers for the monitoring all the RORC-DIU interface signals. The photo of the DIUEXT can be seen on the WEB [10].

The SIUEXT is an extender board, having the same footprint as the SIU. It can be inserted between the SIU and the FEE. There are four connectors on this board, providing connection for logic analyzers for the monitoring all the FEE-SIU interface signals.

The SIMU is a manually controlled simple device, having the same footprint as the SIU. It can be used for the basic hardware tests of the FEE. The SIMU is able to execute all the FEE transactions, according to the DDL protocol.

The FEMU is able to emulate the behavior of all the ALICE detectors. It is based on a HP logic analyzer system (see Figure 10). An interface card has been developed for the connection of the HP-LA to the DDL.

The data traffic on the optical fibres can be studied by using a FCS monitor and analyzer device.

System test within normal working conditions

The DDL first has been tried-out within normal working conditions in the ALICE-TPC test system [13]. In this test setup (see Figure 11) the DDL has been used in indirect configuration (see Figure 4). For requesting the transmission of event data block, a command is sent from the read-out crate to the front-end crate. This action is followed by an event transfer in the opposite direction.

Integration with DATE software

The DATE [] is currently used by the NA57 experiment as data acquisition software. In the future, most of the ALICE sub-detectors will use the DATE for the FEE tests and the beam tests as well. Since the DDL and the RORC will also be key elements of these tests, the integration of the complete read-out chain with the DATE software is a high priority task. Therefore DDL software library has been integrated with DATE during the Q2/1999 [14] and the complete read-out chain has successfully been tested by transmitting several TB of data with different patterns and block lengths.

Performance Tests

The system performance has been tested in DIU-DIU configuration. The task-to-task command delivery time between two MVME 2604 processor is about 6 μs. The read-out speed has been measured in 64-bit block transfer mode by using both MVME 2604 processors and MVME 4604 processors. Table 1 shows the test results of the for the MVME 2604 processor, while Table 2 for the MVME 4604 processor. It was identified in both cases that the block transfer speed is limited by the DMA speed of the processor, but not by the RORC.

<table>
<thead>
<tr>
<th>block size [MB]</th>
<th>400</th>
<th>4k</th>
<th>40k</th>
<th>400k</th>
<th>1M</th>
</tr>
</thead>
<tbody>
<tr>
<td>speed [MB/s]</td>
<td>5.0</td>
<td>19.1</td>
<td>26.4</td>
<td>28.7</td>
<td>28.9</td>
</tr>
</tbody>
</table>

Table 1 Data transmission speed with MVME 2604

<table>
<thead>
<tr>
<th>block size [MB]</th>
<th>400</th>
<th>4k</th>
<th>40k</th>
<th>400k</th>
<th>1M</th>
</tr>
</thead>
<tbody>
<tr>
<td>speed [MB/s]</td>
<td>5.7</td>
<td>23.3</td>
<td>33.7</td>
<td>38.0</td>
<td>38.3</td>
</tr>
</tbody>
</table>

Table 2 Data transmission speed with MVME 4604

References
6. Fibre Channel Physical and Signalling Interface (FC-PH); ANSI X3.230-1994
11. G.Rubin and J.Sulyán: “VME Read-out Receiver Card (RORC) for the ALICE-TPC Test System”; ALICE/97-14, Internal Note/DAQ, 05.05.1997
13. J.Bracinic e.a.: "Status Report on the ALICE Prototype TPC with Ring-Cathode Readout" ALICE/Internal Note
http://consult.cern.ch/alice/ALICE_Weeks/1999/15/abstract
DEVELOPMENT OF THE PRINTED CIRCUIT UNITS FOR MULTIWIRE CHAMBERS

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Abstract

The paper considers finished 16-channel printed circuit units (PCUs), intended to read out and process preliminary the signals of multiwire chambers. Their characteristics reflect the trends in mount density increase (up to 1 front-end channel per 1 cm.cub.).

The PCUs are built with 8-channel ICs of amplifier-shapers and discriminators based on application specific semicustom arrays.

The considered units are implemented with 4-layer PCBs measuring 90*40 mm.sq, which may be simply combined into a 32-channel unit. ICs and other components are mounted by surface mount technology.

The basic electrical characteristics of PCUs and ICs are presented.

1. INTRODUCTION

The designers of the systems of radiation detector signal acquisition face the problem of reducing unit dimensions at channel number increasing. Its solution consists in the improvement of both the design of the PCB itself and the one of the front-end ICs, which must contain a greater number of channels.

Further (see p.3) there are considered finished 16-channel printed circuit units (PCUs), intended to read out and process preliminary the signals of multiwire chambers. The given units are a development of the PCUs presented at the 3-rd and 4-th Workshops [1,2]. The PCUs are built with 8-channel ICs of amplifier-shapers and discriminators based on application specific semicustom array. These ICs are described in the following section.

2. 8-CHANNEL ICs OF AMPLIFIER-SHAPERS AND DISCRIMINATORS

The structural diagram of a single channel is presented in fig.1. It contains a preamp with differential input, main amplifier-shaper, base line restorer (BLR), comparator and output driver. On the basis of one and the same application specific semicustom array (ASSA), manufactured by an npn bipolar technology with unity-gain frequencies above 6 GHz (at collector current 1 mA), there have been manufactured two eight-channel ICs, one containing amplifier-shapers and the other – the subsequent units of the channel.

In fig.2 the simplified schematics of the amplifier-shaper is shown. The schematics of the subsequent channel part was considered earlier in [3].

Standard input dynamic range makes up 5...200 uA. The discriminator (high-speed comparator) outputs provide a quasidifferential output in the GTL standard. The rest of the channel’s electrical characteristics are presented in the table below.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transresistance, kOhm</td>
<td>25</td>
</tr>
<tr>
<td>Input resistance, Ohm</td>
<td>330</td>
</tr>
<tr>
<td>Shaper output rise time, ns</td>
<td>10</td>
</tr>
<tr>
<td>Output pulse duration at base level, ns</td>
<td>50</td>
</tr>
<tr>
<td>Shaper output full swing, V</td>
<td>2.5</td>
</tr>
<tr>
<td>Range of comparator threshold setting, mV</td>
<td>10...2000</td>
</tr>
<tr>
<td>Comparator rise time at C load = 5pF, ns</td>
<td>3</td>
</tr>
<tr>
<td>Comparator fall time at C load = 5pF, ns</td>
<td>5</td>
</tr>
<tr>
<td>Comparator propagation delay, ns</td>
<td>8</td>
</tr>
<tr>
<td>Power consumption per channel, mW</td>
<td>40</td>
</tr>
<tr>
<td>Supply voltage, V</td>
<td>±3</td>
</tr>
</tbody>
</table>

Fig. 1. The structural diagram of a single channel
Fig. 2. The simplified schematics of the amplifier-shaper

The features of the ICs are first of all the large maximal output amplitude of the amplifier-shaper (not less than 2.5 V), allowing to use the amplifier-comparator channel not only for timing signal generation, but also to store and process amplitude information. Moreover, at a standard dynamic range of 100 (from noise and up to the maximal amplitude) this allows to operate with higher comparator thresholds and thereby reduce problems with pick-up and cross-talk in a multichannel system.

3. PRINTED CIRCUIT UNITS

The considered units are implemented with 4-layer PCBs measuring 90*40 mm.sq. ICs and other components are mounted by surface mount technology. The unit is connected with the detector by four 10-pin FPC connectors Harwin F10. At the unit’s output a 40-pin Hirose connector with a pitch of 1.27 mm is used.

Two modifications of the PCU (lower one UP25411L and upper one UP25411U), capable to be joined in a bookstand manner, forming a 32-channel unit, have been manufactured. The mount density increases thereat up to the value of 1 front-end channel per 1 cm.cub.

The general view of the PCUs is presented in fig. 3. At present a new modification of the ICs is prepared, having a greater input sensitivity (gain of preamp).

The work is supported by the International Science and Technology Center (ISTC).

4. REFERENCES


Fig. 3. The photo of UP25411 PCUs (-L and -U modifications)
ANALOG SIGNAL SPLITTER

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Abstract

The high-speed (wide-band) splitter circuit for reading out photomultiplier analog signals is described. The splitter can simultaneously drive loads of the type of CFD, LED, ADC, QDC, TDC and so on.

The photo of the manufactured prototype printed circuit unit (PCU), based on microwave transistors and fitted with LEMO connectors, is presented. The dimensions of the 4-channel PCU are 75*50 mm sq. The splitter provides a high slew-rate of about 2000 V/us, large dynamic range up to 60 dB and low power consumption 250 mW.

1. INTRODUCTION

A number of LHC experiments (for instance, ones with time-of-flight detectors) require high-speed (wide-band) splitters of photomultiplier analog signals. The splitters should have a high slew-rate (up to 2000 V/us), large dynamic range (up to 60 dB) and low power consumption (tens of mW). The main destination of the splitters is to provide simultaneous parallel signal processing by amplitude, charge, time and so on. The splitter can drive loads of the types of CFD, LED, ADC, QDC, TDC and so on.

2. STRUCTURE AND SCHEMATICS

The most acceptable circuital solution in the case of both polarity pulses is the use of push-pull AB stages with complementary microwave bipolar transistors. The elaborated splitter circuit contains an input section (core) and output buffer stages, as shown in Figure 1.

The core is built according to the current feedback schematics. It is responsible for bandwidth, static parameters (input offset voltage and input currents). The latter set a limit to the dynamic range. Taking into account disturbances, cross-talks and the standard offset voltage for a pair of bipolar transistors to be ~1..2 mV, one should assume minimal input signals of ~5..10 mV. Therefore in order to provide 60 dB of dynamic range there must be ensured a maximal output amplitude not less than 5V.

Moreover the core provides the limitation of the output voltage swing by a value of about 6V, thereby protecting the output stages from burnout. This is provided by applying a nonlinear local feedback to the core.

The output buffer stages (compound voltage followers) provide driving low-ohmic loads (as typical – 50 Ohms each). The value of fan-out (number of output stages operating in parallel), can vary from 1 to 6 depending on the total load.

Simplified schematics of a single splitter channel is shown in Figure 2.

Figure 1. Structure of the splitter

Figure 2. Simplified schematics of the splitter channel
3. IMPLEMENTATION AND LAB TESTS

3.1 Prototype Unit

The views of the manufactured prototype printed circuit unit (PCU), based on microwave transistors and fitted with LEMO connectors, are shown in Figure 3. The dimensions of the PCU are 75*50 mm sq.

![Figure 3. Views of the prototype splitter unit](image)

The circuit indeed has determined the structure of the PCU as a multiboard one. The output sections thereat have been designed mechanically in the manner of a bookstand and connected by their input terminals as a wired-OR. This allows to extend simply the fan-out.

Two versions of boards have been elaborated:

- based on caseless matched transistor pairs, having \( f_t \) exceeding 1 GHz for the npn-transistors KT398 and exceeding 500 MHz for pnp-ones KT393.
- both transistor types (npn- KT3130 and pnp- KT3129 ones) have \( f_t \) somewhat above 300 MHz.

In the capacity of output transistors in both cases there have been used more powerful npn-transistors of the type KT642 (\( f_t \sim 5 \text{ GHz at } I_{\text{max}}=120 \text{ mA} \)) and pnp-ones of the type KT658 (\( f_t \sim 3 \text{ GHz at } I_{\text{max}}=100 \text{ mA} \)).

3.2 Lab Test Results

The prototype PCU provides operation at a unity gain and a fan-out of 4 at load resistances of 50 Ohm each. The maximal output amplitude thereat makes up at least 5V. Rise/fall times are within 2.5 ns. Signal polarity can be any. The maximum rate is not less than 200 kHz. Offset voltage for each output does not exceed \( \pm 3 \text{ mV} \). This is achieved at the expense of including trimmer potentiometers in the circuit at the stage of adjustment.

At supply voltages of \( \pm 10 \text{V} \) power consumption is 250 mW/channel.

Considering the high speed and bandwidth (above 100 MHz), along with circuital matters much attention should be paid to mechanical design implementation. Therefore circuit simulation and PCB routing were done taking into account the influence of the reactances of PCB conductors and pads on the electric parameters.

3.3 Outlooks for IC designing

At present the task of miniaturizing the splitter is being solved. It is expected to implement the tested circuitry in the form of a semicustom IC. It is planned to supplement the circuit with a gain control for separate splitter outputs and an electronic adjustment of DC output potentials, aimed at setting them as close to zero as possible.

4. ACKNOWLEDGEMENTS

We acknowledge the helpful discussions with Uli Thoering from Uni. Giessen and Romain Holzmann from GSI (Darmstadt), who gave the start of the splitter development.

Also we thank our colleagues from SRIPT (Moscow) for manufacture of the prototype boards.

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RELATIVE ROBUSTNESS AGAINST PROCESS FLUCTUATIONS OF BASIC BUILDING BLOCKS FOR ANALOG FRONT-END OF PARTICLE DETECTORS

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Abstract

The large number of channels (15.7 millions), needed for the silicon pixel detector under development for the ALICE ITS, requires a careful study of the statistical fluctuations of the front-end electronics performance.

By means of classical techniques, such as the Principal Component Analysis, and of new ones used to perform a “realistic” worst case analysis, various configurations of basic CMOS amplifier stages have been compared to evaluate the relative robustness of their performance against manufacturing fluctuations.

To validate the simulated results on a significant statistical sample, a test pattern containing these basic building blocks has been designed and implemented in a 0.35µm process. In this work we present the theoretical results, achieved by applying the proposed Worst Case Analysis technique. The characterisation of the test chip prototypes is currently in progress.

1. INTRODUCTION

In the Alice Inner Tracking System (ITS) a very large number of pixel channels is required to ensure the needed resolution. As a consequence, a high degree of uniformity between pixel front-end cells is mandatory to reduce channel to channel threshold dispersion, optimise time-walk performance at the system level, and guarantee shaping time accuracy and an acceptable production yield. [1]

The non-uniformity of the performances of the front-end electronics blocks is basically due to technological process variations, such as fluctuations of the oxide thickness and of the charge trapped in the oxide. These process fluctuations induce corresponding variations in the device parameters.

A large amount of preliminary work is needed to perform any statistical analysis of a circuit.

Since the process fluctuations are described in terms of variations in the device parameters, the choice of the device model and of the parameter extraction procedure deeply affects the results of the analysis. We will use the Philips MOS Model 9 [2], which guarantees accurate modelling of transistors manufactured in recent sub-micron technologies, but involves many optimisation steps in the extraction process. These must be performed very carefully in order to obtain optimal extraction repeatability and have a good estimate of the physical parameter statistics [3].

Another issue to be addressed in the statistical characterisation of devices is the choice of the size of the MOSFETs to be measured to characterise the technology. In fact the extracted parameters accuracy often depends on the transistor dimensions [4]. A large number of both PMOS and NMOS devices must then be available in order to achieve statistically significant results, especially when studying the parameter correlation.

Finally a sensitivity study of the circuit performances to the varying model parameters should also be done, in order to choose the most significant parameters for the statistical analysis.

In our work, we focus on worst case analysis of basic building blocks for analogue front-end of particle detectors.

First a review and comparison of classical statistical techniques for worst case analysis is presented in order to assess the required computational effort and the impact of correlation between parameters on the results.

Then we describe a new technique for a “realistic” worst case analysis which preserves correlation between parameters and presents a limited computational complexity [5].

After validating the proposed technique by comparing its results with those provided by an extensive Monte Carlo analysis carried out on a digital inverter, we applied it on a set of basic amplifier stages such as a straight cascode, a folded cascode, and a simple OTA with active load, in order to compare the relative robustness of some of their performances, such as voltage gain and output offset.

Furthermore a test chip containing the whole set of the
considered building blocks has been designed and implemented in a 0.35µm CMOS process, to verify experimentally the results achieved.

2. STATISTICAL TECHNIQUES

2.1 Traditional Monte Carlo analysis

The first step is to consider the traditional Monte Carlo analysis. In this technique, a set of NMOS and PMOS parameters is calculated for each iteration, on the basis of their mean value and standard deviations, by using a unit normal random number generator. A circuit simulation follows. Repeating this procedure a statistically meaningful number of times, the statistical description of the circuit performances is obtained. The variability range of each parameter is fixed to ±3σ with respect to its mean value.

The major problem connected to this procedure is that correlation between parameters is not taken into account and this causes the performance worst case estimation to be too pessimistic.

Furthermore when only a worst case analysis is required, this technique is too computationally expensive and time-consuming.

2.2 Principal Components Analysis

In order to preserve correlation between device parameters both of the same and of the different channel kind, the well-known Principal Component Analysis has to be carried out. It consists in finding a set of linear equations that express the normalised model parameters as a combination of independent unit normal random numbers (Principal Components) [6,7]:

\[ P' = U \Lambda^{0.5} C \]  

where \( P' \) is the normalised model parameter vector, C is the principal component vector, while \( \Lambda \) and U are respectively the eigenvalues and the eigenvectors matrices of the parameter correlation matrix.

The variability of each parameter is expressed through the well known statistical model, presented in eq. 2 [6,7]:

\[ P = \mu_{\text{process}}(P) + \sigma_{\text{stat}}(P)R_{\text{inter}}(P) \]  

Eq. 2 expresses the inter-die variability of the generic parameter P. The unit normal random number \( R_{\text{inter}} \) is obtained from equation (1) and preserve correlation between parameters. The principal components can be generated independently by a random number generator, and by using eq. (1) and (2), a set of device parameters can be obtained for each iteration.

Monte Carlo analysis following this scheme (PCA Monte Carlo) yields more realistic results than the traditional Monte Carlo, but is still too complex a way to obtain a worst case estimation.

In fig. 1 a comparison between traditional and PCA Monte Carlo analysis is shown for a CMOS inverter, while table 1 and table 2 reports respectively the average value and the standard deviations used for the parameters and their correlation coefficients. In this case only the threshold voltages and the transconductance parameters for NMOS and PMOS transistors have been considered.

Table 1. Statistical properties of the parameters employed in the Monte Carlo analysis of a CMOS inverter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mean</th>
<th>St. Dev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vtp</td>
<td>-0.789</td>
<td>1.54E-2</td>
</tr>
<tr>
<td>Vtn</td>
<td>0.672</td>
<td>3.40E-3</td>
</tr>
<tr>
<td>βp</td>
<td>392E-6</td>
<td>4.18E-7</td>
</tr>
<tr>
<td>βn</td>
<td>567E-6</td>
<td>1.25E-6</td>
</tr>
</tbody>
</table>

Table 2. Parameter correlation matrix.

<table>
<thead>
<tr>
<th></th>
<th>Vtp</th>
<th>Vtn</th>
<th>βp</th>
<th>βn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vtp</td>
<td>1</td>
<td>-0.2</td>
<td>0.9</td>
<td>0.3</td>
</tr>
<tr>
<td>Vtn</td>
<td>-0.2</td>
<td>1</td>
<td>-0.3</td>
<td>-0.1</td>
</tr>
<tr>
<td>βp</td>
<td>0.9</td>
<td>-0.3</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td>βn</td>
<td>0.3</td>
<td>-0.1</td>
<td>0.4</td>
<td>1</td>
</tr>
</tbody>
</table>

Fig. 1. DC characteristics for a CMOS inverter: traditional Monte Carlo curves (grey lines) and PCA Monte Carlo curves (black lines).

It is clear from fig. 1 that the DC characteristics spread is reduced by the correlation between parameters, and that the traditional Monte Carlo Analysis provides pessimistic and meaningless worst case results.
2.3 Traditional Worst Case Analysis

Accurate worst case analysis can, of course, be performed by an extensive (more than 2000 simulations) Monte Carlo analysis. It is sufficient to calculate, for each circuit performance, its ± 3σ values with respect to its mean value. But for a simple worst case analysis, a complete Monte Carlo simulation is too time-consuming. It would be better to find directly the “corner points” in the parameter space that correspond to the performance worst case values. A very simple way to try to do this is to run circuit simulations with all the device parameters set to their ± 3σ values, including all the possible combinations.

This procedure is based on the assumption that the function that maps the device parameters space to the circuit response space must be approximately monotonic, otherwise it is not possible to find the performance corner points starting from the device parameter ones [8].

“Approximately monotonic” means that the mapping functions can have some ripples, but such ripples must be small with respect to the full range of variability [8]. A study of the circuit performance sensitivity to the device parameters can be performed to verify this assumption, and to determine the worst case directions for each parameter [9].

The worst case analysis carried out with this simple procedure leads to very pessimistic estimation of the circuit performance corner points. This happens because correlation between parameters is not taken into account so that the corner points chosen in the device parameter space are not physically meaningful.

3. PROPOSED WORST CASE TECHNIQUE

3.1 PCA Worst Case Analysis

The technique we propose, which we call PCA worst case analysis, preserves correlation between parameters. The starting point is to perform a Principal Component Analysis, in order to relate the vector of the n normalised parameters to the unit normal random vector of principal components. Then one parameter is fixed at its upper or lower bound (± 3σ), and a set of principal components is calculated, which provides the chosen value of the parameter.

For instance, for the parameter P1 set at its +3σ value, if the correspondent expression in function of the principal components is:

\[ P_1 = A_{11} C \] (3)

where vector \( A_{11} \) is the first row of the matrix \( UA \)^T. We can write

\[ C = (A_{11})^{-1} 3\sigma \] (4)

The extraction of this vector \( C \) is performed by means of a least square method based on the pseudo-inversion of the matrix \( A_{11} \) [10]: in this way the chosen vector of principal components \( C \) has minimum norm. This implies that the extracted vector is also the most likely to occur among the ones which provide \( P_1 = 3\sigma \).

The values of the remaining parameters \( P_j, j \neq 1 \), are then calculated on the basis of the chosen vector of principal components, through equation (1).

3.2 Example: comparison of different analysis methods for a CMOS inverter

In order to test the effectiveness of this technique an extensive PCA Monte Carlo simulation has been carried out for a simple CMOS inverter (2000 iterations). Then a worst case analysis has been implemented with both the traditional technique and the proposed one. Fig.2 and fig.3 represent respectively the input-output DC characteristics \( V_{out} \)–\( V_{in} \) and the supply current characteristics \( I_d \)–\( V_{in} \). In table 3 a comparison of the maximum relative dispersions provided by the three methods is reported for some of the main circuit performances, such as the input offset, the inversion voltage, the gain and the noise margins.

![Fig. 2. DC Vout/Vin characteristics for a CMOS inverter](image1)

![Fig. 3. DC Id/Vin characteristics for a CMOS inverter](image2)
Table 3. CMOS inverter: comparison between different analysis methods.

<table>
<thead>
<tr>
<th>Performance relative variations [%]</th>
<th>PCA Monte Carlo</th>
<th>Proposed Worst Case</th>
<th>Traditional Worst Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset</td>
<td>4.96</td>
<td>3.60</td>
<td>7.66</td>
</tr>
<tr>
<td>Inversion voltage</td>
<td>4.48</td>
<td>3.13</td>
<td>7.61</td>
</tr>
<tr>
<td>Gain</td>
<td>5.38</td>
<td>4.03</td>
<td>7.29</td>
</tr>
<tr>
<td>High noise margin</td>
<td>9.81</td>
<td>7.93</td>
<td>15.45</td>
</tr>
<tr>
<td>Low noise margin</td>
<td>12.23</td>
<td>10.91</td>
<td>20.91</td>
</tr>
</tbody>
</table>

Fig. 4. Gain histogram of a CMOS inverter, obtained with 2000 PCA Monte Carlo simulations. The worst case limits, obtained with the proposed PCA worst case analysis (PCA WC) and with the simple worst case analysis (Trad WC) are also plotted.

It is evident from table 3 that the circuit performance spreads evaluated by means of the proposed worst case analysis technique are closer to those obtained by a PCA Monte Carlo than the ones calculated with a traditional worst case analysis.

In fig. 4, a gain histogram obtained with the PCA Monte Carlo simulations is presented, together with the worst case limits obtained with both the traditional worst case technique and the proposed one. The performance limits provided by the PCA worst case analysis are estimated to be about a factor 2.5 the standard deviations foreseen by the PCA Monte Carlo, whereas the results of the traditional worst case technique are evidently unrealistic. Thus the estimation of the worst case circuit performances obtained from the proposed technique is just a little less conservative than the one provided by PCA Monte Carlo. This is caused by the use of the minimum norm vector of principal components which results from the above mentioned pseudo-inversion of the matrix $U\Lambda^{0.5}$ rows. In fact more vectors of principal components may exist which give the same $\pm 3\sigma$ value of the current parameter and have not negligible probability of occurrence, even though their norm is non-minimum. These vectors are neglected in our worst case analysis.

4. COMPARATIVE WORST CASE STUDY OF ANALOGUEBUILDING BLOCKS

After validating the proposed worst case technique on a CMOS inverter, we applied it to compare the performances of three basic amplifier stages: a straight cascode, a folded cascode, and an OTA with active load. All the circuits share the same nominal gain value.

Fig. 5. Layout of the OTA stage, showing the NMOS transistors with enclosed structure.

Simulations on these basic analogue stages have been carried out considering the corner points in the device.
parameter space found by means of the PCA worst case analysis, as described in the previous section.

Three performances have been chosen to compare these circuits: the output offset, the voltage gain and the bandwidth. In table 4 the simulation results have been reported.

The OTA with active load exhibits the best results for all the considered performances. This is due to the existence of an intrinsic feedback and to the balanced structure of the circuit. The current mirror used as active load tends to make equal the currents in the two branches of the circuit and improves the robustness of the stage against the inter-die parametric variations. The folded cascode shows better behaviour compared to the straight version of the circuit. This can be explained considering that in the folded structure the main performances of the circuit depend on parameters of MOSFETs of the same kind (NMOS or PMOS), whereas in the straight structure the same performances exhibit dependence on parameters of both NMOS and PMOS devices.

Table 4. Comparison of the performance relative variations for three basic amplifier stages.

<table>
<thead>
<tr>
<th>Performance relative variations [%]</th>
<th>Straight Cascode</th>
<th>Folded Cascode</th>
<th>OTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output offset</td>
<td>54.01</td>
<td>47.71</td>
<td>32.31</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>6.95</td>
<td>2.29</td>
<td>0.29</td>
</tr>
<tr>
<td>f_sub</td>
<td>34.20</td>
<td>11.15</td>
<td>5.63</td>
</tr>
</tbody>
</table>

It must be pointed out that in all the simulations of both versions of the cascode, the reference voltages have been implemented by means of simple CMOS biasing structures instead of ideal voltage sources, since in real circuits this is the most used solution. If the references were realised with independent voltage sources, the results reported in table 4 would be quite different.

5. CONCLUSIONS

A novel technique for a realistic worst case analysis of analogue building blocks has been presented. The proposed method preserves parameter correlation without requiring excessive computational effort. This makes it suitable to perform the statistical analysis of large circuits instead of a time-consuming Monte Carlo simulation carried out together with the Principal Components Analysis.

The technique has been applied to a set of basic CMOS building blocks, such as the straight cascode, the folded cascode, and the OTA with active load, to assess their relative robustness against the process induced parameter fluctuations. The results obtained are referred to a set of performances usually relevant in the design of front-end circuits. The relative degree of robustness of the examined stages is likely to hold even for different statistical input data, while this is not guaranteed if a different choice of the considered performances is made (noise, linearity, etc.). Therefore it is up to the designer the proper choice of the specs to be considered depending on the particular application. Here we intended to propose a technique to make viable the evaluation of the performance spread for circuits of relatively high complexity, such as those encountered in actual front-end channels.

6. REFERENCES

PERFORMANCE AND RADIATION TOLERANCE OF THE HELIX128-2.2 AND 3.0 READOUT CHIPS FOR THE HERA-B MICROSTRIP DETECTORS

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ABSTRACT

This paper presents a description of the HELIX128 frontend chip family installed in the HERA-B silicon vertex detector and the microstrip gaseous chambers of the HERA-B inner tracking detector. Also the ZEUS and HERMES experiments use these chips. Results from performance evaluation, radiation tests and series wafer testing are reported. Furthermore, experience gained in over 1.5 years of detector operation is given.

1 THE HELIX128-2.2 AND -3.0 CHIPS

HELIX128-2.2 and -3.0 are 128 channel pipelined readout chips [1] [2] [3] installed in the HERA-B Silicon Vertex Detector and the microstrip gaseous chambers (MSGCs) of the HERA-B Inner Tracking Detector. The ZEUS Experiment uses the HELIX128-3.0 in its Microvertex Detector and the HERMES experiment uses HELIX128-2.2 chips in a vertex detector upgrade. Furthermore a version with only direct binary readout (called CIPix) was derived for H1’s Central Inner Proportional Chamber upgrade. The chips are manufactured in AMS’ CYE (0.8µm bulk CMOS) process and have the same architectural concept as the FElix chip [4] developed by the RD20 collaboration.

As depicted in fig. 1, each input channel features a low-noise, low-power charge sensitive preamplifier (CSA) frontend and a shaper. These folded cascode [5] designs are optimized for 96 ns full time to comply with the HERA bunch-crossing clock of 10.4 MHz. The output of each frontend channel feeds its signal into a capacitor array (pipeline) and into an AC-coupled differential amplifier type comparator circuit with a common reference voltage for all 128 channels. The outputs of these comparators are ORed together in groups of 4 channels, latched and brought off-chip via open drain pads to derive a level-1 trigger signal.

The pipeline consists of 141 cells per channel, which allows a maximum trigger latency of 128 samples and implements a derandomizing buffer for 8 triggered events. The oldest triggered event is read out of the pipeline via a resettable CSA (pipeamp). The signals are then serialized and
brought off-chip by means of a 2-stage multiplexer and a current driver. The output stages operate at up to 40 MHz readout clock frequency.

To control the pipeline operation, the HELIX128 uses a FIFO based circuit instead of the shift register implementations known from other readout chips [6]. It was synthesized from a functional description (written in Verilog), which besides scalability and portability is much smaller (wrt. chip area) than a shift-register solution. Furthermore, when implemented with standard cells, the circuit only grows \( \propto \ln(n) \times m \) where \( n \) is the latency and \( m \) the number of derandomizer buffers, which store triggered events.

The algorithm of the pipeline control circuit is depicted in fig. 2. It mainly consists of the derandomizer buffer FIFO, and two Incrementers, which calculate the pipeline addresses to be overwritten or triggered respectively. The address to be overwritten is decoded to operate the pipelines write switches, and the address to be triggered is only written to a derandomizer buffer if a trigger signal is present and a free slot in the FIFO is available. Each clock cycle, the Incrementer compares two subsequent pipeline addresses with the contents of the derandomizer buffer FIFO. If an address is not marked for readout, it is stored into a lookAhead FIFO, if there is enough space. Also the pipeline addresses compared in the next clock cycle depend on the number of free buffers in the lookAhead FIFO. The oldest entry in the lookAhead FIFO is the output of the Incrementer.

It is obvious that in worst case this algorithm has to handle \( m \) subsequent triggered pipeline addresses, where \( m = 8 \) is the depth of the HELIX' derandomizer FIFO. To prevent the lookAhead FIFOs from underrun they have to be at least \( m/2 + 1 = 5 \) buffers deep.

All amplifier stages feature forced bias currents to ensure sufficient radiation tolerance. These currents, as well as the voltages that adjust the feedback resistances of CSA, shaper, and the comparator threshold, are generated with on-chip digital-to-analog converters (8 bit resolution). The DACs, together with digital circuits adjusting the trigger latency or the pause between the readout of two triggered events, are programmed via a serial interface using the trigger line for data input.

The clock inputs for readout, sampling and the comparator circuits as well as the trigger inputs use LVDS signals to minimize crosstalk.

Pads for token and monitoring signals allow the daisy-chained readout of two or more chips and the monitoring of their synchronous operation. The HELIX128-3.0 chip also implements a fail safe token scheme, that overcomes (non-adjacent) dead chips in a readout daisy-chain.

Figure 3 shows the layout of the chip. The die size is 14.4 \( \times \) 6.2 mm\(^2\).

2 PROVEN RADIATION TOLERANCE AND ANALOGUE PERFORMANCE

A sample of chips was irradiated with a \(^{137}\)Cs source up to 5.2 kGy. All chips were fully functional after accumulation of their target dose, though the high dose rate of 180 Gy/h induced a temporary failure of the digital circuits after 3 kGy from which the chips recovered after about 210 h under normal operation conditions (i.e. \( T \approx 55^\circ\)C).

Noise measurements show (fig. 4, 5) an increase from 438 e\(^-\) + 38.6 e\(^-\)/pF (which is in good agreement with the theoretical value of 287 e\(^-\) + 35 e\(^-\)/pF [2]) for unirradiated chips to 751 e\(^-\) + 52.0 e\(^-\)/pF after 4 kGy. No significant change of the pulse shape was found after irradiation (fig. 6). Also the power consumption of the chips was found to increase linearly with the accumulated dose from 1.8 mW/Ch before irradiation to 2.6 mW/Ch at 2.7 kGy as shown in fig 7. The discharge of the pipeline storage capacitors due to leakage currents was found to be unaffected by irradiation up to 4 kGy for observation times in the millisecond region.

The analogue performance fully complies with HERA-B requirements: An undershoot-free pulse with 96 ns fall time
2.070 / 3
A0 438.3 ± 7.70
A1 38.59 ± 8900

Figure 4: The equivalent noise charge (ENC) of a non-irradiated HELIX128-2.2. The bias settings chosen (I_{pre} = 350\mu A, V_{fs} = 1.5 V) correspond to a HERA-B-compliant signal at 20 pF strip capacitance can be achieved for input capacitances up to 30 pF, which gives a 50% safety margin. With the recommended receiver circuit, the gain of the chip was measured to be 110 mV/MIP (1 MIP = 24000 e^-) without load, dropping to 80 mV/MIP for 16 pF input load, both measured with fall time adjusted to \approx 100 ns.

The comparator circuits exhibit a measured sensitivity of 267 e^- [7]. By choosing the correct phase of the comparator- and sampling clocks, the switching noise of the comparators can be vastly suppressed on the HELIX128-3.0, where coupling via the substrate has been reduced wrt. HELIX128-2.2.

3 SERIES WAFER TESTING AND YIELD

For series testing of HELIX128 chips a setup based on a Suss PA200 semi automatic wafer prober and a digitizing HERA-B Front end Driver (FED) module was used. By employing parts of the HERA-B DAQ system it is possible to characterize every pipeline cell wrt. offset and gain, to store the results in a database and automatically generate test reports. The probecard (with \approx 100 needles) restricted the sampling and readout speeds to 10 MHz, which resulted in test times of \lessapprox 30 min/wafer (w/o loading) — much faster than 5 min/chip achieved with a HP 82000 chiptester. Up to now 107 wafers with 60 HELIX128 chips each have been tested. The yield was found to be 47% for perfect chips, which is higher than expected from process parameters.

4 EXPERIENCE FROM LARGE SCALE DETECTOR OPERATION

HERA-B’s Silicon vertex detector consists of 8 superlayers, each made up of 8 double sided silicon strip detector modules. The 50×70 mm² detectors are segmented into 1280 strips on the n-side and 1024 on the p-side. The 7 superlayers close to the target are mounted in roman pots, that are inserted into the 2.5 m long conical shaped vertex vessel. The vessel itself is part of the HERA proton ring and also houses the wire target. Targets and roman pots can be retracted from the beam axis to avoid damages when filling the proton ring. Fig. 8 shows a roman pot, carrying one quadrant of the first three superlayers. The shielding caps covering the detectors are removed.

The first parts of this detector system went into operation in May ’98. Since then an increasing number of modules have been installed. At present 44 detector modules are
installed, which equates to about 700 (of 1152) installed chips. As depicted in fig. 9 the newer detector modules nearly reach the theoretical limits for the signal-to-noise (S/N) ratio of 27 for n-sides and 19 for p-sides. The S/N ratio for all installed chips is shown in fig. 10.

The Inner Tracker of the HERA-B experiment is a large system of Microstrip Gaseous Chambers/Gas Electron Multipliers (MSGC-GEM), which is read out with the HELIX128-2.2 and -3.0 chips. The system is organized into ten superlayers, each superlayer consists of 8 to 24 chambers. In total about 150,000 electronic channels have to be read out.

An MSGC-GEM [8] [9] is a flat gas-tight chamber, measuring 30x30x1.5 cm³ (w×h×d) where the rear plate is made of 400µm thick glass with photolithographic applied anode and cathode strips at an anode pitch of 300µm. Two G10 frames with integrated gas supply fix an intermediate double sided copper plated foil with small holes at a pitch of 140µm between the front and rear plate of the chamber. Filled with a chamber gas the high voltage applied to anodes and cathodes as well as to both sides of the GEM foil causes electron multiplication in the respective parts of the chamber. A superimposed drift field causes the electrons generated by ionizing particles to drift via the GEM foil to the anodes on the rear plate. The Signal of such a detector, which has a strip capacitance of 20pF is 50,000e⁻ for a minimum ionizing particle.

Each chamber is read out by 6 HELIX128 chips, directly mounted in pairs on three multi-layer PCBs. The anode strips are DC-coupled to the HELIX128 chips via flexible Kapton bridges which are z-axis glued (i.e. the connection is established by a special glue with anisotropic conductivity) on both ends and a ceramic thin film substrate, which is also mounted on the PCB. This ceramic substrate not only acts as a pitch adapter, it also integrates resistors which are needed for high voltage spark protection.

Operation of first HELIX128 equipped chambers at HERA-B started in spring 1999. The only failure of the complete system encountered up to now was the malfunction of some digital optical receivers (Hirschmann OEDH 50M2) mounted ≈2 m from the beam axis. They turned out to act as silicon detectors for ionizing particles themselves and were replaced by analogue ones with adjustable discriminators to overcome this.

References

Figure 8: Detector modules covering one quadrant of the first three superlayers. The Al caps separating primary and secondary vacuum are removed to reveal (from left to right) the detector wafers, Kapton flex jumpers and the hybrids with the HELIX128 chips

ASIC-33-0697


Figure 9: S/N histogram for a double sided strip detector module

Figure 10: Signal-to-Noise ratio for all chips of the HERA-B vertex detector. The structure in the data arises from the p-n-n-p sequence of the detector sides and their different strip capacitances
Abstract

The microstrip tracker for the CMS experiment at the LHC will be read out using radiation hard APV chips. During high luminosity running of the LHC the tracker will be exposed to particle fluxes up to $10^6 \text{ cm}^{-2} \text{s}^{-1}$. This high rate of particles introduces a concern that the APV could occasionally suffer from Single Event Upset (SEU). In order to evaluate the expected upset rate the APV was run under controlled conditions in a heavy ion beam. The upset cross-sections of the main digital parts of the chip have been measured at two values of incident Linear Energy Transfer (LET). A theoretical prediction of both threshold LET and cross-section is presented along with the experimental measurements.

1. INTRODUCTION

The high radiation environment of the LHC demands that the electronics in the central regions of the CMS detector must be designed to withstand large doses of ionizing radiation. One result of such high rates is to introduce susceptibility to Single Event Effects (SEEs). There are many different SEEs; the one we are interested in is Single Event Upset (SEU), which affects the memory elements of digital circuits.

The CMS collaboration has adopted a readout system based around the APV chip series, a mixed mode amplifier buffer chip with programmable digital control logic. During the research and design phases of the APV chip, much care has been taken to assure a high degree of total dose radiation tolerance. There are two versions of the chip; the APV6, fabricated in the Harris AVLSI-RA Bulk CMOS process [1] and the APVD, fabricated in the DMILL process [2]. Both of these have feature sizes of order 1.2 microns. Extensive testing has been carried out on representative test structures from various processing runs, and the degree of radiation tolerance of these processes has been thoroughly investigated [3]. However, the susceptibility of the APV to SEU is not well known, nor is there much relevant data for comparable types of complex mixed analogue digital chips. A new version of the APV will be fabricated in a 0.25µm technology [4]; therefore future tests will perform a full investigation of the sensitivity of both processes.

With a view to calculating a prediction of the upset rate in the final system, a first evaluation of the SEU sensitivity of the bulk CMOS process has been carried out by placing the APV6 in a beam of heavy ions, at the Tandem accelerator, INFN Legnaro, Italy.

1.1 The APV6

The APV6 front-end chips consist of 128 channels, each of which is made up of a pulse amplifier and shaper that feeds a 160 deep analogue pipeline capable of storing input pulses for up to 4µs. On an external T1 trigger the data is retrieved from the pipeline and then output, via a 128 : 1 multiplexer. The output stream consists of a set of analogue levels retrieved from all 128 channels and a digital header. This header comprises an error flag and an eight-bit address that indicates which one of the 160 pipeline locations had been marked for readout by the trigger pointer. Control of the various chip operation modes and bias settings is achieved via a standard I2C serial bus link.

The vulnerable parts of the chip are the digital circuits. In the APV these comprise the digital pointers of the pipeline, the FIFO address memory, the I2C control logic and data registers and other main control logic. In the first evaluation of the SEU vulnerability, upset cross-sections have been measured for the pipeline logic and FIFO combination, and the I2C data registers. The remaining control logic was masked from the beam.

2. THEORY

2.1 The SEU phenomenon

SEU is a non-destructive phenomenon, which affects both dynamic and static memory registers that temporarily store logic states. It manifests itself as a soft error appearing in a device and is caused by the deposition of charge by an ionizing particle.

Depending on the state of the cell, a sufficient injection of charge at points 1 or 2, in Figure 2.1, will cause the state of the cell to invert.

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Figure 2.1 Schematic representation of a memory cell composed of two cross coupled inverters, and its circuit description.

In the APV soft errors could cause a variety of undesirable effects, some of which would result in temporary malfunction and possible loss of data. In the event of such errors the APV can be reset and after a latency (~ 3 µs), normal operation would resume.

For an upset to occur two basic criteria must be met. The incident particle must provide a high enough LET\(^1\) (Linear Energy Transfer) in order to free electrons and create a charge deposit larger than the critical charge \(Q_{\text{crit}}\), which is the minimum charge required to cause the circuit to invert logic state. The particle must also strike close enough to the sensitive part of the circuit, represented by the arrow in figure 2.1, so that charge can be collected fast enough. The sensitive volume of one memory element is defined as being that volume in which the incident particle must strike to cause an upset, which can be approximated by the drain implant volume of the ‘off’ NMOS transistor and that of the source of the ‘off’ PMOS transistor. The combination of these two volumes makes the total sensitive volume. In actual fact the true sensitive volume is larger, the reason for which is explained in section 2.4.

2.2 Upset cross-section

The cross-section, \(\sigma\), for SEU’s is defined at normal incidence as:

\[
\sigma = \frac{N_{\text{events}}}{\Phi} \left[ \text{cm}^{-2} \right]
\]  

[2.2.1]

Where \(\Phi\) is the total incident particle fluence, and \(N_{\text{events}}\) is the number of events (SEU) counted during the test. Figure 2.1 shows a typical cross-section curve. In the case of heavy ion irradiation these curves typically represent \(\sigma\) of the device as a function of LET of the incident ions.

\(^1\) LET is a measure of a particle’s rate of energy transfer in a particular material and is given by \(LET = \frac{dE}{dx} \frac{1}{\rho}\), where \(\rho\) is the density of that material. All values of LET in this paper refer to energy transfer in silicon.

\[\begin{align*}
\text{LET}_{\text{threshold}} &= 29.2 \text{MeV cm}^2 \text{mg}^{-1} [2.2.3] \\
\text{LET}_{\text{threshold}} &= \frac{E_{\text{crit}}}{z\rho} = 2.9 \text{MeV cm}^2 \text{mg}^{-1} [2.2.3]
\end{align*}\]

This represents a conservative estimate of the expected threshold LET.
2.4 Predicting the upset cross-section

The total number of sensitive nodes in the pipeline logic is 960. The surface area of each node is \(12\times10^{-8}\text{ cm}^2\). Therefore, the total sensitive cross-sectional area of the pipeline logic is:

\[
\sigma_{\text{pipeline}} = 115\times10^{-6}\text{ cm}^2 \quad [2.4.1]
\]

For the I2C registers there are 128 sensitive nodes, hence:

\[
\sigma_{I2C} = 154\times10^{-7}\text{ cm}^2 \quad [2.4.2]
\]

These values represent the total physical cross-section of the sensitive volumes in the circuits. In reality the saturated cross-section will be larger than this, since high LET particles striking near the edge of the sensitive volume can create charge clouds.

3. TESTING THE APV6

3.1 Preparation

Before setting up the system in the beam area a preparatory system was set up in the lab at IC. The system reflected all the requirements of the final system, including long cables to run between the beam area and the barracks, vacuum prepared interface cards and cables. The system was tested fully, making data taking runs as if in the beam. The data from these control runs were stored to be accessed for comparison at a later date.

3.2 Hardware

![Diagram of hardware](image)

*Figure 3.1 Schematic representation of the hardware*

The test beam setup was effectively identical to the APV readout chain in the lab. Main control was performed by a PC running LabVIEW, which communicated with the VME crate via a PCI VME interface. The trigger sequence for the APV was provided by a SEQSI sequencer, and control of the APV performed by a V12C slow control interface. The output from the APV was digitized by a flash ADC.

3.3 Software

The control and data acquisition was carried out by custom designed software developed in LabVIEW. The main tasks were to provide resets and triggers, via the SEQSI, to capture the digitised APV output data frame, via the ADC, to perform rudimentary on-line analysis and to save data to disk. The on-line counting of events was necessary for fine-tuning of the sensitive time in order to ensure that event counting was non-saturated (see section 3.6). Other on-line information included an overall count of upsets and a total sensitive elapsed time counter. The software also included I2C control for testing the APV static registers.

3.4 Masking APV sections

One of the requirements of the system was the ability to mask off sections of the APV. The masks were made from copper plates approximately 1mm thick, to provide an adjustable aperture. This enabled us to select the parts of the chip to test. It was also possible to reduce the upset rate by reducing the exposed area of these parts.

3.5 Seeing upsets

One part of the chip where it was possible to detect upsets, and probably the most useful to test, is the combination of the pipeline logic and FIFO. In the event of an upset there are two possible outcomes: either the error bit in the output data frame is set, or the pipeline address in the output data frame is corrupt. The most likely cause of a corrupted address is an upset changing the pipeline column address stored in the FIFO. The error bit is set if an upset in the pointer logic causes the latency of the trigger pointer to change. Only a small proportion of upsets produce both outcomes simultaneously.

One can also test for events in the I2C registers by writing defined values, reading out the values after a set period of time, and comparing them with initial values. In this case it is possible to detect the individual cells which have been upset.

When measuring upsets in such a chip one has to be careful that upsets do not interfere with chip operation. This can be achieved by exposing only the parts of the chip shown in figure 3.2, masking off the vital control logic and running the chip for short time periods, to ensure only a small number of upsets during each. It is important that the average number of upsets per time interval is less than one (see section 3.6). The running time per measurement, when the chip is sensitive to upsets, is defined as the sensitive time (ST). When measuring the upset rate, following each ST there is a readout period, this is repeated many times to make a
good measurement. For the pipeline a typical run consists of 100,000 STs, and for the I2C, 100.

Figure 3.3 shows the definition of $T_{\text{sensitive}}$ the total sensitive time for one run for the pipeline logic.

\[
T_{\text{sensitive}} = N_{\text{triggers}} \cdot \text{ST}
\]

*Figure 3.3 definition of ST for the pipeline logic*

### 3.6 Non-saturated measurements of events in the pipeline logic

One important issue is undercounting of events in the pipeline logic. Only one error can be detected within each sensitive time interval, as more than one error still only produce symptoms consistent with one error. If we lose events by undercounting then the measured upset rates begin to saturate, hence one must ensure that the number of events is less than half the number of sensitive time intervals. In order to achieve this condition one can adjust the length of the sensitive time interval, adjust the upset rate by changing the beam flux (this method is crude and unreliable) or use masking to change the exposed area of the chip.

### 3.7 The TANDEM Van der Graaf accelerator

The TANDEM is located at the INFN laboratory in Legnaro. Table 3.1 shows the ions that were available for this test and their corresponding LET in silicon.

The TANDEM is capable of producing many more ion species, those in table 3.1 being chosen specifically for this test to cover a useful range of LET values.

### Table 3.1 Available ions for APV6 test

<table>
<thead>
<tr>
<th>Ion</th>
<th>Li</th>
<th>C</th>
<th>O</th>
<th>F</th>
<th>S</th>
<th>Ni</th>
<th>Ag</th>
</tr>
</thead>
<tbody>
<tr>
<td>LET</td>
<td>0.38</td>
<td>1.5</td>
<td>2.9</td>
<td>3.8</td>
<td>8.7</td>
<td>28.7</td>
<td>54.9</td>
</tr>
<tr>
<td>Energy (MeV)</td>
<td>55</td>
<td>92</td>
<td>106</td>
<td>116</td>
<td>153</td>
<td>214</td>
<td>259</td>
</tr>
</tbody>
</table>

The typical beam flux was in the range $1 \times 10^4$–$1 \times 10^7$ cm$^{-2}$ s$^{-1}$. For each ion this value was set to a constant. Due to problems during the experiment there was only enough time to test the APV6 under two ion beams: Oxygen, which had a typical flux of $2 \times 10^6$ cm$^2$ s$^{-1}$ and Silicon, which had a flux of $2 \times 10^6$ cm$^2$ s$^{-1}$. The chip was mounted inside a vacuum chamber, which was held at a pressure of $10^6$ mbar.

### 4 RESULTS AND CONCLUSIONS

Measurements were made for the SEU cross-section of both the pipeline and I2C logic at two values of LET using Oxygen and Silicon ions. For Oxygen a large number of readings with high fluence were made and no upsets were observed. Thus it can be deduced that the threshold for both pipeline and I2C logic is above 2.9 MeV.cm$^2$.mg$^{-1}$. Silicon, on the other hand, produced a significant upset rate, giving the following results.

#### 4.1 Error distribution

In order to be confident that events observed were caused by the ion beam, the distribution of these events with time was measured. For random processes the distribution should be described by Poisson statistics.

*Figure 4.1 SEU distribution for pipeline logic*

Figure 4.1 shows a typical distribution of 200 SEUs observed in the pipeline logic. All data showed a good fit with Poisson statistics.

#### 4.2 Pipeline cross-section

These data represent errors in the pipeline logic only, which are identified as having caused the error bit to be set in the APV6 data header. All of the results that follow were made with a ratio of SEUs to number of sensitive time intervals ~ 1/1000. Under these conditions one would expect the upset cross-section to show no dependence on the sensitive time.

*Figure 4.2 Variation of cross-section with sensitive time*

Figure 4.2 confirms this expectation within an acceptable statistical variation, with the average cross-section of $(4.4 \pm 0.2) \times 10^{-5}$ cm$^2$. 

\[
\text{Sensitive Time} \quad \text{Cross-section} \quad \text{LET} \quad \text{Energy} \quad \text{Si Ions} \quad \text{LET} = 8.5 \text{MeV.cm}^2.\text{mg}^{-1} \quad \sigma_{\text{ave}} = 4.41 \times 10^{-5} \text{cm}^2
\]
A similar test was made by varying the latency of the trigger pointer. Again one would expect to see no variation in the cross-section, and figure 4.3 shows that the measured value varies very little, with an average of $(3.7 \pm 0.1) \times 10^{-5}$ cm$^2$.

If one assumes the cross-section to be constant at one value of LET, the average of all measurements for the cross-section of the pipeline logic can be taken as a first estimate, this gives $(4.1 \pm 0.1) \times 10^{-5}$ cm$^2$.

### 4.3 I2C registers cross-section

Similar measurements made for the upset cross-section in the I2C registers again show consistent results with variation in the sensitive time. Figure 4.4 shows the average cross-section to be about $(1.5 \pm 0.9) \times 10^{-5}$ cm$^2$.

Tests to complete the measurements are planned for later this year. This will then enable extrapolation to CMS to be made and a prediction for the expected upset rate in the tracker. We also intend to test the APV25S0, the new version of the chip fabricated in a 0.25 micron process.

### 4.4 Discussion and future measurements

With only two measurements of cross-section it is impossible to draw a curve of cross-section against LET. Figure 4.5 shows a possible range in which the curve could lie, illustrating the uncertainties that still remain.

It is clear that more points are needed in order to make an accurate measurement of the saturated cross-section, and the threshold LET. From figure 4.5 the threshold lies between 2.9 and 8.5 MeV cm$^2$ mg$^{-1}$.

<table>
<thead>
<tr>
<th>Threshold LET (MeV cm$^2$ mg$^{-1}$)</th>
<th>Prediction</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.9</td>
<td>2.9 – 8.5</td>
<td></td>
</tr>
<tr>
<td>Cross-section I2C (cm$^2$)</td>
<td>$1.5 \times 10^{-5}$</td>
<td>$1.5 \pm 0.9 \times 10^{-5}$</td>
</tr>
<tr>
<td>Cross-section Pipeline (cm$^2$)</td>
<td>$1.2 \times 10^{-5}$</td>
<td>$4.1 \pm 0.1 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

### Table 4.1

Tests to complete the measurements are planned for later this year. This will then enable extrapolation to CMS to be made and a prediction for the expected upset rate in the tracker. We also intend to test the APV25S0, the new version of the chip fabricated in a 0.25 micron process.

### 6. ACKNOWLEDGEMENTS

We thank PPARC for financial support, the INFN and all the technicians at the TANDEM for the time in the beam and technical support at Imperial College and University of Padova.

### 7. REFERENCES


CHARGE AMPLIFIER AND ANALOG MEMORY FOR SILICON DRIFT DETECTORS IN ALICE

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ABSTRACT
In Silicon Drift Detector front-end the signals coming from each anode of the detector are sent to one input of a Preamplifier-Shaper whose outputs are connected to the inputs of an Analog Memory (AM). The AM continuously samples the analog signals at 40 MHz (the bunch-cross rate) and stores all the data. When some suitable conditions are detected, a trigger signal stops the write phase. Then a read phase begins to transfer, at lower rate (1 MHz), the data to another device that performs digitalisation.

SUMMARY
According to our simulations [1], a preamplifier-shaper has been designed. It has 8 channels. Each channel consists of a charge preamplifier and a CR-RC shaper to limit noise. Thermal and shot noise has been simulated as 300 e-. Since the foreseen leakage current is not more than 10 nA, the preamplifier has a sensitivity of 155 mV/MIP, in order to achieve the assigned 7 Mip range. The shaper has a gain of 1 V/V and a driving capability of 7 pF as required by the 256-cell Analog Memory.
A 16 channels 256 cells analog memory has been realised as a switched capacitor array. It works as an analog delay line. The read frequency is 1 MHz driving 15 pF output load and the write frequency is 40 MHz. This device has to be tested. A previous prototype (64 cells 4 channels) working at the same write and read frequency showed during tests the expected performances. Dynamic Range 3.5 V De gain 0.9988.

CHARGE AMPLIFIER
Analog front-end has been designed with a traditional scheme, as shown fig. 1. It consists of an integrator and a CR-RC shaper plus an output buffer to drive the analog memory.

Both preamplifier and shaper stages are based on a single-ended folded cascode as shown fig 2. This solution offers better performances in term of stability and gain compared with standard cascode [2]. For preamplifier stage a choice of PMOS input transistor was addressed for better result in term of flicker noise.

Accurate noise analysis was performed to sizing input transistor taking into account detector capacitance and power dissipation. Coupling capacitor of 20 pF was implemented inside the chip.

Main characteristics are:

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Amplifier Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise</td>
<td>&lt; 500 e-</td>
</tr>
<tr>
<td>Input range</td>
<td>7 MIP</td>
</tr>
<tr>
<td>Output range</td>
<td>1 V</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>155 mV/MIP</td>
</tr>
<tr>
<td>Shaping time</td>
<td>55 ns</td>
</tr>
<tr>
<td>Driving capability</td>
<td>7 pF</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>2.2 mW</td>
</tr>
</tbody>
</table>
Amplifier test results

A 8-channels amplifier has been realised in 0.8 micron AMS CMOS technology. Test results agree with simulations results showed in Table 1. We have some problem with noise performance that is worse compared with simulations, probably due to the parasitic effects of the coupling capacitance at the input of the preamplifier.

Figure 4 shows measured output transient responses of the amplifiers. This work suggests a new solution for DC coupling amplifier with the compensation of the leakage current.

Within the overall system, the Analog Memory operates as an analog delay line, sampling the voltage at its inputs at 40MHz rate and storing its values for each channel in a switched capacitors array. This array acts in parallel as a circular memory rewriting new samples over the cells when the overall channel depth has been reached.

Each channel uses an output buffer for the readout of the stored samples. The maximum rate of this phase is 1MHz because of power dissipation constraints.

The Control Unit simply selects cells in a sequential way at different rates for the write and the read phase. This unit consists of a ring shift register whose outputs lines are fed into one input of an array of two inputs AND cells. The other input of the AND cells of this array is an internally generated validating “enable” signal (Figure 5).

The purpose of this "and" array is to guarantee a non overlapping addressing scheme for all cells along the channel. Two different feed control signals are used during the write and the read phase: while in the write phase it is a fixed 50% duty cycle 40MHz system clock, an external acknowledge-based mechanism is used in the read phase. The digitizing device, following the memory in the read-out chain, requires next cells data whenever ready, while memory reacts with a valid data signal. That scheme goes on until all memory cells are read.

Table 2 ADeLine Family

<table>
<thead>
<tr>
<th>Chip name</th>
<th>Ch. n°</th>
<th>Cell x ch.</th>
<th>Tot. Cells</th>
<th>Resolution Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADeLine1</td>
<td>8</td>
<td>256</td>
<td>2048</td>
<td>Not working *</td>
</tr>
<tr>
<td>ADeLine2</td>
<td>1</td>
<td>8</td>
<td>8</td>
<td>&lt;1 mV *</td>
</tr>
<tr>
<td>ADeLine3</td>
<td>3</td>
<td>64</td>
<td>192</td>
<td>6 mV *</td>
</tr>
<tr>
<td>ADeLine4</td>
<td>4</td>
<td>256</td>
<td>1024</td>
<td>&lt; 1 mV *</td>
</tr>
<tr>
<td>ADeLine5</td>
<td>16</td>
<td>256</td>
<td>4096</td>
<td>Not avail. *</td>
</tr>
<tr>
<td>ADeLine6</td>
<td>16</td>
<td>256</td>
<td>4096</td>
<td>Not avail. Not avail.</td>
</tr>
</tbody>
</table>

ANALOG MEMORY

We have designed different prototypes of the ADeLine family Analog Memories. In this section we merely describe the characteristics of ADeLine4 and ADeLine5 chips.

Table 2 ADeLine summarises family main characteristics.
Main design constraints for the memory as well as for the whole system have been power dissipation and resolution.

**Memory Design**

ADeLine5 memory chip is an analog full custom VLSI ASIC designed in AMS 0.8 $\mu$m CMOS 2 metal/2 poly process. Its sizes are 3.3x3.6 mm$^2$.

The design of the sampling capacitors has been carefully studied to achieve the best matching in order to have high resolution. Dummy capacitors structures was implemented as well.

The memory cells structure (Figure 6) has been designed for a sampling period of 25 ns because of the expected input signals whose rise time exceed 50 ns. This fact imposes an upper constraint to the size of capacitors and input switches size while technology and matching considerations impose a lower constraint.

The output buffers use folded cascode transconductance amplifiers for the readout of the selected cell together with a 3 switches configuration.

The design of the digital control part is completely static, advantaging of the low-power characteristics of CMOS gates design. A binary tree clock distribution scheme was implemented as well.

Mixing on the same chip digital and analog parts has conducd to an accurate grounding scheme to avoid unwanted signals coupling that worse resolution.

The next step will be a chip containing both preamplifier and analog memory in order to test the whole electronic chain.

**REFERENCES**

A LOW COST CAN NODE FOR A/D MEASUREMENTS IN ATLAS

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Seattle WA 98195-1560

ABSTRACT

We have developed a CAN node suitable for A/D measurements and data I/O in the Muon Spectrometer for ATLAS. It is based on commercial hardware and software from Phytec Corporation [1] and programming software from Keil Software [2] and DAvE [3]. The advantages besides very low cost are commercial design and ease of programming and debugging. Phytec provides a CAN node based on the Siemens' C515C 8 bit microprocessor [4] and provides tools for downloading programs. Keil Software supplies an integrated development environment for programming the C515CC. The CAN node along with 48 channels of TMP37 [5] temperature sensors has been radiation tested to 1 x 10^{12} neutrons/cm^{2} [6] and 3 x 10^{12} neutrons/cm^{2} [7] at two sites.

DESIGN CONSIDERATIONS

The ATLAS Muon spectrometer may have on the order of 100,000 voltages to monitor, perhaps on the order of 50,000 temperature generated voltages and low voltages on the MDTs (Monitored Drift Tubes) alone. ATLAS Muon also requires the downloading of chamber constants and the ability to refresh or change programs operating on the CAN nodes over the CAN bus. The ATLAS philosophy for electronics is to use suitable commercial products where available and CAN is the standard for detector control. Hence this development was predicated on finding what might be available in the CAN commercial market upon which to base a design for A/D measurements and data I/O.

The most challenging part of the CAN node was the CAN node itself and software for downloading programs. Within ATLAS Muon there are varying needs of functionality for the CAN nodes as well. Hence the design approach adopted was to find a commercial node with the required computer functionality and memory and to which a daughter board could be easily attached and provide the specific functionality required of the node. The Phytec KitCon 515C meets these requirements. All computer ports are available on a header to which a daughter board can be attached just by plugging it on.

One reason for choosing the Phytec KitCon 515C (www.phytec.com) besides low cost were the availability of software tools for ease of programming. Phytec has on board software tools that allow the downloading of software my means of a built in RS232 port and more recently over the CAN bus itself. Keil Software (www.keil.com) provides tools for writing software and debugging it both in emulation mode and run time mode. DAvE provides many programming examples for the C515C. Other reasons were the large number of multifunctional I/O ports (six), optically isolated CAN bus, 256K flash ROM and the availability of CANOpen protocol.

HARDWARE DESCRIPTION

The Phytec KitCon 515C is full 2.0B CAN compliant. It is optically isolated from the CAN bus using HCPL-0601 optical isolators. This enables the ATLAS grounding rules to be maintained as the power for the front end transceiver and optical isolator front end is supplied from the bus while all the local functionality power is supplied from a locally grounded source.

Figure 1. Shows a block diagram of the C515C processor.

The Siemens C515C microprocessor (see Figure 1.) provides many different internal peripherals including:

- SSC (Synchronous Serial Channel) - serial port compatible with the common SPI interface.
• Full CAN 2.0B controller - Controller Area Network
• 2KB of XRAM
• 256Bytes of RAM
• 2 16-bit Counter/Timers
  – fully compatible with timer/counters 0 and 1 of the 80C51.
• 1 16-bit Counter/Timer with capture and compare
  – Compare : up to 4 PWM signals with 65535 steps at maximum, and 600 ns resolution.
  – Capture : up to 4 high speed capture inputs with 600 ns resolution.
  – Reload : modulation of timer 2 cycle time.
• 8-bit USART - can be used for RS-232 communications, includes its own baud-rate generator.
• Watchdog timer - used to initiate a hardware reset in case of a software upset.
• 10-bit ADC - low impedance A/D converter with 8 multiplexed inputs. Requires an input buffer/amp.
• 64KB of ROM or OTP (optional)

The Siemens C515C microprocessor contains 7 ports; six 8-bit multipurpose ports, and one 1-bit port.

The C515C has the following port definitions:

• Port 0 is a bi-directional 8-bit digital port, alternatively it is used as an Address/Data bus for external memory accesses.

• Port 1 is a quasi-bidirectional 8-bit digital port with internal pull-up resistors; alternatively the pins of this port can be used for the inputs/outputs to the capture and compare unit, it can supply a system clock output, and it also has the Counter 2 input.

• Port 2 is a bi-directional 8-bit digital port, alternatively it is used to supply the high byte of a 16-bit address in association with Port 0.

• Port 3 is a quasi-bidirectional 8-bit digital port with internal pull-up resistors; alternatively the pins of this port can be used as an asynchronous serial port, counter/timer inputs, external interrupts, and the RD/WR control lines for external memory access.

• Port 4 is a quasi-bidirectional 8-bit digital port with internal pull-up resistors; alternatively the pins of this port can be used as the a CANBus serial interface, a Synchronous Serial Channel port, more external interrupts, and the A/D external start pin.

• Port 5 is a quasi-bidirectional 8-bit digital port with internal pull-up resistors; alternatively, Port 5 can also be made into a true bidirectional port which will provide CMOS levels.

• Port 6 is a unidirectional 8-bit port to the internal A/D converter; alternatively the port can be used as digital inputs if the voltage levels meet the high/low input voltages.

• Port 7 is a 1-bit port which can be used as a general digital input/output; alternatively this port can be used as an external interrupt line.

The Phytec KitCon 515C uses the Siemens C515C processors as the heart of its board. The Siemens C515C CPU can address the following:
– up to 64 Kbyte of internal/external program memory
– up to 64 Kbyte of external data memory
– 256 bytes of internal data memory
– 256 bytes CAN controller registers / data memory
– 2K bytes of internal XRAM data memory
– a 128 byte special function register area

Using the capabilities of the CPU to address larger amounts of memory than is currently available on the CPU, Phytec has added a 128KB Flash ROM, and a 32KB RAM chip. As well as an address decoder for accessing these chips. Phytec also provides three pre-decoded Chip Select (CS) lines for the user, to allow adding external devices to the memory bus. Phytec also provides both a RS-232 and CAN transceiver, as well as providing opto-isolation for the CANBus using Hewlett Packard HCPL-0601 opto-isolators. Phytec also includes a 10MHz oscillator crystal and a regulated power input for the CPU. This whole development system is contained on a 6U Eurocard, with half of the space left for a user development area. Phytec has divided the area with a 152 pin header, which contains all of the outputs/inputs of the CPU, and allows a user to attach external devices to it.
A version that we have built was designed for 64 12 bit A/D channels (see Figure 2.). A MAX1241 was chosen for the A/D and three MAX306 were selected for the analog multiplexing channels (www.maximic.com). The MUX units were controlled from three I/O ports on the C515C and the A/D was read out achieved using one of the C515C serial ports. The A/D, MUX, MAX6225 voltage reference and sensor input connectors were laid out on a daughter board that was then plugged into the KitCon.

For testing the 48 channel board we used Analog Devices TMP37 temperature sensors. These had the appropriate range of 0 to 125 °C with output voltage of 0 to 2.5 V or 20 mV/°C. Shielded twisted pair cables were used for the three wire hook up to the sensors. To minimize costs and provide secure connections the sensor cables were attached to a printed circuit board that plugged into SIM connectors mounted on the motherboard.

RESULTS

The noise level for the TMP37 on 6 meter cables was no more than a least count of 0.03 °C. The device was run while collecting $10^{12}$ fast neutrons/cm$^2$. No problems were observed during the approximately two hour run carried out at the University of Washington Hospital’s cyclotron for neutron therapy. Approximately 99% of the neutrons had their energies between 100 KeV and 45 MeV. These high energy neutrons amounted to about three times the worst case dose for the MDT nodes over the expected 10 year running period. A second radiation test was carried out at the French Prospero facility where the dose was $3 \times 10^{12}$ neutrons/cm$^2$.

The KitCon has also been set up to do data I/O using a counter timer chip (chip number) to provide clock signals stepping motors. Additional ports are used to control motor direction and gate off the stepping. The existing library of control software made this a very straight forward application to program.
REFERENCES

[1] PHYTEC Messtechnik GmbH
Robert-Koch-Str. 39
D-55129 Mainz, Germany
(www.phytec.com)

Bretonischer Ring 15
D-85630 Grasbrunn, Germany
(www.keil.com)

[3] DAvE, Infineon Digital Application Engineer, Version 1.0

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(www.infineon.com)

Corporate Headquarters
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P. O. Box 9106
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(www.analog.com)

[6] University of Washington Hospital cyclotron

[7] Prospero, French Nuclear Facility
FERMI - A digital Front End Readout Micro-system for Calorimetric detectors at LHC

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Abstract

The activities within the FERMI Collaboration were completed by the successful assembly of multi-chip module demonstrators fulfilling the technical requirements of the LHC generation of high performance detectors like CMS ECAL. Throughout the project, the Collaboration has been concentrating on providing architectures that fulfil the requirements set by the interested experiments in the domain of calorimeter readout. Currently, readout system architectures based on experience acquired through FERMI are being implemented in CMS and the ATLAS Tiles calorimeter.

The final status of the project is presented, together with a brief description of some ASICs developed by the FERMI collaboration.

1. INTRODUCTION

A calorimeter at LHC spans a dynamic range of in the order of 1 to $10^5$. This corresponds to at least 16 bits in digital representation. The resolution requirement is in the order of 10 to 12 bits for the electromagnetic calorimeters, and slightly less for the hadronic dijets. The LHC accelerator has an interaction rate of close to 40 MHz. In order to give the largest possible probability to detect, and later to confirm the detection of the very rare events searched for at LHC, the readout system has to be dead time free. The space inside and around the experiment is very limited, thus demanding a very high degree of integration.

The FERMI solution is to use MCM-D technology in order to cope with these requirements. The initial concept was directly taken from the requirements stated above. These are coming from assumptions in the ECFA studies (1990) [1]

2. THE FERMI CONCEPT

The objective for the FERMI collaboration is to develop an interface between the detector element and the global DAQ system.

The FERMI concept, see block diagram in figure 1, contains an analogue dynamic range compressor in order to cope with the 16 to 17 bit dynamic range. A sampling analogue to digital converter samples at the bunch crossing frequency. To de-compress the digitised data, a Look-Up Table (LUT) is chosen. This LUT, implemented using a RAM, contains the inverse transfer function of the whole electronics chain in front of the Analogue to Digital conversion. The LUT can compensate for all first order defects in the chain. The de-compressed data is used for the trigger primitive generation, and is at the same time continuously stored in a digital pipeline with programmable length, while waiting for the level 1 trigger decision.

![Fig. 1. FERMI concept block diagram](image)

These two tasks have to be concurrent, and of course in real time, synchronous with the bunch crossings. The latency of the adder and of the filter is constant. In the level 1 trigger processor, a selection operator is applied to the trigger primitive data extracted from all the front-ends after a known delay. The result of the selection process in the level 1 trigger is sent back to the front end. The front end receives the result from the level 1 trigger process at the same time as the corresponding data is coming out from the pipeline. If the result is negative, the data is discarded. If positive, a time frame of about 10 consecutive time samples is transferred to the event buffer, together with event identifiers, waiting for the final readout.

When finally reading out the data from the event buffer, a readout filter is applied to each time frame in order to calculate the energy deposition. The task for this filter is delicate. It has to, as accurate as possible, extract the absolute value corresponding to the energy deposition originating from the bunch crossing corresponding to the level-1 trigger accept. It has also to suppress energy deposits originating from other bunch crossings with as large a factor as possible.

3. THE FERMI BUILDING BLOCKS

The FERMI system implementation consists of a number of channel blocks, each one serving a single channel, and a service block, serving all channel blocks. The channel block contains an analogue dynamic range
compressor, a sampling ADC, a digital decompression stage, a digital pipeline, and a set of event buffers. The service block consists of a trigger part and a DAQ part. On the trigger side, an adder is summing the data from all channels. A real-time digital filter is extracting the energy and time information from the channel sum for the first level trigger process. The DAQ side contains a readout filter and an FPGA readout controller.

### 3.1 The Analogue Dynamic Range Compressor

The chosen architecture uses four differential amplifier stages with a gain of 1, 2, 5, and 16. The four are arranged in parallel, and receives the same input signal. The output from each stage is current limited, so that they saturate at chosen limits. The current output from the four stages is summed in an output stage. The whole arrangement gives a piecewise linear transfer function.

The compressor circuit was prototyped in a mask programmable transistor array from Gennum. It has a bandwidth of about 60 MHz and an output noise of 250 μV at a full scale of 2V, it could give a clean input signal even to a 12-bit ADC. The theoretical dynamic range with a 10-bit ADC is slightly above 16 bits, and with a 12-bit ADC about 17.5 bits. This was also proven in bench tests.

#### 3.1.1 Dynamic Range Compression Constraints

A study of the actual requirements on a compressing circuit has been done [9]. The conclusions apply to any kind of analogue compression based gain stages with different gain factors. Table 1 shows the constraints on bandwidth and slew rate.

<table>
<thead>
<tr>
<th>V$_{diff}$</th>
<th>Error</th>
<th>3dB BW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2mV</td>
<td>0.1%</td>
<td>54MHz</td>
<td>310V/μs</td>
</tr>
<tr>
<td>1mV</td>
<td>0.05%</td>
<td>75MHz</td>
<td>450V/μs</td>
</tr>
<tr>
<td>0.5mV</td>
<td>0.025%</td>
<td>106MHz</td>
<td>600V/μs</td>
</tr>
<tr>
<td>0.25mV</td>
<td>0.012%</td>
<td>148MHz</td>
<td>850V/μs</td>
</tr>
</tbody>
</table>

A design, using the Ericson P28 bipolar technology, has been developed. Spice simulations show that these performances can be reached [10].

### 3.2 The PSA-ADC

When the FERMI project was approved in 1991, one of the main issues was to design a low power sampling ADC able to run at bunch crossing speed. A very tempting architecture, mainly latency wise, is the flash ADC. However, the power hungriness of this architecture excluded this architecture. Another architecture, using only one comparator, thus consuming a minimum of power, is the Successive Approximation ADC (SA-ADC).

The disadvantage of this architecture is of course the latency, and the fact that, for the 10-bit case, only one conversion can be done every 10 clocks. The latter can however be solved by stacking 10 complete ADCs in parallel and interleave the sampling and conversion [2]. This architecture was chosen, see figure 2. The architecture is named Parallel Successive Approximation ADC, or PSA-ADC. Four more SA-ADCs is added in order to permit two auto-zero cycles of the sample-and-hold, one sampling cycle, and one relaxation cycle before the ten conversion cycles. A block diagram is found in figure 3.

The PSA-ADC was prototyped in the AMS 1.2μ CMOS technology. With a core consumption of less than 200 mW for a full 10-bit ADC running up to 70 MHz, this prototype is a masterpiece of its time.

![Fig. 2. Block diagram of a PSA-ADC](image)

The performance is, at 40 MHz sampling rate, statically measured to better than 9.8 effective bits, and dynamically to about 9.4 effective bits.

### 3.3 The Analogue ASIC

In order to decrease the number of chips on the MCM the analogue dynamic range compressor has been integrated with a further developed PSA-ADC. The complete ASIC is implemented using the AMS 1.2μ BiCMOS technology, see photo in figure 3.

![Fig 3. Photo of the Analogue ASIC](image)

Despite minor layout errors, that were quickly found and corrected, the analogue ASIC is a success.
The complete ASIC, including the compressor and the PSA-ADC, consumes in the order of 190 mW at 40 MHz sampling rate. The effective dynamic range at 40 MHz sampling rate is about 15 bits at 9 effective bits of resolution.

One problem was encountered. The simulated 3dB bandwidth of over 80 MHz for the compressor is more than adequate [9]. The ASIC itself turned out to have just above 20 MHz. This adds some second order effects to the digitised pulse shape. A parallel project using the same technology encountered the same problem, pointing towards a process parameter error.

3.4 The Digital Pipeline and Event Buffer

The heart of the FERMI concept is the Digital Pipeline. Several different versions of digital pipeline ASICs have been developed.

The early versions include a 1kword Look-Up Table for linearisation of 10-bit compressed data, a combined Pipeline and event buffer RAM block, and control logic. A high degree of fault tolerance, imposed by the harsh environment inside the LHC experiments, is implemented. The functionality in the later versions is tracking the evolution in the LHC experiments. In the end this leads to the suppression of nearly all redundancy, instead concentrating on error detection in order to preserve the data integrity.

3.4.1 The First Channel Chip

The architecture consists basically of three functional blocks, lineariser, pipeline/derandomiser, and control. It serves three channels and is implemented in 1u CMOS from AMS. Very complex, containing about one million transistors, this ASIC is a pure lab product. Being functionally correct, it suffers badly from simultaneous switching noise, why the chip can not run at full voltage, and subsequently not at specified speed.

3.4.2 The Three-Channel Chip

The three channel chip has the same basic functionality as the first channel chip. All, for test beam purposes, non-vital functions are removed. The chip is implemented in the ES2 0.7μm CMOS process. The three-channel chip is fully functional, and has been used with success in trigger tests together with the CMS trigger and the CMS ECAL.

3.4.3 The One Channel ASIC

The One Channel ASIC is a major rework of the channel functionality. It serves one single channel. Instead of, as in the first channel chip, having a combined pipeline and derandomiser RAM, it has a DPRAM for the pipeline and eight separate event buffers in the derandomiser. A block diagram is found in figure 4.

On the input, a RAM of 1k times 23 data bits is used as LUT. The calibration constants written in the LUT are ECC encoded, capable of 2-bit error detection and 1-bit error correction.

Fig. 4. Block diagram of the channel ASIC

The pipeline is divided in 8 identical blocks of 32 locations. Any even number of blocks between 2 and 8 can be used. The unused blocks can be used for redundancy, and can thus replace a failing block. All eight derandomiser buffers are identical, and each one can be disabled in case of failure.

The one channel ASIC is the last channel ASIC being constructed to reside inside the experiment. Fully reconfigurable, it has a large fault-tolerance.

The ASIC is implemented in AMS 0.8 μm CMOS technology. A photo of the ASIC is found in figure 5.

Fig. 5. Photo of the One Channel ASIC

3.4.4 The Pipeline ASIC

In parallel with the one channel chip, another pipeline ASIC was developed.

It contains a minimal functionality, and is useful for test beam purposes because of its limited complexity and ease of use.

With a 160 clocks programmable pipeline and 5 event buffers, it has been used in ATLAS-Tiles Module0 tests, and in CMS ECAL Prototype -97.
3.5 Trigger feature extraction

The trigger feature extraction function of FERMI consists of an adder and a level-1 filter ASIC. A Finite Impulse Response (FIR) structure was chosen after a systematic evaluation of different architectures.

The level-1 trigger filter is designed to provide accurate energy information and bunch crossing assignment for the global level-1 trigger. It operates on a sum of channels, and consists of two parallel FIR filters, each with six elementary stages (taps) and a three-point maximum finder, see the block diagram in figure 6. The most recent level 1 filter is implemented in the AMS 0.8 μm CMOS technology. A photo is found in figure 6a.

Fig. 6. Block diagram of the level 1 filter

The energy extraction FIR can be optimised to extract the energy in the presence of certain artefacts. Typically it is an averaging operator with a relatively wide response on pulses in the time domain in order to improve the noise suppression.

The timing extraction FIR is optimised to produce a sharp maximum for each pulse even if it partially overlaps with another one. It is combined with a maximum finder in order to assign the output from the energy filter to a bunch crossing.

Fig. 6a and 6b. Photos of a Level 1 and a readout filter ASIC

The coefficient optimisation strategy is based on either analytic calculation or an iteration method. The analytic solution is equivalent to matched FIR filtering. With the iteration strategy, the filter coefficients are obtained by minimising the mean squared error (MSE) between the desired and the actual output for a specific input.

The performance of filter F1 has been simulated using simulated Liquid Argon calorimeter signals with a sample timing uncertainty of 2ns RMS, and electronics noise with 70 MeV RMS, as well as the effects introduced by the compressor, the ADC and the LUT. The amplitude resolution is shown in figure 7.

Fig. 7. Energy resolution of the level 1 filter.

3.6 Readout Feature Extraction

The readout filter is designed to extract a value of the energy with the highest precision allowed by the set-up and the experimental conditions. It takes as input the time frame for an individual channel, and returns a single absolute energy value.

Fig. 8. The readout filter architecture: FIR-OS with 3 coefficient banks

The filter has three parallel FIR filters and an order statistics (OS) operator. The OS operator is programmed to select the largest, the median, or the smallest output of the three filters for every time frame. A block diagram is found in figure 8. The filter coefficients and the OS mode are obtained using iteration, as the non-linear filter structure is too complex to optimise using analytical methods. The most recent readout filter is implemented in the AMS 0.8 μm CMOS technology. A photo is found in figure 6b.

The FIR-OS filter structure offers a greater suppression factor for the different artefacts present in the acquired data compared to a single FIR filter. It also offers an efficient fault tolerant architecture: if a FIR unit fails, it can be switched off from the system, thus gently degrading the global performance.

The performance of the readout filter has been evaluated using the simulated detector sequence described above. The complete system response measured at the output of the filter is again illustrated in figure 9. The data set is the same as for the level-1 filter performance graph above. Please note that the
comparison has been done with a detector with a higher performance.

![Comparison Graph](image)

Fig. 9. Energy resolution of the readout filter.

4. TESTS IN BEAM

Beam tests have been carried out in collaboration with ATLAS-Lar/RD34 [10], ATLAS-Tiles [11], and CMS ECAL/Trigger [12].

The most recent results come from CMS ECAL, testing the analogue ASIC, the three-channel chip and the level-1 trigger filter, together with level-1 trigger circuits.

The detector element was a CMS ECAL prototype crystal matrix.

4.1 Trigger feature extraction

In the three-channel version of the Channel ASIC the channel an adder is included, thus creating a sum of the three linearised channels. The ES2 Level-1 Filter ASIC contains a 3-input adder, providing the final summation of the 3X3 trigger-tower, with the output feeding the Energy and Time FIR filters. The output is sent to the level-1 trigger. As the charge-ADC system has no provision to generate trigger primitives, all trigger tests were made only with the FERMI set-up.

The trigger filter function can be seen in figure 10.

![Filter Function Graph](image)

Fig. 10. Three plots describing the Level-1 filter function

The plot to the left is showing data taken with the filter in transparent mode; i.e. all coefficients but one set to zero, showing the composite (6-channel strip) signal as a function of time. The second plot is the output from the energy filter with the coefficients configured to fit the pulse shape, and finally the third plot shows the energy filter output conditioned by the timing filter and its peak finder.

The energy resolution of the trigger feature extraction was measured at three different energies. The measurements show that the energy resolution of the trigger feature extraction is ranging from $\sigma/E = 3\%$ at low energies down to $3.5\%$ at 50 GeV. This is more than adequate for a first-level trigger process at LHC.

The time resolution of the individual channels with respect to the central crystal, where the beam hits the matrix, was measured to be below $4\text{ns RMS}$.

4.2 Readout resolution

On the readout side, a direct comparison between the charge-ADC reference electronics and the FERMI readout system was done. Figure 11 shows the comparison at four different energies, shows an almost perfect correlation between the two. Figure 12 shows the fractional resolution of the two systems as a function of energy in the range 35 to 150 GeV.

The global results show that the FERMI concept, using a continuous dynamic range compression followed by a sampling ADC would give a satisfactory result for all planned calorimeters at the LHC experiments.

![Readout Resolution Graph](image)

Fig. 11. Comparison of FERMI and QADC readout at four energies

![Fractional Resolution Graph](image)

Fig. 12. Fractional resolution for FERMI and QADC

5. THE MULTI-CHIP MODULE

A number of Multi-Chip Modules (MCM) have been built in order to evaluate the feasibility of the MCM technology. The choice is to use a silicon substrate and mount the different ASICs using a flip-chip technology.
The basic advantage with the MCM as with other hybrids is that each function can be implemented in the most suitable technology. The great advantages with the silicon substrate are the excellent thermal properties, both the great heat conduction and the perfect matching in dilatation with the different ASICs, also on silicon substrates.

Two complete Multi-Chip Modules, or MCMs, have been successfully assembled. The first, to be considered as the termination of FERMI phase 1, has integrated ADCs.

The second is to be considered as the final demonstrator. It uses external ADCs, as required in all LHC implementations, and is specified to fulfil the requirements of CMS ECAL. It has been successfully tested in the lab, see figure 13 and 14.

The result shows that the technology is fully understood, and that a data acquisition system based on MCM technology is a valid option.

6. FUTURE

The results obtained by the FERMI collaboration are available for any detector collaboration. The different building blocks can be used, or only the generic concept. For the LHC experiments, no readout system will, of course, carry the name FERMI. Instead, systems optimised for the actual requirements will be implemented. Many detector groups are currently finalising readout systems at least partly based on experience from the FERMI collaboration.

REFERENCES

The Electronic calibration of the ECAL-CMS


October 13, 1999

Abstract

We present a calibration system developed at LAPP (Annecy-le-Vieux, France) for the electronics of the CMS electromagnetic calorimeter. The system, remotely contolled from the control room, produces a current pulse at the input of the preamplifiers of the read out chain. The pulse amplitude is fixed by a 10 bits DAC and its shape has an exponential decay. It has been founded in DMILL 0.8μm technology. For the injection part, no shift is measurable up to $10^{14}$ neutrons/cm$^2$ and 400 krads in $\gamma$ irradiation. We describe here the system, the different chips that have been founded and the results of the measurements.

1 Introduction

The CMS electromagnetic calorimeter has been designed in such a way that both the front end electronic and the digitization be close to the $PbWO_4$ crystals. This strategic choice imposes the electronics to be radiation hard. The chip we have developped is able to build individual calibration pulses at the input of each amplifier. This calibration will be used during data taking in order to correct eventual drifts in the read out chain due to radiation damages, temperature hazards etc...The chip is composed of 3 parts: the command (Test Pulse Logical System (TPLS), the DAC and the injector.

2 The TPLS

2.1 Functionnality

The TPLS selects the orders for calibration, charges the amplitude of the DAC and triggers the injector. Its functionnality has been described in Verilog language and synthetised with the DMILL library.

2.2 Foundry and measurements

The first prototype has been submitted in February 1999 and tested in July. A specific VME card has been developped, controlled by a PC and LabView. The output were transmitted to a logical analyser HP1662C. The result is shown on figure 1 and 2.

![Figure 1: TPLS analyser results.](image)

The TPLS reacts in 3 steps to orders:
- Coding of the amplitude for the DAC.
- On reception of a specific bit (LD), it loads the...
DAC and unset the LD-DAC bit.

- On reception of a bit (TED) a 428 ns window triggers the injector.

In the preceding prototype, an error bit was set in case of error in the received protocol. This was removed in the present one due to the fact that this information could not be sent back to the control room. In case of error, the maximum amplitude is loaded whatever the received order, and a trigger is sent to the injector.

3 The DAC

In order to determine the amplitude of the pulse, a 10 bit DAC has been designed at LAPP and sent to foundry in August 1999. The aim was to obtain:

- 10 bits resolution
- A $10^{-1}$ precision in a range 0 to 1 V.
- a maximum output current of 20$\mu$A.

The DAC is composed of a band gap voltage that produces a stabilized voltage and a R-2R network.

3.1 The Band-Gap

For the band-gap (see figure 3), we started from a scheme previously developped by CERN for the ATLAS tracker which was modified in order to increase the output current. For this purpose, we added a follower stage with the eventual drawback of an offset drift with temperature. The drift temperature of this new setup is $250\mu V/\degree C$, constant from 20 to 75$\degree C$.

3.2 The R-2R network

For the divider part, because of known instabilities under irradiation of current mirrors structures, we have chosen a R-2R network (figures 4 and 5).

We had to face 2 problems:

- The stability of the system around 0 V (due to the fact that we had a 0-5V power supply). It was thus impossible to implement a common
Several sources of drift have been simulated with no measurable effects: 5% in Rsquare values, resistors voltage drifts (2200ppm/V for $\Delta V = 800mV$), resistor temperature drifts (1300 ppm/K).

### 3.3 The amplifier.

The original circuit was based on a bipolar Darlington as input stage with an operational point at 2.5V. We implemented a PMOS input stage to lower the operational point at 1.25 V, suppressed the now useless Darlington structure and modified the compensations in order to stabilize it at gain 1. The results of simulation (see figure 6) are:

- The gain 1 is obtained for 38 MHz, with a 100° phase, so that it is a first order circuit till the unit gain that insures a good stability.
- The open-loop gain is 39000.
- The offset is 4µV.
- The band width is 1 MHz.
- the Power Supply Rejection Ratio (PSRR) goes from -123 dB to -18.43 dB (1/10 of the signal at 10 MHz).

### 3.4 Layout report

It is a 12220 full custom components circuit. Its size is 1.1 $mm^2$ (core size). Special care has been taken in the implementation of the R-2R network.
In order to reduce dispersions, we designed a very symmetrical network, including dummy resistors around it, and we calculated very precisely the ratio R-2R, including the metallic connections of the resistances.

3.5 The simulated characteristics

- Accuracy and linearity: the amplification stages do not lower the R-2R network performances.
- The DAC is monotonous
- Technological dispersions: the non linearity goes from 0.05% in worse cases to 0.024% in best cases.
- The power consumption is about 70mV.
- The noise is 65μV on 1 MHz band width
- Signal to Noise ratio: 15 for LSB
- Power Supply Rejection Ratio: from -88.5 dB to -17 dB at 10 MHz.
- Output Voltage 0 to 1 Volt.
- Output current 20μA.

4 The Injector.

The injector produces a current pulse, with an amplitude determined by the DAC and has an exponential decay shape. A first prototype in AMS 0.8μm technology has been founded in September 1998 to validate the principle then a first prototype in DMILL technology has been founded in October 1998, a second prototype in February 1999 and a last prototype in August 1999. In its final version, it triggers at the same time the 5 channels of the same front-end card, with the same amplitude.

4.1 Principle

The scheme of the circuit is shown in fig 7.

The chip is composed of 3 parts:

- The input operational amplifier isolates the injector from the $V_{DAC}$ input. It copies precisely $V_{DAC}$ on $R_{ref}$.

![INTEGRATED CHARGE INJECTOR](image)

**Figure 7:** Principle of the injector.

- The command stage is designed in PECL logic. It is mainly a clock adaptation of the logical levels to the output differential commutator and an isolation from the input stage command.
- The output stage, when triggered, topples the conduction from the left to the right branch and the capacity $C_{out}$ is charged through $R_{out}$ and the preamplifier. The shape of the signal (fig. 8) is close to the one produced by the APD reading the PbWO4 crystal. The branch at the left hand (with $R_{ref}'$) compensates the base leak currents $I_{b1}$ and $I_{b2}$ so that $I_{out}=I_{ref}$.

4.2 Measured characteristics

The deviation to linearity of $Q_{out}$ versus $V_{in}$ (output charge vs command voltage) is better than $2\times10^{-3}$ up to $V_{in}=1$ V, corresponding to a physics dynamic range up to 3 TeV.

- $Q_{out}$ excursion: 0 to -70 pC.
- $V_{in}$ excursion: 0 to +1 Volt.
5 Conclusions

The CMS ECAL requirements have never been achieved on any calorimeter. The calibration will be a long and complex process. Our calibration system by charge injection will help to insure the precision of the read out chain during data taking and to debug the detector at the first stages of the installation.

The challenge to be reached by this system is to be more precise and more stable in time than the read out chain with adding a minimum noise to the data read out.
6 Acknowledgements:

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Low Noise BiCMOS Front-end Amplifier in the DMILL Technology

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Abstract

Bipolar transistors become interesting devices for low noise front-end amplifier when the requirement of high speed has to be combined with low power dissipation. This paper presents a low noise front-end design using bipolar technology. This design has been proposed for the MSGC front-end electronics of the CMS tracker to shorten the effective signal length leading to a reduced pile-up probability from tracks belonging to different bunch crossings. It could equally well be used for Silicon detectors.

The detailed simulation of the circuit and the measured performance of several prototype circuits are described. At a power consumption of 1.4 mW/channel, a peaking time of 25 ns, a gain of 90 mV/MIP with a non-linearity less than 5% over ±6 MIPS dynamical range and a low noise performance (Equivalent Noise Charge ENC) of 1000 electrons rms were obtained for a 12 pF detector capacitance.

The radiation hardness of DMILL bipolar transistors has been a crucial issue in the past. Results of an irradiation with a high intensity pion beam are presented in this paper.

1. INTRODUCTION

In the CMS inner tracker will be several million channels of MSGC detectors. The readout requires high-density front-end electronics with an acceptable signal to noise performance, a speed sufficient to enable an event timing at the level of about two bunch crossings and a power consumption limited to a few mW per channel.

In order to reach this goal, the circuit solutions developed in low power specification should cope with the additional constraints of low noise, large bandwidth and high impedance input loads. Indeed, noise-power-speed conflicts exist. The requirement of low power suggests a choice of low currents, which produce low transistor transconductance and therefore low speed and high noise.

Bipolar technology offers nowadays devices with excellent characteristics and is best suited for low power and fast electronics because of the highest transconductance to bias current ratio of BJT. Another potential advantage of using bipolar transistors is a better noise matching compared to CMOS device.

A BiCMOS front-end electronic circuit has been developed. This paper presents the design concept and experimental results.

2. FRONT-END TOPOLOGY

Figure 1 shows the topology of the front-end circuit. A folded cascode topology is chosen for the preamplifier stage. The input transistor is a bipolar NPN transistor. The cascode transistor is a PMOS transistor because of PNP transistors is not available in the DMILL process. For all current sinks and current sources, CMOS transistors are used due to their better performances. The feedback loop consists of a capacitance of 100 fF and a resistance of 350 kΩ. The time constant of the feedback loop is short enough so the signal after the preamplifier does not require any differentiation.

The second stage is constituted by a differential pair. It is used as an active filter to eliminate noise outside the useful bandwidth. The preamplifier and shaper together perform a semi-Gaussian shaping.
3. LOW NOISE OPTIMISATION

The noise performance of the front-end circuit is essentially defined by the equivalent input voltage noise and by the shot noise of the base current of the input transistor. [1]

\[
d v^2 = 4 k T (\gamma_r + \frac{1}{2 g_m}) + 4 k T (\gamma_r + \frac{kT}{2 q I_c})
\]

\[
d i^2 = \left[ 2 q \left( I_r + \frac{I_c}{\beta (\alpha I_c)} + I_{th} \right) + \frac{4 k T}{R_f} \right] df
\]

where

\[
g_m = \frac{I_c}{V_{th}} \frac{2 q I_c}{k T}
\]

\[
\gamma = \frac{C_{inv} + C_T}{C_{inv} + C_T + C_{inv}}
\]

\[
I_r = \text{leakage current delivered by a detector; } r_n = \text{base resistance of the input NPN transistor; } C_T, R_f
\]

are respectively the feedback capacitor and feedback resistor of the preamplifier.

Consider that the preamplifier-shaper together performs a first order semi-Gaussian shaping, the relative contributions of the above two noise sources depend on the shaping time \( \tau_c \) of the preamplifier-shaper and total input capacitance \( C_T \) as shown below:

\[
ENC_{v,eq} = \frac{1.57 e^2 C_T}{4 \pi q} \frac{1}{\tau_c} \left( \gamma_r + \frac{kT}{2 q I_c} \right) + \frac{1.57 e^2}{4 \pi \tau_c} \left[ 2 q \left( I_r + \frac{I_c}{\beta (\alpha I_c)} + I_{th} \right) + \frac{4 k T}{R_f} \right]
\]

To minimise the contribution of the equivalent input voltage noise; the base-spreading resistance of the input transistor has to be reduced. A large dimension should be used for the input transistor, but from radiation consideration [2] [3], a larger input transistor will significantly increase the shot noise of the base current due to the decrease of the current gain \( \beta \); \( \beta \) is more degraded when the current density is low. The size of the input transistor has then to be optimised by a tradeoff between the two noise source contributions: the series noise source of the base spreading resistance and the parallel noise source due to the base current. According to a preliminary analysis [4], and due to only a few emitter area choices available in the DMILL technology, a transistor emitter area of \( L_e \times W_e = 20 \times 1.2 \ \mu\text{m}^2 \) (\( L_e \): emitter length, \( W_e \): emitter width) is chosen for the input transistor. The base spreading resistance for the chosen geometry is around 150\( \Omega \).

The optimum collector current of the input bipolar transistor to minimise noise is:

\[
I_{C_{opt}} = \sqrt{\beta} \frac{V_{th}}{T_o}
\]

For a required peaking time of 25 ns and a 10 pF detector capacitance (\( C_T \approx 1100 \text{pF} \)), the optimum current is 150 \( \mu\text{A} \) (\( I_{C_{opt}} \approx 195 \mu\text{A} \) for a 12 pF detector capacitance) and if a faster shaping is required, a higher current can be used. Figure 2 represents the noise performance from simulation versus collector current for two values of emitter length.

The feedback resistance in the input stage is used both for biasing the input bipolar transistor and for determining the effective gain of the preamplifier. In order to reduce the thermal noise contribution of this feedback resistance, a reasonable high value is chosen.

\[
\text{Noise Degradation}_{\text{opt}, \beta} = \sqrt{1 + \gamma \frac{r_n I_{C_{opt}}}{V_{th}} + \frac{\text{v}_{r_n}}{R_f I_{C_{opt}}} - 1}
\]

The noise contribution due to the feedback resistance can be derived from the above equation and is less than 4%.

4. SENSITIVITY OF THE NOISE TO DETECTOR CAPACITANCE

The usual way to express the performance of a charge amplifier as a linear function of the detector capacitance as shown in the following equation is a good approximation only if the series noise is the dominating component.

\[
ENC = ENC_s + k C_D
\]

In the case of the bipolar front-end, this expression has little meaning if the parallel noise component is significant. An evaluation has been performed to compare these two different noise components. The total \( ENC \) can be represented by the following equation as:

\[
ENC = \sqrt{ENC_s^2 + ENC_p^2}
\]

where \( ENC_s \) and \( ENC_p \) are the \( ENC \) coming from the series noise and parallel noise respectively. Taking into
account these two noises added in quadrature, the series noise is the dominant component in our design before irradiation. It is then interesting to quantify the $ENC$ as a linear function of the detector capacitance $C_{Det}$.

From the Eldo simulation results, an $ENC$ of about of 830 electrons rms was obtained at the detector capacitance equal to 10 pF. The sensitivity of the noise to the detector capacitance around its nominal value of 10pF is 42 e$^{-}$ rms/pF. Figure 3 represents $ENC$ as function of detector capacitance from simulation results.

![Figure 3. ENC versus detector capacitance](image)

**5. EXPERIMENTAL RESULTS**

Figure 4 shows the output pulse shape over ± 6 MIPs (24000 e$^{-}$/MIP) dynamic range. The output pulse shape is very close to that of an ideal semi-Gaussian curve. The undershoot is less than 5%. Figure 5 represents the output peak amplitude (in mV) with an average gain of 90 mV/silicon MIP over ± 6 MIPs dynamic range. The non-linearity is less than 3% in ± 5 MIPs range. Figure 6 shows the peaking time for an input range from -6 up to +6 MIPs. A variation of ±1 ns has been obtained.

![Figure 4. Measured output pulse shapes over ± 6 MIP](image)

![Figure 5. Output linearity](image)

![Figure 6. Measured peaking time](image)

The power consumption of the BiCMOS front-end is 1.42 mW/channel. Power consumption in the emitter follower depends on the total pipeline capacitance of channel. The 600 µW of power consumption in the emitter follower is calculated for a load capacitor of 3 pF. This value of the total pipeline capacitance per channel is considered as the worst case.

![Figure 7. Measured $ENC$ versus detector capacitance](image)

Note that the gain of the amplifier will slightly change when the detector capacitance changes. A constant gain at 12 pF is employed for the $ENC$ calculation. This means the $ENC$ values are smaller than indicated in the curve when the detector capacitance smaller than 12 pF and the
values are greater than indicated in the curve when the detector capacitance larger than 12 pF. The real ENC at 23.5 pF is around 1450 electrons rms. Taking into account the above correction, the average values of the measured noise figure in ENC can be represented as below:

\[ ENC = 450 e^- + 45 e^- / pF \]

The measured and simulated ENC values versus the detector capacitance show a very good agreement.

Figures 8 shows the measured noise performance in ENC versus the input transistor collector current. It can be seen that the optimum collector current for a 12 pF detector capacitor is around 200 µA. This value is very closed to that of the theoretical analysis.

![Fig. 8. Measured ENC vs. collector current of input transistor (C_{Det} = 12 pF)](image)

Figure 9 shows measured output waveforms of the front-end amplifier as function of the input transistor collector current for a detector capacitance of 12 pF (Using the 12 pF is only for the measurement convenience).

![Fig. 9. Output waveforms as function of input transistor collector current (C_{Det} = 12 pF)](image)

Figure 10 shows the peaking time versus the input transistor collector current for the same detector capacitance. Higher collector current is biased, quicker the peaking time is.

![Fig. 10. Peaking time vs. collector current of input transistor (C_{Det} = 12 pF)](image)

6. IRRADIATION

The radiation hardness of DMILL bipolar transistors has been a crucial issue in the past. To verify the circuit’s performances, the circuit was irradiated using a high intensity pion beam with an integrated flux of 1.0 x 10^{15}/cm² which is roughly equivalent to 10 years LHC experience. For a same collector current bias (I_c = 120 µA), variations of peaking time (6%), output pulse shape and its amplitude (15%) are relatively small after irradiation because these circuit responses depend less on β.

As expected, the β is a parameter which has a very large variation before and after irradiation [5]. For example, the β of the input transistor has been changed from the nominal value of 200 down to 30 for a collector current biased between 100 and 140 µA. The current gain β is a function of collector current. From the simulation curve of current gain β versus collector current for the input transistor NPN (L_x W_x = 20 x 1.2 µm²) shown in figure 11, it can be seen that the collector current biased at around 120 µA is just a limit to have a correct performance. A higher collector current should give a better performance.

A weakness in circuit architecture has also been noted with respect to the feedback resistor in the preamplifier. In fact, leakage currents of the bipolar transistor I_{SC} and I_{SE} increase after irradiation, these lead to a DC bias variation via the feedback resistor R_f. In the worst case, the preamplifier is blocked. A feedback transistor can be used to replace that feedback resistor if a single power supply is employed (0 to 4 V). If so, a higher collector
current bias can be used to compensate delay of peaking time and reduce of output wave amplitude. The contribution of the parallel noise can also be reduced if a higher collector current bias is employed.

The ENC at 12 pF after irradiation is estimated around 350 electrons more than the ENC at the same detector capacitor before irradiation. This increase is essentially due to the degradation of the current gain $\beta$. In this case, the shot noise source of the base current of the input transistor is as important as the series voltage noise generated essentially by the base resistor. It is possible to reduce the degradation of $\beta$ by increasing the collector current as explained above.

**CONCLUSION**

In this paper, a low noise, low power consumption BiCMOS front-end using the radiation hard SOI DMILL process has been presented. An ENC noise of 450 electrons at 0 pF with a noise slope of 45 electrons/pF has been obtained for a peaking time of 25 ns, a gain of 90 mV/MIP. The irradiation measurement using a high intensity pion beam with an integration flux of 1.0 x 10^{14}/cm^2 has been performed. With a modification of the feedback device in the preamplifier, the characteristic of the designed front-end circuit will be suitable for use at CMS experiences.

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**REFERENCES**


A 128 CHANNELS ANALOG READOUT CHIP (APVD_DC) FOR DC-COUPLED SILICON DETECTORS OF THE CMS TRACKER

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Abstract

The APVD_DC realised in the DMILL technology is a radiation-hard integrated circuit for front-end readout electronics of the silicon tracker of CMS.

DC-coupled silicon microstrip detectors have significant economical advantages compared to AC-coupled devices mainly due to their less complex fabrication process and better yield. The APVD_DC allows the use of DC-coupled silicon detectors with significant leakage currents as it is expected due to irradiation after several years of LHC operation.

In this paper, a solution is presented with an active individual leakage current compensation technique for each input channel. The APVD_DC contains 128 identical analogue channels, each one composed of a low noise preamplifier, a CR-RC shaper, a 160 cells-deep analogue pipeline and an analogue signal processing stage. A deconvolution filter at the latest stage recuperates the initial fast response function of a silicon detector and confines it to one LHC bunch crossing. The 128 analogue channels are readout by a serial output via a high-speed analogue multiplexer. Slow control is implemented on the chip using an I2C serial bus, which allows to bias, to configure the chip and to run the internal calibration system. A current compensation circuit is added in front of every preamplifier to sink the leakage current coming from the detector. Good performance of the circuit has been measured on prototypes for leakage currents between 0 and up to 10 μA.

1. INTRODUCTION

In the CMS inner tracker, several millions channels of silicon detectors are foreseen to be installed. Front-end electronics can be AC coupled as well as DC coupled to these detectors. The AC coupling technique is widely used for readout of silicon detectors with coupling capacitors and bias resistors integrated on the detector. However, AC coupled silicon microstrip detectors are more complex and expensive in fabrication than DC coupled detectors. The APVD_DC has been developed to allow the use of DC coupled silicon detectors with significant leakage currents as expected due to irradiation after several years of LHC operation.

In this paper, after a brief introduction of the APVD_DC architecture, only the charge sensitive preamplifier with its active leakage current compensation is discussed. More detailed information concerning APV type circuits can be found in [1, 2, 3].

The second objective of this paper is to describe a fully stabilised front-end readout electronic in DMILL technology. In previous versions of the APVD some instability problems were encountered. The problem becomes prominent especially at high bias current settings. This paper is focused on a study of this phenomenon by results of tests and extensive simulations. Finally a solution which resolves the oscillation problem of the circuit is described. This solution has been implemented in the most recent submission.
2. APVD_DC DESIGN FEATURES

The APVD_DC is a second generation of the APVD [2, 3] rad-hard front-end readout chip developed in the DMILL process, after it has been transferred from the former version of the APV6 [1] realised in the HARRIS technology.

As other members of the APV family, the APVD_DC contains 128 identical analogue channels. The current pulse delivered by the detector is transformed into voltage by a charge preamplifier and then amplified and filtered by a CR-RC shaper. The signals are buffered by a source follower that is connected to the analogue pipeline, the ADB (Analogue Delay Buffer), where the signals are sampled and stored at 40 MHz. On receipt of a first level trigger, the signals are read and processed by the APSP (Analogue Pulse Shape Processor). The analogue output current signal is read-out serially at 20 MHz. The control of the circuit is provided by several blocks. The I2C interface allows programming of the main parameters of the circuit for the slow control. It also generates signals cycling the APSP. The pipeline control logic (PCL) controls the writing and the reading sequences of the analogue pipeline. The addresses of the tagged cells are stored in a FIFO. The pulse generation unit generates calibration pulses for testing the analogue chain. The bias generator block is a set of RAM based registers and DAC’s, and it generates all the bias currents and control voltages for the analogue blocks and some digital patterns for the calibration pulse generator. It is programmed through the I2C controller.

In particular, in the APVD_DC circuit, a current compensation circuit is added in front of every preamplifier to sink the possible leakage current coming from the detector. Fig. 1 presents the general architecture of the APVD_DC circuit.

3. FRONT-END ELECTRONICS WITH LEAKAGE CURRENT COMPENSATION

The transistor level circuit diagram of the front-end part is shown in figure 2.

The front-end electronic circuit contains a preamplifier with associated circuitry for leakage current compensation, a shaper and a buffer to drive the pipeline capacitor.

The preamplifier is a single ended folded cascode structure with 300 pF feedback capacitor buffered by a simple source follower. The input PMOS transistor MP1 with size of 1540 μm /1.2 μm is biased at 250 μA in a trade off between noise matching and power consumption. The DC operating point of the high impedance output (the drain of transistor MP3) is set by means of the differential pair MC1 and MC2 with an external voltage VCON. The transistors MC1 and MC2 are designed to operate in weak inversion region with drain currents about 10 nA. In order to achieve the required precision for the current mirroring, the differential pair (MC1, MC2) is biased by a regulated cascode current source MC4-MC6. The DC leakage current can be sanked by a NMOS current source with the transistor MC3.

Figure 3 shows a simplified closed-loop small-signal equivalent circuit of the preamplifier with the leakage current compensation circuit.
The transfer function $H(S)$ of the preamplifier is written as follow[4]:

$$
H(S) = \frac{V_{OUT}(S)}{I_{IN}(S)} = \frac{2C_i}{g_{m_{MC1}} + g_{m_{MC3}} + g_{m_{MC1}}C_iS + 2C_i C_{fp} S^2}
$$

where $g_{m_{MC1}}$ and $g_{m_{MC3}}$ are small signal transconductances of transistors accordingly MC1 and MC3. The stability criterion is given by [4, 5]:

$$
\frac{C_i}{g_{m_{MC1}}} \gg \frac{2 C_{fp}}{g_{m_{MC1}}}
$$

Noise performance of a charge amplifier is determined by two factors: the intrinsic noise generated by the amplifier itself and the signal impedance seen by the amplifier input, in other words the noise matching conditions must be satisfied. As it is well known, both the optimal noise matching condition and the total noise contribution of the charge preamplifier are mainly determined by the input transistor. The choice of the input transistor as well as its bias current is a key point in the design.

The charge preamplifier is followed by the first order CR-RC semi-Gaussian shaping amplifier. The transfer function of the shaping amplifier is given by the following expression:

$$
H_{shaping}(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_s s / \omega_c}{(1 + s / \omega_c)^3}
$$

where $A_s$ represents the DC gain and $\omega_c$ is the central frequency of the shaping amplifier. The shaping time can be calculated by Laplace’s transform when at the input a step signal is applied:

$$
\tau = \frac{1}{\omega_c} = \frac{(C_i + C_{str}) + (C_i + C_{str})}{g_{str}(1 + k)}
$$

where $g_{str}$ is the transconductance of the input transistor in the shaper MS1. $C_i$ is the input capacitance of the shaping amplifier and $C_{str}$ is the stray capacitance seen at the amplifier’s output. The factor $k$ in the above equation can be calculated by:

$$
k = \frac{1}{\sqrt{1 + \frac{C_{str}}{C_i} + \frac{C_{str}}{C_i} + \frac{1}{C_{str} + C_{str}}}}
$$

The buffer is a simple source follower having strength to drive pipeline capacitance.

A very good functionality of the leakage current compensation stage has been demonstrated by a few channel prototype of the front-end amplifier. Figure 4 shows measured ENC of the prototype DC coupled charge amplifier as a function of detector capacitance with different leakage currents. The maximum leakage current which can sunk by the amplifier is 13 µA.

![Fig. 4 Measured ENC vs. Cdet for three values of the leakage currents](image)

<table>
<thead>
<tr>
<th>Leakage Current (µA)</th>
<th>ENC (e^- + pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>446</td>
</tr>
<tr>
<td>5</td>
<td>506</td>
</tr>
<tr>
<td>10</td>
<td>573</td>
</tr>
</tbody>
</table>

**4. STABILITY DESIGN**

Previously submitted APVD circuits suffer from an instability problem. Laboratory evaluations have shown that instability conditions were satisfied in the analogue input stage when front-end channels were biased at high current values. Three main points were investigated in detail to identify causes of the instability:

- Capacitive coupling coming from back side silicon substrate,
- Capacitive coupling between adjacent channels,
- Resistivity coupling via imperfect power lines.

First, measurements were performed to a few chips before and after thinning backside substrate (the total thickness was scaled down from 600 µm to 250 µm and then to 100 µm). The purpose of these tests was to evaluate impact of capacitive feedback via the backside substrate. Results have shown that the feedback via backside substrate had little influence to the stability of the circuit.

Second, the input transistor of the preamplifier can be blocked by bonding its input to a positive DC potential point. Using this method, it was found that there was a critical number of channels to initiate the oscillation in nominal bias conditions. Further measurements have shown that the oscillation is a function of total currents passed through power lines. It was demonstrated by blocking only even (or odd) channels that the coupling between adjacent channels was not critical in the design.

Third, it turned out that the instability problem was essentially caused by imperfect ground and power supply connections. Indeed, this has been demonstrated by several measurements with different impedance...
configurations for the power lines. Two different PCB boards as support for test chips were used, one with backside ground plane and one without. When the common impedances are reduced near to several mΩ on the board equipped with the ground plane, the oscillation is completely stopped.

Because there are number of connections to power supply lines in the analogue channel and because phase shifts in different points of the circuit are significant, it is difficult to investigate the problem of oscillation completely in an analytic way. Instead appropriate simulation models of the imperfect ground and imperfect power supply lines were created. Resistances of the imperfect ground and power supplies were dispatched in 3 parts. First, resistances on chip were calculated by using sheet resistance values of metal levels. Calculated resistances were divided into several parts placed between every two suspected trouble spots of the design. Then, resistances and inductances represented by bonding wires were estimated and included to the simulation. Finally PCB and system cables resistivity was estimated. Ultimately decoupling capacitances with their parasitics were added yielding in a complete model of power supplies connections. Figure 5 presents the model.

![Simulation model](image)

**Fig. 5 Simulation model**

On the base of that model the most critical parts of the previous APVD designs were identified. It turned out that three points in the design are crucial. They are:
- Bulk and source connection of both preamplifier and shaper input transistors and the connection of the output source follower to power supply lines,
- Large load capacitance value formed by the pipeline stray capacitance and the ADB hold capacitor,
- Large value of the AC current flow through positive power supply line charging this capacitor which is seen by the output of the source follower.

Due to distributed resistors present on the power lines, a small signal voltage accumulates on terminals of the input transistors in both preamplifier and shaper. Because in the previous design bulk and source were connected to different power line, the accumulated voltage was amplified via $G_{mB}$. Significant role of the $G_{mB}$ parameter of the transistor was demonstrated. Apart of the feedback paths aforementioned it was also observed positive resistive coupling between the source of the input transistor in the shaper and the input transistor in the preamplifier, as well as some possible positive capacitive feedback have been identified. Other capacitive feedback loops are a feedback path via lost silicon of the chip and a feedback via backside substrate. Taking into account these points, verified by simulations, the following changes were introduced to the APVD_DC design (Fig. 2):

1. The bulk of the input transistor in the preamplifier has been connected to GND. Noise contribution is slightly increased (<1%).
2. The source and bulk of the input transistor in the shaper have been connected to Vdd. This modification forces another change, because of the DC level shift. In the shaper PMOS type source follower and PMOS feedback transistor have been used.
3. Value of the feedback capacitance in the shaper has been increased in order to improve the stability. This change has entailed modifications of the capacitors in the feedback of the preamplifier and coupling capacitance between the preamplifier and shaper.
4. Vdd power line has been split in two paths in order to reduce common resistance on this line.
5. The design of the ADB cell has been changed to minimise the total capacitance seen by the output source follower.
6. Parasitic pole of the preamplifier has been pushed further out in the frequency scale. The $G_{m}$ of the cascode transistor in the preamplifier has been increased by both increasing its W/L and bias current.
7. Almost all large dimension current source transistors situated in critical places have been redesigned in a special parallel layout in order to reduce their $C_{db}$ capacitance.
8. To avoid a capacitance coupling three guard-rings have been employed in the design. A guard ring used as a shielding has been formed by a collector well (Collsink) implanted inside Genpmos wreath down to the SOI level.
9. The 128 channel analogue input pads have been modified in a way allowing for suppressing the capacitive coupling to the back silicon.

Several simulations have been performed to verify the increased immunity to oscillation. Results of the modified design show a total stability of the circuit. They should insure a perfect stability even if several APVD_DC chips would be mounted on the same PCB/hybrid. The circuit submitted on the last June will be delivered on October; this allows us to confirm the stability of the new design.
5. CONCLUSIONS

A 128 channels analogue readout chip (APVD_DC) for DC-coupled silicon detectors of the CMS tracker is presented. It could offer an economic solution for the CMS silicon tracker.

The detailed stability study is also presented in this paper. All of the modifications of the circuit allow us to have a readout electronic satisfying the requirements of the CMS silicon tracker in the DMILL technology.

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REFERENCES


Abstract

A diffused laser irradiation was used to improve laser simulation adequacy of dose rate effects in silicon IC’s with high metallization density. The conversion of coherent output laser irradiation into the diffused one was performed by specialized homogenizer. Test structures with various metallization coverage were designed. Numerical simulations together with laser tests were performed in order to clarify the advantage of diffused laser irradiation before coherent one.

1. INTRODUCTION

The laser simulation of dose rate effects is based on laser beam capability to ionize IC’s semiconductor structures [1]. Associated shadowing effects have been investigated in details [2,3]. It was shown that the metal coverage reduces the simulation adequacy if coherent laser irradiation is used. The influence of shadowing on latch-up threshold in this case was analyzed in [4].

A way to improve dose rate laser simulation adequacy was proposed in [5]. The approach is based on the application of noncoherent (diffused) laser radiation that reduced metallization shadowing effects. The optical model of diffused laser radiation interaction with IC semiconductor structures and appropriate software simulator were presented. It was shown that in the case of diffused laser irradiation the ionizing effect is defined by average metallization coverage of structure and the adjacent area.

In this work we applied the diffused laser irradiation to dose rate ionizing current and latch-up simulation. The specialized test structures were manufactured to experimentally estimate the advantage of diffused laser irradiation before coherent one.

2. TEST STRUCTURES DESCRIPTION

Two structure sets (TSCPHXX and TSCLUXX) are manufactured in conventional 2-µm bulk CMOS process. A structure’s cross-section is presented in Fig. 1. Each structure includes well-substrate p-n junction (48x78 µm) with strip contacts and various metallization coverage. Contact region size is 2x2 µm. The structure set TSCLUXX is similar to TSCPHXX but with different disposition of highly doped regions in order to form SCR (latch-up). The structural parameters are: p-substrate is B doped up to 12 Ω cm. The 6 µm n-well is P doped up to 1700 Ω/µm. The 0.6 µm p+ and 0.35 µm n+ regions are doped up to 110 Ω/µm and 40 Ω/µm consequently.

The structures TSCPHXX have four leads: two anodes (A1 and A2) and two cathodes (K1 and K2) and structures TSCLUXX have leads: base and emitter of parasitic p-n-p transistor (B1 and E1) and emitter and base of parasitic n-p-n transistor (E2 and B2).

Figure 1. TSCPHXX (TSCLUXX) test structures cross-section
Various test structures have the individual metal strip widths. Metal strip parameters of the structures are summarized in Table 1.

**Table 1. Test structures metallization parameters**

<table>
<thead>
<tr>
<th>Test structure</th>
<th>Metallization strip width $l_m$, $\mu$m</th>
<th>Metallization coverage, $S_m/S_{pn}$%</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSCPH2 (TSCLU2)</td>
<td>2</td>
<td>8.3</td>
</tr>
<tr>
<td>TSCPH6 (TSCLU6)</td>
<td>6</td>
<td>25</td>
</tr>
<tr>
<td>TSCPH12 (TSCLU12)</td>
<td>12</td>
<td>50</td>
</tr>
<tr>
<td>TSCPH18 (TSCLU18)</td>
<td>18</td>
<td>75</td>
</tr>
<tr>
<td>TSCPH22</td>
<td>22</td>
<td>91.7</td>
</tr>
</tbody>
</table>

The minimum and maximum shadowing cases are presented in Fig.2. The last strip to the right does not shadow the p-n junction and its width is equal to $10 \mu$m for all structures.

3. NUMERICAL AND EXPERIMENTAL COMPARATIVE RESULTS

In order to perform the test structures transient analysis the "DIODE-2D" software simulator was used which is the two-dimensional solver of fundamental system of equations taking into account the electrical and optical processes including multireflection and free carrier nonlinear absorption [3]. The numerical simulator optical model was modified in order to take into account the diffuse feature of laser radiation.

Pulsed laser simulator "RADON-5E" with 1.06 $\mu$m wavelength and 11 ns pulse width was used [6]. The simulator was supplied by homogenizer that converts purely coherent parallel laser irradiation into diffused mode. The laser pulse maximum intensity was varied from $6 \times 10^2$ up to $2.1 \times 10^6$ W/cm$^2$ with laser spot size covering the entire chip. The ionizing current transient response was registered with "Tektronix TDS-220" digital oscilloscope.

The laser simulation calculated and experimental data of well-substrate junction ionizing current amplitude vs. metallization coverage of TSCPHXX test structures under $V_{cc}=5$V are presented in Fig.3. One can see the better agreement of the diffused model calculation curve with test data. The usage of homogenizer improves the laser intensity uniformity within chip area and decrease the influence of metallization shadowing on test structure ionizing current. For TSCPHXX test structure set when metallization coverage increase from 8.3 to 91.7% (11 times) the ionizing current amplitude decrease only from 10 to 5 mA (2 times) at laser intensity $9.7 \times 10^3$ W/cm$^2$.

![Figure 2. TSCPH2 (top) and TSCPH22 (bottom) test structures view](image)

![Figure 3. Theoretical (curve) and experimental (dots) test structures photocurrent amplitudes vs. metallization coverage at laser intensity $9.7 \times 10^3$ W/cm$^2$: 1 - coherent model; 2 - diffused model](image)
The comparison between theoretical and experimental data for TSCLU2, LU6, LU12 and LU18 test structures under $V_{CC}=5V$ is presented in Fig. 4. One can see that diffused laser irradiation model provides the better agreement with experimental data.

Figure 4. Theoretical (curves) and experimental (o) test structures latch-up levels vs metallization coverage: 1 - coherent model; 2 - diffused model

The experimentally defined TSCLU18 and TSCLU2 test structures latch-up levels equal to $4.3 \times 10^3$ and $2.7 \times 10^3$ W/cm$^2$ accordingly. The ratio of latch-up thresholds does not exceed 1.7 when metallization coverage increase from 8.3 to 75 % (9 times). It can be explained by nonparallel feature of diffused irradiation and by contribution of reflected irradiation from chip bottom [5].

However the numerical estimation for diffused model gives 3.38 value of the ratio. The difference between numerical and experimental values may be explained by contribution of light refraction and scattering in passivation layers, SiO$_2$ and Si neglected under calculation. These factors tend to improve laser ionization uniformity and decrease the difference latch-up thresholds.

To investigate the influence of metallization shape on latch-up threshold level the structures TSCLU23, LU63 and LU18b were designed additionally. They have the individual metal strip topologies shown in Fig. 5. It was found that maximum difference in latch-up thresholds in experiments did not exceed 3% between TSCLU6 and LU23 structures, 5% between TSCLU18 and LU18b structures and 10% between TSCLU18 and LU63 structures. This difference is within the accuracy of laser intensity dosimetry and so the structure pairs listed above may be considered as equivalent under diffused laser irradiation.

Figure 5. TSCLU23 (a), TSCLU63 (b) and TSCLU18b (c) test structures view
The reasons of diffused laser irradiation advantage may be explained on the base of optical model. A homogenizer converts the coherent output laser radiation into the diffused radiation of finite-size source as shown in Fig.6. It causes the mixing of various laser modes and permits the nonparallel radiation to partially penetrate under metallization. The additional effect is due to the reflection of the nonparallel laser beam from the substrate’s bottom (see Fig. 6). As a result the laser radiation can penetrate under metallization from backside and reduce the ionization nonuniformity.

Figure 6. The shadow creation and backside reflection in the case of diffused laser radiation formed by a homogenizer (1)

4. CONCLUSIONS

A method for improving of dose rate simulation adequacy based on the application of noncoherent (diffused) laser radiation was applied and adopted to p-n junction ionizing current and CMOS latch-up threshold estimation. The diffused irradiation was supplied by specialized laser simulator “RADON-5E” with homogenizer. Numerical simulation results were verified against experimental data under specialized test structures with individual metallization coverage and topology.

It was found that usage of homogenizer improves the laser intensity uniformity within chip area and decrease the influence of metallization shadowing on CMOS latch-up threshold. For TSCPHXX test structure set when metallization coverage increase from 8.3 to 91.7% (11 times) the ionizing current amplitude decrease only from 10 to 5 mA (2 times). As for TSCLUXX structures when metallization coverage increase from 8.3 to 75 % (9 times) the latch-up threshold level increase only from 2.7 \times 10^3 to 4.3 \times 10^3 W/cm^2 (1.7 times).

The measured difference between latch-up thresholds of structures with equal metallization coverage and different topology did not exceed 3 - 10%.

Obtained results demonstrate the advantage of diffused laser irradiation for dose rate effects simulation in highly-metallized IC’s.

5. REFERENCES

NEURAL NETWORK TRIGGERS FOR GLOBAL EVENT DECISION AT THE LHC

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Abstract
A global event decision hardware, suitable for the planned LHC experiments, is presented, based on the neural network architecture to be implemented typically at the second trigger level. A prototype for such a system is successfully operating in the H1 experiment at the HERA $ep$ collider. The latency of the network triggers, which are of the feed-forward type, is about 20 microseconds. The inputs to the networks are suitably preprocessed quantities available at level 2. We describe the neural hardware and its use within the overall trigger strategy, exemplified with the H1 experiment. We discuss an interesting application of the network hardware for fast secondary vertex finding at the trigger level, useful for studies of $b$ and top physics and searches for hadronic Higgs final states.

1 Introduction

It is expected that the extremely high interaction rates at the LHC (about 20 events on average per bunch collision, at 40 MHz) will pose a serious challenge to the trigger systems. High selectivity of the interesting physics processes, which are usually rare, is of utmost importance. Typically, the trigger systems have to reduce the rates of order 40 MHz down to a manageable figure of around 10-100 Hz, suitable for permanent logging to tape. Multi-level trigger systems for the large colliding-beam experiments ATLAS [1] and CMS [2] have been proposed, reducing the rate step by step with increasingly complex decision machines, to cope with this formidable task. In Atlas, the first two trigger levels will be realized in dedicated hardware, from the third level onwards general processors (software) will manage the data reduction, while the CMS collaboration plan to go directly to a general purpose processor farm after the first hardware level. We present here a trigger concept, designed for the second level, which is particularly well suited for the typical trigger task of recognizing and discriminating complicated event patterns in a multi-component detector system. The concept is based on the neural network technology, realized in dedicated hardware, which has convincingly demonstrated its potential in a concrete application within the H1 experiment at the HERA $ep$ collider [3].

We summarize here the concepts and the technical realization of the H1 neural network trigger, details on the system can be found elsewhere (see, e.g. [3, 4]). Besides the superior global event decision capabilities à la H1, which can be naturally extended to the LHC experiments, we present a recent pilot study for a fast secondary vertex finder, based on the hit information from the Silicon trackers available at level 2.

2 Prototyping: The H1 Detector and its Trigger Scheme

Modern, large particle detector systems such as ATLAS or CMS at the LHC are designed with the intention to serve as general purpose facilities, pushing into a new kinematic frontier, and be prepared to be sensitive for the expected physics as well as potentially new phenomena. In this spirit, a large variety of detection principles have been foreseen, allowing for efficient detection and measurement of hadronic particles (jets) as well as of photons and leptons (elec-
3 Principles of the H1 Neural Network Trigger

The H1 design of the level 2 neural network trigger is based on the empirical observation [6], that small nets trained for specific physics reactions, working all in parallel, are the most efficient and flexible way to use neural nets at the trigger level (compared to a single large net trained on all physics reactions simultaneously). Most importantly, putting these nets to a real trigger application, the degree of modularity is extremely helpful when a new trigger for a new kind of physics reaction is to be implemented: there is no need to retrain the other nets, the new physics net is simply added to the group of the others.

The present strategy of using the networks is the following: Each of the networks is trained for a specific physics channel and is coupled to a set of level 1 subtriggers, particularly efficient for that physics channel. Because some of the level 1 subtriggers need to be made sufficiently relaxed to be efficient, their rate is usually unacceptably high. The level 2 trigger therefore has the task to reduce the excess background rate in these subtrigger sets while keeping the efficiency for the chosen physics channel high. At present, 12 networks are running in parallel, mostly optimized for electro- and photoproduction of vector mesons, which are difficult to separate from the background at level 1.

4 L2 Trigger Hardware

According to the principles described above, the hardware realization for the neural network trigger is modularized as follows [3]: Receiver cards collect the incoming trigger information of the various subdetectors and distribute them via a 128 bit wide L2 bus to preprocessing units, called Data Distribution Boards (DDB). Each DDB is able to pick up a freely choosable set of items from the L2 input data stream. The DDB can perform some basic operations on the items (e.g. bit summing) and provides an input vector of maximally 64 8bit words for its companion CNAPS/VME board. Controlling and configuring of the complete system is done by a THEMIS
trons and muons). This is no different for the running experiments at the HERA collider, which are presently probing a dramatically enlarged kinematic domain of deep-inelastic scattering.

For triggering the apparatus, H1 has installed a scheme of three levels, two hardware levels and one software level ("level 3"). An intermediate software level ("level 3") is provided, but not used at present. At level 1, each of the detector components (subdetectors) provides a set of triggers to a central trigger box, where they can be subjected to simple coincidence logic. Details on the H1 detector are given elsewhere[5]. The first level trigger is pipelined and does not generate deadtime (the same strategy is applied for the LHC experiments). This architecture implies that the level 1 trigger processors are able to provide a trigger decision for each bunch crossing (BC, a 96 ns interval for HERA, 25 ns for the LHC). For H1, the pipeline memory is 30 BC's long. After about 2.3 μs (24 BC's) a level 1 trigger decision is formed ("L1-keep") and the trigger information from all subdetectors is transferred to the level 2 systems. At this point the primary deadtime starts, no further triggers can be accepted until the event buffers are fully read out or a "fast clear" from the level 2 trigger system has been issued, rejecting the event. When the event is accepted by the level 2, the detector readout is initiated and the entire event information is sent to the level 4 processor farm, where a full event reconstruction is performed and the final event decision, using standard C-code programming, is taken.

At the second hardware trigger level in H1, the decision time is limited to 20 μs in order to digest a maximum of 1-2 kHz from level 1 while keeping the deadtime below 2 %. At level 2, the information from all level 1 trigger processors is available, so that "intelligent" use of this information is possible, exploiting the correlations among the various trigger quantities. The output of the level 2 trigger is around 50 Hz presently, which is the maximum input rate for the level 4 RISC processor farm (30 CPUs). The output rate of level 4 which is limited to about 10 Hz, is dumped to disk and then stored permanently to tape.
4.1 The CNAPS board

The algorithms calculating the trigger decision are implemented on VME boards housing the CNAPS 1064 chip [7] (see fig. 1). It is a parallel fixed-point arithmetic computer in SIMD architecture. The CNAPS-1064 chip (also called array) houses 64 processor nodes (PN). Up to eight chips (512 PNs) can be combined on one VME board. A PN is a processor for itself except that it shares the instruction unit and I/O busses with all the other PNs. An on-chip instruction unit handles the command and data flow. The commands are distributed via a 32 bit PN command bus. The 8 bit wide input and output busses are used for the data transfer to and from the CNAPS array. A direct access to these I/O busses is realized with a mezzanine board developed at MPI Munich. Through the mezzanine board the input vector is loaded into the CNAPS chip and the trigger result is sent back to the DDB. For synchronization reasons the CNAPS boards are driven with an external clock at 20.8 MHz (2 times the HERA clock frequency of 10.4 MHz).

The main internal parts of the PNs are arithmetic units like adder (32 bit) and multiplier (24 bit), logic unit, register unit, 4K memory and a buffer unit. Calculations are done in fixed-point arithmetic with choosable precision. The sigmoidal transfer function is implemented via a 10 bit look-up table (LUT) on chip. A full net with 64 inputs, 64 hidden nodes and 1 output node can be computed in 8 μs at 20.8 MHz, or in 166 clock cycles. To get the same speed with a single conventional CPU one would have to clock it at several GHz.

4.2 The Data Preprocessing

The Data Distribution Board (DDB) resides in a special "L2 VME crate" equipped with the L2 Bus, an 8 times 16 bit parallel data bus running with the HERA clock speed in an interleaved mode, yielding an effective 20 MHz transfer rate. For each subdetector the level 1 data, which are a quite heterogeneous such as calorimetric energy sums, tracker vertex histograms, tracker rays (bits in the $\theta - \phi$ plane), bit-coded muon hit maps etc., are sent serially onto one of the eight subbusses of the L2 backplane. For system control purposes, a special monitor board ("spy") with an independent readout of the data transmitted over the L2 bus is residing in the same crate.

On the DDB, the L2 data received are passed through a data type selection where they can be transformed (e.g. split into bytes or single bits) using a look-up table. After bit splitting, several preprocessing algorithms like summing of bits and bytes, bit selections or general functions (look-up) can be applied. The data may, of course, also be sent unchanged to the selection RAM, where the input vector for the neural network computer is stored. Through the use of XILINX 40XX chips the hardware can be flexibly adapted to changes, e.g. for new data formats in the received input. Using selection masks the data are transmitted via a parallel data bus from the RAM to a mezzanine receiver card directly connected to the local data bus on the CNAPS board. Figure 2 shows the hardware of the neural network trigger operating in H1-experiment. The upper crate
houses the CNAPS neuro-computer boards and the VME control computer (at the left). The lower (9U) crate houses the receiver units for the L1 information (at the right) and the data distribution boards. Each board is associated with its neuro-computer, connected via cable between the backplanes, carrying the preprocessed network input to the CNAPS board.

The system described above can be translated into an LHC environment without any principal problems. Also there, partial (coarse granularity) detector data are available for the level 2 and these informations can be used in full correlation to arrive at highly selective triggers. The main advantage of using neural nets as opposed to standard multi-purpose processors (using a high level computer language) is their inherent speed. It seems also that complex high-dimensional correlations - in absence of known apriori algorithms, which usually is the case at the trigger level - can be exploited in an optimal way with the adaptive methods provided by neural networks.

5 Vertex Finding with Neural Nets

An interesting field not yet fully exploited by neural networks is the tracking area. Here, the basic event pattern is provided by an ensemble of hits from the tracking detectors (two- or three-dimensional information) which give already a pretty clear “view” of the event origin and basic kinematic features. Of particular interest is the information from high precision silicon trackers, which are used offline to find secondary vertices in the events, i.e. to tag heavy flavor decays. Bottom-quarks, e.g., provide a unique signature for many known and new phenomena expected at the TeV scale such as top quark physics, Higgs searches and supersymmetry, in addition to the physics of B-hadrons themselves. By finding the secondary vertex from the B hadron decay at the trigger level, using the fine granular silicon strip information available at level 2, one is in principle sensitive to all B hadron decays, not only to the semileptonic decays considered in present trigger schemes [1].

As a pilot study we investigated the potential to “reconstruct”, at the trigger level, a possible secondary vertex associated with a certain set of tracks. In order to facilitate the network training in this initial study, the silicon strip information to be used was limited to the regions of interest (ROI) defined in the first level calorimeter trigger (the ROI strategy will be employed for the second level triggers at ATLAS). Typical decay lengths for charmed mesons expected in the LHC energy range are several centimeters, whereas the precision of space points for a modern Si strip detector is around 20 microns. This
gives a ratio for vertex distance to space point precision of roughly 100:1. This ratio seems sufficiently large to try fast secondary vertex recognition with the space hits alone as inputs to a neural net. No attempt was made to form tracks from the space points.

Using Monte-Carlo simulation, hits were generated in the various layers of the Si-detector of ATLAS, originating from $D^*$ decays which where given distributions in momentum space according to the expectation from top and Higgs ($m_{\text{Higgs}} = 200$ GeV) production. A typical decay length distribution for the $D$ mesons (coming from the prompt $D^*$ decays) is shown in fig. 3. Without attempting any conventional track reconstruction method, which would be forbiddingly long for a hardware trigger application, the hit pattern originating from the tracks within a cone around the ROI was given to a feed-forward network with 2 hidden layers (typically 20 nodes in each layer) and one output node. The task of the linear output node was to estimate the decay length associated with the hit pattern. Each input to the network is a 1 bit number, either 0 (no hit) or 1 (hit), ordered in rising $\phi$ coordinate, mimicking a realistic readout scenario. The nets were trained with a backpropagation algorithm with a target output value equal to the decay length of the simulated $D \to K\pi$ decay. The training was controlled by an independent sample of events, yielding the result shown in fig. 4, where the difference between the target value and the decay length estimated by the network is plotted. A resolution of $\sigma \approx 1.6$ mm is achieved in the simple case of only two tracks (originating from the $D \to K\pi$ decay).

In order to investigate the stability of the nets against noise, we added additional tracks coming from the primary vertex with corresponding hits to the neural input and repeated the training. As expected, the performance of the networks, keeping the network architecture the same, deteriorated progressively with increasing number of additional tracks. Doubling the number of tracks from the primary vertex resulted in an increase of the resolution for the decay length by about a factor of two ($\sigma \approx 3$ mm). Further details can be found elsewhere[8].

Further studies are required with increased complexity of the network architecture (more nodes in the hidden layers) in order to improve the perfor-
formance in presence of many false tracks close to the two tracks originating from the secondary vertex. In addition, the possibility of more than two tracks coming from the secondary vertex have not been attacked yet. The preliminary results, however, are quite encouraging and demonstrate the ability of the neural networks to extract the relevant information (presence of a secondary vertex) from a complex hit pattern without explicit track reconstruction. Such an algorithm would be extremely fast and well suited for an application at an early trigger level.

6 Conclusions

We have presented the principles and the hardware realization for the second level neural network trigger, operational in the H1 experiment at HERA since 1996 as a global event decision machine. Based on commercially available, massively parallel digital ULSI neural network chips, a 20 μs decision time is achieved for the network trigger. The network inputs are derived from the trigger information provided by the various level 1 trigger systems and are preprocessed by custom-designed hardware.

For the physics data taking at the LHC, e.g. in ATLAS or CMS, such a trigger system could be readily adapted. Depending on the field of application (level 1 or level 2) the preparation of the network inputs needs special attention, both on the electronics level as well as in the successful training of the networks. Besides the proven strength of neural networks in pattern recognition tasks, one of the main motivations of using the neural approach in a trigger application at the LHC is the speed provided by dedicated neuromorphic hardware executing the inherently parallel computations of the neural algorithms.

As a promising physics application we have studied the neural networks ability to recognize secondary vertices in an ensemble of tracks, based on the information from the simulated ATLAS Si-detector. Feed-forward networks were trained to estimate the decay lengths of D mesons from top and Higgs decays, given solely the information from the Si-hits in the various layers of the detector. It is found that the resolution for the decay length is adequate (order of a few mm) to recognize a secondary vertex, thus being able to tag charmed and beauty decays with high efficiency.

References


S. Udluft et al., The H1 Neural Network Trigger - Training and Monitoring, ibid.

L. Januschek et al., Artificial Neural Networks as a Level 2 Trigger at the H1 Experiment - Performance Analysis and Physics Results, ibid.


THE HERA-B HIGH-\(p_T\) LEVEL-0 TRIGGER LOGIC ELECTRONICS

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Abstract
The high-p\(p_T\) trigger has been proposed for broadening of the HERA-B physics program. A dedicated logic system is needed to select events out of a data stream with typical rate of \(10^{12}\) hits/sec. The paper describes the trigger logic electronics system and data processing which provide necessary speed and flexibility for the level-0 trigger selection criteria.

1. INTRODUCTION
One of the main goals of the HERA-B experiment is the measurement of the asymmetry in \(B \rightarrow J/\psi K^0_s\) decay mode. The high-p\(p_T\) ‘hadron’ trigger considerably broadens the HERA-B physics program. It provides the experiment with the ability to measure CKM unitary triangle angles \(\alpha\) and \(\gamma\) by detection of the \(B \rightarrow \pi^+ \pi^-\) and \(B \rightarrow K \pi\) decays [1], the expected numbers of reconstructed events are 500 and 750 per year correspondingly. The high-p\(p_T\) trigger allows either to measure the Bs mixing frequency in Bs \(\rightarrow D_{sh}\) mode, where the expected number of reconstructed events is about 400 per year.

The high-p\(p_T\) Level-0 trigger (pretrigger) selects candidates for particles with large transverse momentum and provides the First Level Trigger (FLT) with initial information to start the track finding process. It is able to detect and encode approximately \(10^8\) track candidates out of \(10^{12}\) possible combinations per seconds.

A description of the main components of the High-p\(p_T\) pretrigger system can be found in [2]. This paper mainly describes the logic electronics.

2. PRETRIGGER HARDWARE IMPLEMENTATION
The high-p\(p_T\) pretrigger is organised using approximately 19000 pads of different size distributed among three layers of chambers located in the magnet. There is a projectivity between position and size of correspondent pads in three layers with respect to the vertex position. Pad sizes are varying in correspondence with their distance from the beam.

For the high-p\(p_T\) pretrigger the following track selection algorithm has been implemented (s. fig.1): each pad of the first chamber layer (PT1) maps to up to five adjacent pads in the second layer PT2, and each pad of PT2 maps to two adjacent pads of the third layer PT3. The tracks with large transverse momentum produce signals in projective or adjacent pads of three chamber layers.

The pretrigger logic electronics has sectional structure and consists of three types of boards, the Link Board, the Pretrigger Board and the Message Generator (Master Card). Each section is covered by one Master Card and up to 8 Pretrigger Boards, while each Pretrigger Board is connected to 6 Link Boards.

The Link Board is located near the detector and provides via optical fibres the fast data transfer to the main trigger Logic.

A Pretrigger Board receives the data of two complete pad rows of all three detector layers. Data which match to the trigger algorithm are encoded and transmitted to the Message Generator on a dedicated bus.

The Message Generator acquires data pattern from a group of connected Pretrigger Boards, transforms them by means of a look-up table into some messages, which are sent to the Track Finding Unit (TFU) of the HERA-B Level-1 Trigger system.

3. LINK BOARD
Fig.2 shows the block diagram of one link channel on the Link Board. It transmits the digital data of two half chamber rows during one bunch crossing interval of 96 nsec. Therefore at first the incoming data have to be stored in registers. With a period of 48 nsec the register outputs are multiplexed to two Autobahn transmitters (Motorola MC100SX1451), which are 32-bit parallel-to-serial transceivers with an effective data rate of 800 Mbit/sec. On the first transfer channel 30 pad bits are sent together with one Bunch Number bit and a Cycle Bit CB, which distinguishes between the two detector rows. The second transmitter sends the
remaining pad bits, the complete Bunch Number BN and again the Cycle Bit.

The serial Autobahn output is connected to an optical transmitter [3], which sends the data to the Pretrigger Board over a distance of about 45 m.

One Link Board contains three link channels. It is operating synchronously with the Bunch Clock. It has been designed as piggy back on the Front End Driver Card, which collects the pad bits for data acquisition.

4. PRETRIGGER BOARD

The Pretrigger Board PTB searches for coincidence pattern as trigger candidates and combines for each trigger road the involved pads to data packages, which are sent to the Message Generator. Fig.3 shows a block diagram of its main components.

4.1 Data Transfer from the Detector

During one HERA bunch crossing interval the Pretrigger Board has to receive and process the complete pad information of two detector rows of all three planes. Since the maximum number of pads per row is 96, every 48 nsec in total 278 detector bits together with redundant bunch number information are sent to the PTB on 12 transfer channels. Each channel consist of a pair of Autobahn transceivers (Motorola, MC100SX1451) and an optical link between their serial ports [3].

4.2 Coincidence Logic

The Coincidence Logic is able to combine each pad of the first detector layer with up to 5 pads of the second and up to 6 pads of the third layer. Fig.1 shows an example of a possible Trigger Road structure. The Logic has been designed as a 3-stage pipeline with a clock period of 48 nsec. With the first strobe a data set of 3*96 bits is stored in the Input Register. For each pad of the first layer, which is found to be a starting point of a trigger road, a Road Starting Flag RSF is set. The resulting RSF pattern together with the pad information of the other layers then is stored with the next strobe. Only if at least one RSF has been detected, a Road Flag (R-Flg) is set and the complete data set is written to the Event FIFO with the third strobe (Zero Suppression).

The Coincidence Logic has been implemented by means of 6 large CPLD’s (Vantis, MACH466), which are in-system programmable. So the coincidence algorithm easily can be modified by reprogramming the firmware. A VME access to the Coincidence Logic is provided for a Mask Register, which allows to disable each input bit individually, and for a Test Register, which in Test Mode emulates the detector input.

4.3 Bunch Number Comparison

On each of the 12 transfer channels to the PTB some Bunch Number bits are transmitted. Since these are the only predictable information, they are used to monitor the reliability of data transfer by comparing 66 bits in real time. If a comparison fault is detected, an error flag is set, and an interrupt can be generated.

4.4 Event FIFO

The Event FIFO stores data sets consisting of a 96 bit RSF pattern, two 96 bit pad pattern of the second and third chamber layer, the 8 bit Bunch Number and the Cycle Bit. It decouples the system clock on the input side, which is synchronised with the Autobahn clock and has a period of 48 nsec, from the output system clock with a frequency of 25 MHz. Addition-
ally it acts as data buffer, because one input data set can generate more than one output data package. The Event FIFO has a depth of 512 words and is built of 17 chips SN74ALVC7804 (Texas Instruments).

4.5 Output Data

The output system clock drives a Finite State Machine controlling the output data generation, which again is organised as 3-stage pipeline process. In the first step a 7-bit Priority Encoder generates a binary code for the actual most significant RSF bit. Then that code is used to address two Multiplexers selecting the corresponding up to 5 pads of the second and up to 6 pads of the third layer. The resulting data together with the 8-bit Bunch Number and the Cycle Bit are written to the Output Register in the last step.

4.6 Data Transfer to Message Generator

Since up to 8 Pretrigger Boards have to be connected to one Message Generator, the output data are transmitted on a bus. The communication protocol has been implemented by 8 dedicated 2-wire handshakes providing fast identification of data source. The data transfer time is 40 nsec.

4.7 Test Facilities

In order to be able to test the Logic of the board, there are Test Registers implemented, which cover the complete input range of 288 bits. The test pattern stored via VME is processed in real time, and the resulting output data are written to a Test FIFO, which can be read-out by VME for comparison with the expected values. The Test FIFO also is useful for monitoring the data stream during data acquisition.

4.8 Additional Features

There are some other important features of the PTB, which for reasons of simplicity are not shown in the block diagram:

⇒ A Veto Logic accept Bunch Numbers distributed by the HERA-B Calorimeter in order to inhibit certain events.
⇒ A 29-bit counter monitors the number of generated output data sets. It can be read-out by VME.
⇒ The maximum number of output data sets per event can be programmed by VME.
⇒ The input system clock is monitored by a watchdog circuit.

5. MESSAGE GENERATOR

The Message Generator receives data sets from several Pretrigger Boards and transforms them to messages, which contain all necessary information according to a standard, which is accepted by the Track Finding Unit TFU of the HERA-B Level-1 Trigger. Fig.4 shows a block diagram of the main components.

5.1 Handshake Logic

The Handshake Logic is responsible for the data transfer protocol between connected Pretrigger Boards and Message Generator. The eight DAV flags indicating on which PTB a data set is available are stored periodically into the input register of an 8-bit Encoder. If there is at least one flag set, the Encoder starts to select the PTB with the highest number by issuing the corresponding DAC signal, which open the connected PTB data port and enables the 27-bit data set to arrive at the Data Input Register, where it is stored together with the 3-bit code of data source (PTB Code). Then the next DAV flags are selected one after another, until
the Encoder Input Register is empty and the next DAV pattern is stored. That method ensures, that all PTB’s are selected with equal probability.

The data transfer rate between Pretrigger Board and Message Generator is 25 MHz.

5.2 Data Input Register

The Data Input Register is the first stage of a 3-stage pipeline. It has a width of 30 bits and distributes 19 bits (RSF Code, PTB Code, Bunch Number, Cycle Bit) to the Data Buffer and 11 bits (pad bits of the second and third detector layer) to the Road Encoder.

5.3 Road Encoder

Together with the Data Buffer the Road Encoder builds the second stage of the process pipeline. It sequentially encodes up to 18 possible combinations between the 11 input pads. Every 40 nsec a new 5-bit code is provided. Together with 11 bits of the Data Buffer (RSF Code, PTB Code, Cycle Bit) and two additional bits, which have been introduced for multiple message generation, it forms the 18-bit address of a Look-up Table, which contains all information necessary to compose the message.

5.4 Look-up Table

The Look-up Table is a 256K*64 bit static RAM with an access time of 15 nsec (IDT7MP4045). For each possible road 57 out of 64 available bits are used to provide all relevant parameters. The table can be written and read-out by VME.

5.5 Message FIFO

The Message FIFO (IDT72205) receives besides the data bits of the Look-up Table the Bunch Number and some 15 constant bits reserved for each subdetector. It is the last stage of the pipeline, which is clocked with 25 MHz frequency. It also acts as message buffer, because the output data stream may be disabled by the connected TFU’s for short times.

5.6 Data Transfer to TFU

The Message Generator is connected to several TFU’s by a 20-bit bus. Therefore the messages have to be split into four parts by a multiplexer. The resulting packages are converted to PECL level and transmitted with a frequency of 100 MHz.

5.7 Test Facilities

Again the complete Logic of the board can be tested in real time by writing data pattern to the Test Register, starting the evaluation process and reading the resulting message packages from the Test FIFO, which monitors the output data stream.

6. SYSTEM LAYOUT

Pretrigger Board and Message Generator are VME boards of 9 height units and 340 mm depth. Two clusters each consisting of one Message Generator and up to eight Pretrigger Boards are located in one VME crate. Four such crates are sufficient for the complete High- P, Level-0 Trigger.

In order to reduce the power consumption 3.3V technology has been used as far as it was available. Nevertheless the power consumption adds up to about 1 KW per crate mainly because of the large number of Autobahn chips used.

7. STATUS

Prototypes of all three boards have been built and tested successfully. Series production has been started and the complete system will be available at the end of 1999.

8. REFERENCES

   A. Schwartz, HERA-B note 97-231
   V. Popov, HERA-B note 97-252
An automated test bench for the ATLAS shapers and SCAs

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Abstract:

An automated test bench has been developed for the ATLAS shapers and the analog memory integrated circuits. The measurement setup is based on a Labview application and the testing printed circuit board has a GPIB bus interface. The testing program works a handshake with a four axis table-top mounted robot, which handles carefully the QFP100 packaged circuits during the positioning pick-up and sorting phase. This test bench provides an autonomy of 660 chips.

I) Introduction:

Testing analog integrated circuits for ATLAS front end is an important challenge regarding the volume of the production needed (200,000 channels), the analog features, and the packaging used. An automated test station has been developed for the shapers and analog memories also called switched capacitors array (SCA). Both circuits are packaged in the QFP100 format to save space on the front end board and to ease the interconnection of the circuits on the front-end board.

This test station consists of an automated measuring system in handshake communication via a series bus with a manipulating robot.

II) The shaper test board:

![Figure 1: Shaper test board schematic](image-url)
A specific test card has been designed to test the shaper production (QFP-100 package) with the LabView environment. To be as close as possible to the real input signal shape, a four channel 0T-hybrid with a common “ATLAS like” calibration input signal generates the pulses to be fed into the four shaper channels. The shaper chip is mounted on a high reliability QFP socket (“Clamshell” from Yamaichi or equivalent). This socket is plugged on a specific support soldered on the test card; therefore changing socket is easy in case of contact failure.

An analog multiplexer, designed with operational amplifiers (CLC410 with disable input), connects one of the 14 shaper outputs (4x3 Gains, Analog Mixer and Reference [dummy stage]) to the oscilloscope.

Two registers are implemented on the board:
- four bits to select the multiplexer channel
- four bits to select the time constant with an extra bit to burn the fuses and fix the time constant (time constant programming)
- a bank of level-shifters is used to enable or disable the mixer inputs via the internal shaper register and analog switches.

Some ancillary logic generates the “handshake dialogue” with the GPIB [IEEE-488] interface via a flat cable. This interface is implemented, on a second card, in a FPGA [ALTERA] with external logic drivers. Figure 1 presents the testing board architecture. We used « Rad-tolerant » components on the testing board, in prospect to employ the same board for shapers irradiations (neutrons and gammas).

### III) MEASUREMENT PROCEDURE

The time constant is calculated for every chip to find a peaking time very close to a well defined target value.

For every gain and for each channel, the input signal amplitude is controlled to reach the highest amplitude at the output, in the linear range. Then the following parameters are measured and stored in the database: the power dissipation, the peaking time, the base-line and its dispersion, the time constant used, and the circuit final qualification (good or not). This qualification results from a comparison of each measured parameters against a well-known template. The amplitude and time parameters are measured using the digital scope functions. For each successfully tested circuit, the time constant is fixed by blowing its integrated fuses. All the measurement software for the shaper is written in Labview.

### IV) PICK AND PLACE AUTOMATION

1) Pick and place system

The FPQ100 package used for shapers and SCA has the benefit of saving space on the front-end board, but it presents the drawback of fragile leads. Therefore great care must be taken to hold them during the production tests. Packaged circuits are delivered on 6*11 unit plates. We use a table-top mounted Scara robot from Adept Technology to handle them for testing and sorting. Figure 2 shows its side view.

![Figure 2: Robot side view](image)

Over the robot working area 20 trays are laid out as in figure 3. On the right side are settled 10 trays filled with circuits to be tested.

![Figure 3: Trays in the robot working area.](image)

On the left are those categorized after testing: there is a set of six trays for successfully tested circuits, a second set of three trays for chips with at least one analog parameter measured out of range; the last tray receives dubious chips found regarding the logic register check or the fuse blowing steps.

To ensure the package leads integrity, great care has been taken against mechanical stress when handling chips. A special silicon conductor sucker is used to approach .5mm close to the chips. This contact point is grounded via the robot arms (figure 4) in order to avoid electric static discharges (ESD) while preserving a smoothly approach.
Then an electric control vacuum pump holds the chips via the suction pad without any stress. A self aligned cavity is added to compensate position errors in the horizontal plane. The package to-be-tested is then moved onto the test board. A “zero insertion force” socket is used at the test point to avoid any damage on the chip leads. Then a pneumatic jack secures the socket before measuring phase starts. The socket “open” and “closed” positions controlled via two inductive sensors fixed on the jack (figure 5). The measuring computer communicates with the robot controller via a RS232 series port, to define when to start measuring and what is the final result.

2) Accuracy and security

The robot position repeatability is +/- 0.02mm in the (x,y) horizontal plane, +/- 0.01mm in the z vertical direction, and +/- 0.03° in the theta position around z axis. The maximum speed is better than 1m/s or 360°/s. We work at a medium speed, which is fast enough to reach the most distant point from the testing board in less than 1s.

Three optical fiber photoelectric switches (OMRON E3X-NH) have been fixed to the socket to control the circuit insertion as shown in figure 6. Two of them control that a plan .5mm above the package of the circuit remains clear. The third optical switch is an extra security element to control that the socket is really empty before inserting another one.

V) CONCLUSION

This test bench is now in its evaluation phase in Grenoble with shaper circuits. It should run 8 hours/day during 7 months for shapers testing, and more than 9 months for the SCA that needs a longer testing time per chips.
LARGE-SYSTEM EXPERIENCE WITH THE ASD-8 CHIP IN THE HERA-B EXPERIMENT

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Abstract

The amplifier-shaper-discriminator chip ASD-8, developed by the University of Pennsylvania for drift chamber applications in high rate environments, is used in large detector systems in the HERA-B experiment. We report on the results of tests performed on some 25000 chips and on the design and tests of the PC-boards. The so far largest system employing ASD-8 chips is the HERA-B Outer Tracker with about 120000 drift chamber channels. We present first experience with the grounding scheme, noise suppression and the slow control system as well as first measurements with the full readout chain in the HERA-B experiment.

1. INTRODUCTION

HERA-B is a fixed target experiment for studying CP violation in B-meson systems using an internal wire target in the proton beam of HERA [1]. To reach the necessary production rate of $b$ quarks an average of 4 interactions per bunch at a frequency of about 10 MHz (96 ns bunch separation) has to be generated. This leads to a high particle density with a radial distribution of the particle flux ($R$ is the distance from the beam): \[ \phi \approx \frac{10^{14} \ldots 10^{15}}{R^2 \cdot \text{year}} \]

The main detector components are a silicon vertex detector, a magnet (2.2 Tm), a main tracker with MS-GCs in the inner and drift tubes in the outer part, ‘High-$P_T$’ Chambers, a RICH, an electromagnatic calorimeter and a muon detector with drift tubes. The detector covers a forward angular range of 220 mrad in the bending plane of the magnet and 160 mrad vertically.

The amplifier-shaper-discriminator chip ASD-8 [2], developed by the University of Pennsylvania for drift chamber applications in a high rate environment, is used in different detector systems of the HERA-B experiment (Outer Tracker, RICH, Muon System, High-$P_T$ Chambers) with a total of about 200000 channels.

In the following we refer mainly to the Outer Tracker which is with about 120000 channels the largest ASD-8 application in HERA-B.

2. THE OUTER TRACKER SYSTEM

The Outer Tracker of HERA-B [1] consists of 13 planar superlayers of drift tube modules. The detector acceptance starts at a radial distance of 19 cm to the beam. Together with the Inner Tracker it allows a precise momentum measurement and provides fast track recognition on the first trigger level.

The drift tubes are folded from gold-coated poly-carbonate foil with an hexagonal cross section (honeycomb tubes). The inner diameter of the cells is 5 mm in the most exposed sections and 10 mm further outside. As drift gas Ar/CF$_4$/CO$_2$ (65/30/5) is chosen. Operating at a gain of about $4 \cdot 10^4$ the drift velocity is about 100 $\mu$m/\text{ns} which allows the track signals to be collected within the bunch crossing time of 96 ns.

Particled densities and radiation levels in the Outer Tracker are comparable to those in similar detectors for LHC. In the hottest area the particle flux is about $2 \cdot 10^3 \text{mm}^{-2} \text{s}^{-1}$. The drift tubes are longitudinally subdivided to limit the single channel occupancy to about 20% (the shortest segmentation near the beam is 20 cm). Because of the planar detector geometry the front-end amplifiers can be placed away from the beam pipe yielding a radiation load below about 30 Gy per year at the location of the ASD-8 boards.

Pattern recognition in a dense particle environment and a precise momentum measurement require a position resolution of about 200 $\mu$m. The corresponding good time resolution can be achieved by triggering on the first electron cluster arriving at the anode. At a gain of $4 \cdot 10^4$ a cluster results in about 1.5 fC after fast shaping. Such a low threshold requires low noise and low crosstalk in the system. The first level trigger requires a high hit efficiency and a fast signal collection within the bunch separation of 96 ns.

In order to fulfil the requirements on tracking and triggering in a large system of about 120000 channels the tracker front-end electronics should have the following characteristics:

- High integration density at low power consumption;
- low per-channel costs;
- fast signal shaping and precise timing;
- low noise: threshold sensitivity of about 2 fC;
Table 1. Performance figures of the ASD-8 chip

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integration density</td>
<td>8 ch. on 2.7 × 4.3 mm² die</td>
</tr>
<tr>
<td>Power consumption</td>
<td>0.3 W/channel (incl. output)</td>
</tr>
<tr>
<td>Cost</td>
<td>about 4 DM/channel</td>
</tr>
<tr>
<td>Signal shaping time</td>
<td>about 10 ns</td>
</tr>
<tr>
<td>Tail cancellation</td>
<td>t₀ ≈ 1.5 ns</td>
</tr>
<tr>
<td>Double pulse resol.</td>
<td>25 ns</td>
</tr>
<tr>
<td>Intrinsic noise</td>
<td>(900 + 70/pF) electrons</td>
</tr>
<tr>
<td>On-chip crosstalk</td>
<td>analog: ~ 0.1%</td>
</tr>
<tr>
<td>Threshold</td>
<td>~ 2 fC</td>
</tr>
<tr>
<td>Baseline shift</td>
<td>0.5 - 1.0 fC/MHz</td>
</tr>
</tbody>
</table>

Figure 1. The front-end electronics of the Outer Tracker.

- low crosstalk, required dynamic range:
  - total charge / threshold charge = 40;
- small rate dependence of the threshold up to about 2 MHz;
- radiation hardness up to a level of about 1 kGy.

These requirements were found to be met by the ASD-8 chip as shown by the actually achieved performance figures listed in table 1.

3. THE OUTER TRACKER FRONT-END ELECTRONICS

For the Outer Tracker drift tubes the anode wires are on high voltage and the cathode foils on ground. The anode signals are AC coupled to the amplifier via coupling capacitors which are placed inside the gas volume (discharge protection). For better accessibility the ASD-8 board is mounted outside the gas box.

The whole readout chain of the Outer Tracker (Fig. 1) consists of an HV board with coupling capacitors for the chamber signals, a connecting twisted pair cable, a feed-through board to transfer the signal through the wall of the gas box, the ASD-8 board, a twisted pair cable and TDCs. The TDCs are read out by digital signal processors. In addition the hit information of 4 selected superlayers (trigger layers) are transferred to trigger link boards.

FEE Components:

**HV board:** The HV boards are printed circuit boards connecting the chamber wires to the high voltage and to the pre-amplifiers. The anode signals are AC coupled to the amplifier via 330 pF capacitors. The boards are located inside the gas volume.

**Feed-through board:** The signal cables (twisted pair, length 25 or 50 cm) from the HV boards are plugged from the inside of the gas-box to the feed-through boards. On their outside the feed-through boards hold the ASD-8.

**ASD-8 board:** On the ASD-8 board the drift chamber signals are transformed to a digital output which is transmitted via shielded twisted pair cables to the TDC’s. The board is described in detail below.

**Time-to-digital converter:** The customized 8-channel TDC chip digitizes the time in 0.5 ns bins with an 8 bit output. Each TDC channel has a GTL receiver on chip. The differential, open collector output of the ASD-8 is terminated at the receiver side (see sect. 5).

The crates housing the TDC boards are mounted on the cable frame of the detector superlayers. The maximal cable length between the ASD-8 boards and the TDC crates is 5 to 10 m.

**ASD-8 power distribution board:** These boards serve three purposes: distribution of the +/- 3V power, slow control of thresholds, currents, voltages and switching of the test pulser.

A distribution board supplies 6 groups with 8 ASD-8 boards each. The threshold is the same for all ASD-8 boards in a group and can be selected out of two threshold values provided on the distribution board. Tests pulses can be sent to selected groups.

The boards are controlled by a SLIO processor and are connected to the slow control system via CAN bus.

4. THE ASD-8 CHIP

4.1. Technical Data

The amplifier-shaper-discriminator chip ASD-8 [2] (fig. 2) has been developed by the University of Pennsylvania for drift chamber applications under high radiation (specifically for SSC). The 8-channel chip is designed in a bipolar process which combines high speed with a low noise level and low power consumption.

Amplifier: The ASD-8 input is a preamplifier with a sensitivity of 2.5 mV/fC, a bandwidth of 100 MHz and an input impedance of 115 Ω. The input is differential...
and symmetric for positive and negative pulses.

Shaper: The two-stage shaper with tail cancellation yields a double pulse resolution of 25 ns. The tail cancellation compensates the ion tail of the drift chamber pulses. Analog outputs are provided for 3 channels per chip, selectable after the 2nd shaper or after the tail cancellation. The output pulse is proportional to the input signal up to about 50 fC (20 mV/fC).

Discriminator: The discriminator is a two-stage differential amplifier with positive feedback. The threshold is voltage programmable for each channel (with 250 mV/fC, maximal about 1.4 V). The differential, open collector output is current programmable to adjust the swing.

4.2. Series chip tests and selection
HERA-B ordered a total of 90 wafers, each with about 335 chips. The yield per wafer was on average 77%. Each chip was tested according to a scheme which evaluated the general functioning, the threshold behaviour and the noise level.

For each channel the threshold $U_{\text{eff}}$ to record a standard 4 fC test pulse with 50% efficiency was determined. The noise behaviour of a chip was characterized by the threshold $U_{\text{noise}}$ for which the noise rate exceeded 2 kHz. The difference $U_{\text{eff}} - U_{\text{noise}}$ is a measure for the signal-to-noise distance and thus of the quality of a channel.

The chip tests revealed an appreciable range for the $U_{\text{eff}}$ threshold from about 900 to 1400 mV (fig. 3). With this variation it is not possible to define a common threshold for the whole system if a homogeneous sensitivity to the first arriving electron cluster should be obtained. On the other hand, to keep the front-end electronics simple and compact, individual threshold settings for each channel should be avoided. Therefore 4 categories of threshold ranges were defined:

$$U_{\text{eff}} = 860 \ldots 950, 960 \ldots 1050, 1060 \ldots 1150, > 1150 \text{mV}.$$  

To account for the signal-to-noise variation for a given $U_{\text{eff}}$ (fig. 3) in each of the 4 gain categories, 3 noise categories corresponding to noise distances had to be defined:

$$U_{\text{eff}} - U_{\text{noise}} = \geq 550, 500 \pm 50, 400 \pm 50 \text{mV},$$

where $U_{\text{eff}}$ are the mean values of the signal categories ($U_{\text{eff}} = 900, 1000, 1100, 1200 \text{mV}$). A chip was assigned to one of the 12 categories according to its minimal $U_{\text{eff}}$ and maximal $U_{\text{noise}}$ values. The assignment was used to mount similar chips on a board (carrying two chips) and combine similar boards to groups which are supplied with the same threshold. Chips with worse noise performance are used in less sensitive areas (lower rates, 10 mm cells).

5. THE ASD-8 BOARD

5.1. The Board Design

Design considerations: The analog inputs of the ASD-8 chips have a very high sensitivity in the order of 1 fC which makes them susceptible to noise and RF pickup. Because of the combination of analog inputs and digital outputs on the chip one has in particular to worry about feedback from the output to the
input. In the design of the printed circuit boards carrying the ASD-8 chips special care was taken for a good grounding scheme, decoupling of the analog and digital parts, noise rejection from power sources and noise and crosstalk separation of different channels in a densely packed environment.

**The board design:** Two ASD-8 chips with 8 channels each are mounted on a multilayer board (table 2, fig. 5).

The chip has a fully differential input: the anode signal is fed into the negative input and the positive input is connected via 10 pF to the chamber ground which reduces the RF pickup.

All supply voltages (±3V) are separated into analog, digital and output drive supplies and have RC filters at the input. Between the analog and digital part of the chip is a gap in the groundplane. Both grounds are connected via an inductance at the input connector. The analog ground is extended to rails along the sides of the board which slide into the holding brackets on the chambers. The brackets are made of CuBe springs providing a fine-mashed shielding between the boards in the densely packaged front-end electronics on the chambers.

Since it was found that the ASD-8 inputs survive voltage spikes only up to about 300 V a diode protection was added. Tests have shown that the diode in combination with an input resistor of 50 Ohms protected the input transistors for discharges of 3000 V fed into the input via a 1 nF capacitor.

Only one voltage level for the thresholds is provided per board. The two chips on each board were therefore matched according to their gain and noise quality class (see chip tests, sect. 4.2). The maximum difference of the reference thresholds $U_{ref}$ of two channels of a single board should be less than 300 mV. In some cases Schottky diodes ( $U_f = 200$ or 380 mV ) were used to shift the threshold of chips or single channels to avoid more categories or to reduce the rejects. The variations of the threshold sensitivities for different boards will be compensated by a threshold correction table.

The differential open collector output is current programmable. Pull-up resistors on the TDC boards of 62 Ω yield at the chosen current of 2 mA a swing of 120 mV (an offset of 1.25 V is added by the receivers on the TDC board). The analog outputs of the chips are not enabled.

Testpulses can be coupled to the positive input via a 1:10 divider (reduction of noise pickup via the test pulse system) and a 1 pF capacitance. The pulses fire all channels on a board at the same time.

### 5.2. Board Tests

The 11000 produced boards had to undergo quality tests and were then sorted according to 12 categories as done for the single chips: 4 categories (1, 2, 3, 4) according to the threshold of 50% efficiency for 4 FC $U_{eff}$ and 3 categories (green, blue, red) of signal-to-noise distance $U_{eff} - U_{noise}$. A board enters into a category according to the channels with minimal $U_{eff}$ and maximal $U_{noise}$.

Table 3 shows the distribution of the boards in different categories. For each board the two chips belong to the same category. The remaining variations of $U_{eff}$ within the 16 channels can be seen in fig. 4 which shows the difference between the maximal and minimal $U_{eff}$ on the boards. Differences larger than 300 mV have been decreased by Schottky diodes as described above. With this procedure the threshold uniformity on the boards is about ±15%. The variations between different boards are accounted for by the threshold setting on the distribution boards.

The board quality is mainly determined by the $U_{eff} - U_{noise}$ category. Table 3 shows that more than 80% are in the two better categories ‘green’ and ‘blue’.

### 6. ELECTRONICS INSTALLATION AND COMMISSIONING

The ASD-8 boards of the different categories were installed such that for the high-occupancy, innermost detector parts amplifiers with a large signal-noise difference (e.g. green) are chosen. The outer detector parts, contributing less to the acceptance, are equipped with boards which have a small signal-noise difference (e.g. red). The CAN bus controlled distribution cards allow to set individual thresholds for groups of 8 ASD-8 boards (see sect. 3).

Cu-Be rails soldered to the gas box are used to provide good ground connection between the gas box and the individual ASD-8 boards. In addition shielding of the output signal cables is necessary to minimize the capacitive feedback of the digital output signals to the amplifier inputs. Care is taken that the shielding has a very good, low impedance contact to the digital ground potential of the ASD-8 board. Bad ground connections between either amplifier and gas box or amplifier and cable shielding leads to oscillations of the amplifiers with their characteristic frequency of about 40 MHz.
Table 3. Distribution of the tested ASD-8 boards in signal-noise categories, 4 categories (columns) for different gains, 3 categories (rows) for different signal-noise distance ($U_{eff}$ = 900, 1000, 1100, 1200 mV).

<table>
<thead>
<tr>
<th>$U_{eff} - U_{noise}$ [mV]</th>
<th>850-950</th>
<th>960-1050</th>
<th>$U_{eff}$ [mV]</th>
<th>&gt;1150</th>
<th>whole range</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 550 (green)</td>
<td>4.6 %</td>
<td>12.6 %</td>
<td>30.3 %</td>
<td>4.4 %</td>
<td>42.0 %</td>
</tr>
<tr>
<td>500 ± 50 (blue)</td>
<td>4.2 %</td>
<td>18.0 %</td>
<td>12.1 %</td>
<td>4.4 %</td>
<td>39.0 %</td>
</tr>
<tr>
<td>400 ± 50 (red)</td>
<td>4.0 %</td>
<td>6.1 %</td>
<td>8.2 %</td>
<td>0.6 %</td>
<td>19.0 %</td>
</tr>
<tr>
<td>whole range</td>
<td>12.8 %</td>
<td>36.7 %</td>
<td>30.6 %</td>
<td>9.4 %</td>
<td></td>
</tr>
</tbody>
</table>

The above measures lead to very low noise of the readout chain. Operated at the threshold values $U_{noise}$ from the laboratory tests the complete chain consisting of ASD-8 boards, plugged to the gas box, 5 m long twisted-pair cable for the connection to the TDC, and TDC boards for the digitization, showed noise occupancies of less than 1 % (96 ns large readout windows).

The connection of the honeycomb modules to the amplifier leads to a higher noise level. To compensate the antenna effect of the up to 2 m long wires, an increase of the threshold voltage by 150 to 200 mV, corresponding to about 0.8 fC, is necessary.

The noise occupancies (readout window of 96 ns) for two sectors of a superlayer after installation in HERA-B are shown in fig. 6. The plot shows a sector with 5 mm cells equipped with ASD-8 boards with low noise threshold (green) and a sector with 10 mm cells and ASD-8 boards from the worst noise class (red) is shown. For the ‘green’ ASD-8 boards the threshold can be set as low as 2 fC, while for the ‘red’ category the threshold has to be increased to about 3 fC to achieve a similar noise level ($< 10^{-2}$).

The well-functioning of the readout chain for large particle fluxes is illustrated in fig. 7. The hit occupancy for the different sectors of a superlayer (magnet chamber) is shown for different target interaction rates (primary proton-nucleus interaction rate). The measured occupancies depend up to 80 MHz linearly on the interaction rate, well above the nominal interaction rate of 40 MHz. There is no saturation effect at high occupancies observed (the offsets at zero target rate results from electronic noise and background from the HERA accelerator).

REFERENCES

SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 µm CMOS technology for applications in the LHC

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Abstract

A dedicated high-speed 18 Kbit static memory featuring synchronous mode, parity and dual port access has been designed and fabricated in a quarter micron 3 metals commercial CMOS technology. This SRAM has been designed to be a test vehicle to measure Single Event Upset (SEU) effects on a real circuit. The measurements have been performed at the cyclotron of Louvain-la-Neuve, Belgium, with a proton and heavy ion beam. We present the experimental cross-section curve for the RAM chip, together with a detailed study of the SEU phenomenon on dedicated test structures (shift registers) integrated in the same technology. Finally, we give an estimate for the upset rate the memory chip will experience in LHC.

1. INTRODUCTION

As a complementary solution to the use of dedicated radiation hardened technologies, we have recently proposed a design approach to increase the radiation tolerance of ASICs designed in commercial deep submicron processes [1]. Such approach, based on the use of enclosed geometry for the NMOS transistors and of guardrings, has lead to the design of circuits able to stand total doses in excess of 30 Mrad integrated in a quarter micron technology [2]. Since the use of guardrings also effectively protects the circuits from Single Event Latchup (SEL) [3], the main radiation-induced problem still needing to be investigated deeply is Single Event Upset (SEU). This is particular important since the trend points to an increased sensitivity to SEU with the down-scaling of CMOS technologies.

In this paper, we present results from heavy ion and proton irradiation of different test structures. From the measurements, we are able to estimate upset rates for basic building blocks in the LHC radiation environment. These results can be used by ASICs designers as a guideline on the architecture to choose for any given radiation environment in order to obtain an acceptable upset rate.

2. EXPERIMENTAL DETAILS

We have actually used two types of test structures in a commercial 0.25 µm CMOS process to validate our SEU measurements. In addition to a dual-ported static RAM, a set of shift registers has been implemented to evaluate the SEU sensitivity of basic building blocks used in ASICs design.

All the designs used the radiation tolerant layout practices described in [1] and aimed at hardening the circuits to total dose effects. Therefore, all NMOS transistors were designed with special geometries, and guardrings were extensively used across the circuit.

2.1 Memory array

The test structure most representative of a real circuit was an 18Kbit Synchronous Dual Ported Static RAM, organized in 2K x 9bit words (8 data bits plus 1 parity bit). This memory is a building block for a high-speed optical link interface ASIC being designed at CERN. However, it can also be used as a generic building block for read-out buffers or FIFOs.

The design features separate address and data busses for the Read and Write ports, thus allowing the execution of simultaneous Read and Write operations. Access operations to the memory are synchronous to the clock signal. A read cycle of the memory is shown in Figure 1, and a read access time of 13.3 ns was measured.

![Figure 1: Snapshot of a sequence of read access cycles showing a read access time of about 13.3 ns.](image-url)
The cell uses PMOS pass devices, as they are smaller than enclosed N type transistors. In addition, special care was applied in the design of the NMOS devices, to make them even smaller than what a conventional enclosed N device requires. The resulting size of the memory cell is only 5.90 µm x 9.94 µm. This is only about 5 times larger than the minimum single port RAM cell that one could achieve with this technology using the most aggressive design rules. The address decoding logic is built with a mixture of static and dynamic cells. Dynamic cells are used wherever it was estimated that SEU was not a potential danger, since some of the nodes – such as the write lines – have a very high capacitance anyway. These nodes are therefore relatively insensitive to SEU effects.

The layout of the memory is shown in Figure 2. The total area of the memory, including the read logic and the address decoders, is 1.18 mm². The memory chip has been fabricated in a 3 metal layer process. No substantial area improvement could be obtained with more metals, as the area is still dominated by the size of the devices in the cells and not by the routing resources.

![Figure 2: Layout view of the memory chip.](image)

The layout of the memory has further been arranged to use a scrambled bit layout, i.e. adjacent bits in a word have not been placed adjacent in the layout, but they are placed far apart in the layout. This avoids that an ionising particle hitting between two adjacent bits could affect two bits in the same word.

The read logic in the memory array does not use sense amplifiers, which could speed up the access time if necessary.

2.2 Shift registers

To better study the SEU phenomena on clocked and unclocked circuits, and to be able to predict SEU rates in LHC for static and dynamic logic, we also integrated a series of shift registers made up of 1024 or 2048 identical flip-flop cells (DFF). The test of such devices is quite simple, and the interpretation of the results is simpler than for more elaborated circuits. Therefore, shift registers represent a convenient test vehicle to understand the SEU mechanisms and to validate procedures developed to estimate the SEU rate in the hadron-dominated LHC radiation environment.

Four different types of DFF, hence of shift registers, have been designed and irradiated to study the SEU. To compare the sensitivity of static and dynamic DFF architectures, we have designed two shift registers composed of, respectively, dynamic and standard static DFF cells. These cells were designed using the minimum transistor size compatible with the requirements of our radiation tolerant layout practice. Two modified versions of the static DFF cell were designed to decrease its sensitivity to SEU. In the first approach, some of the transistors have been designed with a bigger size to increase the node capacitance and the transistor current drive capability ("oversized" DFF cell). In the second approach, the capacitance of the sensitive nodes has been increased by adding a metal-to-metal capacitance on top of the cell ("overloaded" DFF cell). In both cases, the overall size of the DFF is unchanged with respect to the standard DFF.

2.3 Irradiation procedure

Single Event Upset measurements have been performed at the ESA-UCL line of the “Cyclone” cyclotron of Louvain-la-Neuve. Irradiation with both protons and heavy ions took place at room temperature, the particle flux being selected so that the probability to have double errors was always negligible. Figure 3 shows the measurement setup, composed of a mother board, a daughter board, and a laptop PC used as a terminal device.

![Figure 3: Measurement setup for the heavy ion irradiation. For the proton irradiation, the test board was not installed in a vacuum chamber, but in air.](image)
PLD. Two different types of daughter boards were used in our tests, one for the memory and another for the shift registers. The test procedure run by the microcontroller was different for the two structures, as described below.

The test of the memory chips consisted of three phases. During the first phase, the entire memory space was filled up with a pre-selected data pattern. During the second phase no memory access operation was performed. This phase lasted for a predefined time period (1 s). During the third phase consecutive back-to-back read operations were performed and the memory contents were read out and compared with the data pattern originally written. The comparison gave the number of upsets encountered in the memory circuit.

The shift registers were tested in two modes of operation. In the “unclocked” mode, a pattern was pushed into the register at a frequency of 30 MHz, then the clock was frozen for a long time until another train of clock pulses was applied to shift the data out for error detection. In the “clocked” mode, the clock was constantly applied during the whole irradiation test at a frequency variable between 460 KHz and 30 MHz.

For the heavy ion test, the effective Linear Energy Transfer (LET) of the ions could be varied between 6.1 and 74 MeV cm$^2$/mg. This was possible either changing the ion species (Neon, Argon and Krypton were used) or by tilting the circuit of an angle with respect to the incident beam (up to 60$^\circ$). In the heavy ion case, the flux was varied between 5·10$^6$ and 10$^7$ particles/(cm$^2$·s), and the circuits were exposed always at normal incidence.

For the heavy ion test, the effective Linear Energy Transfer (LET) of the ions could be varied between 6.1 and 74 MeV cm$^2$/mg. This was possible either changing the ion species (Neon, Argon and Krypton were used) or by tilting the circuit of an angle with respect to the incident beam (up to 60$^\circ$). In the heavy ion case, the flux was varied between 5·10$^6$ and 10$^7$ particles/(cm$^2$·s).

For each test, with protons or heavy ions, the errors were counted until the desired particle fluence was reached. The ratio of the errors over the fluence, normalized to the number N of memory points (or DFF cells) in the circuit, gives the cross-section value for the given proton energy of heavy ion LET:

\[
\sigma = \text{Errors} / \text{Fluence} \times \text{N}
\]

Repeating the test for different proton energy and for different LET, we could trace the complete cross-section curve that fully characterizes the SEU sensitivity of the circuits under test. The measured points in such a curve are normally fitted using a Weibull function [4]:

\[
\sigma = \sigma_{sat} \left(1 - \exp \left(-\left(\frac{LET - LET_{th}}{W}\right)^S\right)\right)
\]

where $\sigma_{sat}$ is the saturation cross-section, that is the total area of the circuit sensitive to SEU, $LET_{th}$ is the threshold under which the circuit is not sensitive to upsets, $W$ and $S$ are two shape factors.

3. RESULTS AND DISCUSSION

In this chapter, all cross-sections referring to the heavy ion irradiation test are plotted as a function of the effective LET. Such effective LET is calculated in the hypothesis of an 8 µm thick layer of silicon dioxide above the sensitive region. The sensitive region of the circuit is in the silicon itself, and is covered by several layers of silicon dioxide (planarization for metal layers and surface passivation).

3.1 Memory

The memory circuit was irradiated while powered at $V_{dd}=2.5$ V with heavy ions up to an effective LET of about 32 MeV cm$^2$/mg. Even though at the maximum LET used in our test the saturation cross-section was not yet reached, the explored LET region is the most significant for our aims. In fact, to predict the upset rate for a circuit in LHC, we need to have good Weibull fit parameters in the LET region representative of the fragments produced by nuclear interaction of hadrons in silicon. The LET of such fragments do not exceed 15 MeV cm$^2$/mg$^1$.

The cross-section curve measured for the memory chip is shown in Figure 4, where the solid line represents the Weibull curve fitting the experimental points. This curve was drawn writing a pattern of alternate 1’s and 0’s in the memory, but very comparable results were obtained with “all 0” and “all 1” patterns, proving that there is no enhanced sensitivity for either high or low values stored in the memory. This is obvious and expected, as the memory cell actually stores both 0’s and 1’s anyway.

![Figure 4: Cross-section curve for the memory circuit irradiated with heavy ions. The measured points are fitted with a Weibull function (solid line), and the fitting parameters are reported.](image-url)
CMS experiment. The method is based on an extensive simulation work, and we will use it with the hypothesis of a cubic Sensitive Volume (SV) of 1x1x1 μm³. The results of such calculation are reported in Table 1 for different positions in CMS: in the pixel detector (τ=0-0.9, R=0-20 cm), in the outer tracker (τ=0-0.9, R=65-120 cm), in ECAL behind the endcap (R=50-130 cm), in the experimental cavern above the endcap (R=700-1200 cm).

Table 1: Estimate of the upset rate for the memory chip in several positions of the CMS experiment at peak luminosity. The estimated cross-section Σ multiplied for the particle fluence Φ gives the upset rate Φ x Σ (upset/chip-s).

<table>
<thead>
<tr>
<th>Region</th>
<th>Φ x Σ</th>
<th>Φ x Σ</th>
<th>Φ x Σ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>3.4·10⁻⁹</td>
<td>2.0·10⁻⁸</td>
<td>2.2·10⁻⁷</td>
</tr>
<tr>
<td>Outer tracker</td>
<td>2.1·10⁻⁹</td>
<td>2.1·10⁻⁸</td>
<td>2.3·10⁻⁷</td>
</tr>
<tr>
<td>Behind Endcap</td>
<td>2.2·10⁻⁸</td>
<td>6.6·10⁻⁷</td>
<td>1.2·10⁻⁶</td>
</tr>
<tr>
<td>Exp. Cavern</td>
<td>1.4·10⁻⁹</td>
<td>1.2·10⁻⁸</td>
<td>8.2·10⁻⁷</td>
</tr>
</tbody>
</table>

From Table 1, one can see that the upset rate is always dominated by hadrons (including neutrons) of energy above 20 MeV. The contribution from thermal neutrons has been neglected, as it has been shown to be well below that of high-energy particles [5]. The possible exception is for devices with very high boron doping, but the estimate in that case would require the knowledge of the precise doping profile of the chip, which is most often unknown to the designer.

The highest total (> 20 MeV hadrons + 2-20 MeV neutrons) upset rate of 2·10⁻⁹ is found in the pixel detector. If we assume that LHC will run for 5·10⁻⁷ seconds in the foreseen 10 years of its operation, the memory chip will experience a total of about 10000 upsets. In the outer tracker the estimated total number of upsets falls to about 105, behind the endcap of ECAL it is 330, and no upset are expected for this memory in the experimental cavern.

3.2 Shift registers

The shift register circuits have been irradiated with heavy ions and protons in both the “unclocked” and the “clocked” operation mode.

The cross-section curves measured with a heavy ion beam are shown in Figure 5 for the dynamic shift register (clocked mode) and for the standard static shift register (clocked and unclocked mode). The experimental points are fitted with a Weibull curve in all cases. The frequency of the clocked test was 30 MHz.

With the above explained limitation on the confidence level of the Weibull fit, we can use the fitting parameters to estimate the upset rate these shift registers would experience in LHC, as already done for the memory. Also in this case, we will make the hypothesis of a cubic SV of 1x1x1 μm³.

To have a more significant estimate for real ICs integrating a large number of DFF cells, we will make the calculation for a number of 10⁶ cells. The results for the three cases are reported in Table 2. In the clocked mode, the rates for the dynamic DFF are more than two orders of magnitude larger than for the static DFF.

Table 2: Estimate for the upset rate for 10⁶ DFF cells in different positions of the CMS experiment. The estimate is for the total upset rate, including the effects of all charged hadrons above 20 MeV and neutrons above 2 MeV.

<table>
<thead>
<tr>
<th>Region</th>
<th>Dynamic DFF</th>
<th>Static DFF “clocked”</th>
<th>Static DFF “unclocked”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>7.1·10⁻⁹</td>
<td>3.2·10⁻⁸</td>
<td>3.0·10⁻⁸</td>
</tr>
<tr>
<td>Outer tracker</td>
<td>9.7·10⁻⁹</td>
<td>2.5·10⁻⁸</td>
<td>1.8·10⁻⁸</td>
</tr>
<tr>
<td>Behind Endcap</td>
<td>3.1·10⁻⁹</td>
<td>9.5·10⁻⁸</td>
<td>1.1·10⁻⁸</td>
</tr>
<tr>
<td>Exp. Cavern</td>
<td>7.3·10⁻⁶</td>
<td>1.5·10⁻⁵</td>
<td>2.1·10⁻⁵</td>
</tr>
</tbody>
</table>

To verify whether the two modified versions of the static DFF cell, the “oversized” and the “overloaded” cells, have an improved SEU cross-section over the standard cell, we have irradiated them with heavy ions. The resulting cross-sections are reported in Figure 6, where they are compared with the behaviour of a standard static cell integrated in the same test chip. This figure refers to the clocked mode, at a frequency of 30 MHz.
...considered when using these results. This should be a comparison for the dynamic DFF, such estimates might work have been done for a cubic SV. According to the estimates for the LHC environment presented in this work, the necessary simulations for such SV size are not at present available, and all the estimates. Nevertheless, the necessary simulations for such SV size leads to more reliable assumption of that SV size. It appears that the 1x1x0.5 µm, the under-estimate reduces to a factor of 2 only, which is quite a satisfying result also when considering the SEU sensitivity is higher at lower Vdd. If we compare the experimental cross section at 2.5 V with the estimate obtained from the Weibull parameters of the fits in Figure 5, we observe that the estimate is a factor of about 4 lower when we assume a cubic SV of 1x1x0.5 µm. When the SV thickness is decreased to 0.5 µm, the under-estimate reduces to a factor of 2 only, which is quite a satisfying result also when considering the already discussed poor quality of the fit in Figure 5. It appears that the 1x1x0.5 µm is a better guess for the sensitive volume in this technology, and that the assumption of that SV size leads to more reliable estimates. Nevertheless, the necessary simulations for such SV size are not at present available, and all the estimates for the LHC environment presented in this work have been done for a cubic SV. According to the comparison for the dynamic DFF, such estimates might actually under-estimate the real rate. This should be considered when using these results.

Figure 6: Measured cross-section for the different static DFFs irradiated with heavy ions in the clocked mode.

The modified cells are less sensitive to SEU than the standard DFF, with the “oversized” solution being the most effective. This cell pays a penalty in terms of speed and power consumption, but it still easily complies with most of the applications in ASICs for LHC, where a speed of 40 MHz is a standard requirement. The use of the Weibull fit parameters to estimate the upset rate for these cells in LHC reveals that the upset rate for the “oversized” DFF is almost a factor of 2 lower than for the standard DFF, this factor increasing to 10 for the “overloaded” cell.

To understand how precise are all the above estimates for the LHC environment, we can use the same method to estimate the upset rate for a proton beam irradiation. This estimate can then be compared to the experimental results. We have irradiated the dynamic and the standard static shift registers with a proton beam, and varied the energy of the incoming protons between 10 and 60 MeV. The measured cross-section curve as a function of the proton energy is shown in Figure 7 for the dynamic register clocked at a frequency of 30 MHz. The cross-section gets lower when the power supply voltage is decreased to 2 V, in contrast with the common idea that the SEU sensitivity is higher at lower Vdd. If we compare the experimental cross section at 2.5 V and power supply voltages in the clocked mode.

4. CONCLUSION

SEU cross-sections have been measured for a 18Kbit dual-ported static RAM and for a set of test shift registers. From the Weibull curves fitting the experimental points, the upset rates for such circuits in the LHC radiation environment have been estimated. The heavy ion irradiation of the memory has revealed a LET threshold of about 5.4 MeVcm²/mg, higher than for most state-of-the-art commercial SRAMs [6]. We have estimated for such chip an upset rate in LHC varying between 2.10⁻⁻ and 1.2.10⁻⁻ errors/s, respectively in the pixel detector and in the experimental cavern. Measurements with both heavy ions and protons have confirmed that dynamic DFF architectures are at least two orders of magnitude more sensitive to SEU than static ones in the LHC environment. Simple approaches with no area overhead are effective in decreasing the sensitivity of the static DFF cell. In particular, the implementation of an additional metal-to-metal capacitance to load the sensitive nodes has lead to a tenfold decrease in the SEU sensitivity.

REFERENCES

The HERA-B Level 1 Trigger

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Abstract

The HERA-B experiment at DESY, Germany, analyzes interactions of 920 GeV protons with a fixed target to measure CP violation. The described HERA-B First Level Trigger has to process, in real-time, about $10^5$ channels of detector data which are read out every 96 ns. At a latency of at most 10 µs, it has to reduce the 10 MHz event rate by at least a factor of 200. To determine possible particle trajectories it applies a Kalman filter inspired track search method. The tracking can be initiated by one of three independently working pretrigger systems that also provide particle identification. The trigger decision is based on the momenta and masses of reconstructed track pairs.
1 Introduction

The HERA-B detector is designed to observe CP violation in the B-meson system. The experiment, located at DESY, Hamburg, will initially investigate the decay $B^0 \rightarrow J/\psi K_S^0$, the so called Golden Decay. This will be followed by probing other B-decays. The trigger is highly specialized for finding $J/\psi$'s coming from the detached vertex of a B, but it also needs to be flexible enough to incorporate future extensions of HERA-B's physics program [1] [2] [3].

Bottom mesons are produced by inserting thin wire targets into the halo of HERA's $^2$ 920 GeV proton beam. On average one in $10^6$ interactions contains $b$ quarks. In addition, the branching ratios of the rare decays of interest are of order $10^{-5}$. In order to produce a large number of $B$ mesons the interaction rate$^3$ will be 40 MHz. The huge background, but also the large number of detector channels and high event rate, makes HERA-B triggering a special challenge.

Therefore, an efficient, highly selective trigger and a high bandwidth, low latency data acquisition system had to be built. The pipelined trigger system consists of four different levels. The First Level Trigger hardware consists of custom made electronics. All higher level triggers are implemented as commodity PC farms [4].

The initial trigger strategy of HERA-B aims to find $J/\psi$'s from the Golden Decay already in the First Level Trigger (FLT). In 12% of the cases a $J/\psi$ decays into two leptons of opposite charge. The FLT uses this signature and looks for charged tracks in the field free region downstream of the magnet, see Fig. 1.

Extensions of the physics program may require to trigger on high-$p_T$ hadrons. In such cases the First Level Trigger can demand that the event data contain hadrons with large transverse momentum [5].

2 Trigger Scheme

The $J/\psi$ candidate is identified through two opposite charge electrons or muons having an invariant mass consistent with the mass of the $J/\psi$. The FLT reconstructs the lepton tracks, then, measuring the respective momenta and charge, it determines the di-lepton invariant mass. The FLT starts from track seeds provided by a pretrigger. Its tracking algorithm utilizes detector data of the tracking chambers. For an overview of the connection between the FLT and the HERA-B detector, please, refer to Fig. 1.

In total there are three pretrigger systems. The muon pretrigger uses the hit information of the cathode pad chambers of the last two superlayers of the muon system. The electromagnetic calorimeter (ECAL) measures the energy that is deposited in its cells. The ECAL pretrigger electronics sums up the energy of all three by three cell arrays. The energy sum of these groups of nine cells are called cluster energy. Based on a programmable ECAL cluster energy threshold a pretrigger is generated. In addition to this energy threshold there is also the possibility to flag pretrigger candidates with energies above a second much higher cluster energy. ECAL trigger candidates with the higher cluster energy are assumed to be hard photons. This provides an extension to the di-lepton trigger scheme, since it allows triggering on photon decays as well.

The third pretrigger type is directed at finding hadrons with large transverse momentum. The high-$p_T$-pretrigger uses three layers of pad chambers located inside the magnet. This pretrigger can, for instance, trigger on the decay $B^0 \rightarrow \pi^+\pi^-$, or on hadrons from $B_s$ decays and opens the door to study rare $B$ decays [5].

The three pretriggers work in parallel and independently. If a suitable candidate is found, this information is passed on to the FLT. A demanding task of the FLT is to perform very fast online tracking. It uses a Kalman filter inspired method and reconstructs tracks in the field free region, see Fig. 1, using a subset of tracking chambers of the inner tracker (MSGCs), the outer tracker (honeycomb drift chambers), and the muon tracker (tube chambers, gas pixel
chambers) [3]. A hit in every trigger tracking layer is required; an electron, for example, has to be detected by 12 detector layers of four superlayers. A very high detector efficiency is therefore obligatory. Once tracks are reconstructed, their kinematical parameters and the invariant mass of track pairs are determined by the FLT and the trigger decision is derived from these measurements [6].

Using a complete detector and trigger simulation the trigger efficiency was determined. The reconstruction efficiency was found to be 35% for the decay $J/\psi \rightarrow e^+e^-$, 55% for $J/\psi \rightarrow \mu^+\mu^-$, and 28% for $B^0 \rightarrow \pi^+\pi^-$ [7]. These values include the geometrical acceptance of the detector.

3 Hardware

3.1 Implementation

For the design of the FLT several constraints were taken into account. The FLT input rate is close to the proton bunch crossing rate of 10.4 MHz, its output rate should be at most 50 kHz, which is the allowed input rate of the Second Level Buffer. The Second Level Buffer stores all detector data for an event that has passed the FLT trigger criteria until the second level trigger process has decided on rejecting or keeping the event [4]. Therefore the nominal suppression of the FLT must be 200 for all combined trigger channels. Another requirement is that the data transfer to the FLT and pretrigger and decision making must be accomplished within a maximum latency of 10 $\mu$s. This limit is given by the depth of the memory pipeline, which is used for the intermediate storing of data by the detector front end electronics and the data buffers of the FLT itself. A large number of boards had to be designed and built, see Tab. 1.

The pretrigger electronics of the muon and high-p_T systems has a modular structure and consists of three types of boards: a Pretrigger Link Board, a Pretrigger Board, and a Pretrigger Message Generator. The Pretrigger Link Boards are located inside the Front End Driver crates very close to the detector. They transmit the digital data of the detectors to the Pretrigger Boards. In order to achieve this, the electronic signals are serialized by an Autobahn spaceceiver, which is a 32 bit parallel to serial transceiver with an effective data rate of 800 Mbit/s. The serial electronic signal is converted to an optical signal by an optical transmitter board [8]. They are piggy back boards mounted onto the Pretrigger Link Boards, which can easily be replaced in case of failure. Each Link Board has six to eight of such optical links installed. The data are transmitted via a $\approx$60 meter long optical fiber to the Pretrigger Boards. Using optical signals assures a noiseless transmission and a clean ground separation. At the receiving end the optical signals are converted back to electrical signals by a piggy back transmitter module and are parallized back by another Autobahn spaceceiver.

The Pretrigger Board uses the data to detect coincidences between two or three detector superlayers for the muon and the high-p_T system, respectively. The trigger algorithm is programmed into EPLDs$^5$. This feature provides easy up-grade paths for changes in the physics program. If an appropriate trigger condition is fulfilled the parameters of the trigger seed are determined and are converted by a Pretrigger Message Generator to an 80 bit FLT message. The FLT messages contain the complete information of any given trigger candidate. The Pretrigger Message Generator sends it to an FLT Track Finding Unit (TFU) and the FLT processing is started. A detailed description of the pretrigger electronics of the muon system is given in reference [9] and an in depth description for the high-p_T pretrigger electronics can be found in these proceedings [10].

The electronics boards of the ECAL pretrigger are placed very close to the ECAL Front End Driver boards. The data are transmitted via copper cable to the Pretrigger Boards. Data processing and message generation is integrated into just one board. Up to 16 ECAL pretrigger boards are placed into one crate. Each crate has one interface board which sends ECAL trigger seeds to the TFUs. The interface board also arbitrates the message traffic coming from the Pretrigger Boards within one crate.

The TFU network has to process two orthogonal data streams. The pretrigger systems initiate a data flow from the TFUs associated with detector planes far from the target towards TFUs connected to detector planes close to the target (from left to right in Fig. 1). This data flow is heterogeneous distributed over the processing units and is asynchronous with respect to the bunch crossing rate of the experiment. The local data rate is a function of time, physics of the given event, and topology of the processor network. The

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Table 1: Overview of the custom made electronics boards of the FLT and pretrigger system. The FLT has to process over $10^5$ detector channels which are read out every 96 ns.

<table>
<thead>
<tr>
<th>Optical Links</th>
<th>Link Boards</th>
<th>Pretrigger Boards</th>
<th>Interface Boards</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECAL</td>
<td>n/a</td>
<td>128</td>
<td>9</td>
</tr>
<tr>
<td>MUON</td>
<td>400</td>
<td>40</td>
<td>20</td>
</tr>
<tr>
<td>hi-p_T</td>
<td>1100</td>
<td>80</td>
<td>8</td>
</tr>
<tr>
<td>FLT</td>
<td>3400</td>
<td>200</td>
<td>n/a</td>
</tr>
</tbody>
</table>

$^5$Electronic programmable logic device

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Motorola MC100SXI451
second data stream is constant and synchronized by the bunch crossing clock of 10.4 MHz (from top to bottom in Fig. 1). The data is collected by detector Link Boards [11] and is sent via optical links to the TFUs using the same data transmission piggy back boards which have been described for the muon and the high-pT pretrigger systems. The Link Boards are used to “map” the detector onto the FLT network.

The trigger seed of the pretriggers initiates the track finding chain by providing the initial measurements of the particle’s location and direction. This information is used to determine a Region-of-Interest (RoI) for the tracking layer that is used by the TFU (Fig. 2). Each TFU is assigned to a fixed detector region. Even though the TFU network needs to store about $7 \cdot 10^4$ input bits every 96 ns, only a small subset of the data, 1.2 k bits, is stored by each TFU. Out of the 1.2 kbits only a maximum of 100 bits make up an RoI and are used for the individual measurement of a given TFU.

The detector input data rate for one TFU is 16 Gbit/s. In addition, the TFU also receives FLT messages from pretriggers or other TFUs. For short bursts it can receive up to 12 Gbit/s through this channel, see Tab. 2.

The core of the TFU is a “hit finder”, which looks for triple coincidences from three layers of detector wires strung at three different orientations. Once a hit (triple coincidence) is found, this information is combined with previous measurements, the track candidate is extrapolated to the next tracking layer, and the RoI at the following layer is determined. The parameters of the RoI are also influenced by kinematical restrictions, multiple scattering, and the projectivity of the track. By each subsequent hit determination the track measurement is refined. Once the track is reconstructed in all FLT detector superlayers, it is used to determine the charge of the particle and its momentum. This calculation is performed by the Track Parameter Unit (TPU). The TPU is essentially a fast, look-up table based calculator. It also is able to reject duplicated tracks. They can, for example, be generated in overlap regions of different tracking systems.

After the kinematical reconstruction the result is sent to the Trigger Decision Unit (TDU).

The primary function of the TDU, for a photo see Fig. 3, is to form the trigger decision. Typically the TDU will receive tracks from four different TPUs. Tracks that do not fulfill latency requirements are rejected. The remaining tracks are stored in a local message memory. A data processing unit combines tracks belonging to the same bunch crossing to determine their invariant mass. This is done for all possible track pairs. The final FLT decision is based on any combination of two tracks of a given particle ID, charge, momentum, transverse momentum, and invariant mass. In addition, triggers can be initiated based on count conditions, e.g. track multiplicities, according to particle ID of several combinations of one or two tracks.

In case of a positive FLT trigger decision the respective bunch crossing number is sent to the data acquisition system. The data acquisition distributes the trigger decision to all the Front End Drivers of the detector, which subsequently transfer the complete data.

![FLT Track Finding Unit](image1)

**Figure 2:** The FLT Track Finding Unit. Ten such 9U VME boards are housed in each crate. In total 74 TFUs are needed.

![FLT Trigger Decision Unit](image2)

**Figure 3:** The FLT Trigger Decision Unit. Also visible four subcards which perform the calculation of all possible pair masses of a given event.

**Table 2:** FLT data throughput. One individual TFU can process up to 4 Gbit/s trigger candidate data, however it can buffer short bursts of up to 12 Gbit/s.

<table>
<thead>
<tr>
<th></th>
<th>detector input</th>
<th>candidate input</th>
<th>TFU output</th>
</tr>
</thead>
<tbody>
<tr>
<td>single TFU</td>
<td>16 Gbit/s</td>
<td>12 Gbit/s</td>
<td>2 Gbit/s</td>
</tr>
<tr>
<td>entire FLT</td>
<td>1.2 Tbit/s</td>
<td>0.6 Tbit/s</td>
<td></td>
</tr>
</tbody>
</table>
set to the Second Level Buffer. The TDU also transfers the complete record the FLT tracks accompanied by the trigger type to the Second Level Buffer. The results of the FLT tracking are used as starting point for the higher level triggers and the measurement is subsequently refined under less stringent latency requirements.

3.2 Commissioning Status

At the time of the workshop the hardware of the complete system, including the respective pretrigger systems, had been designed, prototypes had been built and the series production was under way.

The electronics of sub-systems were tested by the developing groups, i.e. reliable inter board communication was established and board functionality checked. In addition, several system integration tests of components at the experiment had been performed. In those tests the operation of the interfaces between sub-systems was established.

The FLT without tracking had also been used to provide a physics trigger for the experiment. About a third of the pretrigger system of the ECAL had been installed and operated. Based on the multiplicity of the number of ECAL candidates a trigger was initiated. Data had been written to tape for offline analysis.

TFUs were operated in stand alone mode to establish their operation in the experiment. They were connected via Link Boards to the various trackers. It was shown that the data received by the TFU was identical to the data written to tape. The TFU was programmed to look for hits in a fixed RoI. Also this could be accomplished for the various detectors. The installation of all electronics board is on going and it is planned to complete the trigger by the end of this millennium.

4 Acknowledgments

The trigger system described in this document is the result of the contribution of many members of the HERA-B collaboration.

References

[10] H. Riege et al., The HERA-B High-\(p_T\) Level-0 Trigger logic electronics, proceedings to LEB99
PRELIMINARY IRRADIATION TESTS OF THE APVD CIRCUIT FOR THE CMS TRACKER

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ABSTRACT

The APVD circuit, developed in the 0.8µ radiation hard SOI DMILL technology [2][3][4] from ATME⁄TEMIC-MHS Nantes, for the front end electronic of the CMS tracker, has been irradiated at CERN using a 10KeV Xray beam up to a total dose of 20Mrad. The main performances of the APVD like gain, pulse shape, noise are presented as a function of the radiation dose. In particular the cause of the DAC non linearity in the bias generator part is discussed.

1. INTRODUCTION

The APVD circuit is a 128 channels CMOS analogue pipeline readout ASIC intended to be used on the CMS tracker. This mixed signal circuit is developed into two derived products, the APVD_AC version (the default version) and the APVD_DC version. Those two circuits mainly differ from the front end part. Whereas the AC version is dedicated to AC coupled Silicon detectors or MSGC detectors, the DC version concerns mainly the DC coupled Silicon detectors.

This DC version circuit contains an additional circuitry intended to compensate for the Silicon detector leakage current.

The level of hardness required on the central tracker sub-detector section makes the DMILL technology [2][3][4] use an inevitable choice.

1.1 APVD Chip Overview

The circuit functionality and architecture is well described in [1] and [5]. We just give there a quick overview.

The circuit consists of a 128 preamplifier-shaper array followed by a 128x160 analogue memory operated at 40MHz. A data access mechanism allows the marking and queuing of requested memory location for output processing. The output processing is made by a switched capacitor network which deconvolutes signal off the 50 ns shaping. An output multiplexer ensure the serialisation of the analogue data onto a unique output. Other control functions such as I2C slow control communication interface, programmable bias generator, internal calibration and error checking are also included on this circuit.

141 analogue I/O
19 digital I/O
Chip size : 12 x 6.24 mm
Supplies : +/- 2V
package : hybrid report

fig 1 : APVD chip overview

2. EXPERIMENT DESCRIPTION

2.1 Irradiation conditions

The irradiation test have been carried out with the 10KeV X ray beam at CERN. The advantages of such equipment for circuit radiation level estimation are numerous [6][7] :

- Dose rates ranging from $10^2$ up to $10^5$ rad/min
- No residual activation after exposure, due to the low energy level involved.
- Test set up simplicity (the radiation can be located on a region of the PCB)
- Short test duration and low cost

The obvious constraint is the obligation to use non-closed package, in order to have direct access to the top surface of silicon.
A couple of APVD chips, run 04/98 directly bonded on a PCB have been irradiated under the following conditions:
- Distance between X ray tube and top die : 30 mm
- Dose rate : 15Krad/minute
  (High voltage : 40 KV ; current : 28 mA)

2.2 Test Bench Description

The hardware bench is illustrated in fig2a. It is based on a full automated system driven by a PC through LABVIEW.

The APVD mother board is introduced into the X ray machine and is linked to the external world by a set of cables of approximately 4 meters long. The APVD driving capability is limited in the I2C output, and doesn’t allow the use of such a cable length. An additional buffer has been introduced on the mother board in order to overcome this problem. This mother board is driven by a SEQSI sequencer, in conjunction with an I2C board (clock, trigger, and slow control). All the measurement instruments are driven by LABVIEW via the GPIB and VXI (MXI-2) buses.

2.3 Measurement sequence description

The acquisition for the measurement is shown in fig2b.

The radiation dose rate was set at 15Krad/min. A complete measurement was done each 22 minutes, which gives approximately 330Krad per step. At each step the following measurements were recorded:
- Shape reconstruction under nominal bias settings with external charge injection, in peak mode.
- Noise figures,
- Bias generators DAC transfer function.

3. EXPERIMENTAL RESULTS

3.1 Peak Mode Readout Shape

Fig 3a shows the effect of radiation on the pulse shape in peak mode for a 3Mips input signal. It can be noticed that the peak amplitude decrease slowly with the radiation dose from 88mV at 0rad down to 65mV at 20Mrad. The peaking time increases slightly with radiation dose from 50ns at 0rad up to 59ns at 20Mrad. The shape tail also tends to increase with radiation dose.

The shape distortion is the result of the shift of electrical characteristics on elementary devices mainly transconductance (Gm) and voltage controlled feedback resistors in the preamplifier and in the shaper. During radiation those two characteristics are affected twice - by the mobility reduction effect - and by the bias condition changes. As will be shown in the bias generator current plots, in 3.3, the circuit bias conditions are not intrinsically the same at each measurement step, and cause additional shifts on the OTA operating point.

It is important to note that: although the external bias I2C settings had remained the same during the
irradiation test, the internal biases were not stable, due to the radiation effect on the bias generator function itself.

In the real application, this will be possible to compensate for the radiation effect on the bias generator and, up to a certain extend, for the radiation effects on the pulse shape. This is the role of the slow control functions.

3.2 Noise Figures

Noise Measurement Method

At each radiation step the baseline noise for all channels is recorded with no input signal applied to any of the channel for 500 consecutive triggers. Then the pedestal noise of a peculiar channel is measured taking 50 samples over 25ns. From the pedestal noise voltage the common baseline noise is substracted to give the inherent RMS noise of the channel. The noise in ENC electrons is then calculated from the extracted channel gain which is itself calculated at each radiation step with a known pulse injection.

Noise Measurement Results and Comments

The simple estimation of the noise performance degradation under irradiation is not easy to achieve. On one side an 1/f noise spectral density increase is expected, and on the other side the Gm of the preamplifier input device should decrease whereas the time constant $\tau$ of the CR-RC shaping should increase.

In fact, the variation of $\tau$ is small compared to the gm degradation, so the $1/gm$ coefficient should dominate in the ENC formula:

$$\text{(ENC)}^2 = \frac{e^2 C_{\text{sensor}}^2 KT}{3 gm \tau}$$

The ENC versus radiation dose curve is plotted on fig 3b. It corresponds to the ENC in peak mode with a 1pF input capacitor. A quasi linear increase of the noise can be noticed in the range 0-20Mrad with a slope of around 32 rms electrons per Mrad.

As mentioned before, those measurements have been done without bias correction during radiation which is, in fact a worst case estimation.

It is interesting to note on fig 3c that after 24hours of recovering at ambient temperature the ENC falls to around 800 electrons.

3.3 Bias Generator

Two bias generator channels of the 11 used in the AVPD chip have been characterised these are the IPRE current channel and the VPRE voltage channel. These generator outputs are reachable via special test pads. Thanks to the I2C slow control it is possible to register...
the digital to analogue transfer function of the bias generator internal DAC.

It is important to keep in mind the measurement acquisition flow chart (fig2b) for further understanding on the radiation effect on the current DAC. That is a fixed digital value was loaded into the data register during most of the radiation exposure duration. The data register was scanned over the full range only during the DAC transfer function acquisition whose duration is negligible compared to the duration of the rest of the loop. Two different values were set into the IPRE data register and the VPRE data register, the values which produce the optimal shaper output wave form at 0rad:

- IPRE data = 55 \rightarrow \text{IPRE} = 230\mu\text{A}
- VPRE data = 255 \rightarrow \text{VPRE} = -0.7\text{V}

### 3.3.1 IPRE DAC channel

The IPRE DAC transfer function is plotted on fig 3d. This plot reveals two important things; the existence of steps on certain digital code positions and a continuous step height increase with radiation dose.

![fig 3d: IPRE DAC transfer function](image)

These phenomenon are clearly understood and are the result of different threshold voltage (Vt) shifts on the elementary devices which compose the DAC. This lack of robustness can be corrected by a small design change and is further discussed in chapter 4.

The IPRE DAC channel non-linearity at 10 Mrad is plotted on fig3e.

### 3.3.2 Is non-Linearity a Real Problem for the Application?

During LHC operation it will be possible to tune the circuit bias in order to optimise the readout shape and to reach the highest possible S/N ratio. The biases programmable capability is the key element for this tuning. A moderate resolution DAC architecture can fully match this tuning requirement. That’s why the DAC used in the bias generator function are designed with economical means.

Anyway, the differential non linearity must however be kept in a reasonable range (ie, 2 to 3 LSB at maximum). As can be seen on fig 3e, the apparent step of \#60\mu\text{A} at the digital values 64, 128, 194…, corresponds to around 15LSB. That is, in those regions, the DAC resolution is 15LSB which is more than the allowed non-linearity range.

In the next APVD run, the DAC design will be modified in order to reach the non-linearity limit of 2 LSB.

### 3.3.3 VPRE DAC channel

The voltage DACs is made of the same current mode DAC bloc that composes the current DAC. For the voltage to current conversion P+ resistors are used via sink or source current mirroring depending on the voltage polarity required.

Thus one could expect that the bias generator voltage should reveal under irradiation the DAC current imperfections and in addition the P+ resistor variation. In fact this last term is small (<5%) thanks to the high doping level of this resistor.
The VPRE voltage transfer function is plotted in fig 3f.

We can notice an obvious transfer function slope variation with radiation dose, but curiously, the non linearity and the curve steps differ completely from the IPRE DAC current counterpart. That is, the VPRE voltage DAC seems to be far more robust to radiation than the IPRE DAC. This result is in fact deceitful because the voltage DAC was into a peculiar state during radiation exposure (VPRE data register set at the value 255).

The data register initial setting is responsible for this difference in the DAC behaviour. Let’s consider the key elements:

- In the VPRE DAC, the data register was full range (data=255) in this case all the elementary transistors that compose this DAC were in the same ON state, and thus have exhibited matched Vt shifts.
- In the IPRE DAC, the data register was somewhere between zero and full range (data=55), in that case, some devices were ON while others were OFF, and thus the ON transistors and the OFF transistors have exhibited different Vt shifts.

Concerning the transfer function slope change, it has two origins:

- Small P+ resistor value variation with radiation dose
- Layout configuration; the master chip reference current function is situated far away from the front end and from the DAC arrays. The X ray beam was rather centred on the front end part, and this reference current function has been probably irradiated differently than the front end part due to non homogeneity effect on the beam itself.

4. DESIGN ASPECTS

This chapter describes the present current DAC architecture, the cause of degradation under irradiation, and the design modifications implemented in the next version.

4.1 Current DAC architecture

The basic principle of conversion is illustrated on fig 4a. The DAC comprises a eight bit digital data register and eight weighted current generators. Each current generator delivers a known current, which is a multiple ratio of the reference current Iref. This built-in current ratio depends on the current mirror weight. Each current generator are individually switched ON or OFF by the data register corresponding bit.

The output current expression can be written as:

\[
I_{OUT} = I_{REF} \left(128 \times b_7\right) \left(64 \times b_6\right) \left(32 \times b_5\right) \left(16 \times b_4\right) \ldots \left(8 \times b_3\right) \left(4 \times b_2\right) \left(2 \times b_1\right) \left(1 \times b_0\right)
\]

Concerning the transfer function slope change, it has two origins:

- Small P+ resistor value variation with radiation dose
- Layout configuration; the master chip reference current function is situated far away from the front end and from the DAC arrays. The X ray beam was rather centred on the front end part, and this reference current function has been probably irradiated differently than the front end part due to non homogeneity effect on the beam itself.

4.1.1 Why is this Architecture not Rad Hard Enough ?

The effect of the radiation on the MOS devices is an ageing effect which is to modify their threshold voltage Vt. This is mainly due to the mechanisms of trapping charges in the gate oxide and is directly connected to the quality and the thickness of the oxide. Moreover, the charge trapping mechanism in the gate oxide is also
dependent on the biasing conditions. That is to say that two identical MOS devices biased at two different gate to source voltage do not exhibit the same Vt shift after radiation exposure.

4 dev 32 dev 8 dev 16 dev 64 dev 128 dev

$I_{out}$

$I_{ref}$

$b_0$ $b_1$ $b_2$ $b_3$ $b_4$ $b_5$ $b_6$ $b_7$

fig 4b : present DAC practical realisation

That’s exactly what happens in the DAC shown on fig4b. In the case where the data register takes the value $00$ or $FF$, all the transistors which compose the current mirrors are in the same bias condition. In contrast, for all other data register values, some devices are ON whereas others are OFF. It results that if the DAC is exposed to radiation in this last condition (data register somewhere between $00$ and $FF$) that damages the matching between the different current mirror raw. This mismatching effects cause non linearity and produce steps on the DAC transfer function This is clearly illustrated on fig 3d. The IPRE channel DAC transfer function, with a data register set at $37$ during radiation exposure, exhibits steps. In contrast, the VPRE channel DAC, with a data register set at $FF$ during radiation exposure, reveals no steps.

4.2 New proposed structure

In order to overcome the radiation damage on the DAC, we propose the following design modifications, fig 4c.

In this new scheme, the gate to source voltage remains identical on all the elementary devices whatever the data register value is. The current source raw selection is now done by switching the drain of the devices. When a current source is called to be ON, it is switched to the output node, and when it is asked to be OFF its output drain remains open.

4 dev 32 dev 8 dev 16 dev 64 dev 128 dev

$I_{ref}$

$b_0$ $b_1$ $b_2$ $b_3$ $b_4$ $b_5$ $b_6$ $b_7$

fig 4c : New DAC realisation proposed

The switches in the different current mirror outputs have finite ON resistance and, at high current, can cause DC errors in the digital to analogue transfer function, by the so-called Early effect. So, all switches are not designed with the same geometry. The switch size is adapted to the output current scale in order to produce the same voltage drop on each current mirror output.

4.2.1 Residual non Linearity Effects

Very little steps can, nevertheless, be observed on the DAC transfer function before radiation exposure. This residual effects are due to the mirrors array layout themselves:
• The different current mirrors are basically of different size and are not all closed to the master current source reference transistor.
• It has not been possible, for layout constraints, to draw each mirror with dummy devices.

5. CONCLUSIONS

These preliminary radiation test results on the APVD_AC version are encouraging. The circuit is still fully functional after 20Mrad. This confirms the hardness of both DMILL technology and the APVD design.

Some design weaknesses have been pointed out and corrections have been implemented in the new APVD version, now under foundry processing.

A more complete radiation hardness characterisation will be needed on the final product in order to guaranty the product quality for the LHC.

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REFERENCES

Noise contribution to timing with fraction discriminators

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Abstract
The noise contribution to timing with pulse discriminators processing a fraction of the detector signal amplitude is discussed. The types of discrimination techniques under study do not produce theoretical walk for varying amplitude signals with equal shapes. They are suitable for implementation in the readout of time of flight (TOF) system and tracker. The utilization of the pulse discrimination methods in the nanosecond range with low-noise front-end may require tentative search of the processor parameters to achieve better time resolution. Simulation methods that provide rapid and consistent evaluation of front-end noise contribution to the time resolution are discussed.

Introduction
The interest to on-chip realization of a pulse discriminators that employ constant or double signal fraction in large readout system for a collider experiment requires elaboration of evaluation methods of front-end noise contribution to timing. The choice among one or another realization of constant fraction discriminator (CFD) [1] or double fraction discriminator (DFD) [2] has to be done. Another motivation behind the presented study is to provide a designer with a reliable estimation of time resolution before the designing of a signal processor circuit starts. In this study a semi-analytical approach in evaluation of electronic noise contribution to time resolution is developed. The timing variance may be simulated by implementation of a macro and a goal function within the waveform analyzer of SPICE simulator for any of the above discriminators. Universality of the approach to the timing variance evaluation is outlined. The proposed evaluation principle provides a possibility to bypass a bulky procedure of carrying out parametric analyses of numerous runs with circuits representing delay lines (or their substitutions), fraction and signal difference otherwise needed to analyze time resolution dependence on the signal processor parameters. The simulation results are compared to the measured data for one front-end.

Signal processor modeling
Figure 1a shows usual representation of a processor involving CFD used in timing measurements. The signal is represented by a current source I(t) connected in parallel to the detector capacitor. For the noise analysis the front-end is represented by a two-port with transfer function $A_1$ and equivalent noise generators of series and parallel noises at the input. Whatever the noise generators are the electronic noise may be described by voltage fluctuations with spectral density $S(f)$ at the input node of a processor part representing CFD (the input impedance of discriminator is usually 50 Ohm). Positive polarity for the branch of fraction and inversion for the branch of delayed signal are assumed in Figure 1. The final results are independent of simultaneous signal polarity inversion for the branches of delay and fraction in CFD representation (such representation may also be found in literature). The arming provides a low limit for the range of processed amplitudes triggering the "enable" input of the comparator used for zero crossing detection. The level for arming is normally well above three standard deviations of the signal amplitude fluctuations at the discriminator input. First in this study only "true constant fraction timing" [3] is considered to simplify the discussion. Therefore the amplitudes of the signals at the input of CFD are assumed to depend only on the detected signal charge $Q_{in}$; the shapes of the signals are equal. Let us write an expression for the signal waveform at the input of CFD as:

$$V(t) = E\phi(t), \quad (1)$$

where $\phi(t)$ is the waveform of the response corresponding to some reference charge (or energy) detected, $E$ is a factor of proportionality for the reference amplitude. For the processor schematically presented in Figure 1a the timing variance due to the
electronic noise contribution may be expressed as follows:

$$\sigma_i^2 = \frac{\sigma_N^2}{E^2} \left| (\alpha \phi(t) - \phi(t - \tau)) \right|^2_{t=t_Z}, \quad (2)$$

where electronic noise variance is divided by the square of the signal slope at the moment of zero crossing $$t_Z$$. The denominator in equation 2 takes into account the difference of the input signal of CFD delayed by $$\tau$$ and the fraction $$\alpha$$ of the non-delayed signal.

Electronic noise at the input of CFD may be associated with stochastic train of the impulses with the waveform $$\phi(t)$$ randomly distributed in time domain. The spectral density $$S(f)$$ of this noise may be represented by [4]:

$$S(f) = 2\lambda |F(\psi(t))|^2, \quad (3)$$

where $$\lambda$$ is a coefficient responsible for the intensity of the stochastic train, $$F$$ designates Fourier transformation and the factor 2 appears as a result of transfer to the domain of positive frequency $$f$$. The transfer function of the noise impulse to the input of zero crossing detector is the same as for the signal, i.e. the noise waveform $$\phi_N(t)$$ at this node may be defined by the expression:

$$\phi_N(t) = \alpha \psi(t) - \psi(t - \tau), \quad (4)$$

where $$\tau$$ is delay of CFD. Therefore noise spectral density at the input of zero crossing detector may be presented by the expression:

$$S_N(f) = 2\lambda |F(\psi(t))|^2 |(\alpha - \exp(-j\omega\tau))|^2, \quad (5)$$

Noise variance at the input of zero crossing detector is the integral of the above spectral density over the full frequency band. The variance may be represented as follows:

$$\sigma_N^2 = \int_{-\infty}^{\infty} S(f) (\sin^2(2\pi\tau) + (\cos(2\pi\tau) - \alpha)^2) df \quad (6)$$

The last expression characterizes noise variance in timing with CFD. The correspondence of the expression 6 to the result obtained in time domain may be recognized from formula given in [5].

**Application of the model**

The model discussed was utilized in the simulations of noise contribution to timing measurements with an improved version of the spectrometry front-end [6], the essential details of that are shown in Figure 2. The detector is represented by a capacitor $$C_d$$ of 1000pF to approximate large area Si photodiode used in real application. PSPICE circuit simulator is used in the simulations discussed below. In order to find noise variance $$\sigma_N^2$$ the spectral density $$S(f)$$ at the input of CFD is to be determined. Having found noise spectral density $$S(f)$$ in only one simulation run of noise analysis in PSPICE, the variance at the zero crossing detector node may be evaluated with waveform analyzer Probe for any parameters of fraction and delay according to expression 6. In the presented modeling, $$\sigma_N^2$$ is simulated by implementation of a macro in which the parameter of delay is scanned for each fraction parameter of interest. This approach allows us to obtain full information about noise at the input of zero crossing detector after only one simulation run by using command files with macros corresponding to expression 6.

For the noise simulations the models of the for the shaper operational amplifiers were constructed to fit the specifications of their noise figures, the other models are taken from the supplement library. Figure 3 present plots of noise variance as a function of delay for three parameters of fraction. The noise variances are simulated for two gain factors of the filter-amplifier. Different dependencies of the noise variances $$\sigma_N^2$$ on delay with a fixed parameters of fraction were stored in different files. These data were used in the second simulation run (in the equivalent voltage sources of pwl form [7]) in the time domain transient analysis for the simulations of time resolution. For the time domain simulations the macro corresponding to the denominator of expression 2 is derived for current stimulus representing the detector signal shape ($$\delta$$-shape in our discussion). The amplitude of the stimulus corresponds to charge (or energy) detected. The slope at the instant of zero crossing is defined by a goal function implementation in Probe (see appendix). Simulated time resolution dependencies on CFD delay are presented in Figure 4. Each curve in Figure 4 corresponds to fixed parameter of fraction. Time resolution dependencies in this figure are normalized to 1 MeV energy deposition in Si detector. The shape of the front-end response obtained in the time domain simulations corresponds to one observed experimentally (with 25ns peaking time). The variations of time
resolution in the region of plateau are of the order of 20% of the mean value, the fraction of 0.3 being the optimal one for this region. For the short delays one may improve time resolution by using a higher fraction (for instance 0.5). The contribution of the filter-amplifier noise is not negligible. Therefore time resolution depends on the gain of the filter-amplifier. The simulated dependencies of time resolution are compared to the measured data in Figure 5. The results presented correspond to 50 MeV energy deposition in current $\delta$-shape signal. The contribution of the CFD circuit noise and an optimistic modeling of the front-end noise may be responsible for the observed difference between the simulated results and the measured values.

**The model extension**

The principles used to model signal processor that employs CFD may be extended to comprise DFD pick-off technique (Figure 1b). The timing variance in this case may be routinely derived through noise correlation analysis independently from whatever technique of the time stamp derivation in the back-end is used. If each pick-off of the signal amplitude fraction is taken instantly the resulting expression is as follows:

$$\sigma^2 = \frac{\sigma^2_N}{(\alpha_1 - \alpha_2)^2} E^2 \left( \frac{\phi_i(t_1)}{\phi_i(t_2)} \right)^2 - \frac{2r(t)}{\phi_i(t_1)\phi_i(t_2)}, \quad (7)$$

where $\phi_i(t_1), \phi_i(t_2)$ are the reference signal slopes determined by the signal derivations at the instants that correspond to the signal amplitude fractions $\alpha_1$ and $\alpha_2$, $\tau=t_1-t_2$ is time interval between samples, $r(t)$ is double side normalized noise correlation function. In this case the noise variance $\sigma^2_N$ at the input of the discriminator is the integral of noise spectral density $S(f)$ over the frequency band of the processor, so that $r(t)=R(t)/\sigma^2_N$, where $R(t)$ is double side noise correlation function that may be derived through the inverse Fourier transformation $F^{-1}$ as $R(t)=F^{-1}(S(f)/2)$. The construction of the goal function for time resolution evaluation through the expression 7 is similar to that discussed for CFD in the appendix.

**Conclusion**

This work was motivated by intention to characterize electronic noise contribution to timing with a processor involving fraction discriminator assuming an ideal representation of the discriminator circuit. The developed approach provides a designer with a reliable estimation of time resolution dependence on the processor parameters before the back-end designing of a signal processor circuit starts. The discussed method may comprise amplitude rise time compensation technique with minor modifications. The modeling of ideal discriminator provides a possibility of rapid evaluation of front-end noise contribution to timing. The simulation method may be extended to comprise contribution of the detector signal fluctuations into timing. However certain sources of errors of other nature [8] were beyond the scope of this study. The correspondence of the simulated results to the measured values is found sufficient under the assumptions committed. The simulation results were obtained by using PSPICE version 7.1 based on Microsoft Windows platform.

**Appendix. Goal function usage**

The results of time resolution evaluation by goal function with the name fraotr are shown in Figure 4. The goal function uses four traces to define time resolution in function of the delay for a given fraction. Parametric analysis with varying delay must precede performance analysis with the goal function. The ideal delay is introduced at the output of loaded on 50 Ohm front-end via Laplace transform. The current stimulus used in parametric analysis of this study corresponds to 4.35056 Mev energy deposition in Si detector by $\delta$-like waveform. The trace corresponding to the function under differentiation in the denominator of expression 2 is derived by corresponding macro for each fraction of interest. For each delay parameter the macro takes into account the difference of the fraction of the output waveform and the delayed output waveform. The traces corresponding to these macros are named zerconfi where $i$ is the number indicating the fraction. The body of the goal function with the corresponding operation comments is as follows:

```plaintext
fratr(1,2,3,4)=4.35056*(sqrt(y2)/y4)
```

*Marked point expression to derive normalized to 1 MeV time resolution. This is an equivalent of square root taken for both sides of expression 2.

```plaintext
{1| search forward xval(120n) !1;
* Finds the magnitude of the trace at the
* moment of 120n; constant trace of the
* magnitude equal to the particular delay is
* used.
2| search forward xval(y1) !2;
```
*Finds the magnitude corresponding to the delay value; trace of pwl form representing noise variance dependence on delay (for fixed fraction) is used.

3] search forward (12n, 120n) level(0) !3;
*Finds the moment of zero crossing, the limits of the search are determined by the peaking time of the response and the range of the delay variation; trace corresponding to macro zerconfi is used

4] search forward xvalue(x3) !4;
*Finds the slope at the moment of zero crossing; derivation of trace represented by macro zerconfi is used

References
5. ORTEC Application Note 41. Techniques for Improved Time Spectroscopy, p.9.

Figure 1a. A representation of a processor involving constant fraction discriminator (CFD). The front-end is loaded on 50 Ohm input impedance of CFD circuit, ideal buffer separates the input impedance from the rest of CFD circuit. Figure 1b. A principle of time mark derivation with double fraction

Figure 2. Schematic view of the amplifier circuit used in this study.
Figure 3. Front-end noise variance dependencies on delay of CFD simulated for different parameters of fraction. The data for two gain factors of the filter-amplifier are presented.

Figure 4. Time resolution (r.m.s. values) dependencies on delay of CFD presented for three parameters of fraction. Time resolution shown for two gain factors of the filter-amplifier is normalized to 1 MeV energy deposition, the stimulus is current $I(t)$-function.

Figure 5. Simulated time resolution dependencies on delay of CFD are compared to the measured values obtained with 50 MeV stimulus. The values are presented in f.w.h.m. units. The simulated results are shown in solid lines. The measured values are shown by triangles (Figure 5a) for the filter gain factor of 8 used with 50% fraction, and by rectangles (Figure 5b) for the filter gain factor of 1 used with 30% fraction.
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INDEX
Abbrescia, M. · 457
Abolins, M. · 323
Acosta, D. · 318
Agapito, J. A. · 411
Alberici, G. · 138
Alfke, P. · 36
Altieri, S. · 457
Anderson, K. · 255
Anderssen, E. · 421
Anelli, G. · 157
Anghinolfi, F. · 113, 118, 123, 152, 157
Antchev, G. · 343, 348
Anthony, P. L. · 473
Appel, J. A. · 98
Arai, Y. · 462
Arnold, L. · 147
Atamanchuk, A. · 318
Atkin, E. · 499, 501
Augusto, J. · 361
Azevedo, C. · 175
Bauer, C. · 508
Baumbaugh, A. E. · 260
Bauss, B. · 299
Beigbeder, C. · 242
Belli, G. · 457
Beltrán Almeida, C. · 361
Berglund, S. · 255
Berkhan, K. · 564
Bernier, R. · 242, 561
Berry, S. · 421
Berst, J. D. · 108, 147, 542
Betev, B. · 397
Bevans, B. · 128
Bhasin, A. · 285
Bigga, A. · 208
Bintinger, D. · 421
Bisello, D. · 513
Blair, R. E. · 323
Blanchard, G. · 285
Bloodworth, J. J. · 285
Bocci, V. · 281
Boget, D. · 531
Bohm, C. · 255, 299, 314
Bohner, G. · 274
Bonazzola, G. C. · 138
Bonna, G. · 208
Bonneau, P. · 416, 421
Bonnet, D. · 147
Bonvicini, V. · 138
Borschchov, V. N. · 143
Bossi, F. · 281
Bosteels, M. · 416, 421
Boucham, A. · 147
Bouvier, P. · 421
Bouvier, S. · 147
Branchini, P. · 281
Braun, G. · 383
Brawn, I. · 299
Breton, D. · 242, 561
Brettel, H. · 227
Bright-Thomas, P. · 299
Bruno, G. · 457
Burns, M. · 93
Butterworth, J. · 336

C

Cacéres, T. · 242
Cacho Teixeira, I. · 361
Campbell, D. · 152
Campbell, M. · 93, 157, 189, 194
Cancelo, G. · 98, 483
Cano, E. · 343
Cantatore, E. · 93, 503
Caponetto, L. · 518
Cardeira, F. M. · 411
Cardoso, N. · 361
Carlin, R. · 508
Carter, A. A. · 152
Casas, J. · 411
Castillo, J. · 147
Cavagnino, D. · 138
Cencelli, V. · 93
Cerello, P. G. · 138
Cervelli, G. · 162, 175, 194
Chapman, J. · 448
Charlton, D. G. · 185
Chase, B. · 222
Chatellier, S. · 343
Chernikov, V. · 499
Christian, D. · 98
Christiansen, J. · 41, 194
Cindro, V. · 113
Ciocio, A. · 118, 123, 152
Citterio, M. · 222, 237, 402
Cittolin, S. · 343
Clark, A. · 113, 118, 123, 152
Clauss, G. · 147
Cleland, W. E. · 366
Coffin, J. P. · 147
Colaleo, A. · 457
Colas, J. · 217, 265
Colledani, C. · 108, 147, 542
Collot, J. · 561
Cornat, R. · 274
Corsi, F. · 503
Coughlan, J. A. · 357
Cragg, D. · 421
Crawley, H. B. · 473
Croix, J. · 108
Cros, P. · 242
Csató, P. · 493
Cwienk, W. D. · 227
Czyzew, T. · 180

D

Dabrowski, W. · 113, 118, 123, 152
Dasu, S. · 295
Dawson, J. W. · 323
de Haas, A. P. · 143
de la Taille, C. · 265, 561
De Remigis, P. · 138
De Robertis, G. · 281
De Witt, J. · 152
Deiters, K. · 203
Delagnes, E. · 561
Della Negra, R. · 108, 581
Delmastro, M. · 157
Demidov, A.A. · 547
Dénes, E. · 493
Denes, P. · 397
Deppe, H. · 508
Deptuch, G. · 108, 542
Dinapoli, R. · 93
Ditta, J. · 531
Djambazov, L. · 397
Dolezal, Z. · 118
Dorfan, D. · 113, 118, 123, 152
Dorholt, O. · 118
Dowell, J.D. · 185
Drancourt, C. · 147
Dressnandt, N. · 128
Dröge, M. · 397
Duarte, A. · 411
Dubbs, T. · 113, 118, 123, 152
Dulinski, W. · 108, 147
Dulny, B. · 270
Dumont-Dayot, N. · 265
Dupanloup, M. · 108, 542, 581
Duperray, H. · 208
Dupieux, P. · 285
Dzahini, D. · 561

E

English, R. · 421
Engström, M. · 255, 299, 314
Erazmus, B. · 147
Erhan, S. · 343
Ermoline, Y. · 323
Erö, I. · 309
Evans, D. · 285

F

Faccio, F. · 157, 189, 208, 571
Falchieri, D. · 138
Falconer, N. · 123, 152
Fallot-Burghardt, W. · 508
Falvard, A. · 274
Faure, J.-L. · 397
Feld, L. · 118
Felici, G. · 281
Fent, J. · 227, 270
Feofilov, G.A. · 285
Fernandes, A.P. · 411
Ferrere, D. · 118
Feuerstack-Raible, M. · 167, 508
Fischer, H. · 383
Fischer, P.-A. · 473
Flammer, J. · 576
Fleckenstein, H. · 576
Florian, S. · 157
Formenti, F. · 93
Foryt, P. · 180
Fouque, N. · 531
Franco, F.J. · 411
Franz, J. · 383
French, M. · 123, 152, 162, 513
Fukuda, M. · 462
Fulcher, J. · 513
Grabit,R. · 175
Grassi,T. · 93
Gratchev,V. · 452
Gregor,J.M. · 185
Grieco,G.M. · 427
Grillo,A.A. · 113, 118, 123, 152
Grohmann,S. · 421
Gröpel,A. · 576
Grünemaier,A. · 383
Guarrasi,L. · 457
Guilloux,G. · 147
Gutleber,J. · 343

Haber,C. · 118, 123, 152
Haberer,W. · 270
Haberichter,W.N. · 323
Hähnel,C. · 576
Hall,G. · 162, 513
Hallewell,G. · 421
Halsall,R. · 357
Hanke,P. · 299, 478
Hansen,M. · 525
Hansen,S. · 260
Harnew,N. · 167
Hartley,J. · 357
Hasuko,K. · 331, 443
Hatley,R. · 299
Hauser,J. · 304
Hausmann,S. · 508
Hayes,D. · 336
Hayler,T. · 421
Haynes,W.J. · 357
Hazen,E. · 436
Heijne,E. · 93, 157
Heinsi, F.H. · 383
Hellman, S. · 299, 314
Hennig, L. · 383
Hernández Cachero, A. · 411
Hernandez, R. · 138
Hocker, A. · 255
Hoff, J. · 98
Hoffmann, C. · 108, 537
Hojda, M. · 180
Holmgren, S.-O. · 255
Homer, R.J. · 185
Homma, K. · 443
Hornung, M. · 118
Hrisoho, A. · 242
Hu, L. · 448
Hu, Y. · 108, 537, 542
Hu-Guo, C. · 108, 537, 542
Husmann, D. · 478
Huth, J. · 436

I

Iaselli, G. · 457
Ikeda, M. · 443
Ilie, S. · 421
Iliev, B. · 397
Imbruglia, A. · 208
Ippolitov, M. · 232
Iterbeek, H. · 576
Iwasaki, H. · 443

J

Jacobs, C. · 343
Jakobs, K. · 299, 314
Jarron, P. · 93, 113, 123, 152, 157, 208

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Kadlec, J. · 421
Kaminski, A. · 513
Kandasamy, A. · 452
Kaplon, J. · 113, 118, 123, 133, 152
Karpinski, W. · 103
Keller, M. · 478
Kenyon, I.R. · 185
Ketterer, C. · 118
Kierstead, J. · 237, 402
Kiesling, C. · 270, 551
Kinnison, J.D. · 61
Kinson, J.B. · 285
Kipnis, I. · 123
Kiprich, S.K. · 143
Kirk, A. · 285
Kiss, T. · 493
Klereborn, J. · 255
Kloukinas, K. · 93, 157, 189, 194, 469, 571
Klovning, A. · 232
Kluge, A. · 377
Kluge, E.E. · 299, 478
Kluit, R. · 508
Knöpfle, K.-T. · 167, 508
Kobayashi, T. · 443
Kocper, B. · 285
Kodys, P. · 118
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Kolanoski, H. · 564
Kolovjari, A. · 285
Kondo, T. · 118
Kondratenko, S. · 499
Königsmann, K. · 383
Kötz, U. · 508
Kralik, J. · 285
Kramberger, G. · 113
Krause, J. · 299, 478
Kuah, J. · 448
Kudla, M. · 180
Kudlany, J. · 113
Kuhn, C. · 147
Kuijer, P. · 143
Kurchaninov, L. · 227
Kwan, S. · 98

Lefèvre, F. · 285
Lenti, V. · 285
Lindenstruth, V. · 285
Lindsay, S. · 421
Lo Presti, D. · 518
Löchner, S. · 508
Loddo, F. · 457
Lofstedt, B. · 251
Los, S. · 260
Lübelsmeyer, K. · 103
Ludwig, J. · 118
Luptak, M. · 285
Lustermann, W. · 397
Lutz, J.R. · 147

M

Macina, D. · 113, 118, 123, 152
Madorsky, A. · 318
Maeland, O. · 232
Magazzu, G. · 571
Maggi, M. · 457
Mahboubi, K. · 299, 478
Mahout, G. · 185
Makowiecki, D. · 222
Mandic, I. · 113, 185
Manko, V.I. · 232
Mann, J. · 448
Männer, R. · 576
Manzari, V. · 285
Marangelli, B. · 457
Marchioro, A. · 157, 189, 194, 469, 571
Marent, K. · 431
Marques, J.G. · 411
Martin, L. · 147
Martín, M.A. · 411
Osthoff, A. · 270

Paccagnella, A. · 513
Palutan, M. · 281
Parsons, J. · 222, 452
Parthipan, T. · 357
Patel, B. · 203
Patera, V. · 281
Patti, A. · 561
Payne, B. · 421
Paz, A. · 411
Perera, V. · 299
Pernack, R. · 576
Perret, P. · 274
Perrin, E. · 421
Perrodo, P. · 265
Perrot, G. · 265
Pfeiffer, U. · 299, 478
Phillips, P. · 118, 123
Phillips, P. W. · 152
Pierschel, G. · 103
Pietarinen, E. · 180
Pilcher, J. · 255
Pilling, A. · 421
Pitz, F. · 285
Placidi, P. · 469
Pleshko, A. · 499
Pohl, M. · 564
Pollet, L. · 343
Polychronakos, V. · 452
Popov, V. · 557
Posch, C. · 436
Postranecky, M. · 336
Pozniak, K. · 180

Pritchard, T. · 123, 152
Pugatch, V. · 508
Pugliese, G. · 457
Putzer, A. · 299

Quadflieg, D. · 103
Quast, G. · 299, 314
Quiquempoix, V. · 93

Racz, A. · 343
Radeka, V. · 222
Ramalho, A. J. G. · 411
Randazzo, N. · 518
Ranieri, A. · 457
Rashevsky, A. · 138
Ratnikov, F. · 576
Ratti, S. P. · 457
Rausch, R. · 7
Raykov, P. · 397
Raymond, M. · 162, 513
Razmyslovich, B. · 318
Renker, D. · 203
Rescia, S. · 222, 237
Reßing, D. · 576
Reucroft, S. · 203
Riccardi, C. · 457
Richardson, J. · 83
Richer, J.-P. · 561
Riegel, H. · 557
Riegler, W. · 436
Rieth, G. · 118
Riu, I. · 576
Rivetti,A. · 138, 157
Roberts,B. · 208
Rodríguez Ruiz,M.A. · 411
Roe,S. · 113, 118
Röhrich,D. · 285
Roig,O. · 285
Romaniuk,R. · 180
Romaro,F. · 457
Rongved,R. · 232
Roth,D.R. · 61
Rothe,C. · 576
Roy,C. · 147
Rubin,G. · 493
Rudge,A. · 185
Runge,K. · 118
Rusack,R. · 203
Ruzhitsky,V.M. · 143

S

Sacchi,R. · 508
Saito,M. · 443
Sakhelashvili,T. · 203
Samyn,D. · 343
San Segundo Bello,D. · 93
Sandaker,H. · 421
Sanders,H. · 255
Santiard,J.-C. · 431
Santos,J.P. · 411
Santos,M. · 361
Sasaki,O. · 331, 443
Sato,K. · 443
Schacht,P. · 227
Schäfer,U. · 299, 314
Schatz,V. · 478
Schierloch,M. · 383

Schlereth,J.L. · 323
Schmelling,M. · 167
Schmidt,T. · 383
Schmitt,H. · 383
Schmitt,K. · 299, 478
Schmitt,Ph. · 108, 537, 542
Schneider,B. · 51
Schneider,M. · 448
Schumacher,C. · 290, 299, 478
Schütz,J. · 557
Schwengelbeuer,B. · 508
Sciubba,A. · 281
Scurlock,B. · 318
Seguin-Moreau,N. · 265
Seiden,A. · 123
Seldén,B. · 255
Serin,L. · 265
Sexauer,E. · 167, 508
Seytre,J.-F. · 421
Shah,A. · 299
Shah,T.P. · 299
Shank,J. · 436
Shaylor,H.R. · 185
Shenai,K. · 14
Shivarov,N. · 397
Sibiari,J. · 232
Silverstein,S. · 255, 299, 314
Sinanis,N. · 343
Sippach,W. · 222, 452
Skaali,B. · 232
Skorobogatov,P.K. · 547
Smale,N. · 167
Smith,W.H. · 295
Snoeys,W. · 93
Söhler,J.L. · 108, 542
Soós, C. · 493
Speigel, M. · 377
Spencer, E. · 113, 118, 123, 152
Spíčcas, P. · 343
Spieler, H. · 118, 123, 152
Staley, R. · 299
Stavitsky, I. · 513
Stelzer, B. · 478
Stelzer, G. · 478
Stokes, W.N. · 285, 299
Straumann, U. · 508
Suchodolinská, I. · 285
Suire, C. · 147
Sulyán, J. · 493
Sundal, B. · 118
Sushkov, V.V. · 588
Swain, J.D. · 203
Swoboda, D. · 371
Szczygieł, R. · 113, 118, 123, 152
Szocsó, F. · 391

Torre, P. · 457
Tosello, F. · 138
Tóth, N. · 493
Troska, J. · 185
Trouilleau, C. · 274
Trunk, U. · 508
Truong, K. · 242
Tschirhart, R. · 260
Turala, M. · 118
Turchetta, R. · 108, 542
Twomey, M. · 521
Tynдел, M. · 118, 152

U

Ullan, M. · 118, 123
Unno, Y. · 118
Urban, H.J. · 383
Uwer, U. · 564
Uzelac, J. · 448

V

Vacchi, A. · 138
Vacek, V. · 421
van Bakel, N. · 167
Van Berg, R. · 128
van den Brand, J. · 167
van den Brink, A. · 143
van der Bij, E. · 194, 489
van Staa, R. · 557
Vande Vyvre, P. · 285, 493
Varela, J. · 361
Vascotto, A. · 285
Vasey, F. · 175
Vassiliev, S. · 564
<table>
<thead>
<tr>
<th>W</th>
<th>Y</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vercellin, E. · 285</td>
<td>Williams, H.H. · 128</td>
<td>Zimmermann, S. · 98</td>
</tr>
<tr>
<td>Vesztergombi, G. · 493</td>
<td>Wilson, J.A. · 185</td>
<td>Zinzingus, Y. · 108, 537</td>
</tr>
<tr>
<td>Vikas, P. · 203</td>
<td>Wingert-Seez, L. · 265</td>
<td>Zsenei, A. · 113, 118, 123, 152</td>
</tr>
<tr>
<td>Villalobos Baillie, O. · 285</td>
<td>Wolter, M. · 113, 118, 123, 152</td>
<td></td>
</tr>
<tr>
<td>Viola, L. · 457</td>
<td>Wrochna, G. · 180</td>
<td></td>
</tr>
<tr>
<td>Vitulo, P. · 457</td>
<td>Wu, H. · 255</td>
<td></td>
</tr>
<tr>
<td>Volkov, M. · 232</td>
<td>Wurz, A. · 576</td>
<td></td>
</tr>
<tr>
<td>Volkov, Yu. · 499, 501</td>
<td>Wyllie, K. · 93</td>
<td></td>
</tr>
<tr>
<td>Votruba, M.F. · 285</td>
<td>Wyss, J. · 513</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Wang, S.M. · 318</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wastie, R.L. · 185</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watkins, P. · 299</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watson, A. · 299</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watts, S.J. · 201</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Weidberg, A.R. · 185</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Weilhammer, P. · 113, 118, 123, 152</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Werbrouck, A. · 138</td>
<td></td>
<td></td>
</tr>
<tr>
<td>White, D.J. · 185</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>