Enhanced Radiation Hardness and Faster Front Ends for the Beetle Readout Chip

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Abstract

This paper summarizes the recent progress in the development of the 128 channel pipelined readout chip Beetle, which is intended for the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detectors of LHCb.

Deficiencies found in the front end of the Beetle Version 1.0 and 1.1 chips resulted in the submissions of BeetleFE 1.1 and BeetleFE 1.2, while BeetleSR 1.0 implements test circuits to provide future Beetle chips with logic circuits hardened against single event upset (SEU).

Section I. motivates the development of new front ends for the Beetle chip, and section II. summarizes their concepts and construction. Section III. reports preliminary results from the BeetleFE 1.1 and BeetleFE 1.2 chips, while section IV. describes the BeetleSR 1.0 chip. An outlook on future test and development of the Beetle chip is given in section V.

I. Introduction

The development of the Beetle readout chip started in late 1998. It implements the basic RD20 architecture [4], augmented with a prompt binary readout path like it was implemented on the HELIX128 chip [5] and a pipelined binary operation mode. Besides several (2×2) mm² chips with test structures and components, two complete readout chips (Beetle1.0 and Beetle1.1) have been manufactured in commercial 0.25μm CMOS technology. A detailed description of these chips, their architecture and performance can be found in [1] [2] [3].

Beetle1.0, the first complete pipelined readout chip had to be patched with a focused ion beam to become functional. In turn the second one, Beetle1.1 included all fixes to correct the errors found on its predecessor. However, a few problems still remained:

- Peaking time of the front end t_{peak}(0…100%) ≥ 27ns,
- Decay time of the pulse has a remainder above 30% after 25 ns, too long for the operation of the LHCb vertex detector,
- Maximum input current of ≈ 2nA, too small for the expected occupancies at LHCb
- Digital circuits not robust against SEU.

To overcome these problems, which are primarily related to the actual requirements of LHCb, test chips implementing the necessary circuits were submitted. This allows the test of the circuit’s functionality prior to its implementation on a complete readout chip. Furthermore different approaches to solve the same problem can be evaluated to find the optimum solution.

II. New Front Ends

The front end implemented on Beetle1.1 was developed with an early version of the 0.25μm CMOS design kit in 1998 and submitted on the first test chip BeetleFE 1.0. It consists of a charge sensitive preamplifier, a CR−RC pulse shaper and a buffer. The first two stages use folded cascade amplifier cores, while the buffer is a source follower. Measurements of its characteristics showed that it was considerably slower than
expected from simulation. This discrepancy, however, diminished with the evolution of the design kit and nearly vanished with the last version. A further impetus to develop a faster front end arose from the increasing detector capacitances. While values around 10 pF were assumed for the strip capacitance of the LHCb vertex detector during the development of the BeetleFE 1.0, the current designs predict capacitances of up to 35 pF for the inner tracker detectors of LHCb. Fig. 1 shows the pulse shape of the Beetle1.1 front end for different input capacitances.

![Pulse Shapes of the Beetle1.1’s test channel at indicated capacitances.](image)

To decrease the peaking time and fall time of the shaped signal, the following provisions have been taken:

- Decreased resistance of the preamplifier’s *folded cascade* load branch to decrease the peaking time of the pulse. This also required an increase of the input transistor’s transconductance $g_{m}$ in order to maintain the same open loop gain $A_{0}$.

- Decreased integration time constant $\tau_{\text{sh}}$ of the shaper in order to decrease the fall time of the pulse. The shaper’s amplifier core was in principle not affected by this change.

DC input currents showed up as another problem of Beetle1.1. A thorough investigation of the problem and subsequent simulations revealed that the front end was able to cope with average input currents only below 2 nA, which is too low for the expected occupancies at LHCb.

The cause for this behaviour is inherent to the concept of the Beetle1.1’s front end depicted in fig. 2: The gate potential of the NMOS input transistor is on a potential of around the threshold voltage $V_{\text{th}}(\text{NMOS})$ of the input transistor above $V_{\text{ss}}$. This potential is also the source voltage of the PMOS feedback transistor. In turn the gate potential of this transistor has to be $V_{\text{th}}(\text{PMOS}) + V_{\text{th}}(\text{PMOS})^2$ in order to become conductive. Since the absolute value of the threshold voltage is a bit higher for a PMOS than for an NMOS transistor and since $V_{\text{th}}$ is lower for short transistors like the NMOS input FET, the situation is worsened. Nevertheless, the circuit reaches a stable operating point, since the feedback transistor is usually operated in the linear (sub threshold) region, where the resistance was still about 15 M\ ohm when the gate of the feedback transistor was tied to the $V_{\text{ss}}$ potential.

A first approach to overcome the problem was implemented on the BeetleFE 1.1 chip shown in fig. 3: The length of the feedback transistor was decreased in order to reduce its resistance and threshold voltage.

For the BeetleFE 1.2 (fig. 4) two different concepts were realised: Front ends with PMOS input and feedback transistors and one channel with an NMOS input and feedback transistor.

In case of the PMOS input and feedback configuration (fig. 5), the threshold voltages point away from the power supply rails and thus do not restrict the range of useful voltages $V_{\text{th}}$ on the feedback transistor’s gate. The biggest disadvantage of this circuit is the by a factor of 3 lower $g_{m}/\text{area}$ ratio of the input transistor. On the BeetleFE 1.2 this was partly compensated by the reduction of the channel length and the enclosed waffle geometry of the input transistor.

The solution with NMOS input and feedback transistors shown in fig. 6 is spoiled by the constraints of radiation hard layout techniques: The enclosed geometry limits the $W/L$ ratio to about 4, which together with the minimum $W$ of $\approx$ 12 \ \mu m calls for a series of more than 100 transistors to form the feedback resistance.

\[ \text{since } V_{\text{th}}(\text{PMOS}) \leq 0 \]
Table 1: Design parameters of the front ends of the BeetleFE 1.1 (Set 2) and BeetleFE 1.2 (Set 5 and Set 6) test chips.

<table>
<thead>
<tr>
<th>Set</th>
<th>input transistor</th>
<th>$W$</th>
<th>$L$</th>
<th>feedback</th>
<th>shaper feedback</th>
</tr>
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<tr>
<td>2a...c</td>
<td>NMOS rectangular</td>
<td>3744μm</td>
<td>0.42μm</td>
<td>PMOS</td>
<td>48.8fF</td>
</tr>
<tr>
<td>2d...e</td>
<td>NMOS rectangular</td>
<td>3744μm</td>
<td>0.42μm</td>
<td>PMOS</td>
<td>20.5fF</td>
</tr>
<tr>
<td>5a</td>
<td>PMOS waffle</td>
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<td>0.28μm</td>
<td>PMOS</td>
<td>15.9fF</td>
</tr>
<tr>
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<td>0.28μm</td>
<td>PMOS</td>
<td>18.75fF</td>
</tr>
<tr>
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<td>PMOS waffle</td>
<td>8310μm</td>
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<td>PMOS</td>
<td>37.5fF</td>
</tr>
<tr>
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<td>PMOS</td>
<td>18.75fF</td>
</tr>
<tr>
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<td>7123μm</td>
<td>0.28μm</td>
<td>PMOS</td>
<td>37.5fF</td>
</tr>
<tr>
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<td>0.28μm</td>
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</tr>
<tr>
<td>5g</td>
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<tr>
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<td>18.75fF</td>
</tr>
<tr>
<td>5i</td>
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<td>3744μm</td>
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<td>NMOS</td>
<td>48.8fF</td>
</tr>
</tbody>
</table>

Figure 3: Layout of the BeetleFE 1.1: The new front end channels are indicated

III. FIRST RESULTS FROM NEW FRONT ENDS

Measurements on the BeetleFE 1.1 and BeetleFE 1.2 (figs. 7 and 8) showed that one of the design goals, a rise time well below 25 ns has been reached with both chips. For the BeetleFE 1.2 it was also found, that the front end could achieve a rise time of $\leq 24$ ns with an input capacitance as high as 40 pF. Measurements of the maximum input current, as well as noise measurements are still in progress.

IV. THE BeetleSR 1.0 CHIP

The BeetleSR 1.0 chip implements two blocks of 34 registers, each 8 bits wide. Combinatorial logic calculates the parity of these registers, which is available on two groups of 9 pads. Read and write access to these register blocks is accomplished via two independent F2C interfaces: One is implemented in conventional circuitry, while the other one uses triple redundant flip-flops with majority encoding. The block schematic of the chip is shown in fig. 9, while a triple redundant flip-flop with majority encoder is illustrated in fig. 11.

This chip will permit to measure SEU rates by means of the register blocks, it also allows the calcu-
V. Future Plans

*Beetle1.1* chips will be irradiated up to 10 Mrad (100 kGy) with the X-ray irradiation facility of the CERN micro electronics group. They will also be used in a test beam with prototype detectors of the LHCb inner tracker in October 2001. Studies with the chip bonded to a detector are under way.

The submission of the final version (1.2) of the *Beetle* chip is planned for spring 2002. This chip will implement:

- a modified frontend with a faster shaping and a higher maximum input charge rate, chosen from the front ends on the *BeetleFE 1.1* and *BeetleFE 1.2* chips.

- two single event upset (SEU) detection and correction mechanisms:
  1. triple redundant flip-flops with majority encoding in state machines and other frequently changed registers, and
  2. *ECC*\(^3\) based on hamming encoding for more static registers.

Status reports and further test results will be available at [6].
Figure 7: Pulse shapes of the BeetleFE 1.1 test chip. The left graph shows pulse shapes from different modifications of the "Set 2" (c.f. tab. 1) front end, the right one shows the response for different input charges.

Figure 9: Block schematic of the BeetleSR 1.0 test chip. Two register blocks with parity encoding are controlled via a standard or a SEU robust I²C interface respectively.

References


Figure 10: Layout of the BeetleSR 1.0 test chip. The two register blocks are located on the right and left hand side of the chip. The I²C interfaces are the blocks in the centre, the SEU robust one being the larger block.

Figure 11: Triple redundant flip-flop with majority encoder used in the SEU robust I²C interface of the BeetleSR 1.0 test chip.