Quantum computation and quantum information are two closely related fields that have revolutionized the way we process and understand information. In the early stages of these developments, researchers explored the possibilities of using quantum mechanics to perform computations that are beyond the reach of classical computers.

One of the key challenges in quantum computation is the problem of decoherence, which occurs when a quantum system interacts with its environment and loses its quantum properties. This can lead to errors in the execution of quantum algorithms.

In this context, the concept of a quantum error-correcting code plays a crucial role. These codes are designed to protect quantum information from errors caused by decoherence and other sources of noise. The idea is to encode the quantum information in a way that allows it to be read out even if some of the encoded qubits are in error.

Quantum error-correcting codes work by encoding the quantum information into a larger set of qubits, such that the error can be detected and corrected. This is achieved by performing specific quantum operations on the encoded qubits, which allow the error to be identified and corrected without directly measuring the encoded information.

The effectiveness of quantum error-correcting codes relies on the ability to detect and correct errors without losing the encoded information. This is a challenging problem, as the errors can be caused by a variety of sources, including environmental interactions and electronic noise.

In summary, quantum error-correcting codes are essential tools for building reliable quantum computers, as they enable us to perform quantum computations with high accuracy and precision, even in the presence of unavoidable decoherence.

Quantum computation and quantum information are rapidly advancing fields that offer exciting possibilities for the future. As researchers continue to explore these areas, we can expect to see significant breakthroughs in the coming years.

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The main challenge for designing channel qubits is to provide adequate travel for the sliding electrons. Ideally, when the qubit coupling is turned “off,” the electrons should be well separated. In the “on” configuration, the coupling should be large enough to enable fast operation. To meet this challenge we have developed a bistable quantum dot design (Fig. 2). Using opposing plunger gates, an electron is squeezed into either side of a dot. The flattop “on” condition for $J(V)$ corresponds to the side-by-side configuration of electrons in neighboring dots.

To determine the feasibility of the channel qubit architecture, we model the double quantum dot device of Fig. 2(b), containing one electron per dot. The heterostructure is the same as in Ref. 11. Precise Poisson and Schrödinger equation simulations are performed using finite element techniques. A basis set of single-electron wavefunctions is computed for each qubit in the Hartree-Fock approximation. A two-electron basis set is obtained in the configuration interaction approach, and exact diagonalization is performed on the corresponding Hamiltonian matrix. Image potentials arising from the various gates, due to the qubit electrons, are computed using Green’s functions techniques. The computations are then iterated until self-consistency is achieved. We do not consider impurities here, or other inevitable imperfections in the crystal lattice. However we note that disorder cannot invalidate the basis of pseudo-digital control—the existence of a minimum in the separation between the two qubits.

Fig. 3 shows the simulation results. As the plungers force the electrons into their side-by-side configuration, the exchange coupling grows, exponentially at first. The coupling reaches a peak as the qubits slide past one another; this is the flattop condition we exploit for pseudo-digital control. The bistable dot design clearly enables the desired range of electronic motion, from an “off” state, where the qubit coupling is exponentially small, to an “on” state, where $J(V)$ is flat-topped.

For the device studied here, the exchange coupling achieves a maximum value of 0.4 μeV, corresponding to gate time of 5 ns for the two-qubit SWAP. Faster operation can be achieved with appropriate modifications to the qubit design. In the present work, we have assumed minimum feature sizes of 50 nm for lithographic patterning, giving a qubit separation of 90 nm for the “on” configuration. Since $J$ decreases exponentially with qubit separation, reducing the feature dimensions will increase both $J$ and the gating speed.

One of the key features of the qubits in Fig. 2 is that the plunger gates and the channel gates perform very different roles. The channel gates regulate the maximum value of $J$. Since the channel gate voltages are held constant, this can be accomplished with arbitrary precision. Switching $J$ on and off is the function of the plunger gates, as controlled by classical control electronics. Ideally, plunger gate voltages will be varied quickly, near GHz frequencies, this speed makes them subject to the large uncertainties $|ΔV|/V ∼ 0.01$ associated with high-speed electronics. The key advantage to the shape of $J(V)$ in Fig. 3 is that first order uncertainties in $V$ translate to second order errors in $J$. To estimate
the errors in $J$, we calculate the RMS deviation of $J(V)$ from its mean, assuming a uniform distribution of gate voltages in the range $\pm \Delta V$. This gives $\Delta J / J \approx 5 \times 10^{-4}$ or $\Omega \approx 0.05$. Thus, the channel qubit design decreases coupling errors by two orders of magnitude compared to conventional gating architectures. This improvement is accomplished in spite of the fact that the $J(V)$ curve in Fig. 3 is only “flat” at a single point.

With these results, Eq. (2) suggests that coupling errors $\Delta J$ will only need to be reduced by a factor of 5 to meet the $10^{-4}$ threshold level for fault tolerance. If $10^{-3}$ is more appropriate, then the present scheme will be adequate. [2] This can be accomplished by improvements in existing pulse generators, emphasizing the dependence of scalable quantum computers on cutting-edge classical technology. However, if enhancements in control electronics are not possible or desirable, $\Omega$ may be further reduced by optimizing quantum dot designs. For example, top-gate patterns can be developed that cause qubit confinement potentials to become steeper. Small voltage fluctuations will then have less of an impact on the electron positions, resulting in smaller fluctuations in $J$.

In general, both single and two qubit gates are required for universal quantum computation. So far, we have only demonstrated how to apply pseudo-digital techniques to two-qubit operations. Fortunately, two qubit operations are known to be universal for coded spin qubits. [15, 16] Thus, universal quantum gate operations can be controlled pseudo-digitally.

In this paper, we have shown how to construct qubits that enable fast gating by pseudo-digital techniques. For any quantum computer, gate operations must be performed $10^4$ times faster than the decoherence rate. However, unless special care is taken, fast operation results in large gate errors. In general, an operational “sweet spot” must exist where two fundamental constraints are satisfied: the quantum gates are fast enough to beat decoherence and slow enough to be robust. Here we have developed a hardware design for quantum dot spin qubits that helps meet these criteria by increasing the speed at which gating remains robust. The concept is general and can be extended to many physical systems. [17]

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[12] The error threshold of $10^{-3}$ quoted here is an estimate. More accurate figures can be derived with specific knowledge of the quantum computing hardware; see Ref. 7.
[13] Non-colinear qubit motion was also considered in, M. N. Leuenberger and D. Loss, Physica E 16, 452 (2001).
The plunger gate voltages depend linearly on $e$. Opposing pairs of plunger gates are used to push/pull the electron wavefunction.