The Design of the ATLAS Level-1 Central Trigger Processor (CTP)

• Introduction
• Functionality and Requirements
• Design of the Modules and Backplanes

On behalf of
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Level-1 Trigger - Overview

see talks by G. Mahout & A. Dahlhoff

calo

Preprocessor

Cluster Processor (e/γ & τ/h)

Jet/Energy Processor (jet & energy)

Central Trigger Processor

TTC Partitions

detector front-end

see talk by A. Aloisiò

muon

(RPC) Barrel Trigger

(TGC) Endcap Trigger

Muon-CTP-Interface

see talk by C. Fukunaga
CTP - Trigger Formation (1)

• Input:
  - Calorimeter and muon trigger processors provide trigger information:
    - multiplicities for electrons/photons, taus/hadrons, jets, and muons
    - flags for \( \Sigma E_T, E_T^{\text{miss}}, \Sigma E_T^{\text{jet}} \)
  - Sub-detectors provide calibration triggers.
  - CTP provides internal triggers:
    random, bunch crossing, pre-scaled clock.

  - All trigger thresholds are programmable. Several thresholds are used concurrently for each type of trigger information.

⇒ CTP can accept a total number of 160 input bits to be taken into account at a given time. The total number of input bits can be higher because of selection on CTP input.
**CTP - Trigger Formation (2)**

- **Output:**
  - **Level-1 Accept (L1A),** derived from trigger inputs according to Level-1 trigger menu:
    - 160 trigger items are made from combinations of conditions on the trigger inputs, e.g.
      - $1EM10 \equiv$ at least one electron/photon with $E_T \geq 10 \text{ GeV}$.
    - Generate dead-time in order to prevent front-end buffers becoming full ⇒ select between two priorities for each trigger item.
    - Each trigger item has a mask, a priority and a prescaling factor.
    - L1A is the OR of all trigger items.
  
  - An example of a trigger menu might contain
    - $1MU6$ mask = ON, priority = LOW, pre-scaling = 1000
    - $2MU6$ mask = ON, priority = HIGH, pre-scaling = 1
    - $1EM20 \text{ AND } XE20$ mask = ON, priority = LOW, pre-scaling = 1
      ...
  
    - Additionally, generate 8-bit trigger type word with every L1A ⇒ type of trigger (can be used for processing in detector front-end).
CTP - Trigger Formation (3)

• Additional functionality:
  - Generate **pre-pulse** signal for calibration of sub-detectors.
  - Generate **Event Counter Reset (ECR)**.

• Constraints:
  - Trigger latency, i.e. from trigger input to L1A:
    \[ 4 \text{ BC} \equiv 100 \text{ ns} \]
  - Trigger menu changes with physics/beam/detector conditions.
CTP - Trigger Broadcasting

→ Interaction with TTC Partitions:

<table>
<thead>
<tr>
<th>Calo</th>
<th>Muon</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>LTP</td>
<td>LTP</td>
</tr>
</tbody>
</table>

Central Trigger Processor

CTP sends timing and trigger signals to (~ 40) TTC Partitions.

A TTC Partition consists of
- one Local Trigger Processor (LTP),
- a TTC system proper, i.e.
  one TTCvi, one or more TTCEx/TTCtx/
  TTCvx, TTCoc, TTCrx, etc.
- Fast feed-back BUSY tree, based on
  ROD_BUSY module.

→ LTP is a new concept in ATLAS Level-1 trigger.
**CTP and Trigger/DAQ**

→ Interaction with Trigger/DAQ:

- CTP sends **Region-of-Interest (RoI)** information to the **RoI Builder (RoIB)** which combines it with information from other sources in the Level-1 Trigger and sends it to the Level-2 Trigger.

- CTP sends **event data** to the **Read-out System (ROS)**.

→ *see talk by D. Francis*

- CTP, all LTPs and parts of the TTC system are configured, controlled and monitored via the **Online System**.
CTP - Design

CAL bus (calibration requests)

PIT bus (pattern-in-time)

COM bus (common)

VME bus

→ 9U VME64x
**CTP - Input Module (CTP_IN)**

- **Functionality:**
  - Receive trigger inputs from trigger processors (calo, muon, others).
  - Synchronize w.r.t. clock, check parity and align w.r.t. BCID.
  - Select/route trigger inputs to be sent to PIT bus.
  - Store trigger inputs into test memory; provide trigger inputs from test memory.
  - Monitor trigger inputs integrated over all bunches.

- **Implementation:**
  - Based on FPGAs, dual-port RAM for test memory, switching matrix for selection/routing of trigger information to PIT bus and CERN High-performance TDC (HPTDC) for phase measurement.

- **Status:**
  - CTP_IN is currently under design.
**CTP - PIT/CAL Backplane**

- **PIT bus:**
  - pattern-in-time ≡ synchronized/aligned/selected trigger inputs
  - trigger inputs from **up to three CTP_INs** to CTP_CORE and CTP_MON
  - 160 signals, 80 mm (≡ 5 VMEbus slots), 3 drivers + 2 receivers:
    → SSTL-2-like technology.

- **CAL bus:**
  - requests for calibration triggers from sub-detectors
  - calibration requests from **up to four CTP_OUTs** to CTP_CAL (see later)
  - 128 signals (4 CTP_OUTs, 16 signals, differential), 4 drivers + 1 receiver:
    → LVDS technology.

→ PIT/CAL backplane will be mounted in J5/J6 position.
CTP - Backplanes

**COM Backplane**

**PIT/CAL Backplane**
**CTP - Core Module (CTP_CORE)**

- **Functionality:**
  - Receive and synchronize trigger inputs from PIT bus.
  - Combine trigger input to trigger items according to trigger menu and form L1A.
  - Add preventive dead-time.
  - Send trigger result to COM bus.
  - Form RoI and ROS information and send them to RoIB and ROS.

- **Implementation:**
  - Basic idea: use content-addressable memory (CAM):
    
    \[
    \text{input pattern} \Rightarrow \text{CAM} \Rightarrow \text{trigger items.}
    \]
  - Use large FPGAs for pre-scaling and for monitoring.

- **Status:**
  
  Detailed design of CTP_CORE needs to be done.
**CTP - Monitoring Module (CTP_MON) (I)**

- **Functionality:**
  - Receive and synchronize trigger inputs from PIT bus.
  - Decode and select trigger inputs to be monitored.
  - Monitor trigger information on a bunch-by-bunch basis.

- **Implementation:**
  - Use numerous segmented memories in 4 Altera Stratix FPGAs for counters:
    - \(160 \times 3564 \times 32\) bit = 2.2 MByte

- **Status:**
  - CTP_MON is currently under test.

→ see poster by H. Pessoa Lima
CTP - Monitoring Module (CTP_MON) (2)
**CTP - Output Module (CTP_OUT)**

- **Functionality:**
  - Receive timing and trigger signals from COM bus.
  - Fan out timing and trigger signals to the sub-detectors (LTPs).
  - Receive busy signals and calibration requests from sub-detectors (LTPs).

<table>
<thead>
<tr>
<th>CTP → LTP</th>
<th>CTP ← LTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC</td>
<td>1 bit</td>
</tr>
<tr>
<td>ORBIT</td>
<td>1 bit</td>
</tr>
<tr>
<td>L1A</td>
<td>1 bit</td>
</tr>
<tr>
<td>ECR</td>
<td>1 bit</td>
</tr>
<tr>
<td>trigger type</td>
<td>8 bit</td>
</tr>
<tr>
<td>pre-pulse</td>
<td>1 bit</td>
</tr>
<tr>
<td>calibration request</td>
<td>3 bit</td>
</tr>
<tr>
<td>BUSY</td>
<td>1 bit</td>
</tr>
</tbody>
</table>

- **Implementation:**
  - Basic ideas: fan-out module → drive links to LTPs.

- **Status:**
  Detailed design of CTP_OUT needs to be done.
**Local Trigger Processor (LTP)**

- **Functionality:**
  - Original idea by G. Perrot (LAPP Annecy, ATLAS LAr Calorimeter)
  - Input: CTP/daisy-chain, local input, pattern generator
  - Output: daisy-chain, TTCvi, local output
  
  \[\Rightarrow \text{“Programmable input/output switch for timing&control signals”}\]

- **Run Modes:**
  - **Common mode:** CTP drives the TTC partitions.
  - **Stand-alone mode:** LTP drives the TTC partition (local input or pattern generator).
  - Combine two or more TTC partitions:
    - one LTP is the master (replacing CTP), others are slaves.

- **Status:**
  - Design has been discussed with all sub-detectors.
  - LTP is currently under design,
    \[\rightarrow\] manufacturing of prototype until end of this year.
CTP - Machine Interface Module (CTP_MI)

• Functionality:
  → timing module, i.e. machine interface (to LHC)
  - Receive timing signals from LHC (via TTCmi), or generate locally.
  - Control and monitor busy signals (internal and external).
  - Send signals to COM bus.

• Implementation:
  - Based on FPGAs and CERN High-performance TDC (HPTDC) for phase measurement.

• Status:
  CTP_MI is currently under design.
**CTP - COM Backplane**

- COM bus:
  - timing signals common to all modules
    - for timing: BC, ORBIT;
    - for trigger: L1A*, trigger type*, BUSY;
    - for control: ECR, pre-pulse*.
  * only from CTP_CORE to CTP_OUTs and CTP_CAL.
  
  → LVPECL and Mutlipoint-LVDS (for BUSY) technologies.
  → COM backplane will be mounted on backside of J0 connector.
  
  → see photo of backplanes earlier
**CTP - Calibration Module (CTP_CAL)**

- **Functionality:**
  - Time-multiplex sub-detector calibration requests (per ORBIT).
  - Send calibration requests to CAL bus.
  - Receive external beam pick-up and test signals.

- **Implementation:**
  - Basic idea: collect calibration requests from CTP_OUT (from LTPs) via CAL bus, multiplex signals per LHC orbit and feed to CTP_IN.

- **Status:**
  Detailed design of CTP_CAL needs to be done.
Conclusion

• CTP:
  - Six different types of modules, three different buses (on two backplanes).
  - Design/Manufacturing is in progress.
  - Prototype modules will be available this year, the full system will be available next year \( \rightarrow \) testbeam.

• LTP:
  - Newly defined interface between CTP and sub-detectors:
    allows one to run in common mode and stand-alone (calibration, etc.).
  - Design is in progress.
  - Prototype modules will be available by the end of this year.

• TTC and ROD_BUSY:
  - System and modules are defined and manufactured.
    Cabling and installation is being planned now.