**A CMOS CURRENT PREAMPLIFIER AND SHAPER
WITH 50 Ω LINE DRIVER FOR LIQUID ARGON PRESHOWER**

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A CMOS Current Preamplifier and Shaper with 50Ω Line Driver for Liquid Argon Preshower

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Abstract

In the field of liquid argon calorimetry for the LHC detector program, a CMOS "current conveyor" preamplifier was developed for a cold preshower. It is an improved version of the ICON circuit which had been formerly designed by the RD2 collaboration. This paper also presents a CMOS linear output buffer, featuring a dynamic range close to $\pm 2V$ on a 50Ω load, for a 21 mW power dissipation at 77K. Furthermore a biquadratic 7 MHz bandpass filter was developed, based on a high speed rail to rail CMOS operational amplifier. It is meant to be the filter placed at the output of the ICON preamplifier.

I. INTRODUCTION

A CMOS current conveyor has several benefits for a liquid Argon preshower : the power dissipation (1mW), the peaking time (10 ns) and the possibility to integrate this preamplifier with analog multiplexer or pipeline to minimize the cable length [1] [2].

The circuits have to be placed near the detector and then at cryogenic temperature. This is a challenge for CMOS circuit design, but it offers some advantages due to improved device performance. Low field mobilities are increased by a factor four, providing a corresponding increase in the transistor transconductance and circuit speed or a reduction in the power dissipation. Since the parasitic bipolar transistor current gain decreases at low temperature, the latch-up effect is reduced. Regarding the noise : the channel thermal noise decreases ; but 1/f noise dependence on temperature is different for N and P devices. It decreases with temperature for NMOST while the opposite behaviour is observed for PMOST [3].

However, we point out that the influence of this 1/f noise is limited to low frequencies [4]. For the total integrated noise in the preamplifier bandwidth, the 1/f noise is less important than the channel thermal one.

In this paper, we present the performance obtained with CMOS technology at cryogenic temperature for analog front end circuits : this includes a preamplifier, a 50 Ω driver and a filter based on a fully differential operational amplifier.

II. THE PREAMPLIFIER PRINCIPLE

The schematic diagram of the preamplifier is shown in figure1. The parallel noise is the main problem as it has been published before [1], it is dominated by the channel noise of both mirror transistors (QP2, QP3) and (QN2, QN3).

To decrease the noise we added some degeneration transistors to the current mirrors to reduce respectively the equivalent transconductance G_m for each transistor. G_m could be related to g_m as $G_m = \frac{g_m}{(1 + \frac{g_m}{g_{md}})}$ [5] where g_{md} is the

transconductance of the diode connected degeneration transistor. If we consider the PMOS mirror, its noise contribution can be written :

$$i_n = 4 k T \xi (n G_{m2}) + \left(\frac{G_{m2}}{G_{m3}} \right)^2 4 k T \xi G_{m3}$$

Where ξ is the noise factor situated between $0.67 < \xi < 1$ [4] and n a slope factor related to the body effect transconductance G_{mb} as : $G_m + G_{mb} = n G_m$ [6]. Simulation results give $n=1.1$ and make negligible the bulk noise contribution.

In the same way the mirror ratio G_{m3}/G_{m2} was increased following the channel width ratio. Notice that these modifications reduce the speed of the preamplifier due to the total parasitic capacitance at the current mirror node.

The series noise is not the major problem in our application because the typical detector capacitance is only 20pF. However, by ac ground connecting the gate of the input transistors with CN and CP, the bias stage noise contribution is reduced and series noise slope decreases from 65e-rms/pF to 47e-rms/pF according to the simulations.

Fig 1 : Schematic diagram of the preamplifier

III. CMOS 50Ω LINE DRIVER

Along with fast preamplifier development, high performance analog interface blocks are required, which can operate with the same low supply voltage as the preamplifier.

High linearity at high frequencies is the main difficulty of this design. For large swing applications one has no choice than to use common source transistors at the output. A complementary class AB large swing CMOS output buffer has been developed, intended for preamplifier interface with the measurement room. It employs the pseudo source follower principle shown in figure 2.

Fig 2 : Principle of the line driver

It is composed of a pair of common source transistors and a pair of complementary error amplifiers. The output transistors are included in a negative feedback loop and driven by the error amplifiers [7] [8] [9].

One major drawback of this structure is the sensitivity of the quiescent current and consequently the power dissipation to the offset voltage of the error amplifiers.

Suppose the output transistor QP in the saturation range :

$ID(QP) = \beta (V_{gs} - V_t)^2$ where β depends on the technology and the channel size.

$\frac{\Delta ID}{ID} = \frac{2AEP V_{offset}}{(V_{gs} - V_t)}$ AEP is the error amplifier open loop gain.

Fig 3 : Complete line driver schematic

To keep the quiescent current variation reasonably low we must choose a low value for the gain AEP . But a limit for decreasing this gain is the closed loop nonlinearity due to the

output device distortion. The compromise value used in our design is $AEP = AEN = 18$ dB. In order to maintain a large linearity range we make use of large size for the output devices, especially for the PMOST : $W = 800 \mu m$.

The figure 3 shows the complete line driver schematic. Transistors Q56, Q56, Q65 and Q66 have long channels intended to decrease the open loop gain.

This design was implemented in DMILL technology (Durci Mixte sur Isolant Logico-Linéaire) [10] and its transient response measured with a 50Ω load is shown in figure 4. Figure 5 shows the nonlinearity curve.

Fig 4 : Driver transient response to a step at 77K

nonlinearity

Fig 5 : Driver nonlinearity in full scale range units

Other performances of this driver in the cold (77K) are as follows :

power supply	= $\pm 3V$
power dissipation	= 10 mW
bandwidth	= 30 MHz
output resistance	= 4Ω
slew rate	= $330 V / \mu s$

Compensation capacitors C1 and C2 create dominant poles with the error amplifiers output resistances in order to improve the phase margin.

IV. CMOS PREAMPLIFIER WITH A 50 Ω LINE DRIVER TESTING RESULTS

The current preamplifier shown in part 2 was integrated with the line driver in two different CMOS technologies from MIETEC and AMS. 512 channels of the MIETEC version were utilized to equip 4 preshower modules. Their outputs were integrated by 40 ns gated integrators and digitized by 12-bits ADC's. The muon signal obtained is plotted on figure 6 and compared with the noise fitted as a gaussian. It was reconstructed by adding the contributions of two adjacent cells. The active liquid argon gap was 10 mm [11]. One can see a good performance with respect to the signal to noise ratio (4.3), however the peaking time measured for the impulse response was only 40ns.

Figure 6 : Muon signal and noise in two preshower layers

The speed was the main performance we tried to improve when designing another version of the circuit in AMS technology. A great care was taken about parasitic capacitors. Figure 7 shows the impulse response obtained with the AMS version at 77K, one can see that the rise time is 10 ns. The equivalent noise charge measured without any shaping was 2400 ± 30 electrons rms / pF.

Fig 7 : Impulse response at 77K on a 50 Ω load

The noise can be computed as an equivalent input noise calibrated with the triangular input current amplitude ; this is

called ENI (Equivalent Noise Current), and is shown in figure 8 according to the shaping time of a CR-RC² filter.

Fig 8 : ENI as a function of the shaping time with a 22pF detector capacitor at 77K

The gain calibrated with a triangular current pulse was $67 \text{ mV}/\mu\text{A}$.

The power dissipation depends on the bias voltage of the buffer, the linearity range required and above all on the offset. These parameters explain the following results difference from those indicated at part III for only the driver in DMILL technology. The typical value was 23 mW for a linearity range better than 3% from -1.7V to +1.5V, and $\pm 3\text{V}$ bias voltage. But we measured only 8mW for a -1.1V to +1.3V linearity range with -1.5V to 4.5V bias voltage.

V. CMOS INTEGRATED BIQUAD SHAPER

The shaper is an important element in the readout electronics for two major reasons. It is necessary to improve the signal to noise ratio, but also due to the high counting rates with the LHC, pulse pileup is another important problem. The current signal produced in a LAr preshower detector by a charged particle traversing the gap has a characteristic triangular shape with a drift time typically about 260 ns [12].

It has been shown that the energy deposited information can be obtained in a shorter time by observing a fraction of the induced charge. The shaper is used for this signal clipping. An important point for this pulse shaping is that its impulse response has zero area [13].

During the previous tests of a RD3 preshower prototype discrete component gated integrator and CR RC² shapers have been used. But a RC time constant filter integration is very difficult in CMOS technology because of the important process parameter deviation [14]. We use the so called biquadratic structure because it has low component sensitivity [15]. Figure 9 shows the generalized form for the circuit architecture.

The transfer function is :

$$H(s) = \frac{K \frac{\omega_p}{Q_p} s}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2} \quad \text{where } s = j\omega$$

$$\omega_p = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad \frac{\omega_p}{Q_p} = \frac{C_1 + C_2}{R_2 C_1 C_2}$$

and $K = -\frac{R_2 C_1}{R_1 (C_1 + C_2)}$

The integration of this shaper requires a high performance amplifier [16]. We used a fully differential folded cascode architecture, which is one of the best ways to improve the gain and the speed [17] [18] [19] [20] [21].

The overall schematic of the amplifier is shown in fig. 10.

Fig 9 : Single amplifier bandpass biquad filter.

Fig 10 : Overall schematic of the operational amplifier

The input stage has a complementary architecture. In the linear range, both N and P transistor pairs are active and give a push pull response to the stage which increases the gain.

Transistors M49, M51, M54 and M55 form the folded cascode stage.

Transistors M90 - M98 constitute a common mode feedback (CMF) to set the dc voltage of the two differential outputs Vo1 and Vo2.

The output stage is another important point for this amplifier. It uses the benefits of the complementary and differential nature of the input stage. When one of the intermediate output nodes is close to VDD, the other is close to VSS. As a result, when one of the output transistors is heavily conducting, the other is off. Since the output transistors can have rail to rail Vgs voltage, for a given output current they can have smaller sizes (400 μm for channel width). According to the simulation, this output stage is capable to drive a 50 Ω load, but it increases the power

dissipation.

The simulation results for this operational amplifier are as follows :

supply voltage	$\pm 4\text{V}$
load capacitor	1 pF
dc gain	83 dB
unity gain bandwidth	60 MHz
slew rate	28 V/ μs
phase margin	76°
gain margin	22 dB
dc power dissipation	27 mW.

The circuit has been designed in AMS 1.2 μ CMOS. The typical dc gain measured for the operational amplifier is 64db. The filter's magnitude response measured in the cold has a center frequency of 7 MHz (figure 11); this is equivalent to a fast shaping time of about 23 ns.

Fig 11 : Transfer function mesured at 77K.

The time domain response to a triangular shape signal is shown at figure 12.

Fig 12: Response to a triangular shape signal at 77K

VI CONCLUSION

The results presented show that CMOS is a promising technology for analog front-end electronics at cryogenic temperature. The noise and speed performances make the current conveyor preamplifier suitable for the liquid argon preshower. The linearity range measured for the 50Ω line driver is close to $\pm 2V$, with a 11ns typical step response rise time. The biquadratic architecture shaper results show a 23ns equivalent shaping time ; it will be necessary to optimise this value with an external resistor or capacitor. A DMILL rad-hard technology version will be soon available, for testing in gamma-rays low dose rate environment.

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