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Implementation and Synchronisation of the First Level Global Trigger for the CMS Experiment at LHC

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Abstract

The hardware implementation of the First Level Global Trigger for the CMS experiment at the CERN Large Hadron Collider LHC is described. Special emphasis is given to the algorithm logic and the synchronisation procedure. Up to 128 different trigger algorithms are calculated in parallel by the Global Trigger for every beam crossing taking place in 25 ns intervals. Already at the first trigger level the Global Trigger is able to select complex topological event configurations by performing fast calculations. The electronics is based on VME and relies completely on FPGA technology. The electronic circuits are optimised for speed by exploiting to a great extent the small look-up tables provided in the FPGA chips.

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1 Introduction

The CMS [1] First Level Trigger System is designed to identify every 25 ns, the time between two bunch crossings, signatures for muons (μ), electrons, photons, jets and neutrino-like particles. The trigger receives quadruplets of objects ordered by rank, which is a function of transverse energy (E_T) or momentum (p_T) and quality criteria. Simplified data from the Barrel Drift Tube Chambers and the Endcap Cathode Strip Chambers and data from the Resistive Plate Chambers are combined to find the best four muons with the highest p_T and of best possible quality [2]. The Calorimeter Trigger [3] uses simplified data from the Electromagnetic and the Hadron Calorimeters to calculate the total transverse energy (ΣE_T), the magnitude and direction of the missing transverse energy (E_T^{miss}). In addition it delivers four isolated and four non-isolated electrons/photons, four tau-jets, four jets in the central and four jets in the forward regions. Also numbers of jets for different thresholds in the central and forward region are calculated. The calorimeter data carry besides E_T the spatial quantities pseudo-rapidity η and the azimuthal angle ϕ around the beam line. The muons carry in addition a Charge (or Sign) bit, a MIP bit representing compatibility with minimum-ionizing particles and an Isolation bit, which can be used to set more precise trigger conditions.

The Level-1 Global Trigger (GT), the final part of the Level-1 (L1) trigger system, uses all these quantities to calculate up to 128 different trigger conditions denoted as ‘algorithms’ in parallel. It does not only apply thresholds for E_T and p_T but may also require particles to be in defined pseudo-rapidity or ϕ windows. Muons, electrons and jets for example may be required in the forward or in the central region. The conditions can be combined to find for instance central muons in conjunction with forward jets. For the azimuthal coordinate ϕ the conditions are normally used only for calibration and tests. Furthermore the Global Trigger calculates the distance between two particles in pseudo-rapidity η and in the azimuthal angle ϕ to trigger already at the first level on back-to-back muons, jets and electrons. For muons the Charge bit can be used to trigger for example on muons of opposite Charge.

A final OR-function combines all active algorithms to a Level-1 Accept (L1A) signal that is sent via the Timing, Trigger and Control (TTC) optical network to all readout units of the sub-detectors to move data of the current bunch crossing (bx) from their pipeline- or ring buffers into de-randomising memories. Later the bx-data are fetched by the Data Acquisition (DAQ), first to calculate in software more sophisticated trigger algorithms (High Level Trigger) and finally to store accepted events. Trigger Rates can be kept under control by adjusting energy or momentum thresholds of physics objects or by prescaling algorithms corresponding to large cross-sections. In addition due to rate limitations of some sub-detectors a set of trigger rules is applied to throttle excessive instantaneous rates. These rules are implemented in the logic of the Trigger Control System (TCS) and have to be set such that the overall dead time stays below the order of 1 percent. The concept of the CMS Level-1 Global Trigger is described in detail in [4].

The structure of the Global Trigger electronics has been designed keeping the physicist’s requirements in mind. If one wants to set a new trigger condition all input channels should be available in one place to combine them without any restriction. Also one should not be restricted by other triggers, already in use for some time. Therefore after synchronisation all input channels go to one printed circuit board (pcb), the Global Trigger Logic (GTL) board. As not all data bits can be connected to one FPGA chip, each trigger object or ‘particle’ goes to 2/3 of the ‘Condition Chips’ where all ‘Particle Conditions’ and spatial relations between different types of particles are calculated. Then the Particle Conditions are combined to complete trigger algorithms. The majority of algorithms are created already in the Condition Chips and only the most complicated algorithms are completed in the following Algorithm Chips. The connections between the Condition- and the Algorithm Chips provide the flexibility wanted by the user.

The Global Trigger is implemented in FPGAs using 40 MHz pipelined logic to run without dead time and to provide a trigger decision every 25 ns, synchronously with the LHC clock.

2 System Overview

The Global Trigger crate (VME 9U) contains three different entities, the Global Trigger (GT), the Global Muon Trigger (GMT) and part of the Trigger Control System (TCS). Only the actual Global Trigger will be described in this note. Figure 1 shows the crate layout.

Figure 1: Global Trigger hardware overview

The Pipelined Synchronising Buffer (PSB) input modules synchronise all calorimeter input channels to the local 40 MHz clock, then to the LHC orbit and finally to each other. All input bits are stored there in Dual Port Memories to be extracted in case of readout requests. The muons are already synchronised at the entry of the Global Muon Trigger. The synchronisation procedure compensates for different latencies to combine data from the same bunch crossing for the following algorithm logic.

A Global Trigger Logic (GTL) module combines the input channels and calculates up to 128 trigger algorithms in parallel. In total the GTL logic board for the physics algorithms accepts four muons and 24 calorimeter channels. Four free channels are available for future additions of trigger objects. An algorithm bit, which represents a complete physics trigger condition, is composed by an AND-OR function of Particle and Delta Conditions. Particle Conditions may require that E_T or p_T is above a threshold, that the particles are within a selected window in η and/or in ϕ and/or that two particles are opposite or close to each other in η or/and ϕ etc. Additional 'Delta Conditions' calculate relations in η and ϕ between two particles of different kinds. The logic structure was designed to give physicists already at the first trigger level possibilities to set topological trigger conditions and to run many physics triggers independently in parallel.

The Final Decision Logic (FDL) module combines all algorithm bits by a final OR to generate the L1A signal that starts the Data Acquisition System and the High Level Trigger software. Rate counters for each algorithm and dead-time counters to monitor the trigger system are also foreseen on this module. All algorithms can be pre-scaled to limit the overall L1 trigger rate. Several final OR's are provided in parallel to run sub-detectors independently for tests and calibration.

The Trigger Control System (TCS) module throttles excessive instantaneous L1A rates and provides calibration control signals for all readout and trigger crates. It receives so-called 'Fast Signals' to consider the status of the readout and Level 1 trigger electronics. The fast signals are converted to Channel Link[®] format in a VME 6U crate shown in Figure 1 and sent to PSB modules. The TCS will be described in a separate publication.

The Global Trigger Frontend (GTFE) module collects the trigger data from all modules after a readout request (Level-1 trigger) and sends them like any other detector part to the Data Acquisition System. In case of a Level-1 Accept the Global Trigger data are read like any other subsystem. The readout requests arrive via the TTC network on the Timing board (TIM). The requests are queued, a bunch crossing number is appended and then they are broadcast to all Global Trigger boards, including those of the Global Muon Trigger (GMT). On each board a Readout Processor chip extracts data from the ring buffers, adds format and synchronisation words and

sends the event record to a readout module, the Global Trigger Frontend (GTFE) board. The incoming data are checked and combined to one Global Trigger event record. According to an identifier the events are collected either in monitoring memories or are sent to the DAQ interface.

The Timing (TIM) module provides the clock and other fast control signals for the crate. It contains a timing receiver chip (TTCrx) that is linked to the common clock distribution system (TTC).

The backplane of the Global Trigger crate is fully custom-built. The upper part carries all VME signals for 32-bit access. The lower part contains all point-to-point links between all GMT-, GT- and TCS boards. The leftmost three slots are foreseen for standard VME modules.

3 Input Data

3.1 Input from Global Calorimeter Trigger

The Global Calorimeter Trigger (GCT) sends 4 non-isolated and 4 isolated e/γ , 4 central and 4 forward jets, 4 τ -jets, the total transverse energy ΣE_T , the missing transverse energy E_T^{miss} and 8 numbers of jets above different thresholds two of which are reserved for forward jets. The quadruplets of trigger objects are sorted by rank, which is a function of E_T and quality criteria. If fewer than four objects are found, the channels of lower rank are empty. The bit pattern of particles and jets contains E_T , the pseudo-rapidity η , the azimuth angle ϕ and several control bits. Missing and total transverse energies consist of 12 bits, whereas the numbers of jets above thresholds are represented as 4 bits. The detailed description of all bits is given in [4].

The GCT is located close to the Global Trigger crate and sends the trigger data on Ethernet cables using 21 bit Channel Link[®] drivers. Due to the very low error rate no error bit correction is foreseen. A simple parity check will detect faulty hardware channels. The GCT sends the two least significant bunch counter bits on each channel for comparison with the local GT bunch counter. If the offset (modulo 4) changes during the run the synchronisation to calorimeter data is lost and an error condition is encountered.

3.2 Input from Global Muon Trigger

The Global Muon Trigger (GMT) is mounted in the Global Trigger crate and sends the best four muons immediately as parallel signals via the backplane to the GTL logic boards to keep the latency as small as possible. Besides p_T , η and ϕ , a Charge or Sign bit, an isolation bit, a MIP bit indicating compatibility with a minimum-ionising particle and three quality bits complement the properties of muons [2]. The muons are sorted like the calorimeter channels. The scale of the transverse momentum p_T is non-linear and does not have to be identical for all types of physics runs or different luminosity values. It can be optimised by the Muon Trigger subsystems according to physics requirements.

3.3 Monitoring of input data

All input data are stored in Dual Port Memories (DPM) working as a ring buffer. Every LHC orbit the bunch counter reset (BCReset) signal clears the DPM address counters making the address equal to the bunch crossing number (modulo L, if the DPM of length L does not contain a complete LHC orbit). Data from the previous LHC cycle are overwritten. If data from the first bunch crossing are written into the first memory address then incoming data are synchronised to the LHC orbit as detailed in the bunch crossing synchronisation procedure below.

The size of the memories is chosen to keep the trigger history for a sufficient length of time. The DPMs can be read by the readout processors (ROP) due to a readout request or by VME for tests.

4 Synchronisation

The synchronisation hardware is located in FPGA chips on 12 channel PSB boards shown in Figure 2. The boards are also used by the Global Muon Trigger and the Trigger Control System to synchronise and monitor

other input signals. A 6-channel prototype board (Fig.12) has been built to verify the synchronisation procedures.

Figure 2: PSB board

The incoming Channel Link[®] signals are converted back to parallel words of 21 bits at a rate of 40 MHz. The Channel Link[®] receivers send two channels to each Synchronisation Chip.

Figure 3: Synchronisation Pipeline

In the Synchronisation Chip each input channel is first synchronised to the local 40 MHz clock by fine time adjustment and then to the LHC orbit. Finally all channels are synchronised to each other by starting at the same time the transfer to the GTL logic modules where data from the same bunch crossing arrive concurrently.

Muons from the Regional Muon Trigger Systems are synchronised already to each other and to the LHC orbit by a similar circuit at the input of the Global Muon Trigger. The best four selected muons are sent without any further delay via the backplane to the GTL modules to keep the overall L1 latency as small as possible. Therefore the worst case latency of the Global Trigger has to be seen in context with the Global Muon Trigger.

The waiting time for the calorimeter objects has to take into account the latency of the Global Muon Trigger electronics.

4.1 Fine time adjustment of input channels

As software can change the clock phase of the GCT and Muon Trigger crates relative to the Global Trigger crate, input data from these crates cannot be captured safely by cutting the interface cables to an appropriate length. To find the best 'cable length' the Synchronisation Chip samples all parallel input bits four times per bunch crossing (160 MHz) and selects the best sample to send the input data into the following synchronisation pipeline as shown on the left side of Figure 4. If the phase of an input channel changes a different sample is selected to store the data bits.

To find the best sample a XOR2 gate compares two consecutive samples of a bit to find level transitions, which are then counted during an LHC orbit. This circuit exists four times to compare each sample with the preceding one (pre-4th to the 1st sample, the 1st to the 2nd, etc.). The distribution over the four counters accumulated over several orbits shows the transition time as illustrated in Figure 4. A sample that is far away from the switching time of the input data is selected to send all bits into the synchronisation pipeline. The distribution shows the time stability of an input channel relative to the local clock and can be used to monitor input channels continuously.

To check input data later also by monitoring software all four samples of one bit are appended to the corresponding input word for every bunch crossing. Test measurements on the prototype board have shown that the transition time moves as expected with the length of input cables.

Figure 4: Fine Time Adjustment of input channels

4.2 Bunch Crossing Synchronisation

Each Synchronisation Chip contains a Bunch Crossing (BC) counter, which defines the local bunch crossing time. It receives a common 'Bunch Counter Reset' (BCReset) signal to lock the circuit to the LHC orbit. If the reset signal is not sent every orbit a LIMIT comparator resets the BC counter after 3564 (programmable) bunch crossings automatically. But a common periodic BCRreset signal guarantees that all local counters in the crate run synchronously.

Figure 7: GTL board

5.1 Predefined Conditions and Configuration

To ease the design of a Condition Chip several predefined types of template circuits for each type of 'particles' are used like building blocks to compose predefined Particle Conditions. In the Particle Condition circuit the input data are applied to a set of Single Particle and Correlation templates and the results are combined by an AND-OR function. The predefined Particle Conditions were tested with worst case values to meet a maximum latency and space requirement. Also Delta Conditions as explained below between different 'particle' types are predefined. The predefined Particle and Delta Conditions are then used to compose Algorithms representing a physics trigger.

Actual Particle and Delta Conditions are created loading the look-up tables of all used templates with actual values and placing the circuits on the chip. Several Conditions are then combined either to complete Algorithms or still incomplete Pre-Algorithms and connected to an output pin. A set-up & layout program (Fig.10) is used to define the parameters for actual Pre-Algorithms or Conditions and to place them on the FPGA chip. The program delivers VHDL files, which are appended by the ALTERA Quartus software to the more general VHDL code to complement the design for an actual Condition Chip. A similar set-up program defines the content of the following Algorithm Chips designed either to pass on already finished algorithms or to combine Pre-algorithm bits to entire Algorithms.

5.2 Calorimeter 'Particle' Conditions

The 'single particle' template circuit consists of three comparators for E_T , η and ϕ . A magnitude comparator compares the transverse energy E_T against a programmable threshold. A look-up table (LUT) window comparator searches for particles inside η window(s). A 'forward' window designates actually two windows in hardware corresponding to the forward and backward η -hemispheres of the detector. Another LUT window comparator normally used only for tests finds particles inside ϕ windows. Figure 8 shows a LUT comparator for η windows. The content of the small $n \times 1$ memory defines the function and the thresholds of a window comparator. This circuit allows putting many trigger conditions into one FPGA chip. Recompiling the chip can change the thresholds however. Therefore all checks for E_T and P_T are implemented as standard comparators and the thresholds are loaded via the VME bus.

Figure 8: LUT window comparator

Besides the template for a single particle an η - and a ϕ spatial correlation template checks for two particles opposite or close to each other in η and ϕ . The differences $|\Delta\eta|$ and $|\Delta\phi|$ between two particles are calculated and applied to a look-up table window comparator to find within a defined tolerance region particles opposite or close to each other in η or ϕ .

Both template types are now used to build predefined conditions for two and four particles. The 2-particle condition consists of two single particle templates programmed either with the same or with different values. The four ‘particles’ of a group are applied as pairs in all possible permutations (12,13,14,21,23,24,31,32,34,41,42,43) to the template set. On the chip each single particle template circuit exists four times, once for each particle, but each output goes to three AND2 gates. The following AND2-OR12 logic should find out whether at least a pair of ‘particles’ fulfils the requirements of the template set. (*Remark: The output of an AND2 gate is true if both input signals are true. The output of an OR12 gate is true if at least one of the twelve input signals is true.*)

The 4-particle condition consists of four single particle templates programmed either with the same or with different values. The four particles are applied as quadruplets in all possible permutations (1234, 1243, etc.) to the template set. On the chip each template circuit exists again 4 times, once for each particle. The following AND4-OR24 logic should spot a permutation of particles that fulfils all conditions of the template set. If fewer than 4 particles are required for a particular algorithm the unused templates are set to trivial values.

The 2-particle condition with a spatial correlation consists of two single particle templates and of an η - and a ϕ spatial correlation template. The four calorimeter ‘particles’ of a group are applied pairwise in all possible permutations as above to two single particle templates and additionally to both correlation templates for η and ϕ . On the chip each particle template circuit exists four times, but the $|\Delta\eta|$ and $|\Delta\phi|$ correlation circuits are needed 6 times. The following AND4-OR12 logic searches for a pair of particles that fulfils the requirements of all single and correlation templates. Figure 9 shows the structure of the electronic scheme of this condition and Figure10 illustrates the set-up program for the chip. The example shows a condition for two isolated electrons/photons from the barrel region of the calorimeter. Both particles also have to be opposite to each other in η and ϕ and have to fulfil different threshold conditions for their transverse energies. It should be mentioned that η uses a pseudo sign bit to distinguish between both detector sides. Therefore if a condition requires two

particles opposite to each other in η with a zero difference they are expected to come from opposite η hemispheres.

Figure 9: Two-particle condition with spatial correlation

Figure 10: Set-up of condition for 2 electrons with spatial correlation

5.3 Muon Conditions

For Muons the logic structure resembles the one for the calorimeter particles. Due to the presence of charge, isolation and quality information, the conditions are, however, more complex.

The Single Muon template circuit consists of a $p_T \geq \text{threshold}$ comparator and LUT window comparators for η and ϕ as for the calorimeter data. In addition it contains another p_T comparator to check for the Isolation bit depending on p_T . This is necessary if one would like to accept a muon of very high p_T regardless of the isolation requirement, and a muon of relatively low p_T only if it is isolated. For Quality bits an 8x1bit LUT to find any of the allowed quality values exists.

The η and ϕ -correlation templates check for two muons opposite or close to each other in η and ϕ . Other values of space difference can be checked upon by the Higher Level Triggers.

The Sign (or Charge) correlation template checks for any possible Sign/Charge pattern of up to four muons. A 16x1bit LUT is loaded with '1' at the addresses representing valid Sign patterns and with '0' for unwanted patterns. Also the MIP bit correlation template checking for any required bit pattern is implemented as a 16x1bit LUT. If fewer than four muons are requested the corresponding address-bits for the Sign and MIP look-up tables are set to '0'.

Again the templates are used to compose predefined Muon Conditions. The same three types of conditions as for the calorimeter particles are implemented for two and four muons. They are, however, more complicated. The template circuits are multiplied as above to find a fitting pair or quadruplet of muons. If less than four or two muons are required for a particular algorithm then the dispensable templates are set to trivial values (e.g. $p_T \geq 0$ GeV/c, $0^\circ < \phi < 360^\circ$ etc.).

A dimuon condition consists of two single muon templates, a Sign template and a MIP bit correlation template. The four muons are applied as pairs in all possible permutations to detect the two muons meeting all requirements. A dimuon condition with spatial correlation contains additionally four correlation templates for $\Delta\eta$, $\Delta\phi$, Sign and MIP bits.

A 4-muon condition consists of four single muon templates, a Sign- and a MIP bit correlation template. The four muons are applied in all possible permutations (1234, 1243, 1324, etc.) to a set of templates to find a permutation that fulfils all the conditions.

5.4 Calorimeter Conditions for jet counts and Total and Missing Transverse Energy

Conditions for these trigger objects consist only of simple threshold comparators. For the missing E_T conditions ϕ -windows can be appended for tests. The E_T thresholds are loaded by VME.

5.5 Topological triggers

The possibilities how to select particles in defined pseudo-rapidity η -windows and how to find pairs of particles with predetermined correlations in η or ϕ are described in the following.

η -windows are important to find one particle in the barrel and another particle of the same or of a different type in the endcap region. If jets are involved, for example forward tagging jets, there is an additional possibility to use explicitly the forward jets sent by the Global Calorimeter Trigger. With the logic foreseen in the Particle Conditions the determination of η - or ϕ -correlations between a pair of particles of the same type is possible. One can find objects opposite or close to each other in η and ϕ within a programmable tolerance. For muons, correlations in ϕ will be made with reduced resolution to save logic resources and to meet timing constraints inside the FPGA chips.

For space relations between different types of particles special 'Delta Conditions' have been designed. The $|\Delta\eta|$ and $|\Delta\phi|$ differences between all possible pairs of two particle groups are calculated. The differences are compared to limits to trigger on objects opposite or close to each other in η and ϕ within a programmable tolerance. Both conditions in $|\Delta\eta|$ and $|\Delta\phi|$ can be applied concurrently to trigger on a spatial relation. However, it should be remarked that the trigger does not calculate a true three-dimensional distance in space. If muons are compared with calorimeter 'particles' the muon values, which have greater precision, are converted to calorimeter units using look-up tables. The participating particles have to fulfil also E_T and P_T requirements. An example requiring the Delta Condition would be a trigger on a jet and a muon opposite to each other in ϕ . Both objects could be restricted to a defined η region.

5.6 Special algorithms

Several algorithm bits are reserved for special runs used for data checking, calibration, synchronisation and hardware testing purposes. The conditions cannot be completely fixed at this time since the running-in phase of the CMS detector at the start-up of the LHC will influence the needs for special procedures. Some of the special algorithms will be programmed into the Algorithm Chips, others into the Final Decision FPGA or even appended to the calibration control logic.

The following special triggers will certainly be needed during the entire lifetime of the detector:

- A Random Trigger with programmable rate and start value for calibration and testing,
- A Synchronisation Trigger to trigger at a selected bunch crossing number, with a pre-scale option,
- A Single Channel Trigger for a specific input channel. The algorithm bits are used for synchronisation to the LHC orbit.
- A Minimum Bias Trigger to check trigger efficiencies,
- An external trigger generated by various sources.

6 Final Decision Logic

The FDL module depicted in Figure 11 contains the Final Decision Logic that combines all or a subset of algorithm bits to L1 Accept signals. Up to 8 different final L1A signals are provided for partitions of sub-detectors. The FDL module receives 128 algorithm bits per bunch crossing from the GTL module and some signals from the Trigger Control System where external signals can be combined to generate special trigger signals. Each algorithm bit can be downscaled by a programmable factor to keep the final trigger rate under control. Then all or a subset of algorithm bits are selected by Algorithm Masks to make the final L1 Accept signals, which are forwarded by the TTC system to all sub-systems to save data from the front-end buffers. A common L1 Accept is sent concurrently to the Event Manager to start the CMS data readout. Additional bits inform the Event Manager to which sub-detector partitions the L1 Accept signal has been sent.

All algorithm bits and the final decision for every bunch crossing are stored in DPMs used as ring buffers to be read later by the Data Acquisition System.

Figure 11: FDL Final Decision Logic board

7 Prototypes and Tests

All final modules are conceived as 9U VME boards. Prototypes for the backplane, the PSB and the GTL boards are built as 6U VME boards (A32, D32) [5]. All other boards will be designed only in the 9U final version. The PSB-6U and GTL-6U prototype boards can be used in the final 9U VME crate with the other 9U boards to allow continuous upgrading. Concurrently to board production test software written in the National Instruments CVI environment has been developed.

The 6U VME backplane provides all slots for the Global Muon Trigger and the Global Trigger. It contains the VME signals, all clock and timing signals, the Readout Request bus (RO-bus), the JTAG bus, all point-to-point Channel Links® for the readout and the connections between the PSB input boards and the logic boards of the GMT and the GT. For the VME part 160-pin connectors are used, for all other signals AMP 2mm Z-pack connectors [6]. A pneumatic press and tools have been designed and built for mounting the 'press-fit' connectors on the backplane and VME modules.

The PSB-6U prototype shown in Figure 12 accepts 6 input channels. The synchronisation logic is the same as on the final 9U boards for 12 channels and has been implemented with XC4000XL chips [7]. For the ring buffer DPM chips were used.

The GTL-6U board contains the algorithm logic for the muons and four groups of calorimeter trigger objects; three more groups will be added on the final board. The functions are designed as for the final board but not with the full number of Particle Conditions. The Particle Conditions are implemented in Altera APEX chips. The extended AND-OR logic for finding a valid particle permutation is done in the ESB block of the chips [8].

All boards are connected to the backplane JTAG bus and can be accessed separately using a boundary scan slot number. All FPGA chips with boundary scan pins are included in one JTAG chain per board. An additional JTAG connector on the boards allows stand-alone JTAG tests.

The FPGAs can be loaded either by VME or PROMs or JTAG.

Figure 12: PSB prototype board

8 Summary

The main electronic circuits for the CMS Global Trigger have been designed and built on prototype boards. The synchronisation procedure of input data to the local clock, to each other and to an LHC orbit has been tested.

For the trigger algorithms a feasibility study with an FPGA layout simulating a worst case scenario has been performed. An overall latency of 5 bunch crossings for algorithm calculations including topological conditions for the same type of trigger objects has been achieved already with Altera Apex chips of speed grade -2. It is expected that most actual trigger conditions will be of much simpler structure and will consume less space on the chip and will therefore fulfil the latency requirements more easily. For additional safety faster chips of speed grade -1 can replace the actual FPGAs. Currently the set-up of new trigger conditions needs a considerable time. It is planned to improve the set-up program and to automate the FPGA development cycle.

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