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Delta: A charge sensitive front-end amplifier with switched gain for low noise, large dynamic range silicon detector readout

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Abstract

The design and results of a radiation hard switched gain charge amplifier optimised for a large dynamic range and large input capacitance are described. The peaking time is 25 ns, dynamic ranges are 0.1 - 50 minimum ionizing particles (MIPs) (high gain) and 1 - 400 MIPs (low gain), signal to noise (S/N) > 10 for $C_{in} < 56\text{pF}$ and radiation tolerance to 10 Mrads(Si) and $4 \times 10^{13} \text{ n cm}^{-2}$.

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1 Introduction

The readout of silicon detectors used to measure energy deposition in electromagnetic showers presents a number of challenging design issues for the ASIC circuit designer. For the CMS Preshower detector (1) these include a detector loading capacitance of more than 40pF, peaking time of 25ns, dynamic range from 1 - 400 MIPs (4fC - 1600fC) of input charge, S/N ratio better than 10 (for calibration at the single MIP level) and radiation hardness to 10 Mrads(Si) and $2 \times 10^{14} \text{ n cm}^{-2}$. The Delta amplifier has been designed to meet these requirements and has been manufactured as a BiCMOS ASIC chip in the DMILL technology.

2 The Delta switched gain channel design

Figure 1 shows the Delta channel architecture. It consists of 3 blocks, namely the Delta preamplifier, leakage current compensation (LCC) unit and a switched gain shaper. The preamplifier provides a step like function with a fast edge followed by a slow tail back to the operating point. A CR-RC² shaper is then used to filter the signal (minimizing noise), and to change the gain of the output signal. This latter feature is used to increase the gain of the channel when precision measurement of small signals is required such as during calibration, thus maximizing the S/N of the system. For the CMS Preshower, two modes of operation have been defined :

- Run mode (low gain), full dynamic range (1 - 400 MIPs)
- Calibration mode (high gain), reduced dynamic range (0.1 - 50 MIPs)

The LCC monitors and subtracts detector leakage current from the DC coupled input enabling the preamplifier to operate despite detector leakage currents induced by radiation damage.

Figure 1: The Delta switched gain channel architecture

2.1 The Delta preamplifier design

The schematic diagram of **Delta** is shown in figure 2. The design uses a BiCMOS folded cascode input stage to amplify the signal through **T1** and **Mpc** to node **b**. An emitter follower then replicates the voltage at **b** onto a low impedance output node (**Out**). The detector charge is stored as a voltage across capacitors **Cf1** and **Cf2**. The stored charge then decays through **Rf** restoring the amplifier to its operating point.

For large dynamic range careful consideration needs to be taken with respect to the dc operating conditions. The signal voltage level at the output has a lower limit defined by the saturation voltage V_{dsat} of **Mn2**, which is 400mV. The upper limit is defined by $vdd - (MplV_{dsat} + MpcV_{dsat})$, which is 3.3V (assuming **Vdd**=5V) allowing a total possible negative signal swing of 2.9V. The pre-amp. gain is set to 6.4 mV/MIP, which gives a total possible pre-amp. dynamic range of 450 MIPs.

2.2 The Leakage Current Compensation (LCC) Unit

The leakage current compensation circuit is an Operational Transconductance Amplifier (OTA) connected in the feedback of the preamplifier (2). Figure 3 shows the schematic diagram of the LCC unit.

Figure 2: The **Delta** preamplifier

Figure 3: The leakage current compensation circuit (LCC)

Leakage current is compensated by comparing the Delta output voltage with a reference voltage V_{ref} in Figure 1. Any tendency of the Delta output voltage to drift to a new operating value is corrected by diverting leakage current from the input of Delta into the output of the LCC. The main design criteria for an efficient LCC circuit is extremely low bandwidth, very high output impedance and minimum parallel noise contribution from MNo.

2.3 The switched gain shaper

The shaper is a second order CR-RCⁿ filter. The coupling capacitance C_{cs} during normal operation (low gain) is C_1 . Increased gain is achieved by switching in extra coupling capacitance C_2 in parallel with C_1 (see figure 4).

Figure 4: The switched gain shaper

Figure 5: Circuit diagram of the opamp used in the shaper with switchable input transconductance

It is important to match the central frequency (ω_c) and hence peaking time (T_p) in both high and low gains. The equation for ω_c (3) is:

$$\omega_c = \frac{1}{T_p} = \frac{1}{C_t} \left(\frac{g_{ms} C_{fs}}{C_o} + \frac{1}{R_{fs}} \right) \quad (1)$$

where $C_t = C_{cs} + C_{fs} + C_i + C_p$, $C_o = C_l + C_{fs}$, R_f the feedback resistance and g_{ms} the input transconductance of the shaper amplifier. The condition to match peaking times $\omega_{cHG} = \omega_{cLG}$ can be approximated to equation 2.

$$\frac{g_{msHG}}{C_{tHG}} = \frac{g_{msLG}}{C_{tLG}} \quad (2)$$

Figure 5 shows the circuit diagram for the amplifier used in the shaper. The change in g_{ms} is achieved by switching in an extra differential pair (transistors Mp3 and Mp4) in parallel with transistors Mp1 and Mp2, hence increasing the effective W/L ratio of the input transistors therefore increasing the g_{ms} .

3 Noise analysis

The noise model for the channel is shown in figure 6.

Figure 6: The Delta channel noise model with an ideal filter

Equations 3 to 7 show the rms equivalent noise current and voltage generators when referred to the input (4). Equations 3 and 4 refer to Delta and are defined on the properties of the input NPN transistor (T1) where i_b is the base current, R_{eq} it's equivalent noise resistance, $r_{bb'}$ it's extrinsic base resistance and g_m it's transconductance. The other parameters are (q) the electron charge, (k) Boltzmann's constant and T temperature. Equation 5 shows the contribution from the feedback resistor which is made negligible with a high value R_f . The contribution from the LCC unit is shown in equation 6 and is made negligible due to a low $g_{m(LCCMNo)}$. The rms eq. noise current generator from the detector is given in equation 7. The noise may then be expressed as Equivalent Noise Charge (ENC) as in equations 8 (for parallel noise) and 9 (for series noise) where I_1 and I_2 are weighting functions relating to the filter characteristics (5). The total ENC_t is the quadratic sum of these two components, equation 10.

$$\overline{i_{n\delta}^2} = 2q i_b \text{ where } i_b = \frac{i_c}{\beta} \quad (3)$$

$$\overline{e_{n\delta}^2} = 4kT R_{eq} \text{ where } R_{eq} = r_{bb'} + \frac{1}{2g_m} \quad (4)$$

$$\overline{i_{nf}^2} = \frac{4kT}{R_f} \quad (5)$$

$$\overline{i_{nlcc}^2} = \frac{6kT}{\Gamma} g_{mlcc(MNo)} \quad (6)$$

$$\overline{i_{ns}^2} = 2q i_s \quad (7)$$

$$\overline{ENC_p^2} = \frac{\sum \overline{i_n^2}}{2} I_2 \quad (8)$$

$$\overline{ENC_s^2} = \frac{e_{n\delta}^2 (C_d + C_f + C_{in})}{2} I_1 \quad (9)$$

$$\overline{ENC_t} = \sqrt{\overline{ENC_p^2} + \overline{ENC_s^2}} \quad (10)$$

There are important implications in the design of the input transistor T1 for optimizing the ENC for a given input capacitance. Note that $\overline{e_{n\delta}^2}$ is proportional to $r_{bb'}$, which could be reduced by increasing it's emitter area.

Also $\overline{i_{n\delta}^2}$ is inversely proportional to the β of T1. β however degrades through irradiation, the magnitude of which depends on it's current density. Reducing the emitter area of T1 increases current density resulting in a less severe β degradation after irradiation. Therefore minimum $\overline{i_{n\delta}^2}$ is achieved with minimum emitter area.

In this chip various channels were designed with different size input transistors to investigate this effect. A well modelled NPN device in DMILL technology is DNP10, which has an emitter area of $12 \mu m^2$. Channels were designed with 1, 2, 4 and 8 of these devices in parallel to make up T1. The number of devices in parallel (n) is therefore an important design parameter to optimise noise.

4 Measured Results

All measurements have been made using test pulses to inject charge corresponding to 4fC for each equivalent 1 MIP. Unless otherwise stated the input loading capacitance is 58pF.

4.1 Results before irradiation

The signal response for both high and low gains is shown in figure 7 for 100fC of input charge corresponding to 25 MIPs.

Peaking times in both gains are matched at 25 ns and remain constant for all input signals within the operating range. The undershoot is approximately 14% and returns to the operating point after 600 ns. Crosstalk has been measured at <2% worst case to the nearest neighbour. The gain remains virtually constant for up to $150 \mu A$ of leakage current. This is well beyond the requirements of the CMS preshower which is $20 \mu A$ per channel after 10 years of operation at LHC.

Pile up conditions have been tested using an input pulse corresponding to 20 MIPs at a rate of 5 MHz with no adverse effects on performance. Pythia simulations show the maximum expected pile up condition in the CMS preshower to be 2 MIPs at 2 MHz average.

The dynamic range for both gains can be seen in figure 8.

The required dynamic ranges are met i.e. 50 MIPs for high gain and 400 MIPs for low gain. The channel gain is approximately 30 mV/MIP in high gain and 4 mV/MIP in low gain. It is not perfectly linear. The gain/MIP increases by approximately 7% over the full signal range. This is due to an increase of g_m in T1 for large input signals as predicted by simulation.

The noise performance (measured in high gain) before irradiation is shown in figure 9. The ENC of 7 chips are plotted against input capacitance.

The average ENC is $640e + 33 \text{ e/pF rms}$ based on a linear fit. This shows that to achieve a $S/N > 10$ the total input capacitance should be $< 56 \text{ pF}$.

Figure 7: Signal response in both high and low gain for 100fC of input charge.

Figure 8: Dynamic range for both high and low gain.

Figure 9: Noise performance expressed as ENC for different levels of total input capacitance (measured in high gain)

4.2 Results after irradiation

Two chips were measured after exposure to ionizing radiation to a total dose of 10Mrads (Si) using an X-ray source. Another two chips were irradiated with neutrons to a fluence of $4 \times 10^{13} \text{ n cm}^{-2}$. Measurements were made shortly after irradiation with no attempt to anneal.

The most important device in the circuit from a noise point of view is the input NPN transistor T1. The β of this device was expected to degrade after irradiation and test structures were placed in the chip in order to measure this. The extent of β degradation to ionizing and neutron irradiation is tabulated in table 1 for the channels designed with different values of n for T1.

n	Current density	β w.r.t. ionizing radiation			β w.r.t. neutron irradiation		
		pre-rad.	10 Mrad (Si)	degradation	pre-rad.	$4 \times 10^{13} \text{ n cm}^{-2}$	degradation
1	400 μA	220	145	-34%	207	90	-57%
2	200 μA	219	130	-40%	206	76	-63%
4	100 μA	217	117	-46%	204	66	-68%
8	50 μA	213	102	-52%	201	53	-74%

Table 1: β before and after radiation as a function of the number of NPND10 devices in parallel (n).

Figures 10 and 11 show the measured ENC at $C_{in} = 58\text{pF}$ for 4 channels designed with different values of n for T1 both before and after irradiation.

The effect on the series noise due to the increase in $r_{bb'}$ as n tends to 1 is dramatic for large values of input capacitance. The increased noise after irradiation due to β degradation is hardly visible. The series noise component is by far the most dominant. Based on these results we feel that a suitable design value for n is 3 or 4 which maintains low noise with moderate β degradation.

Figure 10: Measured ENC at $C_{in} = 58\text{pF}$ for channels designed with different numbers of input devices in parallel (n) before and after ionizing radiation.

Figure 11: Measured ENC at $C_{in} = 58\text{pF}$ for channels designed with different numbers of input devices in parallel (n) before and after neutron irradiation.

5 Summary

The design and results of a switched gain charge amplifier (Delta) and shaper optimized for large dynamic range and input capacitance are presented. The results show that Delta is suitable for silicon strip readout with a S/N > 10 for total input capacitance $< 56\text{pF}$. The channel gain is switchable from 4 mV/MIP (dynamic range < 400 MIPs) up to 30mV/MIP (dynamic range < 50 MIPs). The peaking time for both gains is 25ns.

Radiation hardness is demonstrated up to 10 Mrad(Si) of ionizing radiation and $4 \times 10^{13} \text{ n cm}^{-2}$.

All design requirements for the CMS Preshower are met with the exception of neutron radiation harness. Further irradiation tests are necessary to a fluence of $2 \times 10^{14} \text{ n cm}^{-2}$ before this can be confirmed.

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