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Study of Edge Effects in the Breakdown Process of p^+ on n-bulk Silicon Diodes

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Abstract

The paper describes the role of the n^+ edge implants in the breakdown process of p^+ on n-bulk silicon diodes. Laboratory measurements and simulation studies are presented on a series of test structures aimed at an optimisation of the design in the edge region. The dependence of the breakdown voltage on the geometrical parameters of the devices is discussed in detail. Design rules are extracted for the use of n-wells along the scribe line to avoid surface conduction of current generated by the exposed edges. The effect of neutron irradiation has been studied up to a fluence of $1.8 \times 10^{15} \text{ cm}^{-2}$.

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1 Introduction

The silicon microstrip detectors foreseen as tracking elements for the LHC experiments, will be exposed to unprecedented radiation levels. The primary hadron-hadron interactions will produce a high flux of charged particles, gammas and neutrons. It is expected that after 10 years of LHC running, the innermost silicon microstrip detectors will have been exposed to an overall integrated fluence of about 1.6×10^{14} 1-MeV-equivalent neutrons cm^{-2} [1, 2].

All major experiments at LHC plan to employ, for the inner trackers, p^+ on n devices as baseline detectors, in order to reduce the costs and improve the reliability of the system. However, n -type silicon detectors, exposed to such radiation levels, will undergo type inversion and then a substantial increase of depletion voltage. Additionally, overdepletion will be needed to fully collect the charge and to lower the noise by reducing the interstrip capacitance. This requirement is particularly stringent for p^+ on n devices, which suffer from an increase of the interstrip capacitance with irradiation [3]. The possibility of raising the bias voltage during the experiment lifetime is limited by the onset of the breakdown process [4, 5]. The study of this phenomenon is crucial to ensure a large bias voltage domain and thus maintain a good stability in time of the detector system [6, 7].

One of the critical regions as far as breakdown process is concerned is the cut edge of the detectors. The space charge region extends laterally with the increase of the bias voltage and the free charge carriers collected at the exposed edges might act as a limiting factor for the breakdown performance. In order to prevent the space charge region to reach the cut border, n^+ implants in the edge region were proposed in several detector designs. The purpose of the work described in this paper is to find the best geometrical configuration in the region between the last p^+ guard-ring and the detector border. Special test structures were designed and irradiated with neutrons in order to understand the consequences on the avalanche breakdown process due to radiation induced damage.

2 Edge-1 and Edge-2 structures

To perform this study we have designed special structures called Edge-1 and Edge-2. They are simple p^+ implants produced by CSEM (Neuchatel, Switzerland) on lightly doped n -type wafers, (111) oriented and $300 \mu\text{m}$ thick, with the backside uniformly n^+ implanted. The diodes are positioned close to other test structures (MOS and guard-ring diodes) designed to measure device parameters, as the full depletion voltage, and process characteristics like the silicon oxide charge density.

The Edge-1 devices contain 6 circular p^+ implants of 1 mm diameter. The distance W between p^+ and n^+ implants varies from 25 to $250 \mu\text{m}$ (Fig.1).

The Edge-2 structures also have 6 diodes, this time with different diameters. In this case the distance W is fixed to $200 \mu\text{m}$ while the distance D from the p^+ implant to the scribe line varies from 250 to $600 \mu\text{m}$. For both types of structures, the p^+ implants were covered by an aluminium layer extending $5 \mu\text{m}$ outwards [8] and the surface is SiO_2 passivated (Fig.2).

The design reproduces rather well the standard design of edge region of silicon microstrip detectors characterized by the presence of n^+ implants.

For all layouts it is expected that the maximum electric field is situated close to the rounded border of the $p^+ - n$ junction, depending mainly on the fabrication technology (i.e. implant depth and lateral diffusion). The full lines in Fig.1 are the scribe lines used for the cutting procedure on all four sides. Edge-1 diodes are at a large distance ($500 \mu\text{m}$) from the border, to separate the effects given by the two different geometries.

For all geometries we have studied the breakdown performance as a function of the distances W and D . The variation of the breakdown voltage V_{BD} for different values of the Si-SiO₂ interface charge density was also taken into account [11].

3 Computer simulations

The software package used for simulations was ISE (Integrated Systems Engineering AG-ISE), version 4.1, developed at ETH Zentrum, Zurich, Switzerland.

The program models semiconductor devices calculating static and dynamic parameters in the initial conditions supplied by the user. MDRAW-ISE was used as a mesh generator, offering flexible 2-D device structure editing, for computations with DESSIS-ISE.

In the DESSIS-ISE main program, the junction breakdown due to avalanche generation is simulated by computing the ionization integral. The impact ionization process is defined as the generation of electron-hole pairs, under the condition that the electric field is high enough (above $1 \times 10^5 \text{ V cm}^{-1}$) for the charge carriers to participate in the

Figure 1: Layout of the Edge-1 and Edge-2 structures. The numbers on each diode refer to the distance W between the p^+ and n^+ implants and to the distance D between the p^+ implant and the scribe line.

Figure 2: Cross-sectional view of the Edge-1 and Edge-2 structures. Drawing is not in scale.

creation of further electron-hole pairs. The total number of electron-hole pairs created as a result of the generation of a single pair at a distance x from the junction, named multiplication coefficient $M(x)$, is defined as [9]:

$$M(x) = \frac{\exp \left[\int_0^x (\alpha_n - \alpha_p) dx \right]}{1 - \int_0^L \alpha_p \exp \left[\int_0^x (\alpha_n - \alpha_p) dx \right] dx} \quad (1)$$

The avalanche breakdown occurs when this coefficient tends to infinity. In this case, defining the ionization integral I , as:

$$I = \int_0^L \alpha_p \exp \left[\int_0^x (\alpha_n - \alpha_p) dx \right] dx \quad (2)$$

the program considers that the breakdown condition is reached when the ionization integral equals one [10]. The α_n and α_p are the impact ionization coefficients for electrons and holes. They represent the number of electron-hole pairs per unit length created by an electron (hole) traversing the depletion layer L along the direction of the electric field. These coefficients depend strongly on the electric field. For the simulation of Edge devices some data for implant shapes were taken directly from the manufacturer (CSEM, Neuchatel), while for other parameters laboratory measurements have been used (surface recombination velocity: 100 cm/s, carriers life time: 10^{-2} s).

4 Experimental and simulation results

All measurements were performed at INFN Pisa, Italy, using a standard semiconductor device measurement apparatus. The setup for room temperature measurements included an automatic Probe Station Karl Suss PA150. A HP 4142B picoamperometer DC source-monitor was used both as high voltage source and for I-V measurements. The devices were controlled by a computer running National Instruments LabViewTM software. The low temperature measurements were performed using a thermally isolated aluminium box with circulating dry nitrogen, and a cooling system to maintain -10°C inside. In this case, for I-V measurements a HP 4155A semiconductor parameter analyser and a Keithley 237 high voltage source were used. During I-V measurements, the junction side was kept at ground potential and the bias voltage was applied on the back side of the wafer, with the upper side n^+ implant left floating.

We first investigated the dependence of the avalanche breakdown process on the geometrical parameters W and D described above. As breakdown voltage the point where the current rises with an exponential law in a limited voltage range was taken. The I-V characteristics for all layouts were measured either until the breakdown process appeared or the current reached the compliance value of 10^{-3} A. Typical I-V characteristics of Edge-1 devices are presented in Fig.3.

Figure 3: I-V characteristics of a typical Edge-1 device, for varying distance between implants.

Figure 4: Comparison between experimental and simulated results for Edge-1 diodes.

The breakdown voltage initially increases with W and then saturates for values greater than $150 \mu\text{m}$. The same behaviour can be seen in Fig.4, where we plot the breakdown voltage as a function of W for two different devices. For comparison, we also show on the same plot the results of the simulation for two different silicon oxide charge

densities. A clear saturation of the breakdown voltage is seen for W greater than $150 \mu m$, regardless of the silicon dioxide charge concentration. The absolute value of V_{BD} does depend on the oxide charge and is in agreement with simulation data within the experimental errors [11]. This result suggests that, in order to improve the breakdown performance n^+ implants at the cut edge should be no closer than $150 \mu m$ from the outermost p^+ implant.

The I-V characteristics for Edge-2 diodes were measured before and after cutting and are presented in Fig.5.

Figure 5: I-V characteristics for Edge-2 diodes before and after cutting for different D values.

The I-V characteristics for a typical Edge-2 device are shown, in Fig.6. From these measurements we conclude that a safe design rule is to keep the distance D greater than $400 \mu m$.

Some effects are visible in these plots:

- before cutting there is no significant dependence of the breakdown voltage on the distance D to the border.
- after cold mechanical cutting all devices exhibit a sizeable improvement on the breakdown value regardless of the distance D .

Figure 6: Typical I-V characteristics for Edge-2 diodes for different distances from the cut edge.

- an increase of the bulk current is visible for devices with values of the geometrical parameter D up to around $350 \mu m$. For D values greater than $400 \mu m$ this effect is not visible anymore. The current enhancement can be explained with an external charge injection when the space charge region reaches the edge of the crystal cut.

5 Neutron irradiations

The Edge-1 and Edge-2 devices were irradiated with neutrons at three different facilities: Triga Reactor at Josef Stefan Institute, Ljubljana, Slovenia ($1 \times 10^{13} \text{ cm}^{-2} \div 1.1 \times 10^{14} \text{ cm}^{-2}$), Triga Mark II Reactor, LENA, University of Pavia, Italy ($4.5 \times 10^{13} \text{ cm}^{-2} \div 1.8 \times 10^{15} \text{ cm}^{-2}$) and VVR.S- $\Sigma\Sigma$ of NIPNE-HH, Bucharest, Romania ($8 \times 10^{14} \text{ cm}^{-2}$). The irradiations were made at room temperature ($25^\circ\text{C} \div 30^\circ\text{C}$) without bias voltage. Immediately after irradiation, all structures were stored at -20°C . All measurements were performed one week after irradiation and no corrections for self annealing were applied. It should be noted that the higher fluence values exceed the levels expected during the LHC lifetime for the inner tracking detectors.

Together with Edge structures square guard ring diodes of 0.25 mm^2 area were also irradiated, in order to measure the leakage current variation and the full depletion voltage for all fluences.

The values for the damage constant α obtained from the measurements on the diodes irradiated at the three different facilities are globally compatible. The resulting average value $\alpha = 4.5 \times 10^{-17} \text{ A cm}^{-1}$ is in reasonable agreement with measurements performed by other experimental groups [1, 12].

In Fig.7 the full depletion voltage obtained from C-V measurements as a function of neutron fluence for irradiations at the three facilities is presented. The expected values obtained from detailed simulation for different initial bulk resistivities are also shown [13]. The measurements confirm a reasonable agreement of the simulation for low and intermediate fluences while for the higher fluences one can notice significant differences between expected and measured values.

After neutron irradiation the leakage current for all diodes increases by about three orders of magnitude (depending on the neutron fluence). As a consequence, the power dissipated in the device also increases and the onset of the avalanche breakdown process might be influenced. For this reason, irradiated diodes were measured both at room temperature ($18\text{-}19^\circ\text{C}$) and at -5°C and -10°C .

For Edge-1 structures, as a general behaviour, we noticed that after irradiation the dependence of the V_{BD} on the distance W becomes less evident as the fluence increases. This can be explained as a consequence of the silicon dioxide charge increase during the irradiation (due to the unavoidable gamma irradiation background) [14, 15].

For Edge-2 diodes there are two main effects due to irradiation: the border injection current is no longer visible, and the dependence of the diode characteristics on the distance D is reduced.

Figure 7: Full depletion voltage as a function of neutron fluences.

For very high fluence values ($8 \times 10^{14} \text{ cm}^{-2}$ and $1.8 \times 10^{15} \text{ cm}^{-2}$), a substantial increase of the bulk leakage current was observed and no avalanche breakdown process could be detected. Fig.8 shows I-V characteristics for irradiated Edge-1 and Edge-2 diodes. The measurements were performed at two different temperatures. A soft current increase at the same bias voltage is evident for both types of structures. This effect starts before full depletion is reached.

Fig.9 shows the comparison for Edge-2 diodes between I-V curves before and after irradiation at $1.8 \times 10^{15} \text{ cm}^{-2}$. For very high fluence the dependence on the distance D disappears completely.

6 Conclusions

From experimental data obtained from test structures and comparison with simulation results we have extracted design guidelines to optimize the breakdown behaviour for radiation hard p^+ on n silicon detectors:

- i) the n^+ implant used on the detector border should be no closer than $150 \mu\text{m}$ to the last guard ring.
- ii) the distance of the p^+ implant from the edge should be no less than $400 \mu\text{m}$.

We also observe an improvement after cutting, independent of the distance of the p^+ implant from the edge.

For irradiation at neutron fluences up to $1.1 \times 10^{14} \text{ cm}^{-2}$ the dependence of the breakdown voltage on the distance between p^+ and n^+ implants does not change. This indicates that the p^+ implant side remains the critical region for the electric field. Nevertheless, the sensitivity on W and D is reduced as the fluence increases. For higher fluences, up to $1.8 \times 10^{15} \text{ cm}^{-2}$, the dependence of V_{BD} on geometrical parameters disappears.

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Figure 8: I-V characteristics for: a) Edge-1 (all W values) and b) Edge-2 (all D values) diodes irradiated at $8 \times 10^{14} \text{ n cm}^{-2}$ and measured at two different temperatures.

Figure 9: Comparison of I-V characetristics for Edge-2 diodes before and after irradiation with $1.8 \times 10^{15} \text{ n cm}^{-2}$

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