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H. A. Cole

Electronics & Applied Physics Division

AERE Harwell, Oxfordshire

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A DIFFERENTIAL PULSE-HEIGHT DISCRIMINATOR
WITH FULL CHANNEL LOGIC USING TWO
INTEGRATED CIRCUITS

H.A. Cole

ABSTRACT

A differential pulse height discriminator is described which is complete with full channel logic and which may be used with either symmetric or asymmetric expansion of the channel width, or operated as two independent discriminators sharing a common input terminal.

Electronics & Applied Physics Division,
U.K.A.E.A. Research Group,
Atomic Energy Research Establishment,
HARWELL.

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CONTENTS

	<u>Page No.</u>
1. Introduction	3
2. Operating Principles	3
3. Circuit diagram	5
4. Symmetric width expansion	7
5. Asymmetric width expansion	9
6. Discriminators	9
7. Logic circuitry	11
8. Conclusions	13
Acknowledgements	14
References	14

APPENDICES

Appendix 1	15
Appendix 2	16

ILLUSTRATIONS

Figure

1	Block schematic of the differential discriminator with typical operating waveforms
2	Circuit diagram of the differential discriminator (symmetric mode)
3	Variation of threshold bias with channel centre control
4	Variation of channel width (symmetric mode) for channel centre settings of 1V, 2V and 3V.
5	Variation of channel width (asymmetric mode)
6	Overdrive requirements for the LM339 comparator
A1	Modification required for sections 1 and 2 of ICI
A2	Modifications required for choice of channel width expansion

1. Introduction

The advent of the low-power quad amplifier^(1,2,3) and its ability to operate from a single 5V supply, has reduced the circuit complexity and number of components required in many applications. No more so are these advantages appreciated than in the design of differential discriminator circuits^(4,5) (also known as 'window discriminators' and 'single channel analysers').

Earlier circuits of this type^(6,7,8) have made use of dual comparators which have had relatively high power consumptions and have demanded the provision of dual-polarity power supplies - often of different magnitude. In this report two low-cost integrated circuits are used to provide a low-power differential discriminator circuit having either symmetric or asymmetric expansion of the channel width and with full channel logic; all operated from a single 5V supply demanding less than 5 mA load current. A block schematic of the circuit arrangement is shown in Fig. 1.

2. Operating Principles

The positive-going input signal is applied to the common input terminal of two Schnitt-type discriminators (D_H, D_L) which are individually back-biased by the positive voltages V_H, V_L . These voltages are derived from two d.c. amplifiers (A_H, A_L), and define the upper and lower limits of the channel. The difference between these voltages defines the channel width (V_W), and their average value at any given magnitudes defines the channel centre (V_C) i.e. $V_C = \frac{V_H + V_L}{2}$.

The output waveforms produced by the two discriminators are connected to two mono-stable circuits (M_H, M_L). These perform the required logic and ensure that a channel output pulse is produced only when the amplitude of the input signal lies within the confines of the channel. If this signal fails to reach the lower limit of the channel set by V_L , or if it exceeds the upper limit set by V_H , then no channel output pulse appears.

The two discriminators and the two d.c. amplifiers are formed from the National Semiconductor quad comparator type LM339⁽⁹⁾. The two monostable circuits are formed from a CMOS quad 2-input NAND gate type CD4011⁽¹⁰⁾.

Referring to the in-channel waveforms shown in Fig. 1, only the low-level threshold is exceeded by the input signal and only the low-level discriminator produces an output waveform. The trailing edge of this waveform is used to trigger the low-level mono-stable which produces a channel output pulse of duration t_c .

A.E.R.E.-R.8256 FIG.1. BLOCK SCHEMATIC OF THE DIFFERENTIAL DISCRIMINATOR WITH TYPICAL OPERATING WAVEFORMS

Referring now to the over-channel waveforms, both low- and high- level thresholds are exceeded by the input signal and an output waveform is produced by the high-level discriminator. The leading edge of this waveform is used to trigger the high-level monostable which produces an output waveform of duration t_h . This duration is designed to be greater than that of the output waveform produced by the low-level discriminator and its presence serves to inhibit the generation of a channel output pulse when the trailing edge of the D_L waveform occurs.

This method of channel logic is fully automatic and is virtually independent of input pulse shape or rise time. The only essential criterion is that the duration of the M_H output waveform should always exceed the maximum possible duration of the M_L waveform - which can be taken as being equal to the duration (t_p) of the input pulse - plus the duration of the channel output pulse i.e. M_H duration $\geq t_p + t_c$.

3. Circuit diagram

A complete circuit diagram of the differential discriminator is shown in Fig. 2.

Section 1 of IC1 is connected to operate as a unity gain non-inverting summing amplifier, and provides the variable back bias voltage (V_H) for the high-level threshold of the channel. Section 2 of IC1 is connected to operate as a unity gain d.c. subtractor and provides the variable back bias voltage (V_L) for the low-level threshold of the channel.

When the channel width control (R1) is set to zero, R5 and R10 are returned to earth potential and both IC1-1 and IC1-2 function as non-inverting amplifiers deriving a common input from the channel centre control (R2). The voltage gain (A_{V1}) of IC1-1 is given by:-

$$A_{V1} = \left(\frac{R6 + R7}{R7} \right) \left(\frac{R4 \parallel R5}{R3 + R4 \parallel R5} \right)$$

where

$$R3 = R4 = R5 = R6 = 560k\Omega,$$

and $R7 = R4 \parallel R5 = 280k\Omega$; hence $A_{V1} = 1$. The value of R2 ($1k\Omega$) is considered small enough to be neglected.

The voltage gain (A_{V2}) of IC1-2 is given by:-

$$A_{V2} = \left(\frac{R10 + R11}{R10} \right) \left(\frac{R9}{R8 + R9} \right),$$

where $R8 = R9 = R10 = R11$; hence $A_{V2} = 1$. The value of R1 ($1k\Omega$) is considered small enough to be neglected.

* METAL FILM TYPES (50 ppm)
Vcc = 5V

A.E.R.E.-R.8256 FIG.2 CIRCUIT DIAGRAM OF THE DIFFERENTIAL DISCRIMINATOR (SYMMETRIC MODE)

In both amplifiers the source impedances seen by both inverting and non-inverting terminals have been equalised to minimise errors due to input offset currents.

With R1 set to zero, adjustment of the channel centre control provides a positive voltage (V_C) to the non-inverting terminals of both amplifiers, and causes the same voltage to appear at the output terminals i.e. $V_L = V_H = V_C$. The relationship between V_L , V_H and V_C for $V_w = 0V$ is illustrated by the graph shown in Fig. 3. This shows that V_L and V_H increase linearly with V_C and that the useful operating range of the curve is limited to about 4V. Using 0.5% tolerance for the resistors R3 to R11, V_L and V_H remained within 10mV of each other over the full operating range of the amplifiers (this small error was due mainly to a 10mV zero offset on one amplifier).

The linearity of the curve is better than $\pm 1\%$ between $V_C = 1V$ and $V_C = 4V$. At values of V_C below 1V, however, the linearity progressively deteriorates and at $V_C = 0.3V$ the error in V_L and V_H is typically 7%; this is due to non-linearity in the base-emitter junctions of TR1 and TR2. If this degree of error is considered to be unacceptable then a voltage offset cancellation circuit should be added to each amplifier in the manner shown in Appendix 1. When this is done the linearity of the curve over the entire operating range is typically better than 0.2%.

4. Symmetric width expansion

If the channel width control (R1) is initially set to zero, and the centre control set for some particular value of $V_C = V_H = V_L$, then when R1 is adjusted a positive voltage equal to $\frac{V_w}{2}$ is applied simultaneously to the non-inverting terminal of A_H (via R5) and to the inverting terminal of A_L (via R10). The initial value of V_H is therefore increased by $\frac{V_w}{2}$ whilst, at the same time, V_L is reduced by $\frac{V_w}{2}$. The channel width has, therefore, been expanded symmetrically about V_C by $\pm \frac{V_w}{2}$ to yield a channel width equal to $(V_C + \frac{V_w}{2}) - (V_C - \frac{V_w}{2}) = V_w$. The channel centre remains unchanged at

$$\frac{\left(V_C + \frac{V_w}{2}\right) + \left(V_C - \frac{V_w}{2}\right)}{2} = V_C$$

The symmetrical expansion of the channel in this way is illustrated by the full-line curve in Fig. 4, which was produced from actual measurements. At zero width, $V_H = V_L = V_C = 2V$; a value set by R2. At 1V width, $V_H = V_C + 0.5V = 2.5V$, and $V_L = V_C - 0.5V = 1.5V$. At 4V width, $V_H = V_C + 2V = 4V$ and $V_L = V_C - 2V = 0V$. At all values of channel width the maximum deviation from $V_C = 2V$ was found to be less than 0.25%.

A.E.R.E. R8256. FIG. 3. VARIATION OF THRESHOLD BIAS WITH CHANNEL CENTRE CONTROL

A.E.R.E. R8256. FIG. 4. VARIATION OF CHANNEL WIDTH (SYMMETRIC MODE) FOR CHANNEL CENTRE SETTINGS OF 1V, 2V, & 3V.

The dashed-lined curves in Fig. 4 show the relationship between V_H and V_L for channel centre settings of 1V and 3V. Note that for the 1V centre setting the width should not be extended beyond 2V ($\pm 1V$ about V_C) because of the inability of V_L to go below zero. The same limitation on width applies for the 3V centre setting where V_H is unable to rise above 4V.

The main advantage of symmetrical width expansion occurs in applications requiring the positioning of a channel about a particular amplitude in the input signal spectrum. Initial positioning may be carried out using a broad channel which may then be reduced to the required width without upsetting the original centre position.

5. Asymmetric width expansion

Conventional methods of channel width adjustment usually cause the value of the high-level threshold to change relative to that of the present low-level threshold, as illustrated in Fig. 5. This method has the disadvantage that the channel position must be re-centred after each adjustment of width, necessitating adjustment of both V_H and V_L . Nevertheless, in some applications this method of width expansion may be preferred and because of this instructions have been given in Appendix 2 to show how the circuit of Fig. 2 may be modified to operate in either symmetric or asymmetric modes. The instructions also indicate how the circuit may be further modified to function as two separate discriminators sharing a common input signal terminal. The modifications consist simply of re-arranging the connections of the two resistors R3 and R10 and the incorporation of a 2-pole 3-way switch, if required.

6. Discriminators

The high- and low-level discriminators are formed from sections 3 and 4, respectively, of IC1. The positive back-bias voltages V_H and V_L are applied separately to the appropriate non-inverting terminals and the positive input signal is applied to the two inverting terminals which are joined together. The signal load resistor (R18) has a value equal to the parallel-connected value of the bias feed resistors (R13, R16) so that equality of source resistance is maintained for the four input terminals. The values chosen for R13, R16 and R18 are not critical, provided the existing relationship between them is maintained.

In the quiescent (no-signal) condition the output voltage levels of the two discriminators are in the high (1) state and have values close to that of V_{CC} . When the back bias

A.E.R.E. R0256. FIG.5. VARIATION OF CHANNEL WIDTH (ASYMMETRIC MODE)

of a particular discriminator is exceeded by the input signal its output voltage level falls to the low (0) state - typically less than 200mV.

The response times⁽⁹⁾ of the individual discriminators are typically 0.75 μ sec for the negative (1 to 0) transition, but this depends very much upon the duration of the input signal and the degree of input overdrive;* this is illustrated by the curve shown in Fig. 6. From this it is seen that for signal pulse widths in excess of about 1.2 μ sec the overdrive requirement is near steady at about 5%. On the other hand, signal pulses of only 0.5 μ sec duration would (typically) have to provide an overdrive of 55%.

The recovery times of the output waveforms for the positive (0 to 1) transitions are generally much greater than those for the negative transitions and are largely determined by the magnitude of the pull-up resistors R21, R22; the smaller these values, the quicker the recovery times. This is why the discriminators are operated with their outputs normally 'high'. If they were operated in the inverse mode the standing currents in the pull-up resistors would have exceeded that of the remainder of the circuit.

Backlash for the high-level discriminator is provided by the resistors R19 and R13 and for the circuit shown is about 2.5%. In the quiescent condition the output voltage of the discriminator is 'high' and the diode D1 is reverse biased (V_H is never greater than 4V); V_H therefore appears at the non-inverting terminal without attenuation.

Once the discriminator threshold is exceeded, its output level falls to near-earth potential and D1 is forward biased by V_H . The effective value of V_H is then reduced by the factor $\frac{R19}{R13 + R19}$ (ignoring the low forward voltage drop of D1) and the input signal has to fall to this lower value before the discriminator output can return to normal. The degree of backlash is given by the approximate expression:

$$\text{backlash (\%)} = \frac{R13}{R13 + R19} 100.$$

The resistors R20, R16 and diode D2 provide a similar facility for the low-level discriminator.

7. Logic circuitry

The high-level monostable (M_H) is formed from sections 1 and 2 of IC2 and is triggered from the leading edge of the D_H waveform produced by the high-level

*the amount by which the amplitude of the input signal exceeds the back bias.

A.E.R.E. R8256. FIG.6. OVERDRIVE REQUIREMENTS FOR THE LM339 COMPARATOR.

discriminator. The duration (t_h) of the M_H waveform is about 4.8 μsec and is determined by the values of C6 and R23. To a first approximation this duration is given by the expression: $t_h = 0.7C6.R23 \mu\text{sec}$, where C6 is expressed in pF and R23 in $M\Omega$. The expression is imprecise because of the wide variation⁽¹¹⁾ in the switching point of differing CMOS elements (typically 30% to 70% of V_{DD}).

The low-level monostable (M_L) is formed from sections 3 and 4 of IC2 and is triggered by the trailing edge of the D_L waveform produced by the low-level discriminator. The D_L waveform is applied to IC2-3 and also to one of the input terminals of IC2-4, via the diode D4. It is OR'd at this point with the output waveform produced by the M_H monostable, applied via the diode D5.

In the absence of the M_H waveform an in-channel signal causes a D_L waveform to be produced which, in turn, causes M_L to produce a channel output pulse of about 1.5 μsec duration. The duration (t_c) of this pulse is determined by the approximate expression:

$$t_c = C7.R24 \mu\text{sec}, \text{ where } C7 \text{ is expressed in pF and } R24 \text{ in } M\Omega.$$

When a D_H waveform is produced by an over-channel signal, the gate IC2-4 is inhibited by the presence of the resulting M_H waveform and no channel output pulse is produced by M_L .

It is important to note that the OR function performed at the terminal of IC2-4 was possible because of the unique input impedance at the CMOS gate. Such a connection would not have been possible with TTL-type gates and an additional IC would have been necessary to provide the requisite number of gates.

8. Conclusions

Experimental results have shown that a differential pulse height discriminator, complete with full channel logic, and with the ability to operate with symmetric or asymmetric expansion of the channel width, or as 2 separate discriminators, can be constructed using only two inexpensive integrated circuits, and at a total component cost of less than £25.

Linearity of width expansion and position of the channel can be made better than $\pm 0.2\%$ and, using metal film resistor of 50ppm for R3 to R11 (Fig. 2), the temperature coefficient for channel position and width stability is better than $0.01\%/^{\circ}\text{C}$.

Acknowledgements

The author is indebted to Mr. J.E. Smith who constructed the circuit shown in Fig. 2, and who carried out the measurements from which Figs. 3 to 6 were constructed.

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APPENDIX 1

The following illustration shows the modification required to both sections 1 and 2 of IC1 in order to improve the linearity in the low-voltage region of the graph shown in Fig. 3.

With the Width control (R1) set to zero, the Centre control (R2) should be adjusted so that V_C (measured at the wiper contact of R2) = 100mV. The resistor Rx in each of the additional circuits should then be adjusted until $V_H = V_L = 100\text{mV}$.

A.E.R.E. R8256.FIG.A1. MODIFICATION REQUIRED
FOR SECTIONS 1 AND 2 OF IC1.

APPENDIX 2

In the symmetric (S) mode, the circuit operates as previously described.

In the asymmetric (A) mode, R2 varies both V_H and V_L together and functions as a channel position control. R1 varies V_H only and functions as a width control.

In the dual-discriminator (D) mode, R1 varies V_H only and R2 varies V_L only.

In all operating modes both amplifiers operate at unity gain and equality of source impedance is maintained for all input terminals.

A.E.R.E. R8256. FIG.A2. MODIFICATIONS REQUIRED FOR CHOICE OF CHANNEL WIDTH EXPANSION.

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