0.2-10 MHz – 58 dB – 1 KW RF Amplifier (EDA 00097)

M. Paoluzzi
1. DESCRIPTION

1.1. GENERAL DESCRIPTION

The amplifier is designed to provide 58 dB gain in the frequency band of 0.2 MHz to 10 MHz with a minimum output power of 1 kW at 1 dB compression point. A detailed list of the amplifier parameters is given in 1.2.

The input signal, applied to the **RF IN** connector on the front panel (fig.1), is fed to the **15 W AMPLIFIER** (fig.2). The input stage (T₄) simply provides wide bandwidth matching to the 25 Ω gate de-Qing resistors of T₃. This single ended stage pre-amplifies the signal that is then split and applied to the output stage via a balanced to unbalanced transformer (TR₂). The push-pull output stage provides additional amplification and after recombination (TR₁) the signal is applied to the output connector. All the stages are operated in class A and matching of the driver amplifier output impedance to 50 Ω is insured by R₃.

The signal is then applied to the **9 WAYS SPLITTER** (fig. 3) where a delay compensated transformer (TR₁, TR₂ and TR₃) steps down the input voltage by a factor 3 to match the 5.55 Ω impedance of the isolation transformers (TL₁…TL₉) common point. Isolation between the ports is ensured by the 25 Ω resistors composed by R₁ to R₃₆.

Once split to the nine output ports, the signals are fed to the **120 W AMPLIFIER** modules (fig. 4) for final amplification. These modules are built around MRF151G power mosfets mounted in push-pull configuration and operated in class B. A wide bandwidth transformer (TR₁) steps down the 50 Ω input impedance by a factor 9 to match it to the 5.55 Ω gate de-Qing resistors (R₅, R₆). To provide the required output power the load of each of the two mosfet’s drains has to be 6.25 Ω. The single ended, 50 Ω output load is therefore transformed into its balanced equivalent by TR₃ and thus stepped down by a factor four with TR₂. To improve reliability the device is used at about half of its power capabilities and with a reduced drain voltage. Thermal protection is provided simply by a thermal switch mounted on the device case.

The nine **120 W AMPLIFIER** modules outputs are merged in the **9 WAYS COMBINER** (fig.5). This circuit is similar to the splitter. The main difference consists in the current detectors (TR₄₀₁…₉, R₄₀₁…₉, D₄₀₁…₉, R₄₁₁…₁₉ and C₄₀₁…₉) that provide a voltage proportional to the amount of current flowing through the isolation resistors (R₁…R₉). Ideally no current should flow through these resistors if the combiner inputs are driven with voltages of identical amplitude and phase. These signals can thus be used to detect an unbalance drive situation possibly due to the failure of a 120 W module. The recombined signal then goes through a directional coupler and is finally applied to the **RF Out** connector on the front panel.

Simple interlock electronics, protections and DC current measurement complete the amplifier. RF monitors of the forward and reflected power (-46 dB) as well as driver amplifier output signal (-26 dB) are also available on the front panel.

The required DC external supply as well as the cooling water are provided from the rear panel where is also present the **ST/CTL** connector. A short circuit between pins 1-2, 3-4 and 5-6 indicates, respectively, that DC supply is correctly distributed, the balance among the power provided by the nine **120 W AMPLIFIER** modules is within limits and temperature is below the maximum value. External control of the bias conditions is required via the pins 7-8 (**BIAS ON CMD**) that have to be short circuited.
In case of over-temperature trip or removal of the BIAS ON CMD, the amplifier can be forced to work for 2 more seconds by positioning SW101 between points 1 and 2 in the LOGIC CARD (fig. 6).

1.2. SPECIFICATIONS

-3 dB Bandwidth : 0.2 – 10 MHz
-1 dB Bandwidth : 0.5 – 5 MHz
Gain : 58 dB ± 1.5 dB
Output power at 1dB compression : >1 kW
Harmonic distortion : < -15 dBc @ Pout=1 kW
Gain linearity : ± 1 dB
DC to RF efficiency : >35 %
Input impedance : 50 Ω, VSWR 1.1:1 max
Load impedance : 50 Ω, no damage when operated in O.C or S.C.
Protections : Over temperature
Monitoring : Over current
RF driver output (-26 dB ± 0.5 dB)
Output Forward Power (-46 dB ± 1dB)
Output Reflected Power (-46 dB ± 1dB)
Driver and Final stages DC current.
120 W modules power balance.
Power requirements : 35V 100A DC
Cooling : Water
4 litres/min
15°C to 30°C
6 bar max
Δp=0.5 bar ? 1.8 Litres/min
Δp=1.0 bar ? 2.8 Litres/min
Δp=2.0 bar ? 4.1 Litres/min
Δp=3.0 bar ? 5.1 Litres/min
Δp=4.0 bar ? 5.9 Litres/min
Working temperature : 10°C to 35°C
Size : Standard 19” rack mounting cabinet
4U high (176.7 mm)
600 mm deep
Weight : 30 kg
External connections : Rear panel
DC Supply Terminals
ST/CTL (Cannon 15 pins female)
Cooling water In/Out (3” gas male)
Front panel
RF IN (N female socket)
DVR OUT MON (N female socket)
RF OUT (N female socket)
REF (N female socket)
FWD (N female socket)
Figure 1 - 1 kW amplifier (EDA 00097)
The main amplifier schematic diagrams PDF files are available in the following table and plotted below.

<table>
<thead>
<tr>
<th>Description</th>
<th>File ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2 – 10 MHz – 58 dB – 1 kW amplifier - cab (EDA 00097)</td>
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<tr>
<td>0.2 – 10 MHz – 58 dB – 1 kW amplifier - sch (EDA 00097)</td>
<td></td>
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<tr>
<td>50 kHz to 80 MHz, 15W amplifier (EDA 00098)</td>
<td></td>
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<tr>
<td>0.5 – 50 MHZ, 120W amplifier (EDA 00099)</td>
<td></td>
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<tr>
<td>9 ways combiner (EDA 00100)</td>
<td></td>
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<tr>
<td>9 ways splitter (EDA 00101)</td>
<td></td>
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<tr>
<td>Logic card for 1 kW amplifier (EDA 00141)</td>
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<tr>
<td>FP card for 1 kW amplifier (EDA 00142)</td>
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<tr>
<td>RP card for 1 kW amplifier (EDA 00143)</td>
<td></td>
</tr>
<tr>
<td>Distribution card for 1 kW amplifier (EDA 00144)</td>
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</tr>
</tbody>
</table>

Figure 2 - 50 kHz to 80 MHz, 15W amplifier (EDA 00098)
Figure 3 - 9 ways splitter (EDA 00101)

Figure 4 - 0.5 - 50 MHz, 120W amplifier (EDA 00099)
Figure 5 - 9 ways combiner (EDA 00100)
Figure 6 – Logic card (EDA 00141)
## 2. ALIGNMENT

### 2.1. PRELIMINARY ADJUSTMENT

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Water and 35 V supply off.</td>
</tr>
<tr>
<td>2</td>
<td>Remove all fuses on the back panel</td>
</tr>
<tr>
<td>3</td>
<td>Preset P1,P2,P3 15 turns CCW in 15 W amplifier (EDA 00098).</td>
</tr>
<tr>
<td>4</td>
<td>Preset P1 15 turns CCW in 120 W amplifier (EDA 00099).</td>
</tr>
<tr>
<td>5</td>
<td>Preset P101 15 turns CW and SW101 in position 1-2 in Logic card (EDA 00141)</td>
</tr>
</tbody>
</table>
| 6    | Verify isolation from cooling plate of:  
|      | 1. IC101 pin 2 on Logic card (R>500Ω).  
|      | 2. IC1 pin 2 on 15W amplifier (R>100Ω).  
|      | 3. T1 drain on 15W amplifier (R>500Ω). |
| 7    | Discharge filter capacitors C211-291, by short circuiting B2 to ground in the 120 W modules. |
| 8    | Turn on cooling water (4 litres/min).  
|      | Slowly rise the supply voltage to 35 V.  
|      | Verify that:  
|      | 1. The supply current stays below 100 mA.  
|      | 2. The POWER SUPPLY MASTER OK LEDs on FP and RP are on. |
| 9    | Insert AUX fuse.  
|      | Verify that:  
|      | 1. Supply current ~350 mA.  
|      | 2. Blowers are on.  
|      | 3. AUX, COMBINER INPUTS BALANCED and TEMP. OK LEDs on FP are on.  
|      | 4. In the 15 W amplifier, the voltage on the drain of T1 is the same as the supply voltage and the voltage on IC1 pin 2 is 15 V±200 mV.  
|      | 5. In the Logic card, the voltage on IC101 pin 2 is 12 V ±200 mV. |
| 10   | Short circuit pins 7 and 8 of ST/CTL connector.  
|      | Verify that:  
|      | 1. Supply current ~850 mA.  
|      | 2. The BIAS ON led on FP goes on.  
|      | 3. Gate and drain voltages on the 120 W modules stay below 100 mV. |
| 11   | Remove short circuit from pins 7 and 8 of ST/CTL connector and AUX fuse. |
| 12   | Insert F1 fuse.  
|      | Verify that:  
|      | 1. The corresponding POWER SUPPLY OK led on FP goes on.  
|      | 2. The drain voltage on the corresponding 120 W module is the same as the supply voltage and the current stays below 100 mA. |
| 13   | Repeat point 12 with fuses F2 to F9. |
| 14   | Remove all fuses and supply voltage. |
2.2. 9 WAYS SPLITTER TEST (EDA101)

1. Prepare test set-up #1 (fig.7)

2. Connect **Port A** to J10, and **Port B** to J1 and 50 Ω loads (~1 W) on J2 to J9 .
   Channel A measures input matching.
   Verify that measured response is below mask.

![9 WAYS SPLITTER - INPUT MATCHING](image)

3. Channel B measures the splitting response.
   Verify that measured response is within the mask limits.

![9 WAYS SPLITTER - SPLITTING RESPONSE](image)

Move **Port B** to J2… J9 and verify that measured response is within mask.
4. Connect Port A to J1, Port B to J2, 50 Ω load (~1 W) on J10 and leave other ports open. Channel B measures isolation between adjacent ports. Verify that measured response is below mask.

5. Connect Port A to J1, Port B to J3, 50 Ω load (~1 W) on J10 and leave other ports open. Channel B measures isolation between non adjacent ports. Verify that measured response is below mask.
Connect **Port A** to J1 and load other ports on 50 Ω (~1 W). Channel A measures port matching. Verify that measured response is below mask.

**Figure 7 – Test setup #1**
2.3. DIRECTIONAL COUPLER TEST (EDA00100)

<table>
<thead>
<tr>
<th></th>
<th>Remove link from TP1 and TP2 and install an SMA connector on TP2.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Prepare test set-up #1 (fig.7).</td>
</tr>
</tbody>
</table>
| 3 | **Connect Port A** to TP2, **Port B** to *RF Out* connector on the front panel.  
  Channel A measures port matching.  
  Verify that measured return losses are below 30 dB from 50 kHz to 30 MHz.  
  Channel B measures insertion losses.  
  Verify that measured insertion losses are below 0.2 dB from 50 kHz to 30 MHz. |
| 4 | **Connect Port A** to TP2, **Port B** to *FWD* connector on the front panel and load other *RF Out* port on 50 Ω (~1 W).  
  Channel B measures forward coupling.  
  Verify that measured coupling is \(-46.0\pm0.5\) dB from 50 kHz to 10 MHz.  
  Remove load from *RF Out* port.  
  Verify that measured coupling is still \(-46.0\pm0.5\) dB from 50 kHz to 10 MHz. |
| 5 | **Connect Port A** to TP2, **Port B** to *REF* connector on the front panel and load other *RF Out* port on 50 Ω (~1 W).  
  Channel B measures port isolation.  
  Verify that measured coupling is \(<-65\) dB from 50 kHz to 10 MHz.  
  Remove load from *RF Out* port.  
  Verify that measured coupling is \(-46.0\pm0.5\) dB from 50 kHz to 10 MHz. |

**Note:** Directivity is given by the difference between these two measurements.
2.4. COMBINER TEST (EDA00100)

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td>1</td>
<td>Remove link from TP1 and TP2 and install an SMA connector on TP1.</td>
</tr>
<tr>
<td>2</td>
<td>Prepare test set-up #1 (fig.7).</td>
</tr>
<tr>
<td>3</td>
<td>Connect Port A to TP1, Port B to combiner input 1 (J101) and 50 Ω loads (~1 W) on all other inputs (J102 to J109). Channel A measures output port matching. Verify that measured response is below mask.</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="9 WAYS COMBINER - OUTPUT PORT MATCHING" /></td>
</tr>
<tr>
<td>4</td>
<td>Channel B measures splitting function (Note that the combiner is characterized using its splitting characteristics). Verify that measured response is within the mask limits.</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="9 WAYS COMBINER - SPLITTING RESPONSE" /></td>
</tr>
</tbody>
</table>
Connect Port A to input 9 (J109), Port B to combiner input 1 (J101) and 50 Ω loads (~1 W) on all other inputs (J102 to J108 and TP1). Channel A measures input port matching. Verify that measured response is below mask.

Channel B measures isolation between inputs. Verify that measured response is below mask.

Remove SMA connector from TP1 and re-connect TP1 to TP2.
2.5. CURRENT MONITOR ADJUSTMENT

1. Remove JMP1 and JMP2 in 15 W amplifier (EDA 00098).
2. Apply 1V±10mV between B10 (+) and B9 (-).
3. Position the front panel switch on DVR Current-30V.
   Adjust P301 on FP CARD (EDA00142) so as to read 10 A on the front panel meter.
4. Remove voltage generator from B9-B10 and re-install JMP1 and JMP2.

2.6. DRIVER STAGE ADJUSTMENT (EDA00098)

1. Cooling water off.
2. Install T1, T2, T3
3. Remove F1 to F9 on back panel. Leave AUX fuse in.
4. Disconnect cable from RF Out (J1) in the 15 W amplifier.
5. Prepare test set-up #2 (fig.8).
6. Connect Port A to RF IN connector on the front panel, Port B to 15 W amplifier output (J1).
   Set network analyzer Pout = -50 dBm.
7. Turn 35 V supply on.
   With cooling plate temperature laying between 20 °C and 30 °C adjust:
   1. P1, P2 for a T1, T2 drain current of 1.7±0.05 A.
   2. P3 for a T3 drain current of 310±5 mA.
8. Turn cooling water on (~4 litres/min).
9. Verify that voltage on B4 is 28±1V.
10. Set network analyzer Pou t= 0 dBm.
11. Channel A measures input matching.
    Verify that measured response is below mask.

![Graph of 15 W Amplifier - Input Matching](image-url)
Channel B measures gain. Verify that response is within mask.

![Gain vs Frequency Graph]

Write down gain at 100 kHz, 1 MHz, 10 MHz, 20 MHz, 40 MHz.

35 V supply off. Move Port B to DVR Out mon connector on the front panel and connect a 50 Ω load (20 W) to 15 W amplifier output (J1).

35 V supply on. Measure gain at the frequencies indicated at point 12 and verify that the difference is 26±0.5 dB.

Connect an oscilloscope to DVR Out mon connector on the front panel. The instrument has to have an FFT function and 50 Ω input impedance.

Set network centre frequency to 100 KHz and frequency span to 0 Hz. Increase network analyzer Pout until the measured signal has a peak to peak amplitude of 3.5 V. Verify that harmonic distortion stays below -20 dBC. Repeat measurements at frequencies indicated at point 12.

Settings:
- Log. Freq. Sweep
- 10kHz to 500MHz
- Pout=0dBm
- Ch1: Reflection measurement A/R (Normalization at port A)
- Ch2: Transmission measurement B/R (Normalization with port A connected to port B)

Network Analyzer
HP8751A or equivalent

![Test Setup Diagram]

Figure 8 – Test setup #2
2.7. 120 W MODULES (EDA00099)

2.7.1. INPUT TRANSFORMER TEST WITHOUT MOSFET

1. No water, no DC supply and no mosfet installed (MRF151G).
2. Prepare test set-up #2 (fig.8).
3. For each of the nine 120 W modules disconnect input cable from Splitter output and connect it to Port A. Channel A measures input matching. Verify that return losses stay below mask.

![Graph: 120W MODULE - INPUT MATCHING WITHOUT MOSFET]

4. To verify that the wire isolation is not damaged, move the windings inside the input transformer tubing and check that the response on the network analyzer does not change.
2.7.2. OUTPUT TRANSFORMER TEST WITHOUT MOSFET

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>No water, no DC supply and no mosfet installed (MRF151G).</td>
</tr>
<tr>
<td>2</td>
<td>Prepare test set-up #2 (fig.8).</td>
</tr>
</tbody>
</table>
| 3 | For each of the nine 120 W modules:  
   1. disconnect output cable from Combiner input and connect it to *Port A*.  
   2. connect a 12 Ω resistor between the two MRF151G drain connections. |

   Channel A measures input matching.  
   Verify that return losses stay below mask.  

   ![Graph](image)

   Remove the 12 Ω resistor.  

| 4 | To verify stability, move the transformer ferrite and check that the response on the network analyzer does not change. |
2.7.3. 120W MODULE ADJUSTEMENT

<p>| | |</p>
<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>No water, no DC supply.</td>
</tr>
<tr>
<td>2</td>
<td>Prepare test set-up #2 (fig.8) and short circuit pins 7-8 in ST/CTL connector.</td>
</tr>
</tbody>
</table>
| 3 | For each of the nine 120 W modules: disconnect  
   1. input cable from Splitter output and connect it to Port A.  
   2. disconnect output cable from Combiner input and connect it to Port B.  
   3. Install MRF151G and glue the thermostat on top of the ceramic case.  
   4. Insert Aux fuse and fuse for the 120W module under test.  
   5. Channel A measures input matching. Verify that return losses stay below mask. |
|   |   |
| 6 | Turn on 35 V DC supply and cooling water. |
| 7 | Adjust P1 so that mosfet rest current is 1.4 A. |
| 8 | Channel B measures amplifier gain (typical response is given below). Verify that:  
   • gain at 1 MHz is 20 -0/+0.5 dB.  
   • if necessary readjust P1 but rest current must remain 1.4±0.3A.  
   • -3 dB low frequency point < 150 kHz.  
   • -3 dB high frequency point > 70 MHz. |

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![120W MODULE - OUTPUT MATCHING WITH MOSFET](image1)

![120W MODULE - TYPICAL GAIN/PHASE](image2)

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20
Turn off 35 V DC supply and remove fuse.

Reconnect input and output cables to splitter and combiner.

### 2.8. 1 KW ENSEMBLE

1. Prepare test set-up #3 (fig.9) and short circuit pins 7-8 in ST/CTL connector.
2. Water on, all fuses in, 35 V DC supply off.
3. Set network analyzer Pout = -50 dBm.
   Connect Port A to RF IN connector, Port B to RF OUT connector on the front panel.

**Settings:**
- Log. Freq. Sweep
- 10kHz to 500MHz
- Pout=-50dBm
- Ch1: Gain
  Transmission measurement B/R
- Ch2: Phase
  Transmission measurement B/R

Normalization with port A connected to port B and Pout=10dBm

**Network Analyzer HP8751A or equivalent**

**Figure 9 – Test setup #3**
2.8.1. TRANSFER FUNCTION MEASUREMENT

1. Follow instructions of 2.8

2. 35 V DC supply on.

3. Adjust network analyzer output power to -14 dBm and measure the amplifier transfer function. Verify that:
   - The gain at 1 MHz is 58±1.5 dB.
   - The gain variation from 0.5 MHz to 5 MHz is < 1 dB
   - The -3 dB low frequency point is < 300 kHz.
   - The -3 dB high frequency point is > 30 MHz.
   - The delay at 10 MHz is 32±1ns.

References are given below:

![Graph 1: 1KW AMPLIFIER - GAIN AND PHASE](image1)

![Graph 2: 1KW AMPLIFIER - DELAY](image2)
2.8.2. HARMONIC DISTORTION AND GAIN LINEARITY MEASUREMENTS

1. Follow instructions of 2.8 and turn 35 V supply on.
2. Move Port C from the network analyzer Channel B to an oscilloscope input. The instrument has to have an FFT function and 50 Ω input impedance.
3. Set network centre frequency to 350 kHz and frequency span to 0 Hz. Increase network analyzer Pout until the measured signal fundamental component is 20 dBm or 7 dBV (Corresponds to 1 kW).
   - Verify that the highest harmonic (normally the 3rd) stays below -15 dBc.
   - Reduce network analyzer Pout by 30 dB.
   - Verify that the fundamental signal goes down by 30 ± 1 dB.
   - Repeat measurements at 1 MHz, 2 MHz, 5 MHz and 10 MHz.

2.8.3. ADDITIONAL TESTS

1. Follow instructions of 2.8 and turn 35 V supply on.
2. Move Port C from the network analyzer Channel B to an oscilloscope input.
3. Set network centre frequency to 1 MHz and frequency span to 0 Hz. Increase network analyzer Pout until the measured signal has a peak amplitude of 225 V (~500W).
   - Verify that between pins 1-2, 3-4 and 5-6 of the ST/CTL connector on the back panel is < 200 Ω (opto-couplers collectors on pins 1 and 3, dry contact pins 5-6).
   - Alternatively remove F1 to F9.
   - Verify that between pins 1-2 of the ST/CTL connector on the back panel the resistance is > 10 kΩ and that the COMBINER INPUTS BALANCED led on the front panel goes off.
4. Open one of the thermostats links on the 120 W modules.
   - Verify that the TEMP OK led on the front panel goes off, the BIAS ON led goes off ~2s later and the resistance between pins 5-6 of the ST/CTL connector on the back panel is > 10 kΩ.
5. Set SW101 in position 2-3 in Logic card (EDA 00141)

2.8.4. 24 HOURS FULL POWER RUN

1. Follow instructions of 2.8 and turn 35 V supply on.
2. Move Port C from the network analyzer Channel B to an oscilloscope input. The instrument has to have an FFT function and 50 Ω input impedance.
3. Set network centre frequency to 1 MHz and frequency span to 0 Hz. Increase network analyzer Pout until the measured signal fundamental component is 20 dBm or 7 dBV (corresponds to 1 kW).
   - Set network centre frequency to 5.2 MHz, frequency span to 5 MHz and sweep time 5 seconds. Operate the amplifier for 24 hrs.