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Full Crate and Production Testing of the CMS Regional Calorimeter Trigger System

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Abstract-- The Compact Muon Solenoid (CMS) calorimeter regional trigger system is designed to detect signatures of isolated and non-isolated electrons/photons, jets, ℓ -leptons, and missing and total transverse energy using a deadtimeless pipelined architecture. This system contains 18 crates of custom-built electronics, including a backplane, boards, links and Application-Specific Integrated Circuits (ASICs). We present results from testing a completely instrumented and fully functional preproduction system. We also describe the production testing of the final system, including the custom software necessary to automate the process of testing a large quantity of high-speed and dense electronics.

I. INTRODUCTION

THE Compact Muon Solenoid (CMS) is a general-purpose detector that will operate at the Large Hadron Collider (LHC). Its construction is currently underway at the European Laboratory for Particle Physics (CERN) near Geneva, Switzerland. This large detector will be sensitive to a wide range of new physics at the high proton-proton center of mass energy $\sqrt{s}=14$ TeV [1].

At the LHC design luminosity of 10^{34} cm⁻² s⁻¹, a beam crossing every 25 ns contains on average 17.3 events. These 10^9 interactions per second must be reduced by a factor of 10^7 to 100 Hz, the maximum rate that can be archived by the on-line computer farm. This will be done in two steps. The level-1 trigger first reduces the rate to 75 kHz, and then a High Level Trigger (HLT), using an on-line computer farm, handles the remaining rate reduction.

The CMS level-1 electron/photon, ℓ -lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [2]. The RCT plays an integral role in the reduction of the proton-proton interaction rate (10^9 Hz) to the High Level Trigger input rate (10^5 Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and PbWO₄ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$ (pseudorapidity η is $-\ln(\tan(\theta/2))$ where the x-y plane is perpendicular to the beam line defined by z). An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions 0.087x0.087 ($\eta \times \phi$), which corresponds 1:1 to the physical tower size of the HCAL. Since the HF is not used in any electron or photon algorithm, it has a coarser segmentation in η and ϕ .

The algorithm to find electron and photon candidates uses a 3x3 calorimeter trigger tower sliding window centered on all ECAL/HCAL trigger towers out to $|\eta|=2.5$. Two types of electromagnetic objects are defined, a non-isolated and an isolated electron/photon. Four of each type of electron per regional crate are forwarded to the Global Calorimeter Trigger (GCT) for further sorting. The top four candidates of each type are received by the level-1 Global Trigger (GT).

The jet trigger uses the transverse energy sums ($E_{T,ECAL}+E_{T,HCAL}$) for each 4x4 trigger tower calorimeter region in the barrel and endcap [3]. In the very forward region ($3<|\eta|<5$) of the CMS spectrometer, each HF tower is treated

as a single region and their η division matches that of the 4×4 regions of the barrel and endcap. The jet or η -tagged jet is defined by a 3×3 region E_T sum. In the case of η -tagged jets (only $|\eta| < 2.5$), none of the nine regions are allowed to have more than 2 active ECAL or HCAL towers (i.e. above a programmable threshold). Jets in the HF are defined as forward jets. Four of the highest energy central, forward, and η -tagged jets are selected, allowing independent sorting of these 3 jet types until the final stage of jet sorting and trigger decision. In total, there are 12 jets available at the GT level.

II. CALORIMETER TRIGGER HARDWARE

The RCT electronics comprises 18 crates for the barrel, endcap, and forward calorimeters. These will be housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code will be sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards, located on each of 7 Receiver Cards and one Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the one mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts serial data to 120 MHz TTL parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional E_T sums and the electron candidates to the GCT. The GCT implements the jet algorithms and forwards the 12 jets to the GT.

The Receiver Card, in addition to receiving calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Synchronization of all data is done with the local clock and the Phase ASIC (Application-Specific Integrated Circuit--described below). The Phase ASIC also checks for data transmission errors. Lookup tables are used to translate the incoming E_T values onto several scales and set bits for electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

The Electron Isolation Card receives data for 32 central towers and 28 neighboring towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in a Sort ASIC on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S Card also receives E_T sums via the backplane, and forwards them and two types of muon identification bits (minimum ionizing and quiet bits –

described later) to the GCT. A block diagram of this dataflow is shown in Fig. 1.

Fig. 1. Dataflow diagram for the crate, showing data received and transferred between cards on the 160 MHz differential ECL backplane. Brief explanations of the card functionality are shown. For more details see the text or reference [2].

To implement the algorithms described above, five high-speed custom Vitesse ASICs were designed and manufactured, a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [4]. They were produced in Vitesse FX[™] and GLX[™] gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC handles board level boundary scan functions and drivers for data sharing. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/γ . All these ASICs have been successfully tested on the boards described below, and procured on in the full quantities needed for the system.

III. PRE-PRODUCTION PROTOTYPES

The successful conclusion of the first generation prototype program proved the design as described in Chapter 5 of the CMS Trigger Technical Design Report (TDR), which was approved in March 2001 [2]. This marked the start of the construction of full-function pre-production modules based on the TDR. A custom pre-production prototype 9U VME crate, Clock and Control Card, Receiver Card, Electron Isolation Card, and Jet/Summary Card have been produced with the above ASICs. Receiver Mezzanine cards with the Vitesse

7216-1 serial link for the Receiver Card and dedicated test cards have also been constructed.

We have built a pre-production VME crate, shown in Fig. 2, with a backplane that implements all of the level-1 trigger algorithms approved by CMS and the LHCC, and documented in the Trigger TDR [2]. The backplane is located in the middle of the crate between a card cage 400 mm deep in the rear and a card cage 280 mm deep in the front. As shown in Fig. 2, the backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane utilizes 4 row (128 pin) DIN connectors, capable of full 32-bit VME. The two leftmost front slots of the backplane use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pin assignments. Thus, a standard VME system module can be inserted in the two front stations with a form factor conversion between the first slot and remaining slots performed on the custom backplane.

The rear of the crate behind the two standard VME stations is occupied by the VME power supply. An external 48V supply provides power for the on-card DC-to-DC converters. In the data processing section of the crate (the bottom 6U of the backplane) a single high speed, controlled impedance, AMP 340-pin stripline connector is used for both front and rear card insertion. The stripline connectors have a power plane between every four signal pins, producing an impedance of 50Ω . Separate high current contacts, provided for the power plane connections, are used to transmit power to the boards. The connectors are housed in a cast aluminum shell that doubles as a board stiffener. The electrical characteristics of the connectors are excellent, allowing sub-nanosecond rise times with very low crosstalk. Data is transmitted across the backplane in 160 MHz differential ECL.

We have built a Clock and Control Card, (front side shown in Fig. 3), that matches the timing in the new backplane and cards. The Clock and Control Card distributes 160 MHz clocks and resets across the backplane to all cards, with delay adjusts on the back of the card to allow for differences in travel times across the backplane. The 120 MHz clocks for the Vitesse 7216-1 serial links and the Phase ASICs are also sent out to the Receiver Cards and Jet/Summary Card via the backplane. Power distribution on all the cards is handled with DC to DC converters fed with 48 V from the backplane power pins.

Fig. 2. Pre-production crate: rear (top picture) and front (bottom picture) view.

We have constructed eight full function Receiver Cards, shown in Fig. 4 and Fig. 5, on which we installed the Adder, Phase and Boundary Scan ASICs, as well as eight of the new version of the 4×1.2 Gbit/s serial receiver mezzanine card, shown in Fig. 6. The new Receiver Card features mezzanine cards with an improved version of the Vitesse serial receiver chip (VS7216-1) that is more tolerant of clock jitter. Two channels of tower data for each of four channels of serial link are received per mezzanine card for a total of 64 channels of data from the HCAL and ECAL per Receiver Card. Parallel data out of the Vitesse serial link are aligned via the Phase ASIC and then sent to the memory lookup (LUT) to linearize the data and set the electron identification bit for the electron algorithms. From the memory lookup, seven bits of ECAL E_T and one electron identification bit are sent to the Electron Isolation Card via the Boundary Scan ASICs. The Boundary Scan ASICs also handle the shared data coming in from other crates via the SCSI type cables at the front of the card. In addition, a sum of $E_{T,HCAL} + E_{T,ECAL}$, is sent from the memory lookup to two stages of Adder ASICs to form the 4×4 region sums that then travel via the backplane to the Jet/Summary Card.

Fig. 3. Pre-production Clock & Control Card.

Fig. 4. Pre-production Receiver Card (front) showing Adder ASICs and a Mezzanine Receiver Card installed.

We have also built a dedicated Serial Test Card, shown in Fig. 7, for testing the receiver mezzanine cards and performing detailed bit error checking. Additional copies of this card will be used for production testing of the mezzanine cards and integration tests with ECAL and HCAL electronics.

Eight full function Electron Isolation Cards have been built (Fig. 8) on which we have installed the Electron Isolation and Sort ASICs. Data are received over the backplane from the Receiver Card via the Sort ASICs' differential input. The Sort ASIC's sorting feature can be set on or off and is off on the Electron Isolation Card. This data includes 16 towers for each Region and 28 towers of neighbor data coming from adjoining Receiver Cards or neighboring crates via the data sharing cables at the front of the Receiver Card. Alignment in time is done at the Boundary Scan ASIC on the Receiver Card. These 44 towers are sent to two Electron Isolation ASICs which choose the two highest energy electrons of each type, isolated and non-isolated. A memory lookup compresses the seven bit energies to six bits and sets a location bit for each region served by the card. The E_T s and position information for the four electrons are forwarded via the backplane to the Jet/Summary Card.

Fig. 5. Pre-production Receiver Card (rear) showing Phase and Boundary Scan ASICs and lookup tables.

Fig. 6. Close up of a pre-production 4 x 1.2 Gbit/s Copper receiver mezzanine card.

Fig. 7. Pre-production Serial Link Test Card.

A pre-production Jet/Summary Card has been built and the front side is shown in Fig. 9. Via the backplane it receives 14 Region sums from 7 Receiver Cards using two Sort ASICs. These are all forwarded via SCSI cable at 80 MHz to the GCT which will implement the jet-finding algorithm and forward the Jets to the GT. Twenty-eight electron candidates are received from the Electron Isolation Card via the backplane and sorted with two Sort ASICs. Only the top four of each type, isolated and non-isolated, are forwarded to the GCT, where all the electron candidates from the 18 RCT crates are sorted again and the top four of each type sent on to the GT. In addition, a Quiet Bit for each 4x4 Region is set depending on a programmable threshold for each 4x4 region. Fourteen Minimum Ionizing Bits, formed by an "OR," of 16 HCAL quality bits per region on the RC, are forwarded with the Quiet bits to the GCT on the Electron Cables.

Fig. 8. Pre-production Electron Isolation Card with Electron Isolation and Sort ASICs installed.

Fig. 9. Pre-production Jet/Summary Card.

The HF data is received via one receiver mezzanine card located at the top of the J/S card (seen in Fig. 9). Since each HF tower also represents one HF Region, the data are handled by a Phase ASIC, and then two Memory lookups handle the energy assignment of the four different $\square$ slices of the HF. This information is delayed using Boundary Scan ASICs to align it with the Region E_T sums from the Receiver Cards and then forwarded with a quality bit to the GCT.

IV. TEST RESULTS

We have completed a detailed testing and validation program of these pre-production trigger boards. We have tested a fully functional crate with the Backplane, Clock Card, seven Receiver Cards, seven Electron Isolation Cards, and a Jet/Summary Card. These tests have verified all 5 Vitesse custom ASICs and their production is complete. The Receiver Mezzanine Card with the Vitesse 7216-1 transceiver chip has been validated as well. The Receiver Card, Clock Card and Electron Isolation Card have been validated and are being manufactured. The Jet/Summary Card, Crate, and Backplane have been verified and are being readied for production. Verification of data pathways and logic function was checked using Boundary Scan, which is fully implemented on all boards and ASICs. The output of the J/S Card has also been

validated through integration tests with the GCT. A full crate will also be used for planned system integration tests with the Calorimeter in 2004 [5].

Fig. 10. Front of a full crate, Clock and Control, Electron Identification, and Jet/Summary cards showing.

Additionally, we have conducted tests of the pre-production 4 x 1.2 Gbit/s copper serial link system. The cable used in the tests is composed of two 20 m lengths of 22 AWG Spectra Strip Skew-Clear[®] shielded 2-pair cable with VGA-type 15-pin DIN connectors. We have built a special “test,” transmitter mezzanine card to drive the signals over the cables and used two Serial Link Test Cards (STCs) to continuously transmit and receive pseudo-random data over many days with a trap on error, yielding a bit error rate of less than 10^{-15} . The full Receiver Mezzanine Card production run is complete and the STCs are being used to test this production run and have been sent out to other laboratories to assure compatibility of the RCT with the ECAL and HCAL electronics [5].

The detailed testing of the boards in the full crate test has led to the development of production testing sequences for the boards. After visual inspection, the Receiver, Electron Isolation, and Jet/Summary cards have their VME programming checked by reading and writing their command registers. Then the memory look-up tables are loaded with data and read back. The next step involves running the JTAG software on the full crate and verifying the ASIC to ASIC data paths, including those through the backplane. Following that test, the memories are programmed with specific data and the Phase ASIC test vectors are cycled to send known patterns through the regional sum and electron paths. Then the links are verified through reception of data sent from a set of Serial Test Cards. Clock and Control Cards are set up like a working CCC and timing is checked on a single board, then they are placed in a full crate to verify timing in detail. After initial checkout, backplanes are verified with a full set of cards for final validation.

V. TESTING SOFTWARE AND HARDWARE

Testing of the full production run will require specialized software and hardware. A ROOT-based [7] Graphical User Interface (GUI) has been created to simplify the testing of the over 1400 Receiver Mezzanine Cards. For the full RCT crate, custom code currently checks the memory function, implements the JTAG, and programs the memory for data flow tests described above. Currently, efforts are being made to streamline this process and make the users interaction with the code as simple as possible, using a GUI. A custom board, the Jet Capture Card, will use QuickLogic Eclipse FPGAs (Field Programmable Gate Arrays) to check the full output of a crate at the Jet/Summary card versus expected trigger patterns at speed. It will also provide a mechanism for triggering a portion of the full electronics chain including the HCAL electronics and hardware during subsequent integration tests.

VI. SUMMARY

Testing of the CMS level-1 Regional Calorimeter Trigger Pre-production Receiver Card, Electron Isolation Card, Jet/Summary Card, Clock and Control Card, Serial Link Mezzanine Card, Backplane, Crate and five custom ASICs that implement the CMS level-1 calorimeter trigger algorithms is complete. Tests conducted thus far have validated the design of the production boards and the production of the system has started.

VII. ACKNOWLEDGMENTS

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VIII. REFERENCES

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