FUTURE SEMICONDUCTOR DETECTORS USING ADVANCED MICROELECTRONICS WITH POST-PROCESSING, HYBRIDIZATION AND PACKAGING TECHNOLOGY

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Abstract

Several challenges for tracking with semiconductor detectors in the high rate environment of future elementary particle physics experiments are discussed, such as reduction of spurious hits and ambiguities and identification of short-lived 'messenger' particles inside jets. To meet these requirements the instrumentation increasingly calls on progress in microelectronics. Advanced silicon integration technology for 3D packaging now offers post-processing of CMOS such as wafer thinning to 50 μ m and through-wafer vias of <10 μ m. These technologies might be applied to create new tracking detectors which can handle vertexing under the difficult rate conditions. The sensor layers can be only ~50 μ m thick with low noise performance and better radiation hardness by using small volume pixels. Multi-layer sensors with integrated coincidence signal processing could discriminate real tracks from various sources of background. Even in a ~400 μ m thick 3D assembly the vectors of tracks can be determined in ~10 degree bins and this multi-voxel device is called 'vector detector'. The measured vectors can be used to associate the main tracks to their vertices in the interaction region at high luminosity colliders and to establish an on-line, first-level trigger signature.

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1. Semiconductor technology and physics

The development of semiconductor technology has in many ways a profound impact on the progress in physics. Relatively straightforward germanium and silicon detectors have contributed to nuclear science since ~1950. They are also widely used in instruments, for example the electron microscope. In the last two decades silicon chip technology has become essential in experiments with elementary particles both for the tracking detectors themselves and for the computers that are needed in the analysis of the vast amount of data. A striking example of the use of combined semiconductor technologies is the hybrid pixel detector. It has been possible ~1990 to achieve integration of a true 2-dimensional (2D) sensor matrix of microscopically segmented silicon elements and a matching matrix of CMOS readout electronics [1]. Due to the miniaturization of the electrical capacitances the thousands of parallel amplifiers in such an integrated circuit achieve low noise ($\sim 100\text{ e}^-$ rms) signal processing with ns precision for asynchronous MHz pulse rates. With a contiguous matrix of silicon pixels of $\sim 50\mu\text{m}$ dimension a position measurement with $<10\mu\text{m}$ precision can be obtained at nearly 100% efficiency. Programmable event selectivity is now possible for triggered data sets at kHz rate, as reviewed in these STD5 proceedings by Wermes [2]. Moreover, clever use of the industrial $0.25\text{ }\mu\text{m}$ CMOS technology at the same time has led to systems with radiation hardness at MGy level [3]. Pixel detector systems are currently being built for the innermost regions of the future LHC experiments at CERN [2,4,5,6]. The typical area will be a few square meters, covered with thousands of chips and 10^7 to 10^8 sensor elements. The high density interconnections between the sensor cells and the readout are provided by bump bonds, either indium or PbSn solder, with $\sim 20\mu\text{m}$ diameter.

Against this background a session in the Symposium 'STD5' was dedicated to 'High Density Interconnects' HDI technology and other post-processing and packaging developments. Industry is emphasizing this subject and the USA microelectronics R&D consortium SEMATECH has added 3D interconnects to their top technical challenges for 2005 [7]. We have been lucky to have Dr Kenji Takahashi as one of the presenters. He was a prominent member of the Japanese R&D effort 'ASET' (Association of Super-advanced Electronics Technologies) working at the Tsukuba Research Center and the leading author of a review article on ultra-high density 3D packaging [8]. The other presentations in the HDI session were by Unno on advanced multi-layer, fine-pitch substrates [9] and by Kwiatowski on a densely packed multi-sensor imaging module with high performance circuits connected to each sensor [10]. The present introductory paper focusses in sections 3, 4 and 5 on trends in semiconductor technologies that may lead to improvements in tracking performance over the next decade. The challenge is the ever higher rates that are under discussion for future upgrades of the hadron colliders, as well as in the high energy, high intensity electron-positron collider CLIC. Some details will be given in section 2. A proposal for the 'vector detector' based on pixels and HDI is finally described in section 6.

With its hundreds of millions of tracking points the central region of a collider experiment has some resemblance to the earlier workhorses of particle physics: the liquid-filled bubble chamber or the gaseous time-projection chamber, in which multi-track events could be visualized. The main

advantage of the semiconductor hybrid assembly is the potential to individually resolve and temporarily store micrometer scale space coordinates of tracks from collider interactions that succeed each other at 40MHz rate and with thousands of tracks in each beam crossing.

A comparable example of a semiconductor development with significant impact on science is the Charge Coupled Device (CCD) which finds many applications in imaging for astronomy, biology, and also in particle tracking as described in these proceedings by Damerell [11]. The CCD can offer very small ($\sim 10\mu\text{m}$) pixel dimensions in all directions, resulting in even lower noise and better precision. The CCD vertex detector system used in Stanford has shown convincingly the value of true 2D detectors [11]. However, the absence of active circuits for timing and selection in the pixel itself practically excludes the use of CCD in future high intensity hadron experiments which are the primary interest of this paper. Also, the CCD are fragile under irradiation due to their charge transport just under a fairly thick surface oxide.

2. Challenges for tracking in future particle experiments

The trend towards higher intensities is expected to continue in future hadron collider and fixed target experiments because the interesting interactions are only few among a large proportion of 'minimum bias' processes that produce background. Also in an e^+e^- collider such as CLIC [12] the particle density in the vertex detector will be of similar magnitude. It has been pointed out [13] that jets in the calorimeter and high energy muons are becoming less selective as trigger ingredients if a large pile-up of minimum bias events produces multiple jets and muons in each beam crossing. Under those circumstances an adequate trigger selectivity may need tracking signatures as well. However, it is currently not obvious how such critical information can be extracted from the tracker within the $\sim 4\mu\text{s}$ time interval that precedes the first level trigger decision. The signatures of interest as a trigger contribution probably consist of a combination of very high momentum particles that are practically not bent in the magnetic field ('stiff' tracks) and one or more secondary vertex points from decay of short-lived beauty b or charm c containing particles that travel some distance ($\sim\text{mm}$) from their primary vertex. Such b or c particles act as 'messenger' for potentially interesting interactions. With already tens to hundreds of vertices from simultaneous minimum bias interactions it is a real challenge to distinguish secondary vertices at all. To accomodate such a decision process in the short trigger interval of $\sim 4\mu\text{s}$ will require new approaches. Therefore, anything that can speed up pattern recognition will be useful in LHC experiments and true space points from the detector will do much better than projections such as delivered by the ubiquitous silicon microstrip arrays⁺.

In each beam crossing in a hadron collider thousands of hits are registered all over the useful

⁺ In 1980 the author, together with Pierre Jarron [14] created at CERN the first operational silicon microstrip detector system for particle physics and tried it out for tracking and vertexing together with collaborators in the experiment NA11. These devices then proved a succesful, even essential tool to study charm and beauty flavours. In spite of his sentimental attachment the author expects the microstrip detectors to prove less well-adapted to the LHC environment.

tracker area but the hits from high momentum particles occur perpendicular to the beam, at high p_T . In LHC the length ($\pm 3\sigma$) of the interaction region along the beam is ~ 30 cm. Unfortunately, in addition there may be quite a number of background signals from various sources. Electronic noise fluctuations can be reduced nearly to zero by using a large signal/noise ratio such as achievable in pixel detectors. Beam-induced electromagnetic pickup may create spurious signals in detectors very close to the beam, although the beampipe is designed as a shield. There are also physical background signals from neutron-generated ionizing events and from photon conversions, in the energy range few keV-100 keV (see below).

The tracking and vertexing precision in current systems depends more on multiple scattering in the material than on the inherent precision of the sensor devices. Reduction of the overall tracker material has to be achieved while maintaining noise performance, precision and speed. The precision in vertexing especially can be improved by adding layers closer to the primary interaction region, either using a smaller beam pipe or by positioning layers inside secondary or even primary vacuum, but safety margins for reliable beam operation are usually the first concern. In the ATLAS experiment at LHC the innermost pixel layer is planned to be at 50.5 mm radius. In comparison, the CCD vertexing systems at SLC and plans for the future linear electron collider are much more aggressive with beampipe radius of 14 mm and wall thickness of 0.4 mm, which can enable resolving and tagging of jets and the measurement of the vertex charge [11]. These low mass budgets in electron colliders may be impossible to achieve in hadron colliders where the need for high speed processing imposes more power and heavier cooling. One may have to conclude that future mechanical designs for high radiation colliders should be oriented towards easier maintenance by adopting pressure or spring contacts rather than gluing, after experience with the actual LHC trackers. Such a relatively low mass approach has once been tried in UA2 [15]. Miniature, on-chip springs are being developed e.g. by PARC [16]. A major trade-off will be mass against signal disturbances, including pick-up and photon background: a thin detector creates less photons and less scattering and could still deliver a ~ 1200 electron signal. With such a low signal operation one becomes sensitive to photons at lower energies, of which there might be many more. Simulations for LHC have been limited to threshold energies of 100 keV for electrons and 30 keV for photons [17]. Rather than as a single photon of 30 keV, the actual energy deposition, depending on the material distribution around the sensor elements, might proceed as several smaller deposits that still would exceed a threshold ~ 4 keV.

Radiation hardness has to be maintained or improved to levels of $> \text{MGy}$. It is expected that $50\mu\text{m}$ Si sensors still collect sufficient signal at such a high dose and with low noise electronics even diamond or SiC may become possible, if not financially then at least technically. Materials employed should better take into account the activation cross section by the high flux of neutrons.

Ultimately power dissipation and cooling are the major challenges for the future tracker systems, and high frequency operation is synonymous with increased power. Operation of the complete tracking device using capillaries with liquid nitrogen, in closed circuit or with wick evaporation is an option that has not been seriously studied: mechanical aspects are non-trivial, but radiation

hardness should improve as well as electronics noise and signal speed. Industry is also studying cooling of high speed processors using liquid circulation through microchannels inside the silicon chips. Eventually this may result in practical connection and propulsion methods for capillaries and 3D silicon devices.

Elsewhere in these proceedings several presentations discuss in a similar fashion the future challenges, but with varying boundary conditions and conclusions.

3. Miniaturization and wafer-postprocessing

Miniaturization in microelectronics is driven by the reduction of the cost per function if transistor dimensions can be reduced generation after generation. Moreover, large systems with complex functions can now be implemented as 'System on one Chip' SoC and then also physical dimensions and assembly cost can be lowered. In this way the price of e.g. portable phones has become affordable for large scale use. With economy of scale the non-recurrent engineering cost (NRE) of such complex designs can be amortized over millions of units. By using smaller feature size there are additional advantages to be gained such as lower noise, faster signals and larger memory capacity. Critical issues are the increase of power density, loss of transmission speed by thin and narrow connection lines and relative increase of the distance between functional blocks on a chip. Such issues are addressed by increasing the number of interconnect layers in the CMOS technology, now 6 to 8 metals, and by replacing aluminium by less resistive copper lines in some of these layers. One can optimize transistors for power, reduce locally the clock speed or even switch off parts of the processor circuit and in this way achieves active power management [18].

While the chips themselves become ever more complicated also the needs for connections with inputs and outputs push towards new technologies and possibilities. Postprocessing of standard CMOS wafers, hybridization and packaging become focus for intensive development [7]. Additional layers of connections and e.g. local hybrid memory blocks offer a way to improve performance within a CMOS generation. Postprocessing also creates new possibilities for mass-produced sensors (gas, liquid, sugar in blood,...), CMOS imagers (lenses and color filters) and other innovative devices. In sections 4 and 5 a few aspects of the 'back-end technologies' will be described.

For use in physics instrumentation the volume manufacturing aspects of CMOS are hardly relevant, but the enhanced functionality that comes from miniaturization and system integration may be used to achieve completely new approaches. In addition new possibilities in tracking devices will arise from postprocessing technologies.

4. High density interconnect technologies

Electrical connections with integrated circuits consist usually of wirebondings along the edges of

the chip. As the circuit dimensions become smaller, the chip edge is now often not sufficient to accommodate the required number of I/O pads. Therefore one uses solder connections elsewhere on the chip [19]. This follows the principle of solder bumping called C3 'Controlled Collapse Connections' developed ~1965 at IBM for flip-chip mounting on the integrated thermal module processor for their mainframe computers. A complete issue of the IBM J. Res. Dev. was dedicated to this in 1969 [20]. By choosing different solder compositions with a range of melting temperatures from 400C (High Pb content) down to 180C (eutectic PbSn) it is possible to build up a module in successive stages. The metal deposition was achieved originally by evaporation through a metal mask with bump size ~0.3mm. In a later stage several companies developed 'lift-off' techniques which allow smaller bump size, e.g. down to ~15 μm [21,22]. Currently most manufacturers favor wafer-scale electrolytical deposition, and a typical process flow [23] is illustrated in fig.1. After exposing clean metal surfaces, several successive metal deposits and lithography steps are required for adhesion, diffusion barrier and contact area definition. Solder metal is electrodeposited only in cavities in the photoresist, which now even can be made 100 μm thick. A first reflow is done under non-oxidizing conditions and

Fig. 1 Process flow for solder bump deposition on a CMOS wafer. BCB is a spin-on organic photosensitive masking material becoming stable after baking. Under Bump Metallization UBM is a sandwich of metals that provide different functions as mentioned in the text. The plating template uses a thick photoresist. Different solder compositions are available as electrolytical bath. Diagram from ref [23] courtesy MCNC-RDI, Research Triangle Park Durham, NC.

Fig. 2 SEM photograph of a part of the matrix of deposited solder bumps on the Medipix2 readout chip [23].

inspection of bump uniformity is performed. Fig. 2 is a photograph of the resulting bump pattern as obtained on a Medipix2 CMOS readout chip. The actual flip-chip bonding itself needs a machine that provides perfect alignment with micrometer precision in all directions. A second reflow to establish or reinforce connections can then be done in-situ on the flip-chip aligner or separately in an oven, again under non-oxidizing atmosphere. The procedures have been optimized in different ways by different suppliers, and the surface conditions of the starting wafers from CMOS suppliers may not be perfectly compatible with the particulars of the postprocessing. Therefore such postprocessing often requires continuous feedback and tuning.

The lower limits on bump size and pitch of bumps are imposed by wafer scale lithography precision (a few μm over 300 mm) and tolerances in the successive adjustments of masks on the components to be bonded together. The state-of-the art is a diameter $\sim 15\mu\text{m}$ for solder bumps and nearly ten times less for indium bumps, with a pitch $\sim$ twice this. Cost increases steeply at such a small pitch. The 2003 version of the roadmap for packaging technology calls for $90\mu\text{m}$ pitch around the year 2010 for cheap volume manufacturing but this pitch tends to shrink faster than predicted.

Besides accomodating more I/O contacts the impedance of input or output may become lower if the connection can be made with a solder bump close to the functional node on the chip. In this way the transmission speed can be enhanced by shorter leads and smaller capacitance. Industry has been already using bump bonding in a variety of applications for more than 10 years. Volume production exists of high-reliability devices for demanding environments, such as in cars. In that case the number of bumps is limited, bump size is larger and pitch of connections usually $>200\mu\text{m}$.

An application which calls for a large number of connections, even several million bumps, is in hybrid imagers for the infrared, used in space or in environments such as firefighting. The sensor is made of an IR-sensitive material and the concept has been used as a starting point for the development of the particle physics pixel detectors mentioned before [24]. The pixel size in space imagers can be as small as a few μm , and bumps usually consist of indium. This soft metal allows

the sensor and readout chip to have quite different expansion coefficients. This is essential if the IR imagers operate at liquid nitrogen or helium temperature.

Once postprocessing with lithography is applied in order to create adhesion layers and definition of bumps, it is a natural extension to introduce additional layers for power, signal routing, etc. This also allows a redistribution of bumps with respect to the contacts on the chip itself. A typical stack with x- and y-conductor layers is shown in fig. 3 [25]. This approach eventually results in the 'Wafer Level Packaging' concept.

Fig. 3 Cross-section of layers with high-speed interconnect lines, inductors and power-ground decoupling capacitors integrated in the redistribution layers on a Si substrate chip. This is called the Wafer Level Packaging WLP concept which includes also bump bonds for connection to outside. From Walter de Raedt, IMEC, Fig.142 in [25].

5. Wafer thinning and through-wafer vias for multi-layer devices

Among the recent techniques for system integration the 3D stacking of chips is applied in high-end processors, but also becoming widely used for products such as memory sticks and RF tags. In order to keep a small thickness of the final package, the chips that compose the 3D stack are usually thinned. In a CMOS circuit only a few μm on the top of the silicon substrate is used for the actual functions while the rest of the crystalline wafer just serves as handling support during the hundreds of automated processing steps. Wafers can be thinned only after the full CMOS process has been executed and the circuits have to be adequately protected. Some aspects of thinning have been described in the HDI session in Hiroshima by Dr Takahashi from Toshiba [8]. He worked out in detail why silicon wafers become flexible and strong below a thickness $\sim 50\mu\text{m}$, while they still remain quite fragile above $100\mu\text{m}$. The thinned $50\mu\text{m}$ wafers can be handled 'easily' in 3D assembly and packaging and seem to become industry standard. The thinning itself and the remaining processing steps on thinned wafers are often performed with a dummy wafer attached to the thin wafer. UV-detachable glues are marketed for this purpose. One possibility, also developed by Dr Takahashi is illustrated in the diagram of fig. 4, where the wafer is partially sawn before the actual grinding and thinning takes place.

Besides wafer thinning another essential ingredient for 3D stacking is the etching of 'through-wafer vias': perpendicular holes all through the silicon. This etching technology is only one in a wider range of methods for silicon shaping for Micro Electro Mechanical Structures (MEMS). Although currently MEMS are often stand-alone devices, ultimately one aims at integration of mechanical and sensor functions on standard CMOS wafers. If used for interconnectivity the perpendicular

holes are subsequently insulated using oxides or organics, and then filled with conducting metal, most often copper. A simple but very narrow via ($2\ \mu\text{m}$ diameter) is shown in fig. 5a. The thin ($50\mu\text{m}$) wafer with these vias is also shown. A variety of etching methods are being developed and can result in complicated shapes such as shown in the MEMS device in fig. 6 which was produced by K. Baert at IMEC [25]. Recent work at NASA [26] illustrates the interest for through-wafer vias in detector applications, but also shows that significant expertise in processing technology is needed in order to achieve acceptable yields.

Fig. 4 Dice Before Grind DBG process as developed by Toshiba, Disco and Lintec [27]. The fully processed 200 mm diameter, $\sim 725\mu\text{m}$ thick CMOS wafer (top) is diced to a partial depth of $\sim 40\text{--}60\mu\text{m}$ (b). A special top foil is then glued over the diced chips (c), and the wafer is mechanically and chemically thinned to $30\text{--}40\ \mu\text{m}$ thickness (d). Then another foil is attached as backing (e) after which the top foil is UV detached (f). The adhesion of the backing foil is less strong as it does not have to sustain grinding. The chips can be machine-picked from this backing foil. Industrial vacuum picking tools can now reliably handle $50\ \mu\text{m}$ thick chips.

Fig. 5 (Left) Capillary through-via ($\sim 2\mu\text{m}$ diameter) in thin silicon layer. The $50\mu\text{m}$ thin wafer is lifted out of the holder (Right). Work by Chris van Hoof at IMEC, reported in 2003 Annual Report, fig.115 [25].

Fig. 6 SEM image of MEMS device with perpendicular holes in a functional silicon layer (bottom), capped by another silicon layer and a dioxide sealing. From IMEC 2003 Annual Report, fig. 118 [25].

Fig. 7 Through Vias with variable rerouting lines to the bump pattern. From IMEC 2003 Annual Report [25].

Fig. 8 Schematic drawing of 4-chip stack demonstrator with multiple through-vias at 20μm pitch [8]. The overall thickness is ~300μm.

Fig. 9 SEM image of the demonstrator [8]. The metal vias can be seen as a matrix of pillars, because the silicon around it has been etched away. The 'floors' in between are the remains of the intermediate insulating layers.

It is not always possible to make the through-wafer vias at the positions where they make straight contact with the circuit nodes and then one has the possibility of re-routing as shown in figure 7.

This approach can be used also if in a pixel detector the readout cells do not exactly match the homogeneous matrix of the sensor cells. The re-routing allows to have butting sensor units with slightly smaller readout chips and space left over for external connections besides.

A very advanced design of through wafer vias is shown in figures 8 and 9. This demonstrator has been built in the earlier mentioned 'ASET' effort as reported by Takahashi from Toshiba [8]. In the SEM image the silicon has been etched away in order to clearly show the quality of the interconnecting vias that extend between four layers.

Fig. 10 Microphoto of multiple chip layers and ball bonding connections to a packaging substrate [28]. Note the flat loop of the wires.

Fig. 11 Cross sections of multiple (8 shown) chip layers and interposers with 3D connectivity using bump bonding and wire bonding connections [25].

Stacks of thinned chips can be interconnected in a variety of ways. One relatively conventional example [28] is shown in figure 10 where wirebondings along the edges connect to a common substrate, which often is the package. Note the well-controlled, flattened shapes of the wireloops. The ball bonding technology has made great strides over the last decade, and now provides comparable or even better performance than the ultrasonic wedge bonding, which was superior in

control and pitch until the early nineties.

A second example is a stack of 8 chip layers [25] produced at IMEC (Leuven, B) with 3D connectivity achieved with solder bumps of different sizes. This device is designed to be used in a "Bluetooth" module and typical packaging cost is ~\$10 per package in volume production.

6. New detectors: the 'Vector detector'.

It is essential to study the tradeoffs between the interdependent design choices at all hardware levels of a new detector system, and even including the efforts in on-line software and off-line data analysis during the actual experiment. New technologies such as discussed before may lead to innovation and different optimizations in the detector design. The trend in reduction of dimensions of the particle sensor elements allows lower noise and lower power dissipation per pixel besides the obvious improved resolution and precision in the space coordinates of tracking points. The increased number of segments per cm^2 in a pixel detector plane leads to higher power than for e.g. microstrip detectors, but one should also take into account that fewer planes may be sufficient. Equivalent tracking performance can be achieved with single true 2D layers replacing sets of double or triple projective layers, in particular when ambiguities occur in high occupancy environments such as LHC. Lower material density should even improve precision.

The low noise performance of CCD and other true 2D pixel detectors is obtained by the small~10 fF capacitance at the readout node. This performance must not be deteriorated by adding long routing lines and wirebonds and preference should be given to compact bump connections, which also have better reliability. The miniaturization of the sensor cells now allows the use of much lower signals than in mm^2 size pad detectors or microstrip arrays. This is illustrated in fig.12 with measured threshold distributions in the Medipix2 particle imager, with cells of $55\mu\text{m} \times 55\mu\text{m}$ [29]. Signals of ~ 1200 e-h pairs still can be discriminated, which for Si corresponds to ionization by a 4 keV photon, or a minimum ionizing particle (mip) passing through $20\mu\text{m}$. In order to allow millions of pixels to operate all with signals at such a low threshold it must be kept in mind that component parameters in chips do not exactly match but show a distribution of values, within limits that are guaranteed by the manufacturer. Sometimes it is possible to use an electronic feedback loop to stabilize characteristics, such as the effect of sensor leakage current on the output DC level [30]. Using a 3-bit digital adjustment of the threshold settings in each pixel it proved possible [29] to obtain the narrow threshold distribution in fig. 12. The energy/electron signal scale of threshold values was here calibrated by a ^{55}Fe source.

Fig. 12 Measured threshold distributions in a Medipix2 chip with >60k pixels [29]. At the right the broad distributions indicate the thresholds without any additional correction, resp. with 3 bit values added (far right). The tuned values remain quite well adjusted even if they are all shifted down by $\sim 3000\text{ e}^-$ without further corrections.

While these data show that it is in principle feasible to use signals from a layer of only $\sim 20\mu\text{m}$ of Si (as is also the case in the CCD detectors [11]) it is probably more realistic to use larger signals and not go much below $50\mu\text{m}$ silicon thickness. With square pixels of $50\mu\text{m}$ this would result in volume pixels ('voxels') with uniformity in all dimensions. These dimensions are sufficiently small so that they allow combined, directional measurements when at least two sensor planes are stacked at a distance of a few $100\mu\text{m}$ such as already illustrated in figures 8-11. Now one can begin to think of a multilayer detector in which new possibilities can be implemented. If signals from several pixels can be processed and correlated in a CMOS processor plane that is located in between the sensor planes, it becomes possible to certify real tracks by requiring coincidences in pixels in the opposite planes. In a next step one can attribute approximate directional vectors to such certified tracks. The name 'vector detector' is proposed here. This device also can reject photon-induced background or isolated pick-up noise hits which are characterized by a single hit without companion in a small area of opposite pixels. A very approximate sketch of such a 'vector detector' is shown in fig. 13.

Fig.13 Schematic drawing of the principle of the 'vector detector' based on two integrated layers of thin pixels. Not shown are the three to five intermediate silicon layers with routing, signal processing and logic that connect the primary hit sensor matrix at the top and the analysis sensor matrix below. The interposer and re-routing technologies are described in the text. With a separation of $\sim 250\ \mu\text{m}$ it would be possible to classify tracks in ~ 10 degree bins.

Vector information (position and slope) is traditionally used in the off-line analysis of tracks, and probably the highest precision ($\sigma \sim 0.06\ \mu\text{m}$) has been achieved in the CHORUS emulsion tracker [31]. On-line use in an integrated assembly would be a great step forwards. In reality a 'vector detector' will not be quite as simple as shown in fig. 13 because several intermediate layers are necessary for high density interconnectivity, signal and information processing, data output drivers and also some kind of integrated cooling. The development of such 3D structured detectors has to rely heavily on production technologies that will come in use in the microelectronics industry in the coming decade. If particle physics gets access for scientific applications, it will be probably needed to achieve a certain volume of identical units in order to recover the significant cost for non-recurrent engineering and to motivate industry to manufacture such devices at all. This economics may impose the use of the high performance units also in tracker shells where this is not strictly needed for precision.

With the first layer of vector detectors placed around the interaction region at a radius of 30 mm in a SLHC experiment it should become possible to associate high p_T tracks with at most a few vertices out of ~ 200 . If only 1-2 candidates can be tolerated one has some parameters that might be further optimized. The detector can be placed even closer to the vertex or the vector precision can be improved by using smaller pixels. The design of the detector and the vacuum beam pipe have to go hand-in-hand.

7. Conclusion

In the Hiroshima Symposium on Semiconductor Tracker Detectors the session on high density interconnect technology aimed to highlight developments that could have an impact on future detectors in particle physics or on general imaging devices for science. Post processing of standard CMOS wafers allows the combination of high performance processing circuits and application specific features, such as hybrid built-on sensors. Trends towards 3D packaging can be applied for creation of new detectors with adequate characteristics for future high intensity hadron or e^+e^- collider experiments. By using an integrated multilayer detector with selective response for true particle tracks it may be possible to use on-line vector determination and resolve and tag jets for the first level trigger.

This 'vector detector', a new kind of tracking pixel detector on the one hand may solve problems or shortcomings eventually encountered in experiments already on the floor. On the other hand it allows to open up new fields of research, until now not accessible by lack of tools. There is hope that the LHC machine can reach into the energies needed for 'new physics' and as a result there may be opportunities for detectors with new and different performance. As a comparison it is interesting to recall that at the end of the seventies unexpectedly the discovery of charm and beauty particles required an improvement in tracking precision that bubble chambers or gaseous wirechambers could not easily provide in spite of numerous efforts. The silicon microstrip detectors then came at the right moment to the rescue with more adequate tracking precision, fast timing and much higher rate capability.

Pixel detectors, including CCD, so far have been used only in a few particle physics experiments but proved to be a powerful tool for event tagging and event reconstruction. It can be expected that 3D space points with micrometer precision on m^2 detector surfaces are becoming indispensable for tracking of the most interesting, short-lived particles inside jets and also for more trivial issues like the distinction between ionizing tracks and massive numbers of photon conversions. It will require combined efforts to include event-time resolution with ns precision, while keeping in check the precision and the weight of the detector and cooling.

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REFERENCES

- [1] F. Anghinolfi et al., A 1006 element hybrid silicon pixel detector with strobed binary output
IEEE Trans. Nucl. Sci. NS-39 (1992) 654 also: CERN/ECP 91-26
- [2] N. Wermes, Pixel detectors for tracking and their spin-off in imaging applications, these proceedings
- [3] G. Anelli et al., Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects, IEEE Trans. Nucl. Sci. NS-46 (1999) 1690
- [4] C. Gemme et al., The ATLAS pixel detector, Nucl. Instr. Meth. A501 (2003) 87 (Vertex 2001, Brunnen)
- [5] W. Erdmann, Development of the CMS pixel detector, Nucl. Instr. Meth. A518 (2004) 324
- [6] P. Riedler et al., First results from the ALICE silicon pixel detector prototype, Nucl. Instr. Meth. A501 (2003) 111 (Vertex 2001, Brunnen)
- [7] G. Purvis, editorial, Three-Fives Review, 17 No5, p.2, June 2004
- [8] Kenji Takahashi et al., Ultra - high density interconnection technology of three - dimensional packaging, Microel. Rel. 43 (2003) 1267
- [9] N. Unno et al., these proceedings
- [10] K. Kwiatowski et al., these proceedings
- [11] C.J.S. Damerell, CCD-based vertex detectors, these proceedings
- [12] A. Battaglia et al., Physics at the CLIC multi-TeV linear collider, CERN-2004-005
- [13] F. Gianotti et al., Physics potential and experimental challenges of the LHC luminosity upgrade, CERN-TH/2002-078 hep-ph/0204087
- [14] E.H.M. Heijne et al., A silicon surface barrier microstrip detector designed for high energy physics,
Nucl. Instr. Meth. 178 (1980) 331
- [15] R. Ansari et al., The silicon detectors in the UA2 experiment, Nucl. Instr. Meth. A279 (1989) 388
- [16] <http://www.parc.com/research/eml/projects/stressedmetal/>
- [17] M. Huhtinen, private communication
- [18] Takayasu Sakurai, Perspectives on Power-Aware Electronics, Digest IEEE ISSCC 2003 / SESSION 1.2 , ISSN 0193-6530
- [19] J.H. Lau, editor, Flip chip technologies, McGraw-Hill 1995 ISBN 0-07-036609-8
- [20] L.F. Miller et al., IBM J. Res. Dev. 13 (1969) 239
- [21] D.J. Pedder, Flip-chip solder bonding for advanced device structures, Plessey Research Rev. 1989 1989, p.69
- [22] G. Humpston and A.P. Needham, Nucl. Instr. Meth. A395 (1997) 375 (Proc 3rd Pixel Workshop Bari)
- [23] A. Huffman, R. LaBennett, S. Bonafede and C. Statler, Fine-Pitch Wafer Bumping and Assembly for High Density Detector Systems, IEEE 2003 Nucl. Science Symp Conf Rec. R12-5
- [24] E.H.M. Heijne, Semiconductor micropattern pixel detectors: a review of the beginnings,
Nucl. Instr. Meth. A465 (2001) 1 (Proc Pixel- 2000)
- [25] IMEC Annual Report 2003, <http://www.imec.be>
- [26] F.M. Finkbeiner et al., Development of ultra-low impedance Through-wafer Micro-vias, Nucl. Instr. Meth. A520 (2004) 463 (Proc LTD-10 Genoa, 2003)
- [27] <http://www.toshiba.com/taec/technology/> and <http://www.lintec.co.jp/english/>
- [28] <http://www.intel.com/research/silicon/packaging.htm>
- [29] X. Llopert and M. Campbell, First test measurements of a 64k pixel readout chip working in single photon counting mode, Nucl. Instr. Meth. A509 (2003) 157 (Proc IWoRID 2002, Amsterdam)
- [30] F. Krummenacher, Pixel detectors with local intelligence: an IC designer point of view, Nucl. Instr. Meth. A305 (1991) 527 (Proc 2nd Pixel Workshop Leuven)
- [31] Shigeki Aoki, Tracking and vertex reconstruction in modern emulsion experiments, Nucl. Instr. Meth. A473 (2001) 192 (Proc Vertex 2000, Sleeping Bear Dunes)

FIGURE CAPTIONS

Fig. 1 Process flow for solder bump deposition on a CMOS wafer. BCB is a spin-on organic photosensitive masking material becoming stable after baking. Under Bump Metallization UBM is a sandwich of metals that provide different functions as mentioned in the text. The plating template uses a thick photoresist. Different solder compositions are available as electrolytical bath. Diagram from ref [23] courtesy MCNC-RDI, Research Triangle Park Durham, NC.

Fig. 2 SEM photograph of a part of the matrix of deposited solder bumps on the Medipix2 readout chip [23].

Fig. 3 Cross-section of layers with high-speed interconnect lines, inductors and power-ground decoupling capacitors integrated in the redistribution layers on a Si substrate chip. This is called the Wafer Level Packaging WLP concept which includes also bump bonds for connection to outside. From Walter de Raedt, IMEC, Fig.142 in [25].

Fig. 4 Dice Before Grind DBG process as developed by Toshiba, Disco and Lintec [27]. The fully processed 200 mm diameter, $\sim 725\mu\text{m}$ thick CMOS wafer (top) is diced to a partial depth of $\sim 40\text{--}60\mu\text{m}$ (b). A special top foil is then glued over the diced chips (c), and the wafer is mechanically and chemically thinned to $30\text{--}40\mu\text{m}$ thickness (d). Then another foil is attached as backing (e) after which the top foil is UV detached (f). The adhesion of the backing foil is less strong as it does not have to sustain grinding. The chips can be machine-picked from this backing foil. Industrial vacuum picking tools can now reliably handle $50\mu\text{m}$ thick chips.

Fig. 5 (Left) Capillary through-via ($\sim 2\mu\text{m}$ diameter) in thin silicon layer. The $50\mu\text{m}$ thin wafer is lifted out of the holder (Right). Work by Chris van Hoof at IMEC, reported in 2003 Annual Report, fig.115 [25].

Fig. 6 SEM image of MEMS device with perpendicular holes in a functional silicon layer (bottom), capped by another silicon layer and a dioxide sealing. From IMEC 2003 Annual Report, fig. 118 [25].

Fig. 7 Through Vias with variable rerouting lines to the bump pattern. From IMEC 2003 Annual Report [25]. Fig. 8 Schematic drawing of 4-chip stack demonstrator with multiple through-vias at $20\mu\text{m}$ pitch [8] . The overall thickness is $\sim 300\mu\text{m}$.

Fig. 9 SEM image of the demonstrator [8]. The metal vias can be seen as a matrix of pillars, because the silicon around it has been etched away. The 'floors' in between are the remains of the intermediate insulating layers.

Fig. 10 Microphoto of multiple chip layers and ball bonding connections to a packaging substrate [28]. Note the flat loop of the wires.

Fig. 11 Cross sections of multiple (8 shown) chip layers and interposers with 3D connectivity using bump bonding and wire bonding connections [25].

Fig. 12 Measured threshold distributions in a Medipix2 chip with $>60\text{k}$ pixels [29]. At the right the broad distributions indicate the thresholds without any additional correction, resp. with 3 bit values added (far right). The tuned values remain quite well adjusted even if they are all shifted down by $\sim 3000\text{ e}^-$ without further corrections.

Fig. 13 Schematic drawing of the principle of the 'vector detector' based on two integrated layers of thin pixels. Not shown are the three to five intermediate silicon layers with routing, signal processing and logic that connect the primary hit sensor matrix at the top and the analysis sensor matrix below. The interposer and re-routing technologies are described in the text. With a separation of $\sim 250\mu\text{m}$ it would be possible to classify tracks in ~ 10 degree bins.