Electronics Issues & challenges for future linear colliders

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**Vertex technologies**

CMOS (Monolithic Active Pixel Sensor) (MIPS/Strasbourg)
- Concept from visible light detectors
- Fast readout and on-chip analog processing
- Few microns thick silicon layer
- Excellent spatial resolution (10-20 μm)
- Highly sensitive to UV and visible light
- Low background noise

DEPFET (Bonn,mpi)
- FET-Transistor integrated in every pixel (first application)
- No charge transfer
- Very limited power consumption (~1W for the full VD)
- Low noise allows 50 μm thick silicon layers

**Common Challenges**

- Everything ON detector
- Column RO specification
- Power cycling
- Readout during bunch train
- Influence of RF pick-up?

**Technology forecast (2005-2015)**

- FPGA for signal processing and buffering
  - Integrates receiver links, PCI, DSPs and memory...
- Processors and memories
  - Continuous increasing of the computing power
  - Memory size quasi unlimited!
    - Today : 256 MB
    - 2010 : 1 GB... than ?
- Links & Networks:
  - Commercial telecom/computer standards
  - 10-30-100 GBEthernet!
  - Systematic use of COTS products
  - make decision at TO -3 years

**TPC Read Out**

- Main Features
  - VFE: GEM/Micromegas/Digital (Medipix)
  - No active gating
  - Continuous Read Out during the full bunch train (1 ms)
  - Minimize RO material in the end cap

**Data Flow**

- Software trigger concept → No hardware trigger!
  - Trigger: Software Event Selection
  - Event classification
  - Signal processing – digitization, no trigger interrupt
  - Sparcification, cluster finding and/or data compression
  - No hardware trigger!

**Calorimeters Read Out**

- Today
  - CALICE UK group: P. Dauncey
    - APD fibre masks or flat-band connector to SiPM cassette RO printed circuit
  - NA60 (ALICE DAQ scheme)

- Tomorrow investigation
  - NA60 – ALICE DAQ scheme
  - DAQ PC

**Advantages → all**

- Flexible
  - fully programmable
  - unforeseen backgrounds and physics rates easily accommodated
  - Machine people can adjust the beams using background events
- Easy maintenance and cost effective
  - Commodity products: Off the shelf technology
  - commonly OS and high level languages
- Scalable:
  - modular system
  - looks like the ‘ultimate trigger’ → satisfy everybody: no loss and fully programmable.
1. **Estimates Rates and data volume**

- **Physics Rate:**
  - $e^- + e^+ \rightarrow X$: 0.0002/BX
  - $e^- + e^+ \rightarrow e^+ + e^-$: 0.7/BX

- **Background:**
  - VXD inner layer: 1000 hits/BX
  - TPC: 15 tracks/BX

- Background is dominating the rates!

2. **Tesla Architecture (TDR 2003)**

- Detector Channels:

- **Event building Network**

3. **Summary**

- The ILC environment poses new challenges & opportunities which will need new technical advances in VFE and RO electronics.
  - **NOT LEP/SLD, NOT LHC!**

- Basic scheme: The FEE integrates everything from signal processing & digitizer to the RO BUFFER.

- Very large number of channels to manage (Trackers & EM)
  - Should exploit power pulsing to cut power usage during interburst.

- New System aspects (boundaries ..
  - Interface between detector and machine is fundamental.

- Burst mode allows a fully software trigger.
  - Looks like the Ultimate Trigger: Take EVERYTHING & sort later! GREAT! A sociological simplification!

4. **About systems boundaries ….. moving due to !**

- **evolution of technologies, sociology …..**

5. **ICL ‘today’ Data Collection Network model**

- **Event building Network**

- **Detector Channels**

- **Event building Network**

- **Computing resources (Storage & analysis farm)**

- **30 Mbytes/sec → 300 TBytes/year**