Abstract
The CMS Electromagnetic Calorimeter consists of roughly 76000 lead tungstate (PbWO$_4$) crystals and almost 25000 Printed Circuit Boards (PCBs) of 5 different types. About 5500 Gigabit Optical Links are used to process the signals from the photo-detectors and to send the resulting data to the off-detector electronics. The integration of the electronics is described together with its cooling system, mechanical supports, the low voltage distribution, various signal cables and optical fiber patch panels. Complexity and installation sequence require tests at each step of the installation. The test strategy during the installation is described and results of the system performance achieved are presented.

I. INTRODUCTION
The CMS [1] Electromagnetic Calorimeter (ECAL) [2] is divided into the Barrel (EB) and two End-Cap (EE) calorimeters made of 61200 and 14648 crystals, respectively. The EB is made of 36 super modules (SM) with 1700 crystals each and the EE of 4 Dees with 3662 crystals each. In the following we will exclusively talk about the installation of the electronics into the EB super modules.

A. Readout Electronics
The basic building block of the electronics is the readout of a trigger tower (TT) [3], (5 x 5 crystals in $\eta \times \phi$). It consists of 5 Very Front End (VFE) boards, 1 Front End (FE) board, 1 Low Voltage Regulator (LVR) card and a motherboard. Special Kapton cables connect the motherboard to the Avalanche Photo Diodes (APDs), glued onto the crystals, and to the Betherm 100 k$\Omega$ negative temperature coefficient thermistor mounted onto every tenth crystal.

One LVR [4] card is plugged into the motherboard to stabilize the low voltage. It uses three Detector Control Unit (DCU) integrated circuits, for monitoring all its input and output voltages. High voltage for the APDs is directly connected to the motherboard. One VFE card is connected to the motherboard. Each card contains five identical readout channels, comprising one Multi-Gain Amplifier [5] (MGPA) and one 4-channel, 12-bit, 40 MHz ADC [6] (AD41240), followed by a buffer for signal level adaptation. One DCU per VFE card is used to measure the leakage currents of the APD’s, the temperature sensor on the crystal and the temperature on the VFE card itself. The FE card plugs simultaneously into the 5 VFE cards and the LVR card from the top. It is connected to the off-detector electronics by two 800 Mbit/s optical links (GOH), one for the trigger and one for the data. One Clock and Control Unit (CCU) integrated circuit on the FE card provides the interface to the control system, the token ring. One super module has 8 token rings, four with 8, two with 9 and two with 10 FE cards. Each of them connects through a token ring link board (TRLB) to a control fiber ribbon. The control system is partially redundant in the sense that broken FE cards can be excluded from the ring, as long as there are no two consecutive FE cards broken.

B. Installation Items
The following parts have to be installed into each super module and tested:
- 68 motherboards
- 340 VFE cards
- 68 LVR cards
- 70 FE cards (68 for reading the trigger towers and 2 for the laser monitoring electronics module (MEM))
- 8 Token rings including the TRLB
- 138 optical links (GOH – gigabit optical hybrids)
- 12 Distributed fiber patch panels (DFPP)
- 17 Low Voltage Distribution (LVD) blocks together with one remote sense and three inhibit cables

In addition a variety of mechanical supports is necessary to hold cables, LVD blocks, fibers, fiber patch panels and connectors in place.

VFE, LVR and FE cards and the GOHs are labelled with bar codes, providing a unique identification for each individual piece.

C. Installation Sequence
The installation of the parts proceeds in several steps, with each covering the previously installed layers:
1. Installation of the motherboards together with the cooling system
2. Mounting of the trigger tower electronics (VFE, LVR and FE)
3. Installation of the token rings including TRLB
4. Installation of the optical links including the distributed fiber patch panels
5. Installation of the LVD system
6. One week operation and test of the completed super module (commissioning)

The first step is done separately, prior to the shipment of the SM to the ECAL electronics integration center. It is com-
completed with a verification of the motherboard connections to the APDs and temperature sensors and a 20 bar pressure test of the completed cooling system. Finally the cooling circuit is filled with de-mineralized water.

II. ECAL INTEGRATION AREA

The ECAL electronics integration area is located in a part of a large assembly hall. Trucks can directly enter the hall and overhead cranes for loading and un-loading of super-modules are available. The area comprises several zones. Beside the super-module installation and test zone there are several preparation and testing places for electronics components, an air-conditioned storage area for up to 20 super-modules and storage space for materials and components. The availability of a nearby mechanical workshop was very important, especially during the prototyping phase.

The super-module installation and test zone is equipped with three independent integration stands. A possibility to add one additional stand is foreseen in case of schedule needs. Four mechanical support frames are available to hold the SMs during the installation and testing. They can be moved on air pads. For this purpose the floor, including the truck accessible entrance, was covered with an epoxy resin to achieve the required flatness.

Two independent cooling units, each capable of providing the necessary cooling water flow for two super modules, are available.

A. Integration Stands

Each integration stand (see Figure 1) has a CAEN (SY 1527) HV system, identical to the final system for CMS to provide the APD bias voltages for one SM. The stand uses four Wiener PL500 five channel low voltage supplies to power the 17 low voltage channels of one super module. The remaining three low voltage channels are wired to additional low voltage distributions, which are used to temporarily power trigger towers individually during tests. The HV and LV systems are controlled and monitored from a PC, which in addition contains a PCI FEC (Front End Controller) to connect optically to a token ring. A 6U-VME based readout system allows to test each trigger tower individually at each step of the integration, as well as to connect electrically or optically to a token ring, to test up to 10 trigger towers in parallel. One additional two channel linear power supply system serves the laser monitoring electronics module (MEM).

A 532 nm pulsed laser is available to inject test pulses into the crystals. As there is only one system the laser fiber has to be connected to the SM under test. During the test the laser is controlled from the readout electronics of the corresponding integration stand.

B. DCS and ESS

A Detector control system (DCS) identical to the one used in CMS can connect up to three super modules in parallel to read temperature and humidity data. The ECAL Safety System (ESS) can connect up to 4 super modules. It measures the SM temperatures and receives control signals from the cooling units. In case of cooling unit failures it would shut down the low and high voltages and lock the supplies. In addition there is a hard-wired interlock between the cooling unit and the low voltage power supplies. This allows secured unattended operation of the SMs during nights and weekends.

III. INSTALLATION AND TESTS

The fact that the installation follows a sequence, covering partially or fully the previously installed items, requires full
validation at each step. Therefore extensive testing is part of the installation procedure.

Each new SM is prepared for integration by transferring it from a storage frame into the integration stand and connecting its cooling circuit to a cooling unit. The correct HV settings for this SM are retrieved from a database and programmed into the HV supplies of the integration stand. All connections between the motherboards and the APDs and temperature sensors are re-tested.

A. Mounting of the trigger tower electronics

The VFE cards are prepared by mounting an aluminium front cover onto the components side. A thermally conducting gap filling material, Gap Filler 2000 from Bergquist is applied to ensure a good heat transfer between the components and the cover. At the outside of the cover 5 strips of 1 mm thick gap pad VO Ultralast from Bergquist are glued to provide a defined thermal interface of the cover and the cooling bars. The cover is chromatized and electrically connected to the ground plane of the VFE card. Three captive stainless steel screws, to fix the cards to the cooling bars, are mounted to the front covers. The LVR cards are prepared in a similar way, with the difference that their front cover is electrically isolated from the card. FE cards are prepared by adding three strips of 1.5 mm thick gap pad VO Ultralast in the places where they will touch the cooling bars, to achieve a defined thermal contact.

The installation starts with VFE and LVR card mounting (see Figure 2). Five VFE cards and one LVR card are inserted in a motherboard and then fixed to the cooling bars. This procedure is repeated for all 68 trigger towers. The bar codes of the installed cards are scanned using dedicated software, connected to the ECAL construction database. The program verifies that each card is already registered in the database and is good for installation and adds the location of the card in place. All FE cards are mounted on top and their bar codes are also scanned. The FE cards have unique hardwired CCU-IDs. In a SM the numbers 69 and 70 are used for the MEM and the numbers 1 to 68 are used for the trigger towers. During the installation the FE are sorted to match the numbering scheme of the trigger towers.

This installation step is completed by individually testing each trigger tower. High and low voltages are applied. Token ring cables and two GOHs are connected. The single trigger tower test, see section IV, validates the full functionality and the performance of the tower under test.

B. Installation of the token rings

The four Token Ring Link Modules, each serving two token rings are installed and fixed to a separate cooling bar. Starting with rings 7 and 8 the token ring cables are connected to the FE cards and the TRLB (see Figure 3). The control fiber ribbon is connected to the PCI FEC in the test stand and all towers in the ring plus the TRLB are powered. A test program accesses all nodes on the token ring using standard and redundant configurations by skipping successively each of the FE cards. In this way the correct installation of all token ring cables and the TRLB are verified.

C. Installation of Optical Links

The gigabit optical hybrid is a small PCB plugged into an connector on the FE card (see Figure 3). It has a 2 m long fiber pigtail with a so called MU connector at the end. Each distributed fiber patch panel is a flat aluminium box containing a MU single fiber to so called MFS 12-way ribbon adapter. Excess lengths of the GOH pigtales are stored in the DFPP (see Figure 4). The 12-way ribbon is routed to the inline patch panel containing MFS to MFS adapters at the SM patch panel. The installation of the GOH is a very delicate operation, because the fibers are rather fragile and the bending radius of ~4 cm has to be respected. Data and Trigger GOH for a given FE card are always installed at the same time and routed into two different DFPP. The correct operation of each individual GOH is verified by connecting to the MFS adapter at the inline patch panel. The described single trigger tower test is done as previously after the FE installation but now the final GOH of the tower and the corresponding TRLB are used. The procedure continues until all 138 GOH and the 12 DFPP are installed.
D. Low Voltage Distribution

The remaining support plates are installed and the 17 busbar LVD blocks are mounted (see Figure 5). Each block serves the LVR cards for four trigger towers and to the TRLB controlling these towers. The power input connectors are fixed at the SM patch panel. A remote sense cable with 17 twisted pairs of wires terminated with a 37-pin D-sub connector at the SM patch panel is connected to the input of the 17 LVDs. Three inhibit cables terminated with 50-pin D-sub connectors at the SM patch panel are installed to provide the control of the LVR cards. The voltages at the LVD are measured before connecting to the LVR cards. The correct assignment of the inhibit channels is verified.

IV. SINGLE TRIGGER TOWER TESTING

The testing of individual trigger towers explores the full functionality of the corresponding channels and assesses their performance. It uses the VME based readout system and provides a user-friendly interface. The sequence is as follows:

1. The communication with the CCU of the TT is verified by reading the CCU ID, which is soldered as a bit pattern onto the FE card. The number has to agree with the geographical ID, indicating the location of the tower in the SM.

2. All sixteen I2C interfaces of the CCU are tested, by scanning the addresses of all connected I2C devices and comparing the result with the expectation.

3. Initializing the FE card for DAQ purposes checks the accessibility of all the important registers. It includes setting the enabled channels, the power of the GOH, the transmission mode of optical links, the pipeline delay, the number of samples per trigger, the peak finding status, the filter parameters for the trigger and loading the pedestal values. The values are read back and their correctness is verified.

4. The registers of the MGPAs on the 5 connected VFE cards are set and read back for each channel individually.

These registers are calibration pulse enable, pedestal DAC value for each gain and the test pulse amplitude.

5. The pedestal DAC values, corresponding to 200 ADC counts for each channel and at each gain, are computed. For these purposes the pedestal DAC is successively set to six equally spaced values from 40 to 90 and the corresponding pedestal values are measured. A line fit to the measured points determines the DAC values corresponding to a pedestal of 200 ADC counts.

6. Using the previously obtained pedestal DAC settings the pedestals are measured. In total 100 events each with 10 consecutive time samples are taken. The total noise is calculated as the RMS value of all 1000 samples. A low frequency contribution is estimated by computing the RMS of the averages per event. This measurement establishes the performance of the readout channels. At the same time it verifies the correct operation of the complete readout electronics. This requires the correct connection and biasing of the APD, because the noise depends on the input capacitance to the MGPA.

7. For each channel and each gain 10 test-pulses are injected, using the generator internal to the MGPA. The average amplitudes and their RMS values are compared with expectation. The same is done for the trigger data path.

8. Using the three DCU at the LVRB the low voltages are measured. Finally the leakage currents of the APD’s and the capsule temperatures are measured and checked.

Typical distributions of the average pedestals and the RMS of the pedestals are given in Figure 6 and Figure 7.

The trigger tower test system can also be used to read the signals of laser light injected into the front faces of the crystals. This allows a validation of the full readout chain including crystals and APDs.
V. COMMISSIONING

It is foreseen to operate each SM for seven days. All problems occurring during this period are corrected, if possible. A data acquisition and control system identical to the final one is used. Four different types of test runs are foreseen:

- **PEDESTAL SCAN**: to measure the pedestal DAC settings
- **PEDESTAL**: to measure mean and RMS of the pedestals
- **PULSE**: to measure test pulses injected by the MGPA
- **LASER**: to measure test pulses injected by the laser

For each type of test run a corresponding monitoring task is launched automatically at the completion of the run. It analyses the data and compares the results with nominal values. Summary reports and, in case of detected problems, detailed information about the channels concerned are stored in form of tables and histograms on a WEB-server. They are easily accessible through every browser application.

VI. RESULTS

Two super-modules, SM 11 and SM 5, were successfully assembled during April and May 2005. As estimated it took about 4 to 5 weeks to complete one SM.

In SM 11 eight problems were discovered. A channel with about 5 times the nominal noise, could not be cured. The test-pulse was not working correctly on two VFE cards. Two LVR cards were damaged during the installation and testing. In two cases the FE card did not communicate correctly with the DCU’s at the LVR. One channel with an increased noise level disappeared. The reasons for these could be identified and the related procedures were improved. Especially in the case of the VFE and FE cards it turned out that the failing part had not been fully tested prior to their installation.

Five problems were found in SM 5. Two VFE cards got their FE connectors damaged during installation. One FE card appeared not to function correctly and was replaced. Two GOH were replaced. For the later three problems very likely bad contacts or insertion of the connector was responsible. In all cases the problematic components were re-tested after dismounting and found to work correctly.

The noise performance of both SMs is identical. For gains 1, 6 and 12 the averages of the pedestal RMS values found are 0.5, 0.8 and 1.1 ADC counts, respectively. As an example Figure 8 and Figure 9 show the mean and RMS values of the pedestals of SM 5. The noise of 1.1 ADC counts in gain 12 corresponds to ~45 MeV, fully satisfying the requirements.

All the APD leakage current measurements were working correctly, but as the APD’s are not irradiated so far the measured values for all of them is ZERO. The temperature sensor readout for 170 sensors in SM 11 (see Figure 10) shows that all of them are working. Their average value corresponds to the cooling water temperature.

REFERENCES