A 16-channel Silicon Strips Readout Chip in 180nm CMOS technology

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Abstract

A highly integrated readout scheme for Silicon trackers making use of Deep Sub-Micron CMOS electronics (DSM) is presented. In the context of the International Linear Collider (ILC) trackers developments, a 16-channel readout chip for Silicon strips detector has been designed in 180nm CMOS technology, each channel comprising a low noise amplifier, a pulse shaper, a sample and hold and a comparator. Results are presented.

I. INTRODUCTION

A Front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimised keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the most available integrated technologies that allow to minimize the amount of material added to the detector, as well as the connexion capacitances in order to cope with a manageable amount of dissipated power.

For designs that covers of the order of 100 square meters and millions of channels, the multiplexing of tasks such as analogue to digital conversion and data compaction are mandatory. The full context of this work is described in the document available from the Website: http://www.linearcollider.ca/lcws05/h/Savoy.pdf

II. FRONT-END PROCESSING

The foreseen front-end processing is sketched in Figure 1. The Front-end signal processing chips amplify, filter, sample and digitize the input charge. Shaping times between 30ns and 100μs are foreseen, since it is intended to get the hit coordinate along the strip by timing between the two ends of the detector. This timing is presently under investigations.

More precisely, a low noise charge integrator stores the input signal in a 400F capacitor, giving an intrinsic gain of the order of 10mV/MIP at this level, assuming 24,000 electrons are deposited in a 300 μm thickness Silicon detector. The voltage step from the preamplifier is pulse-shaped by a CR-RC stage with a peaking time tunable between 2 and 6μs.

Figure 1: Front-end Processing

Two analog samplers, one fast, one slow, with 10ns and 100ns scale clocks respectively, generate samples of the analogue shaper output stored in two circular analogue buffers of depth 16 running continuously.

In order to store charge signals in the detector above a given threshold, an analogue sum of three neighbouring channels is compared to a voltage level, taken at the output of the slow shapers, for each channel. A trigger decision at this level freezes the analogue buffers, and selects an available set of two buffers for the next pulse to come. The total number of buffers for a given channel depends on the Silicon strips occupancy which is foreseen to be of the order of a few per cents. Therefore, a depth of 16 should cope with even worse detector output rate conditions.

This process runs for the total duration of an ILC train, of the order of one millisecond. At the end of the train, digitisation takes place. In order to minimize the power, a single ramp ADC is foreseen, allowing to digitise in parallel as many channels as possible. The cost in power per channel is due to one comparator stage only.

III. TEST CHIP

A test chip has been designed in a 180nm CMOS technology by United Microelectronics Corporation (Taiwan) available at multiproject cost through Europractice. It includes 16-channels comprising a low-noise preamplifier, a pulse shaper, a sample and hold, a voltage buffer and a comparator.
A single test channel allows to check all blocks reachable through six I/O pads. All stages have bias controls allowing to optimize each DC operating point.

A. Low-noise analogue section

The low-noise preamplifier (Figure 2) is a folded cascode stage with a PMOS input transistor biased under 40 µA, in weak inversion, the inversion coefficient being 0.06. The corresponding transconductance is 0.69mA/V.

The simulated open loop gain is 70dB, the simulated noise from this stage being 485 + 16.5e^-175/pF.

The drain is tied to ground at half the supply voltage, setting the DC point around -0.5V. The 400fF feedback capacitor is reset (or discharged with a given time constant) using a NMOS transistor controlled through an external voltage. The voltage gain of this stage is 8mV/MIP.

The pulse shaper (Figure 3) is an active CR-RC network using the same folded cascode structure as above, buffered with a source follower in order to drive the 600fF sample and hold capacitor. Two analogue controls allow to tune the peaking time in the microsecond range.

B. Sampling and Comparator

The sample and hold is switched with a single NMOS transistor sized to trade off between rise-time, possible leaks, and the injected charge resulting in a voltage offset. A voltage buffer drives the next stage, a comparator, which is a cascoded differential pair followed by inverters driving the output pads.

IV. TEST CHIP RESULTS

A. Gain and Linearity

The measured gain of 8mV/MIP is in agreement with the simulations. Dynamic range is 70 MIPS for the amplifier and 50 MIPS for the shaper, instead of 100 MIPS and 60 MIPS simulated. In addition, the deviation from linearity from the preamplifier is 1.5% instead of 0.5% simulated, and 5% for the shaper, for low amplitudes values. This is understood as a non-linear behaviour of the cascode stages operating in weak inversion, that was not accurately predicted in the simulations.

B. Noise

The electronics noise comes mainly from the low-noise preamplifier input PFET. The measured noise of this stage is 498 + 16.5e^-1/pF, as simulated. The noise from the shaper is 584 + 10.1e^-1/pF; instead of 280 + 8.9e^-1/pF simulated, due to a small bump in the frequency response around 6 MHz, that can be easily removed in a future version.
At 70µW input stage power, 50pF detector capacitance, 3 µs shaping time, the various contributions to the detector and front-end electronics noise are summarized in Table 1.

Table 1: Foreseen detector noise contributions at 50 pF detector capacitance, and 3 µs shaping time

<table>
<thead>
<tr>
<th>Noise source</th>
<th>Value</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input PFET</td>
<td>$g_m = 0.69 mA/V$</td>
<td>1089 e-</td>
</tr>
<tr>
<td>Detector leak</td>
<td>10 nA</td>
<td>588 e-</td>
</tr>
<tr>
<td>Bias resistor</td>
<td>10 MΩ</td>
<td>423 e-</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>1308 e-</td>
</tr>
</tbody>
</table>

According to the noise models from the manufacturer, no 1/f noise should show up, even at 10$\mu$s shaping time. If this were the case, Silicon -Germanium technology could be an effective alternative both for low frequency noise reduction and speed performance having in view the timing measurements.

The 70µW power dissipated in the preamplifier is mainly due to the input transistor biasing, in order to obtain a sufficient gain leading to the noise performance of the stage. In case of lower noise requirements, particularly for long strips, an increase of power could be envisaged, leading for instance to lower noise slopes below 8e-/pF.

C. Power

In order to take advantage of the ILC machine timing, all electronic stages running during the collisions only could be switched off for the readout stage. Therefore, a factor 100 to 200 could be saved at this level. This process has been simulated to be effective with the present front-end electronics provided the integration capacitor is reset before power-off and after power-on.

V. CONCLUSION AND FUTURE WORK

These encouraging results regarding the integration of a front-end electronics for Silicon detectors in Deep Sub-Micron CMOS will be pursued by tests on an actual Silicon detector equipped with wire-bonded bare chips under MIP signals from a radioactive source, and in a particle beam. Results will be compared with other front-end chips off the shelf in the same environment.

A 128-channels version that include fast and slow shapers, the sparsifier stage, analogue samplers and a full ADC, digital section including possibly digital filtering and lossless data compression, power switching, is under design and will benefit from the lessons learnt after this prototyping work.

Acknowledgments

The authors wish to thank Erwin Deumens for his kind help at Europractice (Leuven, Belgium) particularly at the chip post-layout simulations stage, and Guillaume Daubard for designing a suitable chip socket at LPNHE Paris.