Cadence®

High-Speed PCB Design Flow

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(Electronic Applications Support)
Training Description

- **Objective**
  - Cadence front-end PE14.2 high-speed printed circuit board design flow presentation. Based on Constraint Manager concurrently with Concept-HDL schematic and SPECCTRAQuest/SigXplorer signal integrity analysis package.

- **Recommended for**
  - Digital electronics designers using Cadence CAD tools having signal integrity and/or timing issues on their high-speed boards.
  - Designers working with Gigabit channels or using current fast standard logic families (LVCMOS, LVDS, LVPECL, HSTL, SSTL, GTL, etc.).
  - Users of more traditional technologies on big board format such as VME9U.
Programme

- High-Speed Board Design Issues & Solution Available @ CERN
- Constraint Manager Principles
- Basic Layout Data Base Setup
- Designers’ Workflows
- Real Case Study
  - Description
  - Demo: Before Layout
  - Layout Implementation
  - Demo: After Layout
- Conclusion

- Appendix 1: Constraint Manager Enabled Flow
- Appendix 2: IBIS Models Supply and Checking
- Appendix 3: First Switch and Final Settle Delay Measurements Points
High-Speed Board Design Issues
&
Solution Available @ CERN
High-Speed Board for LHCb Experiment

NP4GS3 Network Processor Daughter Board

- 14 layers ± 10%
- Controlled Impedance Board
- 1088-Pin (CCGA) Package
- Fine Pitch 1.27 mm
- 815 I/O

DATA-ALIGNED SYNCHRONOUS LINKS (DASL)
- 2 x 8 EIA/JEDEC JESD8-6 standard channel for differential HSTL
  (Up to 625 Mbps per channel)

Double Data Rate SDRAM INTERFACE
- JEDS8-9A SSTL2 Standard
- Stub Series Terminated Logic for 2.5V
- CLK 133 MHz

2 x 4 GIGABIT MEDIA INDEPENDENT INTERFACE UNITS (GMII)
- (4 GIGABIT ETHERNET)
- Full Duplex 8 bit data Bus 125 MHz Clock
- LVTTL
High-Speed Board Design Issues

- **Typical High-Speed Board Design Issues**
  - Fast edge rates < 500ps
  - Very high pin density
  - Via number control
  - Single ended and differential Zo controlled impedance
  - Various termination types (thevenin, serie, etc..)
  - Min/max propagation delays
  - Cross-talk
  - Total etch length
  - Relative (Matched) length propagation delay
  - Package parasitic effects
  - Clock & Buses timing constraints with accurate set up & hold

- **Multiple constraints exist on each net**

- **Integrating Requirements is Essential for Success!**
High-Speed PCB Design Flow

Based on the New “Constraint Manager” Programme Linking

- Signal Explorer Expert (SigXplorer) pre and post layout exploration tool
- Concept-HDL schematic capture tool
- SPECCTRAQuest SI Expert post-layout SI analysis tool
- ALLEGRO-Expert and SPECCTRA layout implementation tools
**Designer’s Tools**

- **Exploration under SigXplorer**
  - Topologies Analysis Tools
  - Topologies development, signal integrity analysis
  - Electrical constraints development
- **Schematic Capture under Concept-HDL**
  - Electrical constraints capture with Constraint Manager Connected to Concept-HDL (CM2C) and/or SigXplorer
- **Layout Database Setup under SPECCTRAQuest**
  - Layout database setup with Constraint Manager Connected to SPECCTRAQuest (CM2SQ)
  - Electrical constraints mapping
SigXplorer in the High-Speed Design Flow

EX: Pre layout (Exploration) Phase TOPOLOGY development under SigXplorer
Implementation Phase

- Electrical constraints driven placement and routage with Constraint Manager Connected to Allegro-Expert layout editor (CM2AE)
- Interactive (Allegro) or automatic (SPECCTRA) placement and routage
Constraint Manager Principles
What is Constraint Manager (CM)?

- Constraint Manager is a Spreadsheet based Application handling OBJECTS and Electrical Constraints Sets (ECSets)
**Constraint Manager Objects (1/5)**

- **Pin Pair**
  - A *pin-pair* represents a pair of logically connected pins, often a driver-receiver connection.
  - You may specify pin-pairs explicitly (for example, U1.8 – U2.8), or they can be derived based on the following criteria:
    - longest pin-pair
    - longest driver-receiver pair
    - all driver-receiver pair

- **Pin-pair Objects Not Supported in Concept-HDL 14.2**
Constraint Manager Objects (2/5)

- **Net**
  - Basic connectivity as defined in the schematic

- **XNet**
  - An eXtended Net XNet chains through passive discrete device(s) (resistor, inductor, capacitor)
  - XNet can also traverse connector and cables in a multiboard configuration

**XNet Objects Not Supported in Concept-HDL 14.2**
Constraint Manager Objects (3/5)

- **Diff Pair**
  - An electrical differential pair *Diff-Pair* represents a coupled pair of Net or XNet which will be routed differentially

- Diff Pair Objects Not Supported in Concept-HDL 14.2

- **Bus**
  - A *Bus* represents a named collection of diff-pairs, Nets or XNets

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*Cadence® High-Speed PCB Design Flow - Constraint Manager Principles*
Constraint Manager Objects (4/5)

- **Relative/Matched Group**
  - A *Relative/Matched Group* represents a user-specified collection of *pin-pairs* constrained by a relative or match delay or length
  - The following attributes are used to characterize a *Relative/Match Group*
    - **Target**: The pin-pair that is referenced by all pin-pairs in the group
    - **Delta**: The difference between each pin-pair member and the target pin-pair.
    - **Tolerance**: The tolerance allowed when matching members in the group

- **Example (Top Layer View)**

  - Matched Group (M1)
    M1 = Data <0..7> + DQS0

  - To maintain a matched propagation delay, 8 Data Nets (4 in the top layer), are extended to match the length of (DQS0) strobe

  ![Diagram](image-url)
  
  Target (Strobe DQS0)
Constraint Manager Objects (5/5)

- **Design**
  - A *Design* represents a stand-alone board or a board in a system
  - In a multi-board configuration, each board becomes a separate design in the system

- **System**
  - A *System* represents a configuration of designs (boards) including XNets that traverse these design and their interconnecting cables and connectors
Object Hierarchy

- **Goal is to assign constraints at the highest possible level**
  - Constraints that you specify at the top level of the hierarchy become inherited by the next lower-level object
- **Special exception cases can be handled by overrides at lower level**
Electrical Constraint Sets (ECSets)

- **What is an ECSet?**
  - AN ECSet is a *collection* of *generic simulated* and/or *computed* CONSTRAINTS requirements.
  - You define one or more ECSets to capture design requirements.
  - You then assign the appropriate ECSet to objects in your design.

- **ECSets Types**

  - [Electrical Constraint Set]
    - [Signal Integrity]
      - Reflection/Edge Distortions
      - Xtalk/SSN
    - [Timing]
      - Switch/Settle Delays
    - [Routing]
      - Wiring
      - Impedance
      - Min/Max Propagation Delays
      - Total Etch Length
      - Relative Propagation Delay

  - **Simulated (post layout)**
  - **Computed (real time)**
**Computed ECSets Types**

- **Routing ECSets**
  - Routing constraints analysis (handling *lengths/*prop delay* and *impedances*) does not need simulation,
  - Are calculated and flagged in *real time* by *Constraint Manager* (CM)

- **Routing Constraint Violation Example**

```
<table>
<thead>
<tr>
<th>Objects</th>
<th>Prop Delay</th>
<th>Prop Delay</th>
<th>Prop Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Actual</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td>mil</td>
<td>mil</td>
<td>mil</td>
</tr>
<tr>
<td>System</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mez_55 routed reference</td>
<td>-455.19 MIL</td>
<td>-576.08 ...</td>
<td>-576.08 ...</td>
</tr>
<tr>
<td>D6_ADDR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_DATA</td>
<td>-455.19 MIL</td>
<td>1476.00 ...</td>
<td>-576.08 ...</td>
</tr>
<tr>
<td>D6_DQS</td>
<td>1476.00 ...</td>
<td>1476.00 ...</td>
<td>1476.00 ...</td>
</tr>
<tr>
<td>D6_DQS0</td>
<td>1476.00 ...</td>
<td>1476.00 ...</td>
<td>1476.00 ...</td>
</tr>
<tr>
<td>IC1_AL3886.1</td>
<td>0 MIL</td>
<td>1476.00 ...</td>
<td>1476.00 ...</td>
</tr>
<tr>
<td>R6.23G4.51</td>
<td>0 MIL</td>
<td>2400 MIL</td>
<td>1872.43 ...</td>
</tr>
</tbody>
</table>
```

High-Speed PCB Design Flow - Constraint Manager Principles -
Simulated ECSets Types

- **Signal Integrity & Timing Constraints**
  - Signal Integrity & Timing constraints analysis values are the result of analogue simulations.
  - Electrical Constraints simulations results are displayed in CM worksheets and/or SPECCTRAQuest simulation reports.
  - The Cadence TLSim simulator is a SPICE-like engine using DML Cadence proprietary format.
  - DML (Device Model) format is the Cadence implementation of IBIS behavioural signal integrity models for signal integrity analysis.
  - IBIS is a “component centric” standard ideal for board level simulation. It is widely supported by ICs manufacturers.

Simulations results displayed in CM Switch/Settle Delays worksheet.
Invoking Constraint Manager

- **Standalone for Design Exploration**
  - Unix prompt type → `consmgr`

- **From Concept-HDL (CM2C)**
  - Tools → Constraints → Edit
  - Should only be run on a PACKAGED schematic
  - Constraint Manager invoked from Concept-HDL does not presently support Pin Pairs, XNets and Differential pair (only supported by layout data base)

- **From SPECCTRAQuest (CM2SQ)**
  - Setup → Electrical Constraint Spreadsheet...
  - Icon
Worksheet Selector

- The worksheet selector is the only way to select (open) the various worksheets within CM.

The “Electrical Constraint Set” worksheets are used for creating and/or editing the Rule Sets.

The “Net” worksheets are used for interfacing with the design objects such as applying the rules or seeing if they can be met.
Constraint Manager User Interface (2/7)

- Example: Min/Max Propagation Delay Worksheet Selection
Constraint Manager User Interface (3/7)

- Objects Column in a Nets Folder Routing Worksheet

- Design

- Buses

- Net

- Pin Pair

- XNet

- Pin Pairs
**Constraint Manager User Interface (4/7)**

- **ECSet Mapping to Objects**
  - On individual Net, selected Nets, Bus, selected Buses, etc..
  - 3250 Mils Longest/Shortest Driver/Receiver Max length

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**Electrical Constraint Sets: Routing**

<table>
<thead>
<tr>
<th>Objects</th>
<th>Pin Pairs</th>
<th>Min Delay</th>
<th>Max Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mez_55_placed_reference_bis</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTRL_ADD</td>
<td>Longest/Shortest Driver/Receiver</td>
<td>3250 MIL</td>
<td></td>
</tr>
<tr>
<td>DA_DQS</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Nets: Routing**

<table>
<thead>
<tr>
<th>Objects</th>
<th>Referenced Electrical CSet</th>
<th>Pin Pairs</th>
<th>Prop Del</th>
<th>Prop Delay</th>
</tr>
</thead>
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<td>System</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mez_55_placed_reference_bis</td>
<td></td>
<td></td>
<td></td>
<td>-209.53 ...</td>
</tr>
<tr>
<td>D6_ADDR</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CNTRL_ADD</td>
<td>Longest/Shortest ...</td>
<td>3250 MIL</td>
<td>-209.53 ...</td>
</tr>
<tr>
<td></td>
<td>IC1.A128:IC4.29</td>
<td></td>
<td>3250 MIL</td>
<td>16.06 MIL</td>
</tr>
<tr>
<td></td>
<td>IC1.A126:IC4.30</td>
<td></td>
<td>3250 MIL</td>
<td>-209.53 ...</td>
</tr>
<tr>
<td></td>
<td>D6_ADDR2</td>
<td>CNTRL_ADD</td>
<td>3250 MIL</td>
<td>-209.53 ...</td>
</tr>
<tr>
<td></td>
<td>IC1.AE24:IC4.31</td>
<td>Longest/Shortest ...</td>
<td>3250 MIL</td>
<td>64.88 MIL</td>
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<td>D6_ADDR3</td>
<td>CNTRL_ADD</td>
<td>3250 MIL</td>
<td>-209.53 ...</td>
</tr>
<tr>
<td></td>
<td>IC1.AG26:IC4.32</td>
<td>Longest/Shortest ...</td>
<td>3250 MIL</td>
<td>29.05 MIL</td>
</tr>
</tbody>
</table>
Constraint Manager User Interface (5/7)

- Viewing ECSets References

- DA_DQS ECSets applied to BUSES
- CNTRL_ADD ECSets applied to BUSES and NETS
Colour Coding

- Cells are BLACK and BLUE colour coded to indicate inheritance for constraints.
- Results status displayed in YELLOW, GREEN or RED

**Blue** indicating the ECSet has been originally applied in this cell

**Blue** indicating that this cell was overwritten (3500 Mils) on NET D6_ADDR0

**Black** indicating the ECSet are inherited on each NET

3250 Mils in **black** indicating that this value is inherited on Pin Pair from “CNTRL_ADDR” ECSet (Prop Delay/Max Length) constraint value
Constraint Manager User Interface (7/7)

- **STATUS BAR Information Type**
  - Progress meter for simulations
  - Brief description of commands
  - Reasons why items are greyed out

Placing cursor over an object in the display provides information on the STATUS BAR below.
Constraint Manager Enabled Flow
Vs
Traditional Flow

 мер First Time you Invoke Constraints Manager from Concept-HDL and/or SPECCTRAQuest-Expert
- You are in CONSTRAINT MANAGER ENABLED FLOW
- You can not go back automatically to the traditional flow

 мер If you Have Launch Constraint Manager by Mistake
- You can go back to the TRADITIONAL DESIGN FLOW deleting files and director automatically created, SEE APPENDIX1: Constraint Manager Enabled Flow
Basic Layout Data Base

Setup
Basic Layout Data Base Setup From SPECCTRAQuest-Expert

- **Layout Cross Section**
  - Define by Designer WITH AGREEMENT OF LAYOUT DESIGNER EXPERT AND/OR BOARD MANUFACTURER
  - You can define a set of typical microstrip and stripline. Later in the design flow it will be easy to add or erase conductors layers
  - SQ Setup Form: Setup → Cross Section
  - Provides data for SPECCTRAQuest Field Solver to compute accurate transmission line modelling of traces
  - Determines trace characteristics such as impedance and propagation velocity

Microstrip or Stripline Impedances are computed in real time by the Field Solver each time we change a parameter (line width etc..), helping designer to find optimum combination of material, thickness and PCB CLASS
Identifying DC Nets

- SQ Identify DC Nets Form: Logic \( \rightarrow \) Identify DC Nets.
- Makes sure simulations in SPECCTRAQuest or SigXp have the correct voltage for circuits.
- Prevents XNets from including wrong nets.

![Identify DC Nets Form](image-url)
Discrete (R, L, C) DML Signal Model Assignment

- Signal Model Assignment Form: Analyse → SI/EMI Sim → Model..
- DML discrete models assignment are the minimum models assignment (also called Espice models) that must be done for all analysis cases (Routing or SI & Timing)
- Without this assignment the system will not be able to develop XNet from the layout database
- If component libraries include CLASS, VALUE and PINUSE, Auto Setup button automatically setup this process for 2 pin discrete
- Discrete with more than 2 pins could be easily created via Create Model button

Ex: DML (or ESPice) models assigned to resistors terminations

This button will automatically make Espice models for all 2 pins discretes
**Optional IBIS (DML) Models Assignment**

- Signal Model Assignment Form: **Analyze → SI/EMI Sim → Model**...
- Optional assignment that must be done on ICs
- Simulated analysis supported by **Signal Integrity** or **Timing** workbooks needs IBIS models assignment
- See APPENDIX 2: IBIS Models Supply and Checking
- It is not necessary to assign IBIS models for computed analysis (see later workflow)

Default models are automatically assigned by the system.

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**Ex: IBIS (DML) models:**
6 x K4H280838C_TC DDR SDRAM memory model

**Ex: IBIS (DML) models:**
1x NP4GS3B Network Processor Model

**Start IBIS (DML) process assignment for active devices (ICs)**
Designers’ Workflows
## Typical Designers’ Workflows

<table>
<thead>
<tr>
<th>Designers’ Workflows Type</th>
<th>Purpose</th>
<th>Post-layout Signal Integrity and/or Timing simulations needed</th>
<th>Need of IBIS models</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1</strong> Rules based</td>
<td>To implement layout rules from components manufacturer</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>2</strong> Rules based</td>
<td>To implement layout rules from components manufacturer</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>with PCB simulations</td>
<td><em>Then check them (simulate)</em> on post-layout board</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>3</strong> Constraints</td>
<td>To develop yourself layout rules. Any guideline available</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>development</td>
<td>from manufacturer  <em>Then implement</em> them</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>4</strong> Constraints</td>
<td>To develop yourself layout rules. Any guideline available</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>development</td>
<td>from manufacturer  <em>Then implement</em> and check them (simulate) on post-layout board</td>
<td></td>
<td></td>
</tr>
<tr>
<td>with PCB simulations</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
- Workflow - Rules Based

- A → schematic capture with Concept-HDL
- B → ECSets capture under Constraint Manager (CM2C)
- C → export physical (Packager-XL + NETREV)
- D → Basic layout DTB setup: cross section, DC nets identification, discrete (R, L, C) Autosetup models assignment
- E → ECSets mapping to physical NETs
- F → post layout constraints check (calculated)
- H → (optional) ECSets change back annotation

To/From Layout

Before layout

After layout
- Workflow 2 - Rules Based With PCB Simulations

- **Workflow 1**: Same as Workflow 1
- **D1**: Ibis libraries setup & models assignment
- **G**: Simulated constraints analysis (from Signal Integrity & Timing Workbooks)
- Workflow ③ - Constraints Development

**Capture**
- Concept-HDL
  - Constrained Schematic
  - Constraint Manager Connected to Concept-HDL
  - ECSets
  - SigXplorer
    - Constrained Topologies

**Design Sync**
- Export Phys
- Import Phys

**Layout DTB Setup**
- SPECCTRAQuest
  - Constrained Board Database
  - Constraint Manager Connected to SPECCTRAQuest
  - Physical NETs
  - ECSets

---

- **A + C + D + E + F + H** \(\rightarrow\) same as Workflow ①
- **B1** \(\rightarrow\) Ibis (Dml) libraries declaration
- **B2** \(\rightarrow\) constrained topologies development from SigXplorer
- **B3** \(\rightarrow\) constrained topologies importation in Constraint Manager connected to Concept

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**To/From Layout**
- Before layout
- After layout

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*Cadence® High-Speed PCB Design Flow - Designers’ Workflow -*
- Workflow - Constraints Development
With PCB Simulations

A + B1 + B2 + B3 + C + D + E + F + H → same as Workflow
D1 → Ibis models assignment
G → simulated constraints analysis (from Signal Integrity & Timing Workbooks)
Real Case Study

(Description)
To layout WITH MANUFACTURER GUIDELINES a subset of NP4GS3 DDR SDRAM interface

- 64 MB DDR SDRAM
- 6 Samsung (32X4) K4H280438C-TCA2
- I/O technologies Stub series Terminated Logic 2.5V (SSTL2) & CMOS
- 66 pins TSOP II Package

D6 INTERFACE ARCHITECTURE
- 18 bits DATA BUS
- 13 bits ADDRESS BUS
- Differential Clock
- Clock Cycle 133 MHZ
- Double-data rate architecture; two transfers per clock cycle
- I/O technologies Stub series Terminated Logic 2.5V (SSTL2) & CMOS
**CNTRL & ADDR Manufacturer Guidelines**

**CNTRL_ADDR Lines Constraints**

- Control and address lines are six-drop lines terminated into a $50 \, \Omega$ equivalent circuit.
- Board Stackup controlled impedance = $55 \, \Omega \pm 10 \%$
- The distance from NP4GS3 to the furthest SDRAM must not exceed 3.25 inches.
- The stub to the SDRAM pin should not be more than 0.25 inches.

**50 Ohms Thevenin Equivalent Terminations**

$Z_{o} = 55 \, \Omega \pm 10\%$

$L \leq 3.25 \text{ inches}$

$\text{Stub} \leq 0.25 \text{ inches}$
DATA & DQS Manufacturer Guidelines

- **DA_DQS Lines Constraints**
  - All DATA and DQS nets must be terminated with a 22-29 Ω series resistor placed no more than one inch from the NP4GS3.
  - No more than 25% of the trace should be on the NP4GS3 side of the terminating resistor.
  - Each set of DATA and DQS lines must be no shorter than one inch and no longer than 3.25 inches.
  - For each set of four DATA lines and its respective DQS line, there can be no more than ±70 ps of flight time difference from the NP4GS3 to the RAM. Use IBIS simulation to be sure that there is no more than ±70 ps difference between DQS and its corresponding DATA lines.

![Diagram showing DATA & DQS lines with constraints and placements](image-url)
**Demo Workflow**

- **A** → **Concept-HDL**: schematic capture
- **B** → **CM2C**: CNTRL_ADD ECSets capture
- **B1** → **SigXp**: Ibis (Dml) libraries declaration (DDR SDRAM & NP4GS3) before DA_DQS (XNet) topology capture
- **B2** → **SigXp**: DA_DQS constrained topology capture
- **B3** → **Concept-HDL**: DA_DQS constrained topology importation from SigXp (ECSets)
- **C** → **Concept-HDL**: export physical (Packager-XL + NETREV)
- **D** → **SPECCTRAQuest-Expert**: Basic layout DTB setup; cross section, DC nets Identification, discrete (R, L, C) Autosetup models assignment
- **D1** → **SPECCTRAQuest-Expert**: Ibis models assignment: (6 x DDR SDRAM & 1 x NP4GS3)
- **E** → **CM2SQ**: CNTRL_ADD & DA_DQS: ECSets mapping to physical NETs
- **F** → **CM2SQ**: post layout constraints check
- **G** → **CM2SQ**: DATA Timing skew simulation

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*Cadence® High-Speed PCB Design Flow - Real Case Study (Description) -*
Real Case Study

(Demo: Before Layout)
Concept-HDL: Schematic Capture [ Step A ]

Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: Before Layout) -
**CM2C: CNTRL_ADD ECSet Capture [ Step B ]**

- **To Create an object**
  - From CM2C: Objects → Create → Electrical CSet..

<table>
<thead>
<tr>
<th>Objects</th>
<th>Topology</th>
<th>Stub Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td>PinUse</td>
<td>Daisy-chain</td>
</tr>
</tbody>
</table>

**Stub length** for daisy chain routing

**Daisy-Chain schedule** consists of connecting the pins of the topology with minimum connection length but only allowing each pin to connect to a maximum of two other pins.

**Mapping mode** is used when the ECSet schedule is applied to XNets/Nets in physical data base. **Pinuse** map the ECSet’s pins to the Net using the PINUSE setting.

---

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**Mapping mode** is used when the ECSet schedule is applied to XNets/Nets in physical data base. **Pinuse** map the ECSet’s pins to the Net using the PINUSE setting.
Comments on CM2C Wiring Worksheet
Mapping Mode & Pre-Defined Schedules

<table>
<thead>
<tr>
<th>Objects</th>
<th>Mapping Mode</th>
<th>Verify Schedule</th>
<th>Schedule</th>
<th>Stub Length mil</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mezzanine1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTRL_ADD</td>
<td>Pinuse</td>
<td>Yes</td>
<td>Daisy-chain</td>
<td>250.00</td>
</tr>
<tr>
<td>DA_DQS</td>
<td>Pinuse and Refdes</td>
<td>Yes</td>
<td>TEMPLATE</td>
<td></td>
</tr>
</tbody>
</table>

Pre-defined Mapping Mode:
- Pinuse
- Refdes
- Pinuse and Refdes
- Clear (any)

Pre-defined Shedule:
- Minimum spanning Tree
- Daisy-chain
- Source-Load Daisy-chain
- Star
- Far-end cluster
- Clear (any)

XNets scheduling is not pre-defined by the system. But any structure of TOPOLOGY TEMPLATE could be captured then imported from SigXplorer

Following steps [ B1 + B2 + B3 ] are Mandatory to Capture DA_DQS XNet Topology Template
SigXp: Ibis Libraries Declaration for DA_DQS Topology Capture [ Step B1 ]

- Libraries Declaration
  - From SigXp: Analyse → Libraries

28h4088a.ibis (or dml) library file downloaded from SAMSUNG Web Site

Models used for DA_DQS constrained topology development (next slide)

np4gs3b.ibis (or dml) library file delivered by the manufacturer
SigXp: DA_DQS
Constrained Topology Capture (1/4) [ Step B2 ]

- **DA_DQS Topology Edition**
  - File: da_dqs.top

NP4GS3 Packaged IBIS I/O Model
SSTL2 Technology

DDR SDRAM Packaged IBIS I/O Model
SSTL2 Technology

Constrained Topology
(da_dqs.top file)

55 Ohms Transmission Lines

Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: Before Layout) -
SigXp: DA_DQS Constrained Topology Capture (2/4) [ Step B2 ]

- **To capture Constraints**
  - From SigXp: Set $\rightarrow$ Constraints

- **DA_DQS Impedance Constraints Capture**

- **DA_DQS Length Constraints Capture**
SigXp: DA_DQS Constrained Topology Capture (3/4) [ Step B2 ]

- DA_DQS_M1 Skew Rule Capture

A Relative propagation delay constraint identifies a group of pins pairs with DELTA and tolerance. One of the pin pair will be later in the physical data base selected as the TARGET and all of other pin pairs will be matched against this target within the given delta and tolerance.

Rule Name “DA_DQS_M1” M1 = Matched group1 OBJECT

All members of the group; a set of 4 DATA lines and its respective DQS line, must match (Δ=0 ns) within 15ps tolerance.
SigXp: DA_DQS
Constrained Topology Capture (4/4) [ Step B2 ]

- DA_DQS Pin Sequencing Constraints Capture

Mapping mode is used when the ECSet schedule is applied to XNets/Nets in the physical data base. “Pinuse and Refdes” maps the ECSet’s pins to the Net using the “da_dqs” topology (pinuse & refdes) combination.

Template schedule means the topology template scheduling should follow “da_dqs.top” topology.
Concept-HDL: DA_DQS ECSets Importation from CM2C [ Step B3 ]

- ECSets Importation in CM2C then Concept-HDL update
  - CM2C: File → Import → Electrical CSet..
  - Then Concept-HDL: Tools → Constraints → Update Schematic

- ECSet: Wiring Worksheet
- ECSet: Impedance Worksheet
- ECSet: Min/Max Propagation Delays Worksheet
- ECSet: Relative Propagation Delay Worksheet
Concept-HDL: Export Physical [ Step C ]

- Packaging with ECSets Exportation
  - Concept-HDL: File → Export Physical...

6 layers 55 Ω ± 10% mezzanine board template

Electrical constraints enabled

Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: Before Layout) -
Step D: Basic Layout DTB Setup

- Mezzanine Cross section
  - Mezzanine cross section
  - Already presented in previous “Basic Layout Data Base Setup” section
- Mezzanine DC Nets
  - Three voltage (0V, 1.8V, 2.5V) DC Nets identification
  - Already presented in previous “Basic Layout Data Base Setup” section
- Terminations (R) Models Assignment
  - Auto Setup terminations models assignment (22 Ω, 100 Ω, 10 K Ω)
  - Already presented in previous “Basic Layout Data Base Setup” section

Step D1: Ibis Models Assignment

- NP4GS3 & K4H280838C Ibis models assignment
- Already presented in previous “Basic Layout Data Base Setup” section
CM2SQ: CNTRL_ADD & DA_DQS (1/4) 
ECSets Mapping [ Step E ]

- Impedance ECSet Mapping

[Diagram with ECSet reference and Objects column shown]

Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: Before Layout) -
CM2SQ: CNTRL_ADD & DA_DQS (2/4) ECSets Mapping [ Step E ]

- Min/Max Length ECSet Mapping

Min/Max Length ECSet Mapping on Physical NETs

- CNTRL_ADDR ECSet
- DATA0 Pin Pair
- DA_DQS ECSet
CM2SQ: CNTRL_ADD & DA_DQS (3/4) ECSets Mapping [ Step E ]

- Wiring ECSet Mapping

[Image of Cadence Constraint Manager showing ECSet mapping on physical nets]
CM2SQ: CNTRL_ADD & DA_DQS (4/4) ECSets Mapping [ Step E ]

- Relative Propagation Delay ECSet Mapping

- Match Group Object (M1) Automatically Created on DA_DQS ECSet Mapping

- Match Group M1 5 Pin Pairs Membership

- Pin Pair Target (DQS0)

- DQSO TARGET Pin Pair Selection

- No analyses result for the target
Real Case Study

(Layout Implementation)
Layout Designer’s Workflow

1 → 4

From/To Designer

1️⃣ DTB check: layout impedance cross section with SPECCTRAQuest exclusively
2️⃣ DTB check: DC Nets assignment with ALLEGRO-Expert or SPECCTRAQuest
3️⃣ DTB check: discrete (R, L, C, ) model assignment with ALLEGRO-Expert or SPECCTRAQuest
4️⃣ DTB check: active (ICs) models assignment with with ALLEGRO-Expert or SPECCTRAQuest
5️⃣ DTB check: ECSets mapping to physical NETs with Constraint Manager connected to ALLEGRO-Expert
6️⃣ constraints driven placement and routing with ALLEGRO-Expert and optionally SPECCTRA

It is recommended to review steps 1 to 5 with the layout expert
Interactive (Allegro) or automatic (SPECCTRA) placement and routage

Once the constraints are present in the ALLEGRO database, they are used to drive the placement and routing process for those signals.

The constraint manager is completely integrated with the Allegro design rules checking system, this means that the different high-speed rules can be checked in real-time as the design process proceeds, with the results presented as part of the CM spreadsheets.

Any design parameters that do not meet their associated constraints values are highlighted. At any point during physical design users can launch the Constraint Manager to view high-speed constraint information associated with the design.
Real Case Study

(Demo: After Layout)
CM2SQ: Post layout Constraints Violation Check (1/5) [ Step F ]

- **Mezzanine Board Database From Layout**
  - Mezzanine fully placed and partially routed:
    - Components placed on two sides
    - Routed lines ADD <0..3> and DATA <0..3> + DQS0

Constraints violation check, two forms:
- Electrical DRC marker
- CM2SQ Violation parameters and color
CM2SQ: Post layout Constraints Violation Check (2/5) [ Step F ]

- CM2SQ: Constraints Violation Check on Mezzanine Database

Any constraint violation
CM2SQ: Post layout Constraints Violation Check (3/5) [ Step F ]

- CM2SQ: Example of Constraint (Length) Violation

Example of length violation on DQS0 line
CM2SQ: Post layout Constraints Violation Check (4/5) [ Step F ]

- **SPECCTRAQuest DQS0 Length Violation Form 1**
  - Electrical DRC bow tier marker enable
    - SPECCTRAQuest: **Display → Color/Visibility (DRC THROUGH ALL ON)**

  R6 DQS0 serial termination resistor is placed too far from the driver

- **CM2SQ DQS0 Length Violation Form 2**
  - Red colour on violated parameters constraints

DQS0 pin pair from the NP4GS3 driver to the serial termination resistor is over 800 MIL maximum length
**SigXp: Topology Check (5/5) [ Step F ]**

- Post Layout ADDR1 SigXplorer Topology Extraction

**ADDR1 Daisy Chain Topology**

**Stub Length ≤ 250 mils**

---

**Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: After Layout)**
**CM2SQ: DATA / DQS0 Timing Skew Simulation**

[Step G]

- **Min First Switch Max Final Settle Simulations**
  - APPENDIX 3:
    - First Switch Delay Measurements Points
    - Final Settle Delay Measurements Points

### Cadence® High-Speed PCB Design Flow - Real Case Study (Demo: After Layout) -

#### Constraint Manager (connected to SPECTRAQuest SI Expert 14.2) – [Nets: Timing]

<table>
<thead>
<tr>
<th>Objects</th>
<th>Reference</th>
<th>Min First Switch Delay Measurements Points</th>
<th>Rise Actual</th>
<th>Fall Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.303</td>
<td>1.223</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.101</td>
<td>1.066</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.307</td>
<td>1.200</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.175</td>
<td>1.198</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.337</td>
<td>1.313</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.147</td>
<td>1.172</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.418</td>
<td>1.566</td>
<td></td>
</tr>
<tr>
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<td>DA_DQS</td>
<td>1.236</td>
<td>1.251</td>
<td></td>
</tr>
<tr>
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<td>DA_DQS</td>
<td>1.376</td>
<td>1.316</td>
<td></td>
</tr>
<tr>
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<td>DA_DQS</td>
<td>1.155</td>
<td>1.100</td>
<td></td>
</tr>
<tr>
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<td>DA_DQS</td>
<td>1.550</td>
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<td></td>
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<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.418</td>
<td>1.439</td>
<td></td>
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<td>DA_DQS</td>
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<td>DA_DQS</td>
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<td>1.940</td>
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<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.939</td>
<td>1.972</td>
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<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.283</td>
<td>1.485</td>
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<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.615</td>
<td>1.547</td>
<td></td>
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<tr>
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<td>DA_DQS</td>
<td>1.660</td>
<td>1.497</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.543</td>
<td>1.479</td>
<td></td>
</tr>
<tr>
<td>DE_DATA</td>
<td>DA_DQS</td>
<td>1.492</td>
<td>1.453</td>
<td></td>
</tr>
</tbody>
</table>
### CM2SQ: DATA / DQS0 Timing Skew Simulation [ Step G ]

- **Min First Switch Max Final Settle $\Delta$ max**

<table>
<thead>
<tr>
<th></th>
<th>Min First Switch</th>
<th>Max Final Settle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Rise</td>
<td>Fall</td>
</tr>
<tr>
<td>DATA0</td>
<td>1383 ps</td>
<td>1323 ps</td>
</tr>
<tr>
<td>DATA1</td>
<td>1397 ps</td>
<td>1336 ps</td>
</tr>
<tr>
<td>DATA2</td>
<td>1373 ps</td>
<td>1313 ps</td>
</tr>
<tr>
<td>DATA3</td>
<td>1418 ps</td>
<td>1356 ps</td>
</tr>
<tr>
<td>DQS0</td>
<td>1376 ps</td>
<td>1316 ps</td>
</tr>
</tbody>
</table>

+ $\Delta$ max = DATA(X) max – DQS0

- $\Delta$ max = DATA(X) min – DQS0

#### CONCLUSION

Layout Satisfied Manufacturer Constraints

2 ps above manufacturer guidelines
Conclusion
Conclusion on Cadence PSD 14.2
High-Speed PCB Design Flow
Using Constraint Manager

◆ Proposed High-Speed Workflows Advantages

- Cadence’s PSD14.2 “High-Speed PCB Design Flow” based on Constraint Manager provides a consistent way to create, manage and validate Designer’s intent.
- Drive design through constraints provided by chip vendor or user defined through simulation.
- Able to take into account high-speed design constraints early in the design flow up to layout enhancing reliability and minimising prototype iteration development time and cost.
- Formalise highly constrained boards design avoiding misunderstanding between designers and layout experts.
- Clear responsibilities sharing between designers and layout experts.
- Help and secure layout expert in the implementation of critical boards.
- Facilitate documentation and maintenance for long life projects such as those we have at Cern.
Current PE 14.2 Limitations
&
Future Enhancements

◆ Limitations on CM2C (PE 14.2)
  ◆ Does not support Pin Pairs, XNets and Differential Lines
  ◆ Differential Lines will be supported on release 15.0 (autumn 2003)

◆ Limitations on CM2SQ (PE 14.2)
  ◆ Does not support Differential Lines
  ◆ Differential Lines will be supported on release 15.0 (autumn 2003)

◆ Differential Lines Support Enhancements in PE 15.0 Release
  ◆ Ability to define a comprehensive set of rules for differential signal in all High-Speed Workflow allowing constraint driven placement and routing.
  ◆ Capability in to treat differential signal pairs as a single entity while interactively routing them with a heads-up display that shows information on phase or delay control and options to use various via patterns
  ◆ Custom stimulus and custom measurement capabilities allow SPECCTRAQuest users to make complex measurements such as common mode offset measurements from die pads inside the IC package. A user can now quickly understand the influence of the package on the performance of differential signals.
I Can Help You
- To implement your high-speed workflow
- To find/check IBIS models
- In advanced usage of Cadence’s high-speed tools SPECCTRAQuest/SigXplorer Constraint Manager
- To analyze your signal integrity problem
- To report problems or to get more advanced support from Cadence European Response Center

You Have High-Speed Problems on a Existing Boards or Systems Developed With Cadence PSD Tools
- I can help you too for post-layout analysis in order to find solutions

http://cern.ch/support-specctraquest
- High-Speed design support at Cern
- Release 13.6 (without constraint manager)
- Will be updated for coming release 15.0

Jean-Michel Sainson CERN IT-PS/EAS
- BA 513 1-010
- Tel: 77561
- Email: J-M.Sainson@cern.ch
SPECCTRAQuest Community Web Sites

- **http://www.specctraquest.com**
  - The reference site for high-speed board designers using Cadence high-speed tools
  - A lot of very interesting and useful FAQ, tips, applications notes, white papers, presentations, forums, seminar movies (webinar), etc..
  - Fully maintained by Cadence

- **http://www.xilinx.com/ise/alliance/rocketio_kit.htm**
  - Xilinx RocketIO Design Kit for Cadence SPECCTRAQuest
  - RocketIO Design Kit for SPECCTRAQuest will help you to evaluate the behavior of the Multi-Gigabit transceivers on your PCB system before you design and fabricate it.
Appendix 1: Constraint Manager Enabled Flow

**Conditions to Run Constraint Manager Enabled flow**

- When you launch Concept if the `<design_name>.dcf` file exists in the constraints view of the root design, **YOU ARE USING THE CONSTRAINT MANGER ENABLED FLOW.**
- **You can not go back to the TRADITIONAL FLOW** (without constraint manager)

A **constraints** view is automatically created on the first use of Constraint Manager containing a file named `<design_name.dcf>` which contains a snapshot of electrical constraint information in the design.

Export Physical Packager-XL creates five pst*.dat files under the **packaged** view; two more (pstmdb.dat - pstmcbc.dat) than the traditional design flow without constraint manager.

Import Physical Packager-XL creates six *view.dat files under the **packaged** view; two more (cmdbview.dat – cmbcview.dat) than the traditional design flow (without constraint manager).
Appendix 2: IBIS Models Supply and Checking

1) Automatic IBIS syntax check
2) IBIS to DML translation
3) Automatic DML syntax check

- Invoking Model Integrity
  - Standalone
    - Unix prompt type → `modelintegrity`
  - From SPECCTRAQuest
    - Tools → Model Integrity...

- Invoking SigXplorer
  - Standalone
    - Unix prompt type → `sigxp`
  - From SPECCTRAQuest
    - Tools → Topology Editor...
  - From Constraint Manager
    - Tools → SigXplorer...

Recommended Electrical Checking:
- Basic simulation of I/O CELLS
- Driver/Receiver simulation on same technology (without transmission line)
- Static and dynamics characteristics check vs Data Sheets

DML File “NP4GS3.dml” Loaded in Custom Local Lib Directory: `root_design_name/physical/loc_lib/`
DML File “28H4088A.dml” Loaded in Custom Local Lib Directory: `root_design_name/physical/loc_lib/`
Appendix 3: First Switch Delay Measurements Points

- **Buffer Delay**
  - Buffer delay is the time it takes the voltage of a driver to reach a predefined measurement voltage (Vmeas)

- **First Switch Delay**
  - Is the time to reach the first threshold voltage encountered minus the Buffer Delay for the driver:
    - First Switch (rising) = time to reach Vil - buffer delay
    - First Switch (falling) = time to reach Vih - buffer delay
Appendix 3: Final Settle Delay Measurements Points

- **Buffer Delay**
  - Buffer delay is the time it takes the voltage of a driver to reach a predefined measurement voltage ($V_{meas}$)

- **Final Settle Delay**
  - Is the time to reach the second threshold voltage encountered and stay above or below it, minus the Buffer Delay for the driver:
    - Final Settle Delay (rising) = time to reach $V_{ih}$ - rising buffer delay
    - Final Settle Delay (falling) = time to reach $V_{il}$ - falling buffer delay