High-Speed PCB Layout Flow

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(Electronic Applications Support)
Training Description

- **Objective**
  - Cadence back-end PE14.2 high-speed printed circuit board layout flow presentation. Based on the new *Constraint Manager* application concurrently with *ALLEGRO/SPECTRA* layout implementation tools.

- **Recommended for**
  - *Cadence/ALLEGRO layout experts* receiving jobs that have been previously constrained by the designer under *Constraint Manager*.
Programme

- High-Speed Board Design Issues & Solution Available @ CERN
- Constraint Manager Principles
- Layout Designer’s Workflow
- Real Case Study
  - Description
  - Demo: Layout Data Base Review
  - Demo: Constraints Driven Placement & Routing
  - Demo: Impedance Driven Routing
- Conclusion

- Appendix 1: Constraint Manager Enabled Flow
High-Speed Board Design Issues
&
Solution Available @ CERN
High-Speed Board for LHCb Experiment

NP4GS3 Network Processor Daughter Board

- 14 layers ± 10% Controlled Impedance Board
- 1088-Pin (CCGA) Package
  - Fine Pitch 1.27 mm
  - 815 I/O
- 2 x 4 GIGABIT MEDIA INDEPENDENT INTERFACE UNITS (GMII)
  - 4 GIGABIT ETHERNET
  - Full Duplex 8 bit data Bus 125 MHz Clock
  - LVTTL
- Double Data Rate SDRAM INTERFACE
  - JEDS8-9A SSTL2 Standard
  - Stub Series Terminated Logic for 2.5V CLK 133 MHZ
- DATA-ALIGNED SYNCHRONOUS LINKS (DASL)
  - 2 x 8 EIA/JEDEC JESD8-6 standard channel for differential HSTL
  - (Up to 625 Mbps per channel)
High-Speed Board Design Issues

- **Typical High-Speed Board Design Issues**
  - Fast edge rates < 500ps
  - Very high pin density
  - Via number control
  - Single ended and differential Zo controlled impedance
  - Various termination types (thevenin, serie, etc.)
  - Min/max propagation delays
  - Cross-talk
  - Total etch length
  - Relative (Matched) length propagation delay
  - Package parasitic effects
  - Clock & Buses timing constraints with accurate set up & hold

- **Multiple constraints exist on each net**

- **Integrating Requirements is Essential for Success!**
Cadence’s PSD14.2 High-Speed PCB Design Flow

- Based on the New “Constraint Manager” Programme Linking
  - Signal Explorer Expert (SigXplorer) pre and post layout exploration tool
  - Concept-HDL schematic capture tool
  - SPECCTRAQuest SI Expert post-layout SI analysis tool
  - ALLEGRO-Expert and SPECCTRA layout implementation tools

High-Speed PCB Design Flow

Exploration  | Capture  | Layout DTB Setup  | Implementation
---|---|---|---
Concept-HDL  | SPECCTRAQuest  | Allegro
SigXplorer  | SigXplorer  | SigXplorer

Constraint Manager
Designer’s Tools

**Exploration under SigXplorer**
- Topologies Analysis Tools
- Topologies development, signal integrity analysis
- Electrical constraints development

**Schematic Capture under Concept-HDL**
- Electrical constraints capture with Constraint Manager Connected to Concept-HDL (CM2C) and/or SigXplorer

**Layout Database Setup under SPECCTRAQuest**
- Layout database setup with Constraint Manager Connected to SPECCTRAQuest (CM2SQ)
- Electrical constraints mapping
SigXplorerer in the High-Speed Design Flow

EX: Pre layout (Exploration) Phase TOPOLOGY development under SigXplorer
Implementation Phase

- Electrical constraints driven placement and routage with Constraint Manager Connected to Allegro-Expert layout editor (CM2AE)
- Interactive (Allegro) or automatic (SPECCTRA) placement and routage
What is Constraint Manager (CM)?

- Constraint Manager is a Spreadsheet based Application handling OBJECTS and Electrical Constraints Sets (ECSets)
Constraint Manager Objects (1/5)

- **Pin Pair**
  - A *pin-pair* represents a pair of logically connected pins, often a driver-receiver connection.
  - You may specify pin-pairs explicitly (for example, U1.8 – U2.8), or they can be derived based on the following criteria:
    - longest pin-pair
    - longest driver-receiver pair
    - all driver-receiver pair

- Pin-pair Objects Not Supported in Concept-HDL 14.2
Constraint Manager Objects (2/5)

- **Net**
  - Basic connectivity as defined in the schematic

- **XNet**
  - An eXtended Net XNet chains through passive discrete device(s) (resistor, inductor, capacitor)
  - XNet can also traverse connector and cables in a multiboard configuration

- XNet Objects Not Supported in Concept-HDL 14.2
Constraint Manager Objects (3/5)

- **Diff Pair**
  - An electrical differential pair *Diff-Pair* represents a coupled pair of Net or XNet which will be routed differentially

- **Bus**
  - A *Bus* represents a named collection of diff-pairs, Nets or XNets

- Diff Pair Objects Not Supported in Concept-HDL 14.2
Constraint Manager Objects (4/5)

- **Relative/Matched Group**
  - A *Relative/Matched Group* represents a user-specified collection of *pin-pairs* constrained by a relative or match delay or length.
  - The following attributes are used to characterize a *Relative/Matched Group*:
    - Target: The pin-pair that is referenced by all pin-pairs in the group.
    - Delta: The difference between each pin-pair member and the target pin-pair.
    - Tolerance: The tolerance allowed when matching members in the group.

- **Example (Top Layer View)**

  Matched Group (M1)
  M1 = Data <0..7> + DQS0

  To maintain a matched propagation delay, 8 Data Nets (4 in the top layer) are extended to match the length of (DQS0) strobe.
Constraint Manager Objects (5/5)

- **Design**
  - A *Design* represents a stand-alone board or a board in a system
  - In a multi-board configuration, each board becomes a separate design in the system

- **System**
  - A *System* represents a configuration of designs (boards) including XNets that traverse these design and their interconnecting cables and connectors
Goal is to assign constraints at the highest possible level
- Constraints that you specify at the top level of the hierarchy become inherited by the next lower-level object

Special exception cases can be handled by overrides at lower level
Electrical Constraint Sets (ECSets)

- **What is an ECSet?**
  - AN ECSet is a **collection** of **generic simulated** and/or **computed** **CONSTRAINS** requirements.
  - You define one or more ECSets to capture design requirements.
  - You then assign the appropriate ECSet to objects in your design.

- **ECSets Types**

![Electrical Constraint Set Diagram]

- Simulated (post layout)
- Computed (real time)
Computed ECSets Types

- **Routing ECSets**
  - Routing constraints analysis (handling *lengths*/*prop delay* and *impedances*) does not need simulation,
  - Are calculated and flagged in **real time** by *Constraint Manager* (CM)

- **Routing Constraint Violation Example**
  - Electrical DRC (ED) displayed under SPECCTRAQuest
  - Same "Prop Delay/Length" constraint violation displayed under CM2SQ

<table>
<thead>
<tr>
<th>Objects</th>
<th>Prop Delay</th>
<th>Prop Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min <em>mil</em></td>
<td>Actual</td>
</tr>
<tr>
<td>System</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mez_S5 routed reference</td>
<td>-455.19 MIL</td>
<td>-576.08 ...</td>
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<tr>
<td>D6_ADDR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_BVTEEN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_DATA</td>
<td>-455.19 MIL</td>
<td>1476.08 ...</td>
</tr>
<tr>
<td>D6_DQS</td>
<td>1476.08 ...</td>
<td>-576.08 ...</td>
</tr>
<tr>
<td>D6_DQS0</td>
<td>1476.08 ...</td>
<td>-576.08 ...</td>
</tr>
<tr>
<td>IC1_AL39:R6.1</td>
<td>0 MIL</td>
<td>1476.08 ...</td>
</tr>
<tr>
<td>R629C451</td>
<td></td>
<td>2400 MIL</td>
</tr>
</tbody>
</table>
Simulated ECSets Types

- **Signal Integrity & Timing Constraints**
  - Signal Integrity & Timing constraints analysis values are the result of analogue simulations.
  - Electrical Constraints simulations results are displayed in CM worksheets and/or SPECCTRAQuest simulation reports.
  - The Cadence TLSim simulator is a SPICE-like engine using DML Cadence proprietary format.
  - DML (Device Model) format is the Cadence implementation of IBIS behavioural signal integrity models for signal integrity analysis.
  - IBIS is a “component centric” standard ideal for board level simulation. It is widely supported by ICs manufacturers.

Simulations results displayed in CM Switch/Settle Delays worksheet
Invoking Constraint Manager

- **Standalone for Design Exploration**
  - Unix prompt type → `consmgr`

- **From Concept-HDL (CM2C)**
  - Tools → Constraints → Edit
  - Should only be run on a PACKAGED schematic
  - Constraint Manager invoked from Concept-HDL does not presently support Pin Pairs, XNets and Differential pair (only supported by layout data base)

- **From ALLEGRO-Expert (CM2AE) or SPECCTRAQuest (CM2S)**
  - Setup → Electrical Constraint Spreadsheet...
  - Icon
Constraint Manager User Interface (1/7)

- **Worksheet Selector**
  - The worksheet selector is the only way to select (open) the various worksheets within CM.

The "Electrical Constraint Set" worksheets are used for creating and/or editing the Rule Sets.

The "Net" worksheets are used for interfacing with the design objects such as applying the rules or seeing if they can be met.
Example: Min/Max Propagation Delay Worksheet Selection

- Object column
- ECSet reference
- Constraint values
Constraint Manager User Interface (3/7)

- Objects Column in a Nets Folder: Routing Worksheet

- Design

- Buses

- Net

- Pin Pair

- XNet

- Pin Pairs
**Constraint Manager User Interface (4/7)**

- **ECSet Mapping to Objects**
  - On individual Net, selected Nets, Bus, selected Buses, etc..
  - 3250 Mils Longest/Shortest Driver/Receiver Max length

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**Electrical Constraint Sets: Routing**

<table>
<thead>
<tr>
<th>Objects</th>
<th>Pin Pairs</th>
<th>Min Delay</th>
<th>Max Delay</th>
</tr>
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<tbody>
<tr>
<td>System</td>
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<td>ps</td>
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<tr>
<td>mez 55 placed reference bus</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTRL_ADD</td>
<td>Longest/Shortest Driver/Receiver</td>
<td>3250 MIL</td>
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</tr>
<tr>
<td>DA_DQS</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Nets: Routing**

<table>
<thead>
<tr>
<th>Objects</th>
<th>Referenced Electrical CSet</th>
<th>Prop Del Min</th>
<th>Prop Del Actual</th>
<th>Prop Del Margin</th>
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<tbody>
<tr>
<td>System</td>
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<tr>
<td>mez_55_placed_reference_bus</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_ADDR0</td>
<td>CNTRL_ADD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC1.AL28:IC4.29</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_ADDR1</td>
<td>CNTRL_ADD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC1.AN26:IC4.30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6_ADDR2</td>
<td>CNTRL_ADD</td>
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<td>IC1.AE24:IC4.31</td>
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<tr>
<td>D6_ADDR3</td>
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<tr>
<td>IC1.AG26:IC4.32</td>
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<td></td>
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<tr>
<td>D6_ADDR4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Constraint Manager User Interface (5/7)

- Viewing ECSets References

- DA_DQS ECSets applied to BUSES
- CNTRL_ADD ECSets applied to BUSES
- CNTRL_ADD ECSets applied to NETS
# Constraint Manager User Interface (6/7)

- **Colour Coding**
  - Cells are BLACK and BLUE colour coded to indicate inheritance for constraints.
  - Results status displayed in YELLOW, GREEN or RED.

### Colour Coding Examples:
- **Blue** indicating the ECSet has been originally applied in this cell.
- **Blue** indicating that this cell was overwritten (3500 Mils) on NET D6_ADDR0.
- **Black** indicating the ECSet are inherited on each NET.
- **Black** indicating that this value is inherited on Pin Pair from “CNTRL_ADD” ECSet (Prop Delay/Max Length) constraint value.

### Table Example:

<table>
<thead>
<tr>
<th>Objects</th>
<th>Referenced Electrical CSet</th>
<th>Pin Pair</th>
<th>Prop Delay</th>
<th>Prop Delay</th>
<th>Prop Delay</th>
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<tbody>
<tr>
<td></td>
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<td></td>
<td>Min</td>
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<td>System</td>
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</tr>
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<tr>
<td>D6_ADDR0</td>
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<tr>
<td>IC1.AG28:IC4:32</td>
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<td></td>
</tr>
</tbody>
</table>

- **Results status** displayed in YELLOW, GREEN or RED.
- **Location**: Constraint Manager (connected to SPECCTRAQuest SI Expert 14.2) – [Nets: Routing]

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**Cadence® High-Speed PCB Layout Flow - Constraint Manager Principles**
Constraint Manager User Interface (7/7)

- **STATUS BAR Information Type**
  - Progress meter for simulations
  - Brief description of commands
  - Reasons why items are greyed out

Placing cursor over an object in the display provides information on the STATUS BAR below.
Constraint Manager Enabled Flow
Vs
Traditional Flow

First Time you Invoke Constraints Manager from ALLEGRO (Expert or Designer)
- You are in CONSTRAINT MANAGER ENABLED FLOW
- You can not go back automatically to the traditional flow

If you Have Launch Constraint Manager by Mistake
- You can go back to the TRADITIONAL DESIGN FLOW deleting files and director automatically created, SEE APPENDIX1: Constraint Manager Enabled Flow
Layout Designer’s Workflow
High Speed PCB Layout Workflow

1. DTB review: layout impedance cross section under SPECCTRAQuest (more accurate)
2. DTB review: DC Nets assignment with ALLEGRO-Expert or SPECCTRAQuest
3. DTB review: discrete (R, L, C,) model assignment with ALLEGRO-Expert or SPECCTRAQuest
4. DTB review: active (ICs) models assignment with ALLEGRO-Expert or SPECCTRAQuest
5. DTB review: ECSets mapping to physical NETs with Constraint Manager connected to ALLEGRO-Expert
6. Constraints driven placement and routing with ALLEGRO-Expert and optionally SPECCTRA

It is recommended to review steps 1 to 5 with designer.
Constraints Driven Place & Route

- Interactive (Allegro) or automatic (SPECCTRA) placement and routage
- Once the constraints are present in the ALLEGRO database, they are used to drive the placement and routing process for those signals
- The constraint manager is completely integrated with the Allegro design rules checking system, this means that the different high-speed rules can be checked in real-time as the design process proceeds, with the results presented as part of the CM spreadsheets.
- Any design parameters that do not meet their associated constraints values are highlighted. At any point during physical design users can launch the Constraint Manager to view high-speed constraint information associated with the design.
Real Case Study

(Description)
Demo Scope

To layout WITH MANUFACTURER GUIDELINES a subset of NP4GS3 DDR SDRAM interface

- 8Mx16 DDR (D3)
- 8Mx16 DDR (D2)
- 8Mx16 DDR (D1)
- 2x 8Mx16 DDR (D0)
- 2x 8Mx16 DDR (D6)
- 2x 8Mx16 DDR (D4)
- 2x 512kx18 SRAM (LU)
- 512kx18 SRAM (SCH)

64 MB DDR SDRAM
- 6 Samsung (32X4) K4H280438C-TCA2
- I/O technologies Stub series Terminated Logic 2.5V (SSTL2) & CMOS
- 66 pins TSOP II Package

D6 INTERFACE ARCHITECTURE
- 18 bits DATA BUS
- 13 bits ADDRESS BUS
- Differential Clock
- Clock Cycle 133 MHZ
- Double-data rate architecture; two transfers per clock cycle
- I/O technologies Stub series Terminated Logic 2.5V (SSTL2) & CMOS
CNTRL & ADDR Manufacturer Guidelines

- **CNTRL_ADDR Lines Constraints**
  - Control and address lines are six-drop lines terminated into a 50 Ω equivalent circuit.
  - Board Stackup controlled impedance = 55 Ω ± 10 %
  - The distance from NP4GS3 to the furthest SDRAM must not exceed 3.25 inches.
  - The stub to the SDRAM pin should not be more than 0.25 inches.

50 Ω Thevenin Equivalent Terminations

Zo = 55 Ω ± 10%

L ≤ 3.25 inches

Stub ≤ 0.25 inches
DATA & DQS Manufacturer Guidelines

**DA_DQS Lines Constraints**
- All DATA and DQS nets must be terminated with a 22-29 Ω series resistor placed no more than one inch from the NP4GS3.
- No more than 25% of the trace should be on the NP4GS3 side of the terminating resistor.
- Each set of DATA and DQS lines must be no shorter than one inch and no longer than 3.25 inches.
- For each set of four DATA lines and its respective DQS line, there can be no more than ±70 ps of flight time difference from the NP4GS3 to the RAM. Use IBIS simulation to be sure that there no more than ±70 ps difference between DQS and its corresponding DATA lines.
Concept-HDL Schematic

Cadence® High-Speed PCB Layout Flow - Real Case Study (Description) -
Real Case Study

(Demo: Layout Data Base Review)
To be Done Exclusively with SPECCTRAQuest-Expert

Layout Cross Section

- Specified by Designer and DESIGNED IN COLLABORATION OF LAYOUT EXPERT AND/OR BOARD MANUFACTURER
- SQ Setup Form: Setup → Cross Section
- Provides data for SPECCTRAQuest Field Solver to compute accurate transmission line modelling of traces
- Determines trace characteristics such as impedance and propagation velocity
- All application dependent power and ground planes must be created
- Conductors layers count is not mandatory. Later in the design flow layout expert can decide to add internal layer(s) having same structure (stripline) and impedance (Zo)

Microstrip or Stripline Impedances are computed in real time by the Field Solver each time we change a parameter (line width etc..), helping designer to find optimum combination of material, thickness and PCB CLASS.
DC Nets Assignment Review

- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert

- Identifying DC Nets
  - SQ Identify DC Nets Form: Logic → Identify DC Nets.
  - Makes sure simulations in SPECCTRAQuest or SigXp have the correct voltage for circuits
  - Prevents XNets from including wrong nets
Discrete (R, L, C) Model Assignment Review

- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert

- Discrete (R, L, C) DML Signal Model Assignment Review
  - Signal Model Assignment Form:
    Analyse → SI/EMI Sim → Model..
  - DML discrete models assignment are the minimum models assignment (also called Espice models) that must be done for all analysis cases (Physical or Electrical)
  - Without this assignment the system will not be able to develop XNet from the layout database
  - If component libraries include CLASS, VALUE and PINUSE, Auto Setup button automatize this process for 2 pin discrete
  - Discrete with more than 2 pins could be easily created via Create Model button

Ex: DML (or ESPice) models assigned to resistors terminations

This button will automatically make Espice models for all 2 pins discretes
Active (ICs) Models Assignment Review
(Case 1: Default Models)

To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert

Optional IBIS (DML) Models Assignment

- Signal Model Assignment Form:
  Analyse → SI/EMI Sim → Model..

- It is not necessary to assign IBIS models for computed (routing workbook) analysis. Default models are automatically assigned by the system.

Any models have been assigned by designer. In fact, default models are automatically assigned by the system.
Active (ICs) Models Assignment Review

(Case 2: Designer’s Models)

- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert

- **IBIS (DML) Models Assignment**
  - Signal Model Assignment Form:
    Analyse → SI/EMI Sim → Model..
  - Optional assignment that must be done on ICs
  - Simulated analysis supported by Signal Integrity or Timing workbooks needs IBIS models assignment

Ex: IBIS (DML) models: 6 x K4H280838C_TC DDR SDRAM memory model

Ex: IBIS (DML) models: 1x NP4GS3B Network Processor Model

Start IBIS (DML) process assignment for active devices (ICs)
ECSets Mapping to Physical Nets Review

- Impedance ECSet Mapping
- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert
ECSets Mapping to Physical Nets Review

- Min/Max Length ECSet Mapping
- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert
ECSets Mapping to Physical Nets Review

- Wiring ECSet Mapping
- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert
ECSets Mapping to Physical Review

- Relative Propagation Delay ECSet Mapping
- To be Done with ALLEGRO-Expert or SPECCTRAQuest-Expert
Real Case Study

(Demo: Constraints Driven Placement & Routing)
Constraints Driven Placement

- (ALLEGRO-Expert + CM2AE) or (SPECCTRAQuest-Expert + CM2SQ)
  - Max propagation delay constraint violation on IC5 placement

CM2AE
Min/Max Propagation Delays worksheet

<table>
<thead>
<tr>
<th>Objects</th>
<th>Min Actual Margin</th>
<th>Max Actual Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min n3</td>
<td>Actual</td>
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<tr>
<td>System</td>
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<td>mez_55_constrained_reference</td>
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<td></td>
</tr>
<tr>
<td>D6_ADDR</td>
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<td></td>
</tr>
<tr>
<td>D6_ADDR0</td>
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<td>3073.94 MIL</td>
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<td>176.06 MIL</td>
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</tr>
<tr>
<td></td>
<td>3250 MIL</td>
<td>3050.71 MIL</td>
</tr>
</tbody>
</table>

Constraints violation interactive check. Two forms:
- Electrical DRC marker
- CM2AE Violation parameters and color
(ALLEGRO-Expert + CM2AE) or (SPECCTRAQuest-Expert + CM2SQ)
- Max length constraint violation on R6 (DSQ0) serial termination placement

R6 (DSQ0) serial termination resistor place too far (1150mils) from NP4GS3 driver.
ADDR<0..3> Constraints Driven Auto-Routing (SPECTRA)

- (ALLEGRO-Expert + CM2AE) or (SPECTRAQuest-Expert + CM2S)
  - Daisy-chain bus topology schedule constrained with 250 mils max stub length automatically routed by ALLEGRO
ADDR 1 Post-Layout Topology Extraction

- SigXplorer (ADDR1) Post-Layout Topology Extraction from CM2AE

ADDR1 Daisy Chain Topology

Stub Length ≤ 250 mils
DATA <0..3> & DQS 0 Constraints Driven Auto-Routing (SPECCTRA)

- (ALLEGRO-Expert + CM2AE) or (SPECCTRAQuest-Expert + CM2S)
  - DATA <0..3> & DQS 0 multiple constraints automatically taken into account by ALLEGRO

Wiring worksheet:
Match Group (DA_DQS_M1)

<table>
<thead>
<tr>
<th>System</th>
<th>Relative Delay</th>
<th>Actual</th>
<th>Margin</th>
<th>Length</th>
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Worst case margin # 8 ps
**DATA <0..3> & DQS 0**

**Impedance Driven Routing (SPECTRA)**

- **Unmatched Mezzanine (MEZ2) Cross Section**
  - Homogeneous dielectric thickness of 4.72 mils
  - Computed impedance (# 66 and 42 Ω) respectively for strip lines and micro-strip lines are outside tolerances (55 Ω ± 10%)

### Layout Cross Section

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<tr>
<th>Etch Subclass</th>
<th>Type</th>
<th>Material</th>
<th>Thickness</th>
<th>Electrical Conductivity</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
<th>Negative</th>
<th>Shield</th>
<th>Line Width</th>
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<td>52.04 Ω</td>
</tr>
</tbody>
</table>

Total Thickness: 56.139 MIL

**Cadence® High-Speed PCB Layout Flow - Real Case Study (Demo: Constraints Driven Placement & Routing)**

5 mils lines width hypothesis (CLASS 6)
DATA <0..3> & DQS 0
Impedance Driven Auto-Routing (SPECCTRA)

- (ALLEGRO-Expert + CM2AE) or (SPECCTRAQuest-Expert + CM2S)
  - DATA <0..3> & DQS 0 multiple constraints including now impedance marching are automatically taken into account by ALLEGRO.

![Table](chart.png)

- Impedance controlled line width
- $55.00 \, \Omega \ll Zo \ll 55.01 \, \Omega$
Conclusion
Conclusion on Cadence PSD 14.2
High-Speed PCB Design Flow
Using Constraint Manager

**Proposed High-Speed Workflows Advantages**

- Cadence’s PSD14.2 “High-Speed PCB Design Flow” based on **Constraint Manager** provides a consistent way to create, manage and validate **Designer’s intent**.
- Drive design through **constraints provided by chip vendor or user defined** through simulation.
- Able to take into account high-speed design constraints early in the design flow up to layout **enhancing reliability and minimising prototype iteration development time and cost**.
- **Formalise highly constrained boards design** avoiding misunderstanding between designers and layout experts.
- Clear **responsibilities sharing** between **designers** and **layout experts**.
- **Help and secure layout expert** in the implementation of critical boards.
- **Facilitate documentation and maintenance for long life projects** such as those we have at Cern.
Current PE 14.2 Limitations & Future Enhancements

- **Limitations on CM2C (PE 14.2)**
  - Does not support Pin Pairs, XNets and Differential Lines
  - Differential Lines will be supported on release 15.0 (autumn 2003)

- **Limitations on CM2AE or CM2SQ (PE 14.2)**
  - Does not support Differential Lines
  - Differential Lines will be supported on release 15.0 (autumn 2003)

- **Differential Lines Support Enhancements in PE 15.0 Release**
  - Ability to define a comprehensive set of rules for differential signal in all High-Speed Workflow allowing constraint driven placement and routing.
  - Capability in to treat differential signal pairs as a single entity while interactively routing them with a heads-up display that shows information on phase or delay control and options to use various via patterns
  - Custom stimulus and custom measurement capabilities allow SPECCTRAQuest users to make complex measurements such as common mode offset measurements from die pads inside the IC package. A user can now quickly understand the influence of the package on the performance of differential signals.
IT-PS/EAS
Electronic Applications Support for High-Speed Design

◆ I Can Help You
  - To implement a high-speed workflow in collaboration with designer
  - To review constrained board in collaboration with designer before placement and routing
  - To check/simulate board in collaboration with designer after placement and routing
  - In advanced usage of Cadence’s high-speed tools SPECCTRAQuest/SigXplorer Constraint Manager

◆ You Have High-Speed Problems on a Existing Boards or Systems Developed With Cadence PSD Tools
  - I can help you too for post-layout analysis in order to find solutions

◆ http://cern.ch/support-specctraquest
  - High-Speed design support at Cern
  - Release 13.6 (without constraint manager)
  - Will be updated for coming release 15.0

◆ Jean-Michel Sainson  CERN  IT-PS/EAS
  - BA 513 1-010
  - Tel: 77561
  - Email: J-M.Sainson@cern.ch
Cadence-Xilinx
High-Speed Communities Web Sites

- **http://www.specctraquest.com**
  - The reference site for high-speed board designers using Cadence high-speed tools
  - A lot of *very interesting and useful* FAQ, tips, applications notes, white papers, presentations, forums, seminar movies (webinar), etc..
  - Fully maintained by Cadence

- **http://www.specctra.com**
  - The SPECCTRA Community is a place where *high-speed designers* meet to share, contribute, and exchange information on how to *best use* SPECCTRA
  - Fully maintained by Cadence

- **http://www.xilinx.com/ise/alliance/rocketio_kit.htm**
  - Xilinx RocketIO Design Kit for Cadence SPECCTRAQuest
  - **RocketIO Design Kit for SPECCTRAQuest** will help you to evaluate the behavior of the *Multi-Gigabit transceivers* on your PCB system before you design and fabricate it.
Appendix 1: Constraint Manager Enabled Flow

**Conditions to Run Constraint Manager Enabled flow**

- When you launch Concept if the `<design_name>.dcf` file exists in the constraints view of the root design, YOU ARE USING THE CONSTRAINT MANAGER ENABLED FLOW.
- You can not go back to the TRADITIONAL FLOW (without constraint manager)

A constraints view is automatically created on the first use of Constraint Manager containing a file named `<design_name.dcf>` which contains a snapshot of electrical constraint information in the design.

Export Physical Packager-XL creates five pst*.dat files under the **packaged** view; two more (pstmdb.dat - pstmcb.dat) than the traditional design flow without constraint manager.

Import Physical Packager-XL creates six *view.dat files under the **packaged** view; two more (cmdbview.dat – cmcbcview.dat) than the traditional design flow (without constraint manager).