Introduction to PCI Express

A Hardware and Software Developer's Guide

Adam H. Wilen
Justin P. Schade
Ron Thornburg

INTEL PRESS
## Contents

**Acknowledgements**  xi

**Chapter 1  Introduction**  1
- A Quick Overview  2
- Why Develop a New I/O Technology?  4
- Who Should Read This Book  6
  - System Integrators  6
  - Hardware Developers  6
  - Software Developers  6
  - Product Marketing Engineers  7
  - Application Engineers  7
- The Organization of This Book  7
  - Beyond PCI  7
  - The Technology  8
  - Adopting PCI Express  9

**Chapter 2  The PCI Legacy, Successes, and Challenges**  11
- The Introduction of PCI  11
- PCI Successes  13
  - Industry Acceptance  14
  - Defined Specifications  15
  - Processor Architecture Independence  16
  - Full Bus Mastering  18
  - Plug and Play Operation  18
  - High Performance Low Cost Implementation  19
Introduction to PCI Express

PCI Challenges
  Bandwidth Limitations 19
  Host Pin Limitations 21
  Inability to Support Real-Time (Isochronous) Data Transfers 23
  Inability to Address Future I/O Requirements 24

PCI Moving Forward 25

Chapter 3 Goals and Requirements 27
  Scalability, Stability, and Performance 27
  Stability Requirement: Stability for the Next Decade 28
  Scalability Requirement: Growth Options for the Future 29
  Performance Requirement: Pin and Link Efficiency 31

Market Segment Support 39
  Market Segment Requirement: Mobile 39
  Market Segment Requirement: Desktop 40
  Market Segment Requirement: Servers 41
  Market Segment Requirement: Communications 41

System-Level Cost Parity 42
  Cost Requirement: Ability to Use Common Printed Circuit Board Fabrication Technology 42
  Cost Requirement: Common Connector Manufacturing Technology 43
  Cost Requirement: Routing in Four-Layer Motherboards 43
  Cost Requirement: Usability on Multiple Silicon Process Technology 44

I/O Simplification 45
  Simplification Requirement: I/O Consolidation 46

Backward Compatibility 49
  Compatibility Requirement: Legacy Operating System Support 49
  Compatibility Requirement: Existing System Form Factor Support 50
  Compatibility Requirement: Allowing Coexistence During Transition 50
Chapter 4  PCI Express Applications  51
Benefits of PCI Express  51
  High Performance  52
  I/O Simplification  53
  Layered Architecture  54
  Next Generation Multimedia  55
  Ease of Use  56
Evolutionary Applications  58
  PCI Express for Computing Graphics Applications  59
  PCI Express for Gigabit Ethernet  62
  PCI Express as a High-Speed Chip-to-chip Interconnect  65
Revolutionary Applications  72
  Multimedia and Isochronous Applications  72
  PCI Express Module Applications  73
  Communications Applications and Advanced Switching  76

Chapter 5  PCI Express Architecture Overview  79
System Level Overview  79
  Links and Lanes  80
  Device Types  83
PCI Express Transactions  85
  Transaction Types  85
Build Layers  86
  Packet Formation  87
  The Big Picture  89
  Transaction Layer  90
  Data Link Layer  92
  Physical Layer  94

Chapter 6  Transaction Layer Architecture  97
Transaction Layer Overview  97
Transaction Layer Packets  98
TLP Headers  100
  Memory Request Headers  103
  I/O Request Headers  107
  Configuration Request Headers  108
  Message Headers  109
  Completion Packet/Header  115
Introduction to PCI Express

TLP Data Payload 117
TLP Digest 119
TLP Handling 120
  Request Handling 121
  Completion Handling 122

Chapter 7 Data Link Layer Architecture 123
Data Link Layer Overview 123
Building on the TLP 125
  Sequence Number 125
  CRC 128
Retries 128
Data Link Layer Packets (DLLPs) 131
  Ack and Nak DLLPs 132
  Flow Control DLLPs 135
  Power Management DLLPs 136
Processing a DLLP 136
Data Link Layer Control 138

Chapter 8 Physical Layer Architecture 141
Physical Layer Organization 141
  Logical Sub-Block 143
  Electrical Sub-Block 151
Link and Lane Training 156
Surprise Insertion/Removal 172
  Surprise Insertion 172
  Surprise Removal 173
Power Management Capabilities 173
  L0s Active Power Management State 173
  L1 Active Power Management State 174

Chapter 9 Flow Control 175
Transaction Ordering 175
Flow Control 178
  Flow Control Rules 179
  Flow Control Credits 182
Virtual Channels and Traffic Classes 186
  Traffic Class to Virtual Channel Mapping 188
  Virtual Channel Initialization 190
Isochronous Support 197
## Chapter 10  **PCI Express Software Overview**  201

- Software Initialization and Configuration  201
- Refresher on PCI Configuration  202
- Configuration Mechanisms  204
- Error Reporting  206
  - Error Classification  207
  - Error Signaling  209
  - Advanced Error Capabilities Configuration  210
- Error Logging  212

- Software Particulars for Key PCI Express Features  214
  - PCI Express Power Management  214
  - PCI Express Hot Plug  215
  - PCI Express Differentiated Traffic Support  218
  - Virtual Channel Capabilities Configuration  219
  - Available Arbitration Mechanisms  220
  - The Virtual Channel Arbitration Table and the Port Arbitration Table  222

## Chapter 11  **Power Management**  227

- Building on PCI Power Management  227
  - PCI Power Management Software Base Operations  229
- PCI Bus States versus PCI Express Link States  232
  - PCI Express Link State L0 and PCI Bus State B0  235
  - PCI Express Link State L0s  235
  - PCI Express Link States L1, L2, and PCI Bus State B2  236
  - PCI Express Link State L3 and PCI Bus State B3  237
  - PCI Express Link State L2/L3 Ready  237
  - PCI Express Link Recovery State  237
  - PCI Express Link Training States  238
- PCI Express Active State Power Management ASPM  240
  - Software Requirements for PCI Express Active State Power Management  241
  - L0s Active State Power Management  244
  - L1 Active State Power Management  245
  - Power Management Messages and Packets  245
Chapter 12 PCI Express Implementation 249

System Partitioning 249
  Desktop Partitioning 251
  Mobile Partitioning 254
  Server Partitioning 256
Impact on System Architecture 258
  Form Factors 259
  Connectors 261
  Routing Implications 265

Chapter 13 PCI Express Timetable 273

Anticipated Schedule 273
  Application Roll Out 273
  Factors Affecting Adoption and Schedule 274
Profile of an Early Adopter 278
  Challenges of Early Adoption 280
  Benefits of Early Adoption 281
  Tools for Early Adopters 282
Profile of a Later Adopter 284
  Challenges of Late Adoption 284
  Benefits and Tools for Later Adopters 286

Chapter 14 PCI Express Product Definition and Planning 287

PC Graphics Components as an Example 287
  Market Assessment 288
  Design Tradeoffs and Key Decisions 288
Motherboard Vendors as an Example 298
  Market Assessment versus Cost 298
  Design Tradeoffs and Key Decisions 301
Conclusion 302
Appendix  PCI Express Compliance & Interoperability  305

Compliance and Interoperability Terminology  306
Compliance Development Process  307
  Compliance Testing  308
  Platform Components  308
  Add-in Card Components  309
  Interoperability Testing  310
  Plugfests  311
Useful References  311

Glossary  313

Index  319