LARGE ECL SYSTEMS ON WIRE-WRAP BOARDS
INTRODUCTION

A support tool for hardware prototype development using the wire-wrap technique has been developed in the DD Division 1).

The main features resulting from the use of this tool are:

1. Computerised preparation of wiring lists, including error cross checks.
2. Semi-automatic wiring from computer generated numeric control tape.
3. Standardised computer generated documentation.
4. Rapid corrections of design errors (hours for wire-wrap, instead of weeks for printed circuits).
5. The same wire-wrap tape can be used as a starting point for the multiwire technique. This can be an attractive and economical solution for small series (4-10) production.

The wire-wrap technique is well suited to relatively slow Logic families such as TTL. However the faster ECL Logic families transmit signals over transmission lines which should be terminated with the characteristic line impedance to prevent reflections, thereby minimising the signal settling times (Fig. 2, 3, 4). In order to test whether the wire-wrap technique can successfully provide the required transmission line environment, a 4K memory using MECL 10.000 series ECL Logic has been constructed and tested.

THE WIRE-WRAP BOARD

For this test a special version of one of the existing wire-wrap boards has been developed (see fig. 1-4).

In order to provide the wire-wrapped lines with a well defined characteristic impedance, the component side is filled in, as much as possible, with a ground plane. On the wiring side, one of the two power supply connections of each line of circuits can be chosen for connection to +5V (TTL) or -5,2V (ECL).

Single in-line resistor packages can be placed between the integrated circuits to provide transmission line termination to -2V.

THE MEMORY CIRCUIT

To test the behaviour of the wire-wrap board a large ECL circuit has been built consisting of a 4096 word x 18 bit fast memory with two switchable interfaces. The memory itself is built from 1024 word x 1 bit memory integrated circuits (MC 10146).

Care has been taken to layout the circuitry on the board in such a way that it is natural to the data stream, mainly to keep the different layers of wiring crossing over each other limited to a minimum.
TESTING

Extensive testing using the fast ECL interface, coupled to a sequential number generator as address and data source, and a logic state analyser, has shown good functioning of the memory up to the fastest speed of the latter instrument (70 nsec) some signals of this test are shown in the fig. 5-7.

After completion of this test the memory was interfaced to the UNIBUS of a PDP-11 minicomputer, using the other interface.

All standard DEC memory test programs compatible with the functioning of the memory could be run and no errors were detected.

CIRCUIT SPECIFICATION

4096 word x 18 bit memory
read cycle 25 nsec Fig. 5-7
write cycle 30 nsec Fig. 6-7
first interface fast ECL Interface
second interface TTL Level Unibus
connection with selectable base address.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>Total of ECL integrated circuits</td>
<td>105</td>
</tr>
<tr>
<td>Total of TTL integrated circuits</td>
<td>18</td>
</tr>
<tr>
<td>Total of wire-wrap connections</td>
<td>1750</td>
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Power consumption

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>1A</td>
<td>5 Watt</td>
</tr>
<tr>
<td>-5.2V</td>
<td>9A</td>
<td>46.2 Watt</td>
</tr>
<tr>
<td>-2V</td>
<td>2A</td>
<td>4 Watt</td>
</tr>
<tr>
<td></td>
<td></td>
<td>55.8 Watt</td>
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</table>

CONCLUSION

If boards with a full surface ground-plane are used, wire-wrap techniques can be successfully used for large circuits of more than 100 ECL 10.000 integrated circuits. However some care should be taken to obtain a good layout.

ACKNOWLEDGEMENT

The Author wishes to thank Mr. K. Zumbrock for making the printed circuit board, and Dr. D. Wiskott for adapting the existing software package to generate the wiring list for this board.

REFERENCES


Ref. 5 Peripherals and interfacing handbook. Digital Equipment Corp.
Fig. 1. Component side of the full card

Fig. 2. Wiring side of the full card

Fig. 3. Detail of the component side

Fig. 4. Detail of the wiring side
Fig. 5
Read cycle at a cycle time of 40 nsec.

ADDRESS BIT 00

DATA OUT
BIT 00

Fig. 6
Write cycle at a cycle time of 40 nsec.
Note that data out is inhibited during the Write enable

Write Enable
Address 00
Data out 00

Fig. 7
Write and change address read.

Write Enable
DATA IN
ADDRESS
DATA OUT