The ATLAS Insertable B-Layer Detector (IBL)

F. Hügging on behalf of the ATLAS IBL collaboration

Pixel 2010
5th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging, Sept. 6 – 10, 2010 Grindelwald, Switzerland
The ATLAS Pixel Detector

- 3 Barrel + 6 Forward/Backward disks
- 112 staves and 48 sectors
- 1744 modules
- 80 million channels
The ATLAS Pixel module

- 16/frontend chips (FE-I3) modules with a module controller chip (MCC)

- 47232 pixels (46080 R/O channels), 50 x 400 µm² (50 x 600 µm² for edge pixel columns between neighbour FE-I3 chips)

- Planar n-on-n DOFZ silicon sensors, 250 µm thick

- Designed for $1 \times 10^{15}$ 1MeV fluence and 50 MRad (500kGy)

- Opto link R/O: 40÷80 Mb/link
Phase 1 Upgrade: IBL

- Insertable B-layer in 2016:
  - Fourth pixel layer at $r = 3.2$ cm in addition to existing detector.
  - Insertion together will a new beam-pipe.
  - Peak luminosity $2 \times 10^{34}$ cm$^{-2}$ s$^{-1}$, 75 pile-up events and $3 \times 10^{15}$ n$_{eq}$ cm$^{-2}$
- this constraints the design of the IBL:
  - Mechanical layout is challenging, service routing is complex.
  - Electronics/readout has to fit to current pixel detector (ROD, BOC etc.)
The 4th Pixel layer: Insertable B-Layer

- Add a 4th low-mass pixel layer inside the present B-Layer: The Insertable B-Layer:
  - Improve performance of existing system.
  - Maintain performance when present B-Layer degrades.
  - Existing Pixel Detector stays installed and a 4th is inserted inside the existing pixel system together with new beam pipe → requires new, smaller radius beam pipe to make space.
  - It needs to be inserted in a long shutdown (at least 9 months required). Build detector ready for installation in 2016.

- It serves also as technology step from now to sLHC:
  - IBL project will be first to use of new technologies currently under development for sLHC.
  - Radiation hardness $5 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ or 250 MRad (2.5 MGy).
  - Front-end (FE-I4): go to IBM 130nm process and improve readout architecture.
  - Sensors: investigate new planar Si sensors, 3D-Si sensors and CVD diamond sensors.
  - Readout system & optolink: 160MB/s for data transmission.
  - CO$_2$ cooling system & mechanics: develop light-weight support.
• The envelopes of the existing Pixel Detector and of the beam pipe leave today a radial free space of 8.5mm.
• The reduction of 4mm in the beam pipe radius brings it to 12.5mm.
• Entire IBL has to fit in this space!
IBL Layout (2)

- Baseline geometry defined:
  - 14 staves
    - \( R_{in} = 31\text{mm} \)
    - \( R_{out} = 34\text{mm} \)
    - \( \langle R_{sens} \rangle = 33\text{mm} \)
    - \( Z = 664\text{mm} \)
  - 32 FE-I4’s per stave with sensors facing the IP.
  - Stave tilt angle in \( \Phi = 14 \)
  - No tilting in z-direction.
  - Total sensor surface only \( \sim 0.2\text{m}^2 \).
Main target is to keep performance of the pixel system:
- for more pile up events at higher luminosities.
- for failures of modules esp. in the ‘old’ b-layer.
- b-tagging efficiency without ‘old’ b-layer.

Older studies (ATLSIM/GEANT3) show improved performance with the addition of IBL.
→ see low mass Higgs b-jet tagging plot on the right.
IBL Performance

- Physics performance studies ongoing for the IBL TDR using ATHENA/GEANT4.
- Performance improvement due to low mass and smaller radius of IBL:

<table>
<thead>
<tr>
<th>Component</th>
<th>% $X_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>beam-pipe</td>
<td>0.6</td>
</tr>
<tr>
<td>New BL @ R=3.2 cm</td>
<td>1.5</td>
</tr>
<tr>
<td>Old BL @ R=5 cm</td>
<td>2.7</td>
</tr>
<tr>
<td>L1 @ R=8 cm</td>
<td>2.7</td>
</tr>
<tr>
<td>L2 + Serv. @ R=12 cm</td>
<td>3.5</td>
</tr>
<tr>
<td>Total</td>
<td>11.0</td>
</tr>
</tbody>
</table>
IBL Module Design

- Sensor technology independent.
- Each FE chip has 336x80 pixel of 50x250µm².
- Decision on sensors after prototyping with FE-I4.
- Common sensor baseline for engineering and system purposes.
  - 3D / Diamond sensors → single chip modules
  - Planar sensors → 2 chip modules
- Sensor/module prototypes for ~10% of the detector in 2010/2011
  - Stave prototype tested with modules and cooling
Bump Bonding

• Requirements for bump bonding of IBL modules are:
  – a fine bump pitch of 50µm
  – a high bump density of 80 bumps per mm² (26,880 bumps per IC)
  – high yield with defect rate < 10⁻⁴.
  – IC thickness below 200µm to save material.

• Large volume bump bonding experience from ATLAS Pixel Detector.

• Program to qualify for FE-I4 and different sensor technologies.
  – Goal is go below 200µm IC thickness: target is 90µm.
  – Crucial point is the behavior of the thinned IC during the high temperature reflow process.
  – See L. Gonella‘s talk “Towards minimum material trackers for HEP experiments at upgraded luminosity” on Thursday for more details.

Prototype test of advanced AgSn bumping with 90µm FE-I4 size dummies.

<table>
<thead>
<tr>
<th></th>
<th>Indium (Modules)</th>
<th>PbSn (Modules)</th>
<th>Total (Modules)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembled</td>
<td>1468</td>
<td>1157</td>
<td>2625</td>
</tr>
<tr>
<td>Rejected</td>
<td>172</td>
<td>35</td>
<td>207</td>
</tr>
<tr>
<td>Accepted (total)</td>
<td>1296</td>
<td>1122</td>
<td>2418</td>
</tr>
<tr>
<td>Accepted as delivered</td>
<td>1101</td>
<td>1035</td>
<td>2136</td>
</tr>
<tr>
<td>Accepted after reworking</td>
<td>195</td>
<td>87</td>
<td>282</td>
</tr>
</tbody>
</table>

JINST 3 P0707 (2008)
Module design: Electrical interface

- Basic idea: flex cable glued to stave backside carries all signal and voltage traces for a half stave, i.e. 8 2-chip modules.
- Connection to module via a wing which is bent to stave front side for each module.
- Wire bond connects to module onto a small module flex.
- At the end of stave all signals and voltages connects to type1 cables via low mass connectors
- 2 prototypes are under development for the stave cables:
  - Multilayer flex solution
  - thin single sided Al-flexes

Stave flex prototype: thin Al flex
Sensors for IBL (1)

- Requirements for IBL sensors:
  - Integrated luminosity seen by IBL is 550fb\(^{-1}\) → survive until sLHC phase 2
  - NIEL dose: 3.3\times10^{15} + „safety factor“ = 5\times10^{15}\ n_{eq}/cm^{2}.
  - Ionizing dose = 2.5MGy (250Mrad)
  - Low dead area in Z: slim or active edge
  - Max. Sensor power density < 200mW/cm\(^2\) normalized to -15°C sensor temperature
  - Max. Bias voltage (system issue) = 1000V

- Fit made for 2 < r < 20cm for L = 550fb\(^{-1}\).
- For IBL @ 3.2cm: \Phi = 3.3\times10^{15}n_{eq}/cm^{2} (1.6MGy)
• 3 sensor concepts are being considered for IBL:
  – Planar n-in-n silicon sensors:
    • Similar design as for ATLAS Pixel.
    • Radiation tolerance proven to several $10^{15}n_{eq}/cm^2$.
    • Main focus in development of slim edges.
  – Planar n-in-p silicon sensors, thinned to 150µm:
    • Utilize the advantages of thinned sensors at a given maximum bias voltage
    • Standard 450µm wide inactive edge
    • Special passivation layer (BCB) needed for HV operation

→ More details given on Wednesday morning by D. Münstermann, A. Macchiolo and Y. Unno.
3D silicon n-in-p sensors:
- Radiation tolerance is achieved by short charge collection distances decoupled from sensor thickness (230µm).
- 2 design option with different edge sizes:
  - Full 3D active edge design $\rightarrow$ 50µm edge.
  - Double column design $\rightarrow$ 200µm slim edge
- More details given on Wednesday by A. Micelli.

Diamond pixel sensors:
- Sufficient radiation tolerant for IBL fluencies and basically no leakage tolerant.
- Slim edges possible.
- 2 manufacturer (DDL, II-VI) with acceptable performance (CCD > 230µm) under investigation.
- Full processing (pixel metallization and UBM) are industrialized at IZM, Berlin.
- **Reason for new FE chip:**
  - Increased radiation tolerance required: 2.5MGy
    - Go to smaller feature size technology 130nm and utilize their improved radiation hardness.
  - New architecture to reduce inefficiencies at higher luminosities.
    - Local storage of hit in pixel matrix until trigger arrives.
    - Higher output bandwidth.
  - Improve cost effectiveness:
    - Larger chip improves the ratio between active area and periphery and is advantageous for bump bonding while the yield can still be high.

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### FE-I3 inefficiency @ r = 5cm

- **Double-hit Inefficiency**
- **Busy/Waiting Inefficiency**
- **Late Copying**
- **Total Inefficiency**

- **10xLHC**
- **3xLHC**
- **LHC**
The first version of full FE-I4 chip has been submitted by end of June 2010 and is expected back on 14th of Sept.

- Biggest chip in HEP to date (70 millions transistors, 6 Cu and 2 Al routing layers)
- Lower power: don’t move hits around unless triggered
- No need for extra module control chip: significant digital logic block on array periphery.

FE-I4 collaboration:
- CPPM: D. Fougeron, M. Menouni.
- Genova: R. Beccherle, G. Darbo.
- Nikhef: V. Gromov, R. Kluit, J.D. Schipper.

More details on FE-I4 on Tuesday by M. Barbero’s talk “FE-I4 Chip Development for Upgraded ATLAS Pixel Detector at LHC”.

<table>
<thead>
<tr>
<th></th>
<th>FE-I3</th>
<th>FE-I4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size [µm²]</td>
<td>50x400</td>
<td>50x250</td>
</tr>
<tr>
<td>Pixel array</td>
<td>18x160</td>
<td>80x336</td>
</tr>
<tr>
<td>Chip size [mm²]</td>
<td>7.6x10.8</td>
<td>20.2x19.0</td>
</tr>
<tr>
<td>Active fraction</td>
<td>74%</td>
<td>89%</td>
</tr>
<tr>
<td>Analog current [µA/pix]</td>
<td>26</td>
<td>10</td>
</tr>
<tr>
<td>Digital current [µA/pix]</td>
<td>17</td>
<td>10</td>
</tr>
<tr>
<td>Analog Voltage [V]</td>
<td>1.6</td>
<td>1.4</td>
</tr>
<tr>
<td>Digital Voltage [V]</td>
<td>2.0</td>
<td>1.2</td>
</tr>
<tr>
<td>Pseudo-LVDS out [Mb/s]</td>
<td>40</td>
<td>160</td>
</tr>
</tbody>
</table>

FE-I3 74%  FE-I4 ~89%

Pixel 2010  Fabian Hügging, University of Bonn
Thermal runaway happens in sensors if not adequately cooled:

> Leakage current shows exponential behavior.

Stave thermal figure of merit ($\Gamma = [\Delta T \cdot \text{cm}^2/W]$) main parameter for thermal performance.

Power design requirements for IBL:
- Sensor Power: 200 mW/cm² @ -15 °C
- FE power: 400 mW/cm²

Stave prototype qualification program:
- Titanium / carbon fiber pipes (D = 2÷3 mm)
- Cooling CO₂ and C₃F₈
- Carbon foam density: 0.25÷0.5 g/cm³

Radiation length: 0.36÷0.66 %X/X₀
- Pipe + stave structure + coolant
IBL stave structure

Stave structure made of carbon foam + cooling pipe:
- The stiffness is provided by a carbon fiber laminate:
- Carbon foam diffuses the heat from the module to the cooling pipe

Additional technical requirements:
- Max pressure of cooling pipe: 100 bar.
- Develop pipe joints and fittings.
- Gravitational / thermal deformation < 150 μm.
- Isolation of the carbon foam from sensor high voltage.
- Mock-up for thermal measurements.

<table>
<thead>
<tr>
<th>STAVE TYPE</th>
<th>Omega Thickness [μm]</th>
<th>Foam Density [g/cm³]</th>
<th>Pipe Material</th>
<th>Pipe Diameters [mm]</th>
<th>Radiation Length X/X₀ [%]</th>
<th>Thermal Figure of Merit Γ [°C·cm²/W]</th>
<th>Thermal Def. [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti pipe Stave</td>
<td>300</td>
<td>0.25</td>
<td>Ti grade II</td>
<td>ID=2 OD=2.2</td>
<td>0.57</td>
<td>1.166</td>
<td>11</td>
</tr>
<tr>
<td>CF Pipe Stave</td>
<td>150</td>
<td>0.25</td>
<td>CF</td>
<td>ID=2.4 OD=3</td>
<td>0.36</td>
<td>0.956</td>
<td>25</td>
</tr>
</tbody>
</table>
Conclusions

• IBL is the upgrade for the ATLAS Pixel Detector in LHC phase 1 upgrade:
  – A 4\textsuperscript{th} layer will be inserted into the Pixel system.
  – IBL will improve physics performance of ATLAS and it is a “safety insurance” for present B-Layer.
  – TDR and MoU in progress – project cost evaluated.

• IBL is a challenging project:
  – Tight envelopes, material budget reduction, radiation dose and R/O bandwidth requirements.
  – New technologies are in advanced prototype phase:
    • Sensors, FE-I4, light supports, cooling, etc.
  – Can also benefit to sLHC tracker upgrades.
Backup
Installation scenario

- Two global support / installation scenarios: IBL support tube (1) / no tube (2):
  - An IBL support tube would have advantage on stiffness and simplicity/safety for IBL installation, but drawbacks are envelope needs (~1÷1.5 mm) and increase of radiation length.

- Procedure studied on mock-up at bld.180 - procedure (1) animation:
  - The beam pipe flange on A-side is too close to the B-layer envelope - need to be cut on the aluminum section.
  - A structural pipe is inserted inside the Beam Pipe and supported at both sides.
  - The support collar at PP0 A-side is disassembled and extracted with wires at PP1.
  - Beam pipe is extracted from the C-side and it pulls the wire at PP1.
  - New cable supports are inserted inside PST at PP0.
  - A support carbon tube is pushed inside the PST along the structural pipe.

Started to setup a 1:1 mock-up of Pixel/beampipe/PP1 in Bat 180