ASSOCIATIVE MEMORY DESIGN
FOR THE FAST TRACKER PROCESSOR (FTK)
AT ATLAS

A. STABILE for the AMchip collaboration

NSS, Valencia, Spain
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Complex system, many units:

- **48 Data Formatters (DF)**
  - Clustering Mezzanine

- **128 Processing Units**
  - **AUX Board (FPGA):**
    - Data Organizer (DO)
    - Track Fitter (TF - 8 layers)
    - Hit Warrior (HW)
  - AM Board with 10M patterns on AMchip04 custom CAMs

- **32 Final Boards (FPGA)**
  - Final Fit (11 layers)
  - Final Hit Warrior

FTK will reconstruct all tracks above 1 GeV using as inputs Inner Detector data.
The Associative Memory

- Dedicated device - maximum parallelism
- Each pattern with private comparator
- Track search during detector readout

Associative memory is similar to the bingo game!

<table>
<thead>
<tr>
<th>Approach</th>
<th>Tech.</th>
<th>Num. of Pat.</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full custom</td>
<td>700 nm</td>
<td>0.128 kpat/chip</td>
<td>6</td>
</tr>
<tr>
<td>FPGA</td>
<td>350 nm</td>
<td>0.128 kpat/chip</td>
<td>6</td>
</tr>
<tr>
<td>STD cells</td>
<td>180 nm</td>
<td>5.0 kpat/chip</td>
<td>6</td>
</tr>
<tr>
<td>STD cells + Full custom (new for FTK)</td>
<td>65 nm</td>
<td>80 kpat/chip</td>
<td>8</td>
</tr>
</tbody>
</table>
1 Flip-flop (FF) for each layer stores layer matches
All patterns are compared in parallel with incoming data (HIT)
Fast pattern matching and flexible input
the AM readout is based on a modified Fischer Tree \(^1\)

\(^1\) P. Fischer NIM A461 (2001) 499-504
AM Chip Memory Layer

To save power we have used two different match line driving scheme\(^2\)

- Current race scheme
- Selective precharge scheme

Each layer stores a word position: 12 bits + 3 “don’t care” bits (value 0,1,x)

CAM layer timing diagram

Simulation done in nominal conditions:
Transistors models → TT
VDD → 1.2V
Temperature → 27 °C

4 NAND cells: 2.6 x 1.8 μm each
14 NOR cells: 2.6 x 1.8 μm each
Latch SR + ML discharge: 4.7 x 1.8 μm
The full custom cell

2 layers = 1/4 pattern

128 layers + 1 dummy layer in the middle

64 pattern vertically
The AMchip has an area of 14 mm².

CAM is organized as 22 column x 12 row of full custom macro blocks.

Each block is 64 x 2 layers.

Between two row of blocks there is the majority logic and the fisher tree made using STD cells approach.

In the center there is the control logic and JTAG made using STD cells approach.
“Variable resolution” in the AMchip

Ternary cells: “Don’t care bits”

We can use don’t care on the least significant bit when we want to match the pattern layer at large resolution or to use all others bits to match with a thinner resolution. Coincidence window is programmable layer by layer and pattern by pattern.

\[\text{An new Variable Resolution Associative Memory for High Energy Physics ATL-UPGRADE-PROC-2011-004}\]
AM chip status

Completed:
- Full Custom memory block layout and simulation with back-annotate schematics
- Floor plan of entire chip including IO cells and pad ring placement
- Place and Route by means of the Foundation Flow by Cadence Encounter
- Creation of a memory block verilog model for full chip simulation

in progress:
- Improvement of the verilog model to add some new features
- Logic simulations to obtain exhaustive results
- Complete AMS simulation of some critical cases

Future:
- By increasing the area we want to enlarge the bank from 8k patterns for chip to 80k patterns for chip
- How to implement power saving architecture and full custom design to gain in memory density

AM chip summary (about 1M of comparisons in parallel)

\[
\text{Number of comparisons} = \text{Number of pattern} \cdot \text{Number of layers} \cdot \text{Number of bit}
\]

\[1179648 = 8192 \cdot 8 \cdot 18\]