Variable resolution pattern generation for the Associative Memory of the ATLAS FTK project

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The Fast Tracker processor

The FTK processor is an upgrade of the ATLAS Trigger. It will reconstruct tracks with pT>340 GeV/c and |η|<2.5 using the full pool of hits and hit clusters at the full load-1 output rate of 100 kHz with a typical latency of ~160 ps. Fallback tracks will be provided as input to High Level Trigger (HLT) algorithms that will identify physics object signatures and take the trigger decision. The FTK exploits a high-bandwidth connection with the detector & HW optimized for the specific tasks. The LHC will provide high luminosity in the coming years, with the possibility to reach up to lhc-run2019 and up to 2020-2023 with HighLuminosity-LHC [1]. Tracking information will therefore be highly valuable in a high pileup environment because it can separate particles from the hard scattering vertex from those originated by pileup pp collisions.

The FTK reconstructs tracks using up to 12 layers. The combinatorial problem of tracking in solved in two steps. The first one is pattern recognition in 8 layers using the Associative Memory (AM) [2]. The AM searches for track candidates using enough silicon hits (tracks) using a reduced spatial resolution. It pushes the parallelism to the maximum level since all detector hits are compared in parallel with a set of pre-stored track patterns. The track search occurs during detector readout without the need for additional time. The FTK AM system will store 12077 patterns. The second step is a linearized track fitting using full resolution detector hits. The track fitting determines the final track quality.

Pattern recognition with the AM

Over a narrow region in the detector, equations linear in the local silicon hit coordinates give resolution nearly as good as a time-consuming helical fit. This is equivalent to approximating the 3D manifold of valid tracks in the space of hit coordinates with a tangent plane. We find that the linear approximation works well within a sector: a single silicon module in each detector layer.

The use of variable resolution AM

The "variable resolution" AM exploits ternary logic. In the AM each detector "bin" can be identified by 0, 1, or X, where X means "don’t care" (DC) in the hit-to-stored-value comparison. The X value can be used to logically OR neighboring high-resolution bins. We can vary the shape of each pattern, layer by layer.

The impact of variable resolution is evaluated by simulating FTK tracks for simulated events with 75 overlapping pp collisions. These results show the use of up to 1 “don’t care” bit per layer applied in the φ-direction.

Variable resolution achieves a factor 3 pattern bank reduction with respect to thin fixed resolution, or a factor of 7 reduction in fakes with respect to the large resolution.

The variable resolution brings pattern shape optimization to a new level. Fourteen years later pioneer studies in shape optimization achieve big reductions in fake rate for a fixed number of patterns. Using up to 2 DC bits for pixel layers in the FTK, it was possible to define a valid working configuration for the FTK upgrade [7]. The table shows the results for tracking in simulated events with 60 overlapping pp collisions, which correspond to a LHC instantaneous luminosity of 310^34 Hz/s. This configuration combines with the hardware limits for each of 64 φ triggers: AM patterns < 16.8*10^5, read/evnt < 16*10^5, f/s/evnt < 80*10^5, where the last two parameters represent the workload for the track filter.

Results