Vertex-Detector R&D for CLIC

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ABSTRACT: A detector concept based on hybrid planar pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. In this paper the CLIC vertex-detector requirements are reviewed and the current status of R&D on sensors, readout and detector integration is presented.

KEYWORDS: Silicon pixel vertex detector, Linear Collider, CLIC.

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1. Introduction

The proposed Compact Linear Collider (CLIC) concept of a linear electron-positron collider with a centre-of-mass energy of up to 3 TeV has a large physics potential, complementing and extending the measurements of the current LHC experiments [1, 2, 3]. It will allow for precision measurements of standard model physics (e.g. Higgs, top) and of new physics potentially discovered at the LHC (e.g. SUSY). Moreover, direct and indirect searches for new physics over a large range of mass scales will be performed. The demands for precision physics in combination with the challenging experimental conditions at CLIC have inspired a broad detector R&D program. In particular the vertex-detector systems have to fulfil unprecedented requirements in terms of material budget and spatial resolution in a location close to the interaction point, where the rates of beam-induced background particles are very high. The ongoing CLIC vertex-detector studies focus on ultra-thin hybrid pixel detectors and aim for integrated solutions taking into account constraints from mechanics, power delivery and cooling.
2. The CLIC machine environment

The CLIC project studies the feasibility of a linear electron-positron collider optimized for a centre-of-mass energy of 3 TeV with an instantaneous luminosity of a few times $10^{34}\text{cm}^{-2}\text{s}^{-1}$, using a novel technique called two-beam acceleration [1]. A drive beam of rather low energy but high current is decelerated, and its energy is transferred to the low-current main beam, which gets accelerated with gradients of 100 MV/m. The two-beam acceleration scheme thus removes the need for RF power sources along the accelerating main LINAC. It is expected that the machine will be built in several stages with centre-of-mass energies ranging from a few hundred GeV up to the maximum of 3 TeV, corresponding to an overall length of the accelerator complex up to 48 km. In order to reach its design luminosity of $6 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ at a maximum centre-of-mass energy of 3 TeV, CLIC will operate with very small bunch sizes ($\sigma_x \times \sigma_y \times \sigma_z \approx 40\text{nm} \times 1\text{nm} \times 44\text{µm}$). Accelerating structures of 12 GHz drive the two main beams and collisions occur in bunch crossings (BX) every 0.5 ns for a train duration of 156 ns. The train repetition rate is 50 Hz. The short train duration implies that triggerless readout of the detectors, once per train, will be implemented. The power consumption of the detectors, and therefore the material required for cooling infrastructure, can be reduced by switching off parts of the frontend electronics during the 20 ms gaps between trains.

3. Beam-induced backgrounds

The very small beam sizes lead to strong electromagnetic radiation (Beamstrahlung) from the electron and positron bunches in the field of the opposite beam. The creation of the Beamstrahlung photons reduces the available centre-of-mass energy of the $e^+e^-$ collisions and their interaction leads to lepton pairs and hadrons, most of which are produced at very low polar angles and are therefore contained in the beam-pipe by the axial magnetic field [4]. The dominant backgrounds in the inner detectors are incoherently produced electron-positron pairs (approximately 60 particles / BX) and $\gamma\gamma \rightarrow$hadrons events (approximately 54 particles / BX). The electron-positron pairs are predominantly produced at very small transverse momenta and low polar angles. The detector occupancies in the innermost layers can therefore be reduced to an acceptable level by a careful design optimisation of the inner- and forward-detector regions. The central beam-pipe walls have to be placed outside the high-rate region and the inner detectors have to be efficiently shielded from back-scattered particles originating from the forward region. The particles produced in $\gamma\gamma \rightarrow$hadrons interactions, on the other hand, show a harder transverse momentum spectrum and a more central polar-angle distribution, resulting in large rates of background particles with every bunch crossing, reaching the outer detector layers. While at most one interesting physics event is expected in each train, $\approx 1000$ hadronic background events are produced. Pile-up rejection algorithms based on hit time stamping are needed to separate the physics from the background events.

The radiation exposure of the main detector elements is expected to be small, compared to the corresponding regions in high-energy hadron-colliders. For the non-ionizing energy loss (NIEL), a maximum total fluence of less than $10^{11}n_{eq}/\text{cm}^2/\text{year}$ is expected for the inner barrel and for-
ward vertex layers. The simulation results for the total ionizing dose (TID) predict approximately 200 Gy/year for the vertex-detector region.

4. Vertex-detector requirements

The primary purpose of the CLIC vertex detector is to allow for efficient tagging of heavy quarks through a precise determination of displaced vertices. Monte Carlo simulations show that these goals can be met with a high-momentum term in the transverse impact-parameter resolution of $a \approx 5\mu m$ and a multiple-scattering term of $b \approx 15\mu m$, using the canonical parametrization

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot GeV^2 / (p^2 \sin^3 \theta)},$$

where $p$ is the momentum of the particle and $\theta$ is the polar angle with respect to the beam axis. These requirements on the measurement precision exceed the results achieved in any of the currently existing full-coverage vertex systems. They can be met with multi-layer barrel and endcap pixel detectors operating in a magnetic field of 4-5 T and using sensors with a single-point resolution of $\approx 3\mu m$ and a material budget at the level of $< 0.2\%$ of a radiation length ($X_0$) for the beam-pipe and for each of the detection layers. The single-point resolution target can be met with pixels of $\approx 25\mu m \times 25\mu m$ and analog readout. The material-budget target corresponds to a thickness equivalent to less than 200 $\mu m$ of silicon, shared by the active material, the readout, the support and the cooling infrastructure. This implies that no active cooling elements can be placed inside the vertex detector. Instead, cooling through forced air flow is foreseen, limiting the maximum power dissipation of the readout to $\approx 50$ mW/cm$^2$. Such low power consumption can be achieved by means of power pulsing, i.e. turning off most components on the readout chips during the 20 ms gaps between bunch trains.

Time slicing of hits with an accuracy of $\approx 10$ ns will be required to separate beam-induced backgrounds from physics events.

5. Detector concepts

The two detector concepts CLIC_ILD and CLIC_SiD are currently under study. They are adaptations of the two validated detector concepts ILD [5] and SiD [6], developed for the International Linear Collider (ILC) [5] with a centre-of-mass energy of 500 GeV. The main CLIC-specific adaptations to the ILC detector concepts are an increased hadron-calorimeter depth (7.5 $\Lambda_i$) to improve the containment of jets at the CLIC centre-of-mass energy of up to 3 TeV, and a re-design of the vertex and forward regions to mitigate the effect of high rates of beam-induced backgrounds.

Both detectors have a barrel and endcap geometry with the barrel calorimeters and tracking systems located inside a superconducting solenoid providing an axial magnetic field of 4 T in case of CLIC_ILD and 5 T in case of CLIC_SiD. In the CLIC_ILD concept, the tracking system is based on a large Time Projection Chamber (TPC) with an outer radius of 1.8 m complemented by an envelope of silicon strip detectors and by a silicon pixel vertex detector. The all-silicon tracking and vertexing system in CLIC_SiD is more compact with an outer radius of 1.3 m.
5.1 Vertex-detector layouts

Both CLIC detector concepts include silicon vertex detectors with $25\mu m \times 25\mu m$ pixel size. They are integral parts of the full coverage tracking systems, designed to improve the accuracy of the track reconstruction, in particular for low transverse momenta. In case of CLIC_ILD, both the barrel and forward vertex detectors consist of three double layers, reducing the material thickness needed for supports. Figure 1 shows a sketch of the inner tracking region of CLIC_ILD. For CLIC_SiD, a geometry with five single barrel layers and 7 single forward layers was chosen. For both concepts the acceptance extends down to polar angles of approximately $7^\circ$.

![Figure 1](image)

**Figure 1.** View into the inner and forward tracking region of the CLIC_ILD simulation model. Shown are the vertex barrel (VXB) and endcap (VXEC) pixel layers, the two inner silicon barrel strip layers (SIT 1/2), the forward tracking disks (FTD), the beam pipe, and the support shells for the silicon layers.

For CLIC_ILD, the central beryllium beam-pipe and innermost detection layers are placed at a radius of 29 mm and 31 mm, respectively. The larger magnetic field in CLIC_SiD leads to a larger suppression of low-pT charged particles from beam-induced background and therefore allows for a reduced radius of the beam-pipe and innermost detection layers of 25 mm and 27 mm, respectively. Stainless steel conical sections with a wall thickness of 4 mm extend in the forward and backward directions and provide shielding against backscattering backgrounds.

5.2 Vertex-detector performance optimisation

The vertex-detector performance with the baseline geometries has been evaluated in Geant4-based [7] full-detector simulation studies. The achieved impact-parameter resolutions are as precise as $3\mu m$ for high-momentum tracks ($p \approx 100$ GeV) and the momentum resolution of the overall tracking systems reaches the required value of $\sigma_{p_T}/p_T^2 \approx 2 \times 10^{-5}$GeV$^{-1}$.

Fast parametric simulation studies have been performed, to evaluate the effect of changes in the assumed pixel size, material budget, arrangement of sensitive layers, and inactive material [8, 9]. In addition, Geant4-based full-detector simulations have been performed for selected geometries, probing the influence of key design choices and detector parameters on the expected flavor-tagging performance [10]. The multi-variate flavor-tagging package LCFIPlus [11] is used for this study, with dedicated training and testing samples for each geometry. Figure 2 shows the b-tagging and c-tagging performance for 200 GeV dijet events for two double-layer detector layouts with a spiraling endcap geometry. The default layout with $\approx 0.2\%X_0$ per double layer (double_spirals) is compared to a layout with an increased material budget of $\approx 0.4\%X_0$ per double layer (double_spirals_v2).
The fake rates increase by between approximately 5% and 35% for the double_spirals_v2 layout, compared to the default layout.

Figure 2. Flavor-tagging performance for two double-layer detector layouts with a spiraling endcap geometry and with different amounts of material (double_spirals and double_spirals_v2). Shown is the background misidentification probability (light flavors and c/b backgrounds) as a function of the signal efficiency for b-tagging (left) and c-tagging (right) of 200 GeV dijet events. The bottom panels show the ratio of the misidentification probabilities (double_spirals_v2 / double_spirals).

The effect of changes of the flavor-tagging performance on the physics performance of the detectors was estimated for the production of SM Higgs bosons at 3 TeV centre-of-mass energy in the process \(e^+e^- \rightarrow H\nu\bar{\nu}\), with subsequent decay of the Higgs bosons in pairs of b and c quarks [12]. The change in precision of the \(\sigma \times \text{BR}\) measurement is estimated for a 20% change in the fake rates of the dominating light-flavor background, which results in a 6-7% change in the precision of the \(H \rightarrow bb\) decay channel and in a 15% change in the precision of the \(H \rightarrow cc\) decay channel.

6. Hybrid readout technology

The R&D on pixel sensors and readout is focused on hybrid solutions, combining high-resistivity sensors with high-performance readout ASICs. The target thickness for both the sensor and readout layers is only 50 \(\mu\)m each. Slim-edge sensor designs are under study and Through-Silicon Via (TSV) technology is foreseen for vertical interconnection. The hardware R&D on sensors and readout is complemented by silicon signal simulations, to evaluate the impact of the technological parameters on the detector performance under various operating conditions.

6.1 Thin-sensor assemblies

Planar pixel sensors with 55\(\mu\)m pitch and different thicknesses (50-300 \(\mu\)m) were procured from Micron Semiconductors [13] and from Advacam [14]. Assemblies with Timepix readout ASICs
(100 and 450 µm thickness) were produced by IZM [15] and by Advacam and characterised in laboratory measurements and beam tests. Slim-edge sensor designs (250–450 µm, two guard rings) are compared to designs with active edges (20–50 µm, one guard ring above the edge pixels). Preliminary results show very good efficiencies in both cases, extending beyond the edge pixels. Single-point resolutions of approximately 3 µm have been extracted for clusters of two pixels using charge interpolation and taking into account non-linear charge sharing.

Alternative sensor concepts possibly suitable for the CLIC vertex detectors include Low-Gain Avalanche Detectors (LGAD) with charge multiplication [16] and active sensors with capacitive charge coupling, implemented in a high-voltage CMOS process (HV-CMOS CCPD) [17].

6.2 CLICpix readout chip

The CLICpix hybrid readout chip [18] will be implemented in a 65 nm CMOS process. The pixel size is 25 µm × 25 µm. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. A photon counting mode allows for threshold equalization. A compression logic is implemented with three selectable readout modes: (1) no compression; (2) pixel-to-pixel compression; (3) pixel-, cluster- and column-based compression. The full chip can be read out in less than 800 µs (for 10% occupancy), using a 320 MHz readout clock. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm². The total average power consumption can be reduced to a value below the target of 50 mW/cm² by means of power gating for the analog part and clock gating for the digital part.

A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a fully functional 64 × 64 pixel matrix and power-pulsing capability. Readout tests have confirmed that the chip is fully functional and the power consumption and performance are in agreement with simulations [19]. Figure 3 shows the result of a ToT scan for various values of the feedback current. Higher feedback currents correspond to a faster return to the baseline, thus increasing the dynamic range of the energy measurement.

Figure 3. ToT counts of one pixel, averaged over 256 samples, as a function of the injected charge and for different values for the feedback current. The bottom plot shows the deviation from a linear fit.
Table 1. Comparison of simulated and measured parameters of the CLICpix demonstrator chip.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ToA Accuracy</td>
<td>&lt; 10 ns</td>
<td>&lt; 10 ns</td>
</tr>
<tr>
<td>Gain</td>
<td>44 mV/ke⁻</td>
<td>40 mV/ke⁻</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>up to 40 ke⁻</td>
<td>up to 45 ke⁻</td>
</tr>
<tr>
<td>Equivalent Noise (bare chip)</td>
<td>σ = 60e⁻</td>
<td>σ = 51e⁻ (average)</td>
</tr>
<tr>
<td>DC Spread (uncalibrated)</td>
<td>σ = 160e⁻</td>
<td>σ = 128e⁻</td>
</tr>
<tr>
<td>DC Spread (calibrated)</td>
<td>σ = 24e⁻</td>
<td>σ = 22e⁻</td>
</tr>
<tr>
<td>Minimum threshold</td>
<td>388 e⁻</td>
<td>417 e⁻</td>
</tr>
<tr>
<td>Power consumption per pixel</td>
<td>6.5 µW</td>
<td>7 µW</td>
</tr>
</tbody>
</table>

Table 1 summarizes the results of the characterization measurements and compares them to the expectations from simulations. Good agreement between measurements and simulations is observed.

6.3 Through-Silicon Via (TSV) technology

Through-Silicon Via (TSV) vertical interconnects remove the need for wire bonding connections on the side of the readout ASICs and therefore allow for an efficient tiling to form larger modules with minimal inactive areas.

A “via last” TSV process developed in collaboration with CEA-LETI has demonstrated the feasibility of TSVs on functional detector chips from the Medipix/Timepix chip family [20]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology, which include landing pads for the I/O circuitry, as well as dedicated TSV test structures at the periphery of the wafers. The backside finishing is designed to be compatible with ball grid array (BGA) packaging. The balls are to be placed in a 10 × 10 matrix, with a pad diameter of 750 µm and a pitch of 1300 µm.

The “via last” process proceeds in the following steps: (1) deposition of the Under-Bond-Metallization (UBM) on the front-side of the chips; (2) temporary bonding of the front side to a support wafer and thinning to 120 µm from the back side; (3) etching and isolation of vias with 60 µm diameter; (4) deposition of a 5 µm thick copper layer and patterning of the via trenches; (5) passivation and UBM on the backside; (6) de-bonding of the front-side support wafer and attachment of the back side to dicing tape.

Tests on the processed wafers show good results, with a low resistivity of the vias (<1 Ω) and a sufficient isolation to the outside (leakage current <1 µA at 1 V). Preliminary functional tests on a sub-sample of the chips before and after TSV processing indicate no significant deterioration of the performance.

6.4 Simulation of signals in silicon

Monte-Carlo simulations and validations in test beams are performed to study the signal development in the silicon sensors and extract parameters such as the charge rise time, collection efficiency, charge sharing between pixels and signal/noise ratio. The dependence on the type, momentum and incident angle of the particles and on the electric and magnetic field are studied using TCAD [21] and Monte-Carlo charge-transport [22, 23] simulations.
The combination of the electric and magnetic field in the sensors leads to a spread of the charge cloud due to the Lorentz-angle effect, thus affecting the charge sharing between neighboring pixels in the barrel layers. This effect will be of particular importance in the very thin sensors foreseen for the CLIC vertex detector. For a p-in-n sensor with a resistivity of 10 kΩcm and a thickness of 50 µm, the depletion voltage is only $V_{dep} \approx 1$ V, leading to an average field in the sensors of only 200 V/cm. The resulting calculated Lorentz angle between the direction of the electric field lines and the direction of the drifting charge carriers is $33^\circ$ ($7^\circ$) for electrons (holes), assuming a magnetic field of 4 T and a temperature of 27 °C [24]. For an increased operation voltage of 40 V, the Lorentz angle is reduced to $19^\circ$ ($6^\circ$) for electrons (holes). Such values have a sizeable effect on the detector resolution and therefore need to be taken into account in the choice of the readout polarity (electrons or holes), the layer placement, and the sensor operation voltage.

7. Detector integration

The detector performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components. The powering, cooling, mechanical supports and the service lines are therefore addressed in an integrated approach at an early stage of the detector design.

7.1 Powering

The ambitious power-consumption target of less than 50 mW/cm$^2$ in the vertex detectors can only be achieved by means of pulsed powering, taking advantage of the low duty cycle of the CLIC machine. The main power consumers in the readout circuits will be kept in standby mode during most of the gap of 20 ms between consecutive bunch trains. Furthermore, efficient power distribution will be needed to limit the amount of material used for cables. Both the power pulsing and the power-delivery concepts have to be designed and thoroughly tested for operation in a magnetic field of 4-5 T.

A powering scheme based on constant current sources, Low Drop-Out regulators (LDOs) and local energy storage with silicon capacitors has been proposed for the power delivery and power pulsing of the CLIC vertex detectors [25]. The scheme takes advantage of the low duty cycle of the CLIC machine, to limit the current and thereby the cabling material needed to bring power to the detectors.

The ladders of the barrel vertex detector are assumed to consist of 24 readout chips covering a surface area of approximately 24 cm$^2$. Powering and readout will be connected on either side. Figure 4 shows the analog and digital power consumption states during a CLIC bunch-train cycle for the 12 CLICpix chips in a half ladder. The indicated values for the expected power dissipation in each state are obtained from simulations and measurements on prototypes of the main building blocks of the chips. The nominal operation voltage for both the analog and digital components in the chips is 1.2 V. The minimum time needed with stable conditions in the analog components is approximately 20 µs, in which both digital and analog power are at their peak values of 48 W and 2.4 W, respectively. The rise and fall times can be tuned by design of the readout chips within certain limits and are both assumed to be of the order of 1 µs. During the remaining time of the 20 ms cycle the analog power can be switched off. For the digital components, on the other hand,
an average continuous power of 0.54 W per ladder is still required, in order to sequentially send
the data off detector and keep the chips in a standby mode.

**Figure 4.** Analog and digital power consumption states during a CLIC bunch-train cycle for the 12 CLICpix chips in a half ladder.

Figure 5 shows a sketch of the proposed powering scheme for a half ladder in the barrel vertex
detector. A programmable current source located in the back end provides a constant current to
charge up the on-detector storage capacitors. The small duty cycle allows for a low continuous cur-
rent of only approximately 20 mA for a half ladder. Flex cables consisting of aluminum conductors
on a Kapton substrate bring the power to storage capacitors mounted on the individual CLICpix chips of the half ladder. LDOs are used to provide a constant voltage of 1.2 V (1 V) to the analog (digital) components of the chips. The LDOs for the analog part are only operated during 250 µs
around the 20 µs acquisition time, while the LDOs for the digital part are always on. The voltage
at the LDO input is continuously sensed at the back end and used as feedback for an FPGA con-
trolling the programmable current source. This way the load current is adapted after each cycle, to
provide enough charge to the storage capacitors for the next high-power period.

**Figure 5.** Powering scheme for one half ladder in the barrel vertex detector, consisting of 12 CLICpix readout chips.

A mockup has been built and operated to test the proposed powering scheme under realistic
load conditions. In this model the CLICpix chips are represented by programmable loads emulating
the expected current consumption of the chips. Figure 6 shows the achieved power regulation for
both the analog and digital components of a half ladder. The voltage regulation for the analog
components is stable at the level of approximately 16 mV, while the less critical regulation of the
digital voltage is approximately 70 mV. With this scheme, the current into the half ladder is limited
to less than 300 mA and a total power dissipation of approximately 45 mW/cm² is achieved. The
measurements are in agreement with equivalent-circuit simulations.

![Graph showing load current, load voltage, and back-end current](image)

**Figure 6.** Measurement results for the analog (left) and digital (right) components in a half ladder. Shown are the load current, \( I_{\text{load}} \), the load voltage, \( V_{\text{load}} \), the voltage at the LDO input capacitors, \( V_{\text{cap}} \), and the back-end current, \( I_{\text{BE}} \).

The average contribution of the flex cable, the LDOs and the silicon capacitors to the material
in the ladder area corresponds to 0.1\% \( X_0 \) per single detection layer. The use of thinner conductors
and future improvements of the silicon-capacitor technology are expected to decrease the material
budget even further.

### 7.2 Cooling

A total power of approximately 500 W will be dissipated in the vertex detectors alone. The small
material budget for the inner tracking-detectors constrains severely the permitted amount of cooling
infrastructure. For all pixel layers, forced air-flow cooling is therefore foreseen.

Feasibility studies have been performed for an inner-detector cooling system with sufficient
heat removal capability [26]. A spiral arrangement of the endcap pixel disks allows for air flow
through the disks on one side, into the barrel region and out through the endcap-disks on the other
side (Fig. 7 (left)). Figure 7 (right) shows the resulting temperature profile in the pixel detector
barrel layers, obtained from an ANSYS finite element simulation. With an air temperature of 0 °C
and an average flow velocity of 11 m/s at the end-cap inlet, the temperature in the innermost barrel
layer reaches up to 40 °C and stays below 30 °C in the other layers. The temperature span between
inlet and outlet is up to 20 °C. Heat transfer through conduction has not been taken into account in
the simulation.

Further R&D is ongoing to demonstrate the feasibility of this air-flow cooling scheme using
a thermo-mechanical mockup. A simplified geometry consisting of a single stave mockup with
heating elements has been implemented inside a wind tunnel. Temperature and vibration ampli-
tudes are monitored as function of air-flow velocity and the results are compared to finite-element
simulations.

### 7.3 Mechanical integration

Low-mass mechanical solutions are under study, to provide sufficient support for the sensors, the
readout chips and the cabling infrastructure, while leaving enough clearance for air-flow cool-
Figure 7. Air flow in a vertex detector layout with spiral endcap geometry (left) and finite element simulation of the resulting temperature profile in the barrel layers (right).

Assembly and in-situ testing scenarios taking into account the constraints from the surrounding detector elements have been developed. Realistic cabling layouts are proposed and evaluated in terms of their impact on the global and local material budget. Various prototype stave supports made of carbon-fibre reinforced polymers (CFRP) have been produced and tested for bending stiffness. The results of the tests are compared to analytical calculations and to finite-element simulations. Support structures including silicon carbide (SiC) foam are also under study.

8. Conclusions

The CLIC machine environment and the requirements for precision physics measurements place challenging demands on the vertex-detector systems. Initial detector layouts meeting these demands have been proposed and are currently being refined in line with results from detector-optimisation and hardware development studies. An active R&D program on sensor and readout technologies, simulation, power delivery and power pulsing, mechanical integration and cooling is in place.

References


