M10.6.7: Design and manufacturing of high linearity multichannel downconverter

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Abstract:

To achieve the required beam stability for the FLASH a cavity field stability for the accelerating sections in amplitude of 0.01% and in phase of 0.01 degree the design of a high performance multichannel downconverter was necessary. The designed module can operate with both 1.3 GHz and 3.9 GHz input frequencies used at FLASH. This milestone concerns designing of an eight-channel prototype downconverter and its performance evaluation. Specification for the designed module is given and the design issues are described in the following sections of this report. The last section of this document contain measurement results, conclusions and future plans for the developed device.
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1. INTRODUCTION

The electron beam is accelerated in the FLASH facility by high gradient fields generated in superconducting cavities. Group of eight cavities with all necessary surroundings creates one accelerating module (ACC). There are seven accelerating modules at FLASH. The accelerating field is controlled by a feedback loop including field detector, controller and actuator. The most important function of the detector is frequency downconversion from RF of 1.3 GHz or 3.9 GHz to an IF frequency acceptable by digitizing hardware. In the case of FLASH the IF value is 54 Hz. The locations of downconverters (DWC) at FLASH is shown in Fig. 1.

Fig. 1: Location of downconverters in the accelerator

There are three signals from each cavity in an accelerating module that are detected (probe, forward and reflected). It gives 24 signals to be detected from each accelerating module. For best hardware allocation it is a natural choice to design an multiple of eight-channel DWC.
The performance of the controlled accelerating field strongly depends on the DWC parameters. Amongst most important there are linearity, noise and crosstalk.

The outcome of this milestone is the prototype design of an eight-channel DWC with strong focus on achieving the high linearity, low noise and high crosstalk values. The prototype was characterized in laboratory and at FLASH during successful operation.

2. DESIGN REQUIREMENTS

Electrical requirements:
- **RF in**: 1300 MHz or 3900 MHz, level: up to 20 dBm,
- **LO in**: 1354 MHz or 3954 MHz, level: 0 - 10 dBm for all 8 channels,
- **IF out**: 54 MHz ± 10 MHz level: 700 mV peak at max. input level,
- **SNR**: >80 dB for nominal IF level of 500 mV peak (Note: corresponds to spectral noise density of 20 nV/sqrt(Hz)),
- **Linearity** for vector sum (VS) of 32 cavities: 0.01,
- **Drift**: offset < 0.1 mV / deg. C,
- **Phase drift**: < 0.1 deg./deg. C,
- **Crosstalk**: -50 dB between the 8 channel,
- **Crosstalk**: -80 for external noise sources.

Other Requirements:
- □SMA connectors for LO and RF signals, 8 channels
- □Di
erential and single ended IF outputs (congurable by jumpers)
- □Multicoax connector for IF output
- □Power supply Vpos 2< 7V; 15V >, Vneg 2< -15V; -7V >.
- □On-board LO power level monitor
- □Fixed LO attenuators for channel isolation improvement at each channel
- □Shielding option

3. DOWNCONVERTER DESIGN

The eight-channel downconverter module was designed. Design was split into eight identical DWC cells for simplification of the designing process and for easier crosstalk optimization. Block diagram of a single cell is shown in Fig.2. An active high IP3 mixer chip (LT5527) was used that exhibits excellent channel isolation with relatively low LO power. It was an important issue because the LO splitting and distribution introduces significant losses, therefore use of passive mixers could yield to unacceptable power levels required at the DWC module LO port. The mixers output is filtered and amplified by a high performance amplifier. The selected mixer chip can cover both of the required RF frequencies – 1300 MHz and 3900 MHz. Therefore by little modification of input components the designed DWC module can be
used for both application – accelerating cavity field control and operation in the 3.9 GHz system.

![Basic block diagram of single DWC cell](image)

*Fig. 2: Basic block diagram of single DWC cell*

Photograph of two adjacent cells is shown in Fig. 3. One can see LO input tracks at the bottom. The RF and IF paths are hidden on inner layer of the PCB. An 8-layer board was designed to make it possible to transmit all necessary signals, provide power supply and assure sufficient grounding and channel separation.

![Photograph of DWC cells](image)

*Fig. 3: Photograph of DWC cells*
Photograph of the entire DWC module is shown in Fig.4. In front of the channel cells one can distinguish LO distribution section. There is one LO input, in the middle of the crate front panel. RF signals are connected directly from front panel to cells. IF signals output are located at the rear side with use of multicoax connectors. By this connecting or disconnecting of IF signals is simplified.

Each cell and the LO distribution are are surrounded with ground areas with holes prepared for fixing metal shielding in case of too large interference from external noise sources.

4. SELECTED PERFORMANCE MEASUREMENT RESULTS

Due to the installation of the 3.9 GHz system at FLASH, the 3.9 GHz version of the DWC was assembled and tested in the laboratory. Amongst the most important measurements are the items listed below.

4.1. CONVERSION POWER GAINS

Conversion power gains are defined as:

$$G_n[\text{dB}] = P_{f_n}[\text{dBm}] - P_{RF_n}[\text{dBm}]$$

They were measured in conditions:

$$P_{LO} = 9\text{dBm}, \quad f_{LO} = 3.954\text{GHz}$$
$$P_{RF_n} \approx 1.5\text{dBm}, \quad f_{RF} = 3.900\text{GHz}$$
Measurement results are collected in the Table 1. Less than 10% of differences between gain values show very good repeatability of channel design.

<table>
<thead>
<tr>
<th>n</th>
<th>$P_{RFn}$ [dBm]</th>
<th>$P_{IFn}$ [dBm]</th>
<th>$G_n$ [dB]</th>
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<tbody>
<tr>
<td>1</td>
<td>-1.56</td>
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<tr>
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<td>7</td>
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<tr>
<td>8</td>
<td>-1.55</td>
<td>5.28</td>
<td>6.83</td>
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4.2. THE 1 DB COMPRESSION POINTS

The 1dB compression point it is a pair of RF and IF power levels where the conversion gain is 1dB smaller than the small signal conversion gain. Measurement results are collected in Table 2. Again, results are repeatable between channels. This table gives an information about operating values of the LO and RF signals for which no significant harmonic distortion is observable.

<table>
<thead>
<tr>
<th>n</th>
<th>$G_{\Delta dBn}$ [dB]</th>
<th>$P_{RFn_{dB}}$ [dBm]</th>
<th>$P_{IFn_{dB}}$ [dBm]</th>
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<tr>
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<td>8</td>
<td>5.83</td>
<td>8.83</td>
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4.3. CHANNEL CROSSTALK

Channel cross-talks were measured as: $I_{nk} = P_{IFn}[dBm] - P_{RFk}[dBm]$ where n; k - numbers of channels (n 6= k).
Measurement conditions:

- PLO = 9dBm
- PRF = -3; 5dBm

Results are collected in the table 3. Values of 60 dB for adjacent channels fulfil the design requirements. Other channels exhibit excellent crosstalk values of up to 87 dB.

5. SUMMARY

The eight-channel DWC module was designed and assembled. Presented measurement results show that it fulfils the design requirements. The 3.9 GHz version of the module was installed successfully at FLASH and is currently in operation there [1].

6. REFERENCES


7. ONGOING ACTIVITIES

Intensive work is performed to design the compact, RTM version of the developed DWC module for the xTCA based LLRF system. The designed module will contain platform management circuits for intelligent power supply control. There will also be more diagnostics incorporated and connected via digital links to the control system. The size of the new module will be smaller, but basing on the current tests we have concluded that there should be no significant performance degradation.