M10.6.8: Integration of downconverters and upconverters in RTM (ATCA)

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INTEGRATION OF DOWNCONVERTERS AND UPCONVERTERS IN RTM

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INTEGRATION OF DOWNCONVERTERS AND UPCONVERTERS IN RTM

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Abstract:

The Low Level RF control system for FLASH accelerator is composed of among of digitizer modules, digital processing module and Vector Modulator (VM) that are required to close the feedback loop. To achieve the required beam stability for the FLASH a cavity field stability for the accelerating sections in amplitude of 0.01% and in phase of 0.01 degree the design of a high performance Vector Modulator is necessary. The designed module can operate with 1.3 GHz and 3.9 GHz input frequencies used at FLASH. This milestone concerns designing of RTM module with two independent Vector Modulator channels designed according to MTCA specification. The second part of this deliverable refers to a compact version of a multichannel downconverter module in an RTM standard.
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INTEGRATION OF DOWNCONVERTERS AND UPCONVERTERS IN RTM

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1. INTRODUCTION

The development of the Vector Modulator card started with an AMC (Advanced Mezzanine Card) format developed for the ATCA based LLRF system [1]. The one channel card was developed to prove the principle in years 2009 and 2010. It was successfully tested and it was fulfilling requirements [2]. Designed and manufactured board is shown in Figure 1.

After the change of standard from ATCA to μTCA, the designed prototype was used as a base of a 2-channel μTCA version of the board, which is a subject of this report.

The μTCA-based Vector Modulator (μVM) is designed to be used as a μRTM module of μTCA-based Controller. It offers two output channels with independently adjustable phase and amplitude. The output power is controlled by an adjustable attenuator, hence the resolution of operation is not compromised when reducing the output level. The analogue RF-chains have build-in power monitoring capabilities. The board offers a variety of control and data interfaces including high-speed serial links and equalized LVDS parallel buses to uTC AMC module. The photograph on the module is presented in Figure 2.
Figure 2. A prototype of μTCA-based Vector Modulator
1.1. DIGITAL PART

The VM module modifies the phase and amplitude of the reference high frequency RF signal using I and Q components delivered by the LLRF controller. I and Q signals are serialised and transmitted to VM board using Z3 multiboard connector. On the VM module the signals are deserialised and delivered to DACs and used for modulation.

This part of specification concentrates mainly on digital part of VM: signal transmission channel based on Rocket IO transceiver provided by Xilinx FPGAs, FPGA device, module management and monitoring (IPMI) and digital power supply.

1.1.1. Selected components

The following components were selected to fulfil requirements defined in chapter 2:

- FPGA: Xilinx Spartan 6 XC6SLX45T-3FGG484, package FGG484 (7000 slices, 400 kb dist. RAM, 4x GTP, 296x IO),
- Power supply DC/DC converters: LTM4619EV#PBF (2x4 A),
- MMC controller functionality based MTCA.4 using an EEPROM, IO Extender, Temp Sensor,
- Digital thermometer with I2C bus: MAX6626RMTT (12-Bit Temperature-to-Digital Converter),
- Voltage monitor.

The VM module should be equipped with a local oscillator (f=50 MHz) connected directly to the FPGA, RS232 to USB converter (FTDI FT232R, mini USB connector), Xilinx Jtag (dual-row male 2.00 mm pitch) and power connectors for debugging purposes.

The VM should provide the following RF connections:

- Single high frequency RF input (preferred SMA connector) f=1.3 GHz (3.9 GHz),
- 2x double high frequency RF output (TBD) f=1.3 GHz (3.9 GHz).

1.2. ANALOGUE PART

The block diagram of analogue part of VM is presented in Figure 2.
1.2.1. Vector Modulator Specification

**Functional specification**

- Operation Pair (connector pin compatibility):
  - VM operation
  - 2 VM Channels Output Broadband Drive
  - Processed internal RF power level
  - Shortterm noise
  - Longterm amplitude/phase stability
  - Nonlinearity, Sideband Carrier Suppression (i,Q Plane)
  - VM1, VM2 Channel crosstalk
  - VM1, VM2 Channel isolation
  - DAC selection, 16-Bit, >100Mps, Low Noise
  - DAC IQ Filter, 2nd order (passive + OPV roll-loff)
  - Selection of Low noise components
  - Internal RF-switches (RF-gates provided by MHF-P)
  - Coupler chain diagnostic for

Controller - VM RTM
ADC SIS8300 Board - VM RTM
Single sideband operation
1.3GHz, 3.0GHz, 3.9GHz
>0dBm
-160dBc/sqrt(Hz), @ +10dBm input power
<0.05%, <0.05 deg (forever-10Hz)
<-60Bc, <0.1% error
<-70dB (fadditonal fixed att. for spliiting ?)
> 80dB
81MHz data throughput
arround 50MHz or jumpered to 1kHz
VM < -160dBc floor
diagnostic
MO signal,
VM1 output (before endswitch1),
VM2 output (before endswitch2)
2. DESIGN

2.1. SYSTEM OUTLINE
The whole LLRF system may use the MO reference signal provided either through the SMA connector (RF IN 2, see Figure 4) or by the analog backplane connector (Radiall Coaxipack2 series, RF IN 1). The power of the input signal is monitored. Reference signal is split between two RF chains and local clock distribution circuit. In case of analogue RF chains, the signal is first modulated, then amplified, attenuated, monitored and finally directed to the output through the RF gate (RF OUT 1 and 2). The local distribution circuit divides the frequency of the input signal. This low frequency clock is used for clocking the DACs and part of the FPGA circuit. The FPGA drives the fast DACs working in current source, constant voltage mode. The resulting output current is converted to voltage with differential trans-impedance amplifier. Common mode of this signal is shifted to appropriate level (controllable through slow DAC). Finally, the signal is provided for the Quadrature Amplitude Modulators (QAM) of output channels. The FPGA may be controlled using the serial Gigalink or LVDS bus available at the μRTM connector or using the SFP transceiver via optical connection. The board can also operate in a stand-alone mode.

Figure 4. Block diagram of the Vector Modulator
2.2. RF INPUT CHANNEL AND CLOCK DISTRIBUTION CIRCUIT

MO reference signal provided either through the SMA connector or by the analog backplane connector is coupled into the power monitoring circuit and then split between two output RF chains and a local clock distribution circuit (see appendix). Source of the signal is controlled electronically using SPDT switch (HMC349).

First divider (HMC705, 1 – 17, programmable) is used only in 3.9 GHz versions, otherwise it is bypassed. It is used due to main clock divider and clock distribution IC (AD9516) maximum input clock frequency limit of 2.4 GHz. Alternatively clock from analog backplane or Zone 3 connector (configured with 0402 shorts) can be distributed. Clock signal is provided for DACs in LVPECL standard (termination on receiver side), while other components:

- FPGA
- MGT (optionally)
- Diagnostic connector
- Zone 3 connector.

receive clock in LVDS standard. VCO and PLL capabilities of the AD9516 chip are usually not used, but a space on the board has been left for loop filter.

2.3. QUADRATURE AMPLITUDE MODULATORS AND RF OUTPUT CHANNELS

The μVM uses HMC497 as Quadrature Amplitude Modulator (see appendix). This integrated circuit has differential inputs and single-ended output. The input LO signal is internally shifted in phase by +45 and -45 degrees, then amplified proportionately to baseband signals. The I and Q inputs are differential, and should have common mode of 1.5 V.

Signal on the output of modulator chip is amplified by roughly 15 dB, attenuated (15 dB to 0, excluding insertion losses), coupled to power monitor and feed through gate to SMA connector.

2.4. DIGITAL-TO-ANALOG CONVERTERS AND BASE BAND CIRCUIT

The μVM uses AD9777 DAC. It has 16 bit resolution, two output channels with differential outputs, programmable channel gain, offset adjustment and differential clock inputs. Outputs work as current sources, with compliance range of -1 to +1.25V. First stage differential trans-impedance amplifier converts 20 mA full scale signal to 1.0 V full scale signal with common mode of 0.5 V (see Figure 5). Second stage amplifier shifts common mode of signal to 1.5 V (value set by AD5624 slow DAC, amplified by factor of two and low-pass filtered in analog circuitry). Voltage reference of 4.096V has been used for this slow, 12-bit DAC, which simplifies calculations.
2.5. POWER MONITORING

The power of input and output signals on the μVM are monitored using HMC602 Logarithmic Detector. Input of this integrated circuit has been impedance matched accordingly to the documentation of the evaluation PCB. Output voltage signal is low-pass filtered, amplified by factor of two and low-pass filtered in analog circuitry (see Figure 6). Finally it is converted to digital format using MCP3204 ADC (using same voltage reference as slow DAC).

2.6. DIGITAL SUBSYSTEM WITH FPGA

The μVM communicates with μTC using digital signals only. The μRTM connector is used to carry three types of links that may be used freely by the VM application (no taking into account the signals required by PICMG specifications), see Figure 7:

- 2 Low Latency Links: one to the μVM FPGA and one to the SFP transceiver connector on uVM face-plate,
- 8 differential tuned LVDS pairs of equalized length,
- 16 differential tuned LVDS pairs of different lengths.
Moreover, one high-speed serial link is provided between the FPGA and SFP transceiver socket. There is also a data path with four signals between μRTM connector and 8P8C modular jack on the VM face-plate, where the μVM FPGA is used to control operation of the M-LVDS drivers.

![Figure 7. Block diagram of the digital module of Vector Modulator](image)

The μVM FPGA controls main DACs, clock distribution circuit, attenuators, RF power monitoring circuit, monitoring ADC, base-band DAC using seven independent SPI buses. It can interface remote systems by means of har-link connector and USB emulated serial port. The main data connection of both dual DACs consists of two ports of 16 bits per DAC channel, totaling to 64 bits for all the four channels.

The FPGA can be configured using an SPI FLASH memory or a Platform FLASH circuit. The Platform FLASH memory and the FPGA circuit are directly accessible using the JTAG interface. The Xilinx ISE environment is able to program SPI memory using the JTAG channel by uploading the programmer core into the FPGA circuit. The JTAG chain can be accessed using a dedicated Xilinx connector or the μRTM socket. The VM JTAG chain is automatically included in the main JTAG chain of uTC when VM is activated by MMC (M4 state).

### 2.7. MANAGEMENT HARDWARE

The μVM board is equipped with basic management on monitoring hardware, illustrated in Figure 8. The heart of this subsystem is an 8-bit expander. It is responsible for reading hot-swap sensor, driving optical indicators and monitoring power supply good signals. It also provides two-wire interface to the FPGA and controls the 'write protect' signal of the on-board serial EEPROM.
memory. The EEPROM is used to store information on the μRTM module capabilities according to IPMI and AMC standards and is protected against undesirable write. The board is also equipped with four MAX6626 thermometer circuits placed in the most critical parts of the PCB board.

*Figure 8. μVM management and monitoring hardware*
3. FACE-PLATE

The μRTM has a double-width mid-size AMC module front-panel with mounting screws. The AMC handle is mechanically connected to the hot-swap switch SW1.

3.1. INPUT SMA CONNECTOR (J16)

This connector should be used for feeding the VM with the main MO reference signal (frequency dependent on the version of VM: 1.3, 3.0 or 3.9 GHz). The input power should be about +10 dBm, not more than +13 dBm.

3.2. OUTPUT SMA CONNECTORS (J13, J14)

This connectors provide modulated output signals with adjustable power level. J14 is output of 1st channel, while J13 is output of 2nd channel.

3.3. 8P8C MODULAR JACK (U34)

The modular connector offers four differential pairs in the M-LVDS standard. The data lines are forwarded to the μRTM connector using the LVCMOS_33 standard. The direction of the M-LVDS buffers is controlled by the VM FPGA.

3.4. HAR-LINK CONNECTOR (J5)

The Har-link connector provides eight general purpose signals connected to the FPGA. All signals are passed through MAX3002 bidirectional buffer, and have voltage level of 3.3 V. To use these lines, the buffer must be first enabled by the FPGA.

3.5. SFP TRANSCEIVER CONNECTORS (U28)

The SFP transceiver cages are connected to the VM FPGA and to the μRTM connector. Every SFP is accompanied by two LEDs informing the user of the presence of the optical signal and of the fault of the transmitter.

3.6. LED INDICATORS

The V1 (blue), V16 (green) and V17 (red) diodes are driven by the MMC, using the 8-bit \textsuperscript{1}C bus expander. Diodes V12, V13, V14, V15 are connected to the SFP cages\textsuperscript{1}. The FPGA\_LED diodes are available for the FPGA application.

\textsuperscript{1}Due to the design bug, these 4 LEDs are not used in this revision (wrong placement).
4. CONNECTORS AND INDICATORS ON THE PCB

Many of the board configuration options may be altered by placing or removing configuration resistors and capacitors. The module also offers a few on-board connectors that may be very useful during firmware development stage, e.g.: JTAG connector for the FPGA, USB virtual serial port or power supply connector for out of the shelf operation.

Figure 10 is provided as a guide of connectors and indicators which are placed on the PCB. These components will be described in detail in the following sections of the manual.

4.1. MRTM CONNECTORS

The µRTM is interfaced using two connectors. The draft of the MTCA.4 specification provides following names for these connectors: J30 and J31. These correspond to the connectors J12 and J4 of the design respectively. J30 connector passes not only data signals, but also power buses, JTAG
port and a management interface.

4.2. ANALOG BACKPLANE INTERFACE

The analogue backplane is interfaced using two connectors:

- U72: Radiall Coaxipack 2 (R694 252 106) – provides reference signal
- J15: Erni ErmetZD 3-10 (973028) – provides differential clock of 81.25 MHz and analogue power supply of +7.0 and -7.0 Volts.

5. EXPERIMENTAL RESULTS

5.1. MEASUREMENT SETUP

The following components were used in test setup:

- VM_RTM board (19.0003, Rev. 1.0, 1.3 GHz version)
- Agilent E5052A and E5052B Signal Source Analyzer
- Rohde & Schwarz ZVS series vector network analyzer
- Holtzworth HS2004A

5.2. REFLECTION COEFFICIENTS

In this section the input and output reflection coefficients measurements done using calibrated Rohde & Schwarz ZVS series vector network analyzer on 17th August 2011 are described. Measurements were done in 200 MHz band centered at 1.3 GHz.

Input reflection coefficient was measured on the SMA input of the board in following states:

- Input switch set to SMA, Biased modulator, Minimum attenuation
- Input switch set to SMA, Biased modulator, Maximum attenuation
- Input switch set to SMA, Unbiased modulator, Minimum attenuation
- Input switch set to Backplane

In all those states the outputs of the board were matched. Measurement results are presented in Figure 11. The input reflection coefficient is -15 dB or better in all states. When input is set to SMA the match is -18 dB or better. Such results are fully satisfying.
Output reflection coefficient was measured in following states (the input and the second output were always matched, in all but the last state the output gate was turned on):

- Minimum attenuation, Matched Input
- Minimum attenuation, Shorted Input
- Minimum attenuation, Opened Input
- Output gate turned off

Measurement results are presented in Figure 12. At 1.3 GHz frequency the output reflection coefficient is in range of -9.6 to -9.8 dB. Such a poor matching is probably caused by too many corners in the signal path (result of a very small area reserved for each channel) and too big reflection coefficient at the output of the amplifier. If possible the output impedance matching should be improved in the next revision of the board.

Matching at the output is worse in case of the output turned off then at the input in case of the input switched off (the same switch is used) due to much lower losses (the transmission line from the input SMA connector to the input gate is 15 cm or longer, while at the output the line is 3 cm long).
5.3. OUTPUT SPECTRUM.

Output spectrum of the board was measured in cases of positive modulation of the carrier by frequency 81.25 MHz / 64 = 1.270 MHz and 81.25 MHz / 32 = 2.540 MHz.

As it can be observed, the worse component is 3\textsuperscript{rd} negative and 5\textsuperscript{th} positive harmonics (Tables 1. and 2 and Figures 13 and 14), but they can be filtered if necessary with an external band-pass filter. In worse case, their level is -35.9 dBc (after calibration, Table 1.). Calibration allows to achieve carrier suppression as good as 70.5 dB (un-calibrated modulator only 15.5 dB, Table 2.).

Table 1. Output spectrum (1.27 MHz modulation)

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<tr>
<th>Harmonic</th>
<th>-5</th>
<th>-4</th>
<th>-3</th>
<th>-2</th>
<th>Unwanted sideband</th>
<th>Carrier</th>
<th>Wanted sideband</th>
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<td>Power level (dBm) without calibration</td>
<td>-56.2</td>
<td>-48.6</td>
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<td>-34.8</td>
<td>-19.1</td>
<td>-10.5</td>
<td>5</td>
</tr>
<tr>
<td>Power level (dBm) with calibration</td>
<td>-80.2</td>
<td>-64.4</td>
<td>-33.5</td>
<td>-56.7</td>
<td>-55.1</td>
<td>-61.3</td>
<td>5.5</td>
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Figure 13. Output spectrum (1.27 MHz modulation)

Table 2. Output spectrum (2.54 MHz modulation)

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<th>-2</th>
<th>Unwanted sideband</th>
<th>Carrier</th>
<th>Wanted sideband</th>
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<th>3</th>
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<tr>
<td>Power level (dBm)</td>
<td></td>
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<tr>
<td>without calibration</td>
<td>-36.8</td>
<td>-34.9</td>
<td>-19.1</td>
<td>-10.5</td>
<td>5</td>
<td>-25.6</td>
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<td>Power level (dBm)</td>
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<td>-53.0</td>
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<td>5.5</td>
<td>-57.5</td>
<td>-73.0</td>
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6. VECTOR MODULATOR SUMMARY

The developed VM boards (1.3 and 3.9 GHz) were manufactured and assembled. The boards were debugged and measured at DESY. The Figure 1 shows the 1.3 GHz VM board used during demonstration of uTCA-based LLRF system in September 2011. All the required functionalities were operating correctly. Minor problems were found during the tests. The problems are corrected in the second revision of the board.

7. COMPACTIFIED MULTICHANNEL DOWNCONVERTER RTM MODULE

The multichannel downconverter was designed and tested successfully as described in the deliverable report 10.6.7 [3]. The last part of task in this area was devoted to compactification of the designed module and production of board compatible to xTCA RTM standard. The design was performed in fall 2010/beginning of 2011. The manufactured compact version of the downconverter is shown in Figure 15. Performance was successfully tested and is comparable with results achieved by the “bigger” prototype. Therefore it was decided not to put similar results into this report.
Figure 15. Multi-channel RTM downconverter module.

8. REFERENCES


APPENDIX – VECTOR MODULATOR BLOCK DIAGRAMS

Figure 16. Clock distribution system schematics (1.3 GHz version)

Figure 17. Clock distribution system schematics (3.9 GHz version)
Figure 18. RF input channel structure and part of the clock distribution circuit (1.3 GHz version)
Figure 19. RF input channel structure and part of the clock distribution circuit (3.9 GHz version)