**The Development of a General Purpose ARM-based Processing Unit for the TileCal sROD**

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**Computing for High Energy Physics**

High Energy Physics (HEP) projects such as the Large Hadron Collider (LHC) generate enormous amounts of raw data which presents a serious computing challenge. After upgrades in 2022, the data output from the ATLAS Tile Calorimeter will increase by 200 times to 41 TB/s (5 TB/s) [1]. It is infeasible to store the entirety of this data for offline computation.

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**Single System on Chip Benchmarks at 1 GHz**

<table>
<thead>
<tr>
<th></th>
<th>Cortex-A7</th>
<th>Cortex-A9</th>
<th>Cortex-A15</th>
</tr>
</thead>
<tbody>
<tr>
<td>HPL (SP GFLOPS)</td>
<td>1.76</td>
<td>5.12</td>
<td>10.56</td>
</tr>
<tr>
<td>HPL (DP GFLOPS)</td>
<td>0.70</td>
<td>2.40</td>
<td>6.04</td>
</tr>
<tr>
<td>STREAM MB/s</td>
<td>2001</td>
<td>4484</td>
<td>6114</td>
</tr>
<tr>
<td>Peak Power [W]</td>
<td>2.65</td>
<td>5.03</td>
<td>7.48</td>
</tr>
<tr>
<td>DP GFLOPS/Watt</td>
<td>16.63</td>
<td>2.78</td>
<td>0.91</td>
</tr>
</tbody>
</table>

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**References**


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**Contact Information**

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**LHC ATLAS TileCal Phase II Upgrade**

**Current TileCal Read Out Architecture:** Many of the components are analog and situated on the detector.

**Upgraded TileCal Read Out Architecture:** The design is fully digital with complex electronics moved to the back-end.

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**Out Of Time Pile-Up in ATLAS TileCal**

Conditioned PMT Pulse: 7 samples per pulse (40 MHz ADC) are used for energy reconstruction.

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**Optimal Filtering vs. a Matched Filter:** With increasing OOT pile-up, the reconstructed energy diverges, resulting in errors.

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**PC Express HARDWARE**

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**PCI-Express Pair Tests**

**CPU memoryc DMA (EP)**  **DMA (RC)**

<table>
<thead>
<tr>
<th>Read [MB/s]</th>
<th>1741 ± 0.3%</th>
<th>256 ± 0.2%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write [MB/s]</td>
<td>236 ± 0.3%</td>
<td>352 ± 0.3%</td>
</tr>
<tr>
<td>DMA (PCIE)</td>
<td>577 ± 0.4%</td>
<td>577 ± 0.4%</td>
</tr>
</tbody>
</table>

Three tests were done using the PCI-Express Adapter 1.0 (Wave Board Pair). The first was a simple CPU-driven memory of 2 MB data. The Image Processing Unit (IPU) was then used for Direct Memory Access (DMA) copying of a 2 MB data file initiated by the End Point (EP) and Root Complex (RC). The RC is faster because of driver optimisations.

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**PC Express Cluster and Future Research**

A custom Linux device driver is being implemented to encapsulate standard Ethernet packets and transmit them over PCI-Express. This will allow existing applications to use the high data throughput PCIe-based cluster without modification.

There are several new ARM cores (Cortex-A50) being released with 64-bit capable processors which enables higher performance. It is important to benchmark and characterise these for the purposes of scientific computing.

Other low power and cost-effective platforms will be considered in future, such as Intel Atom. Previous generations of Atom are inferior to ARM but now, as yet unavailable, Atom SoCs will be tested when they become available.

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