Trigger Data Serializer ASIC Chip for the ATLAS New Small Wheel sTGC Detector

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Nov. 12, 2014
Outline

- Background: Overview of Trigger Data Serializer (TDS) in sTGC trigger
- Design of TDS
  - strip-TDS as an example
  - first prototype of TDS (TDS version I: TDSVI)
  - Parameters on TDSVI
- The Serializer in TDSVI: GBT-SER-DM
  (The GBT Serializer in IBM 130 nm CMOS DM323 Metallization)
  - Architecture of GBT-SER-DM
  - Prototype of GBT-SER-DM
  - GBT-SER-DM performance
  - A stable, fixed latency link with TDS Serializer and serial protocol
- Conclusion
NSW trigger concept

- Phase I upgrade: Increased backgrounds, but must maintain existing trigger rate
- Filter “Big Wheel” muon candidates to remove tracks that are not from the IP
  Only track “A” should be a trigger candidate: pointing: $\Delta \theta < \pm 7.5\text{mrad}$

New Small Wheel – defines basic layout and envelopes
- 16 detector layers in total
- 2 technologies, MicroMegas and sTGC

Lorne Levinson, Overview of NSW trigger electronics
sTGC trigger scheme

1/16th sector

On Rim of NSW FPGAs

Pad Trigger

Router

USA 15

sTGC Trigger Processor

Problem: no BW to read all strips
Pad trigger uses pad tower coincidence to choose ONLY the relevant band of strips.

Physical pads staggered by ½ pad in both directions

Logical pad-tower defined by projecting from 8 layers of staggered pad boundaries

Pad-tower coincidence = 2 × 3-out-4 overlapping pads

Lorne Levinson, Overview of NSW trigger electronics
Design of TDS: strip-TDS

- Three parts: VMM interface, Preprocessor, Serialization
- Challenges in design include: large number of inputs, short latency required, low power consumption, radiation tolerant, etc.

TDS: for strips, pads

- IBM 8RF-DM 323, 130 nm CMOS; 1.5 Volt supply
- Each strip-TDS:
  - 128 channels, covering strips from 2 VMMs
  - add BCID for each strip
  - programmable delay for BCID clk
- Accept pad Trigger, select matching strips
- Send out strips charge via SER @ 4.8 Gbps per trigger

- Each pad-TDS:
  - 96 channels, covering 96 pads from (2) VMMs.
  - Sample and Time-stamp pad inputs (96 pads)
  - Send out yes/no info of pads at 4.8 Gbps each BC
First Prototype of TDS: TDSVI

<table>
<thead>
<tr>
<th>Type</th>
<th>Instances</th>
<th>Area</th>
<th>Area %</th>
</tr>
</thead>
<tbody>
<tr>
<td>sequential</td>
<td>47081</td>
<td>1387708.800</td>
<td>46.7</td>
</tr>
<tr>
<td>inverter</td>
<td>13335</td>
<td>80242.560</td>
<td>2.7</td>
</tr>
<tr>
<td>buffer</td>
<td>1455</td>
<td>16752.000</td>
<td>0.6</td>
</tr>
<tr>
<td>logic</td>
<td>104516</td>
<td>1489987.200</td>
<td>50.1</td>
</tr>
<tr>
<td>total</td>
<td>166387</td>
<td>2974690.560</td>
<td>100.0</td>
</tr>
</tbody>
</table>

Die: 5.2 mm x 5.2 mm

2.3 mm x 2.3 mm

CERN ePLL IP core
0.3 mm x 0.4 mm

2x 640 Mbps RX
0.1 mm x 0.2 mm

GBT SER DM
1 mm x 1 mm
Power, Latency, Package and Current Status

- Total deliverables: design, prototype, production and test of 3,700 TDS chips.
- The total power of one TDS < 1 W:
  - digital ~ 300 mW (estimated) + SER 300 mW (tested) + IO 150 mW (estimated) + other
- Strip-TDS latency (<100 ns, estimation from simulation)
  - 18.75 ns for BCID and pad trigger matching
  - 12.5 ns to re-align all selected strips after 8-1 sequencers
  - 12.5 ns for trigger data preparation and format
  - 6.25 ns for buffer the trigger data for ping-pong FIFO
  - 6.25 ns for scrambler and CRC
  - 4 ns for serializer
  - 22 ns to deserialize the pad trigger data and decode trigger information
  - 12.5 ns to access pad Look-up-Table (LUT) and find the starting strip address

- Wire-bond BGA, 400 pins, 1 mm pitch
  - Package is currently under design at I2A, INC.
- Design submitted on August 18 (MOSIS MPW), Die expected back in mid-Nov.
  - Design of Test-board is in progress.
With respect to the CERN GBT SER IP core:

1: The metallization is converted from IBM 8RF LM62 to IBM 8RF DM323

2: Changes to Part I

- Instead of running at 40 MHz to load 120 bits, we run at 160 MHz to load 30 bits
- In this way, the waiting time is reduced to 6.25 ns for 160 MHz
  And could seamless interface the logic part which works at 160 MHz

Changes to Part 2

- Reduce the length of each shift register from 40 bits to 10 bits

No changes on Part 3

GBT-SER in DM core:
- 1 mm x 1 mm
- 1.5 Volt; 300 mW power
- Line rate: 4.8 Gbps, Ref Clk: 40 MHz

A prototype of this core was submitted with VMM2, and tests have been done at UM
Prototype of GBT-SER-DM

- A recent prototype went with BNL ASD chip (VMM2) submitted at Jan. 31st, 2014
- Serializer core:
  - ~1mm^2, 300 mW power, 1.5 Volt supply
- Prototype in a QFN 100 Package
Performance of GBT-SER-DM

4.8 Gbps: Eye of GBT-SER-DM serial output without repeater

4.8 Gbps: Eye of GBT-SER-DM serial output after 4 m mini-SAS 8f36 cable with repeater

<table>
<thead>
<tr>
<th></th>
<th>TJ (ps)</th>
<th>RJ (ps)</th>
<th>DJ (ps)</th>
<th>PJ (ps)</th>
<th>Width@BER (ps)*</th>
<th>Height (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SER</td>
<td>49.73</td>
<td>3.351</td>
<td>9.869</td>
<td>9.869</td>
<td>158.6</td>
<td>~600</td>
</tr>
<tr>
<td>SER+Cable+Repeater</td>
<td>145.97</td>
<td>10.482</td>
<td>11.175</td>
<td>11.175</td>
<td>62.364</td>
<td>612.37</td>
</tr>
</tbody>
</table>

*: For BER = 1E-12, tests done with PRBS-31

Cable DS100BR410

Mini-SAS 8f36 cable

4 m cable

Cable Test board
A stable fixed latency link with TDS Serializer

Data: 120 bits / trigger
Need additional bits for building a stable serial link with router

120 bits of data occupied 4 frames of 30 bits, plus additional serial overhead,
At least we need 5 frames to send out all the info.

At the presence of a valid pad trigger
- Use five 160 MHz clks to send out all data from a pad trigger, 30 bits/frame
- When no pad trigger appears
  Send out a NULL packet (30 bits)

Example of a data frame
- header: 1010 for establishing link;
- flag “10” and “01” used for router to quickly identify data or NULL: cutting through switching
- 24*5 bits data are scrambled to be DC balanced
- Scrambler: \( G(x) = 1 + x^{39} + x^{58} \)
A stable fixed latency link with TDS Serializer

KC705 board

Test Pattern Generator --- Scrambler --- TDS-SER

Repeater

Artix-7 GTP RX

Packet Syn

Descrambler

Packet Analyzer

Delay: 113.2 ns
RMS: 35.6 ps

Latency includes: (RX end: ~ 60 ns)
TX: ~22 ns + 25 ns cable+ 6.25 ns Reading time
Conclusions and Outlook

Conclusions:
✓ Design of TDS has been done.
✓ A first Prototype of TDS has been submitted, and currently in design of its BGA package
✓ Successfully converted the CERN GBT SER to be used in TDS
✓ A prototype of TDS Serializer-only chip has been done, and good performance is demonstrated
✓ A stable and fixed latency link has been established with TDS protocol and its embedded Serializer core

Future work:
☐ Lab-test of TDS first prototype
☐ Radiation test of TDS
☐ TDS chip test in real detector setup with VMM2
☐ Aiming for a second prototype of TDS: TDSVII
Back up materials
Block diagram of pad-TDS

- Three parts: VMM interface, Preprocessor, Serialization
- Pulse Detection: detects pad pulses from VMM, and latches BCID
- Preprocessor: compare the current BCID with the BCID of pad pulse, to assign yes/no info
- Share the same SER interface with pad-TDS: Scrambler/CRC are not exactly the same but similar
- Use shift registers to avoid manual control of memory locations
- Manual control of the memory locations would suffer from SEU
- Upon trigger, contents of four mem locations in a channel will all be read and compared against the BCID provided.
Preprocessor (2): Trigger matching algorithm

- Upon trigger, the range of interested strips are specified as following:

- In BCID comparison of trigger BCID with strip-BCIDs in the ring buffer:
  - if a strip with a BCID flag ‘invalid’, exact BCID matching will be done
  - if a strip with a ‘valid’ BCID flag, the BCID comparison is done as:
    - e.g., a strip with BCID m, and BCID flag = 1, trigger BCID is k,
      - we will compare both m with k and m-1 with k in this case, respectively.
      - if in either case there is a match, we output it.
  - This is because a strip with BCID m and flag =1, may also belong to the previous cycle (BCID m-1)
  - Set matching window to 25 ns can turn this function off.
Preprocessor (3): 8-1 selector and sequencer

- 132 chnls are arranged in 17 groups, each group has 8 strips
- For the 8 strips in a group, they are arranged from the 132 chnls by every 17 strips
  e.g., denoted 132 chnls as strip #0- strip #131, in the first group there are: strip #0, #17, #34 ... #119
- The reason for the above arrangement is: we only send out 17 consecutive strips per trigger,
  With the above scheme, there will only be one valid strip at most in each group.
- A sequencer follows the 8-1 selector to maintain the nature sequences of the strips

2-1 Priority Sequencer Truth Table

<table>
<thead>
<tr>
<th>a0</th>
<th>a1</th>
<th>flag0</th>
<th>Flag1</th>
<th>o</th>
<th>flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>1</td>
<td>x</td>
<td>a0</td>
<td>1</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>1</td>
<td>a1</td>
<td>1</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>a1</td>
<td>0</td>
</tr>
</tbody>
</table>

2-1 Priority Sequencer

Implementation of 4-1 selector with 2-1 selector cell
two 4-1 selector plus a 2-1 could build a 8-1 selector

e.g., for interested strips #15- #31,
The output sequence from the 17 8-1 SELs is:
#17, #18, ..., #31, #15,#16. (from Sel0-Sel16)

Sequencer will “correct” the order so there will not be confusion to the following circuits
pad-logic to strip-TDS interface

Data format

<table>
<thead>
<tr>
<th>Line</th>
<th>Format</th>
<th>Details</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>“10”</td>
<td>12 bits trigger BCID</td>
<td>12</td>
</tr>
<tr>
<td>1</td>
<td>“10”</td>
<td>13 bits phi ID + band ID</td>
<td>13</td>
</tr>
</tbody>
</table>

LVDS inpt: 640 Mbps

320 Mbps to 320 Mbps

320 MHz to 160 MHz

ePLL

Syn. and Trigger Info Decoder

160 MHz_ser

Trig_valid

Trig_bcid

band_phi_id