ATLAS Fast Tracker Simulation Challenges


To deal with Big Data flood from the ATLAS detector most events have to be rejected in the trigger system. The trigger rejection is complicated by the presence of a large number of minimum-bias events – the pileup. To limit pileup effects in the high luminosity environment of the LHC Run-2, ATLAS can use the full tracking provided by the Fast Tracker (FTK) implemented with custom electronics.

The ATLAS simulation workflow is composed of many steps: generate hard-processes, hadronize signal and minimum-bias (pileup) events, simulate energy deposition in the ATLAS detector, digitize electronics response, simulate triggers, reconstruct data, derive the reduced data formats for physics analysis. The FTK simulation is part of the workflow simulating the trigger response.

Fast tracking allows to separate different collisions and the originated objects: Specific topologies (i.e. b-jet or r) can be efficiently identified with high quality track reconstruction. Beyond these examples, FTK tracks will be widely used in trigger event selection. FTK tracks will be one of trigger’s best tools against pileup and the prohibitive time of full scan tracking.

FTK hardware performs global tracking in two steps: pattern matching and track fitting: Pattern matching and initial track fitting use 3 pixel, 4 SCT axial and 1 SCT stereo layers. The pattern matching uses custom Associative Memory (AM) ASICs pre-loaded with one billion patterns, with all patterns matched in parallel.

FTK Simulation Computational Challenge

Simulating the custom hardware is challenging as CPU requirements and resources usage:
- The AM system emulation requires to store 10^9 patterns, requiring 36 GB minimum with a real use of about 60 GB to use indexed searches
- Both pattern matching and track fitting are CPU intensive Unlike the whole events processing (traditional for HEP computing), the FTK simulations use the production system workflow with sub-events processing.

The event segmentation is natural given the HW modular structure and allow to fit within the worker nodes limits and exploit and parallelism of the computing farms.

FTK Simulation Goals and Structure

The entire FTK data processing pipeline has to be simulated in preparation for LHC upgrades, as we need to:
- Develop trigger strategies at high luminosity
- Support hardware design/initialization

These two goals provide complementary requirements:
- Physics performance studies require many millions of events
- Efficient use of CPU is important

Design requires lesser data sample, but accurate emulation To achieve both, the FTK simulation mimics the hardware:
- All the internal steps are reproduced with the possibility to change all internal parameters to evaluate carefully the impact of firmware or boards’ designs
- Detector hits can be read from MC events or from real data

Conclusions and next steps:
- The use of custom hardware based on AM ASiCs and FPGAs provides unprecedented computing power for the trigger system
- FTK simulation emerged as a foundation to support the use of FTK hardware
- Dozens of samples totaling 9.6 M of fully simulated events were produced
- The next production of a multi-million event sample is under preparation.

References: