L1Track: A fast Level 1 track trigger for the ATLAS high luminosity upgrade

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1. Introduction

The Large Hadron Collider [1] upgrade program [2] foresees two major long shutdowns (LS2 and LS3) allowing detector and machine upgrades. These are interspersed between collision periods for physics (Run II–IV). The high-luminosity phase corresponds to Run IV and requires such an extensive upgrade program to be considered in many respects a new project: significant R&D activities are under way to maximally exploit this phase. The high-luminosity upgrade will start after 2022 with the aim of reaching a peak instantaneous luminosity between $5 \times 10^{34}$ Hz/cm$^2$ and $7.5 \times 10^{34}$ Hz/cm$^2$: ATLAS aims at integrating $\geq 3$ ab$^{-1}$ in this phase. As of today, a full picture of the achievable analyses in this regime cannot be drawn, but the aim of this upgrade definitely includes ATLAS accessing large fraction of the SUSY phase space [3] and the expansion of its Higgs physics reach [4] and precision measurements of the Higgs and top-quark sectors. ATLAS will be facing challenging conditions: event pile-up is expected to increase to the level of $< \mu > \approx 200$. Because of such conditions and in order to prepare for the unforeseen, the design of the ATLAS trigger system [2] aims to implement sufficient redundancy to be robust and flexible. The trigger primitives relevant to the 3 ab$^{-1}$ physics program are hard to predict but will most likely focus on objects with masses in proximity to the electroweak scale. In order to gain full trigger efficiency at those scales, it is imperative to have the ability to identify and select events with leptons at momenta of the order of 10 GeV. The L1Track project will implement hardware-based charged track reconstruction to obtain 5× background reduction for single leptons through track matching. With a target of 95% efficiency, this will provide a flexible key instrument for rate control at early trigger stages. In order to attain this efficiency, tracks must be reconstructed with high-efficiency for $p_T \geq 4$ GeV.

2. L1Track in the context of the ATLAS upgrade program

The ATLAS trigger and data acquisition system processes data from the detectors front-end electronics and proceeds in two major stages. These correspond to the hardware (Level 1) and software (HLT: High Level Trigger) steps of its trigger path. Upon event acceptance, Level 1 primitives are communicated to the HLT as Regions of Interest (RoI): geometrical sub-regions of the ATLAS detector that can be identified, readout and processed by the early HLT stages. In parallel with the trigger decision stages, data are readout, merged and built into a single event and output to permanent storage.

The upgrade of the ATLAS TDAQ system [5,2] will happen incrementally through the LHC upgrade phases, evolving into a much higher performance system by the end of Phase 2 (LS3). The just concluded Phase 0 (LS1) [6,7] has been characterised by the merging of the two HLT stages into a single entity, the inclusion of topological capabilities in the Level 1 trigger hardware and the improved pile-up suppression of the Level 1 calorimetric trigger hardware. In Phase 1 (2018–2019, LS2), this suppression will be further enhanced by refining the calorimeter readout granularity at trigger level, thus improving the clustering algorithm [8]. The
ATLAS muon trigger system is also being progressively enhanced: in Phase 0 the extended barrel muon (1.0 ≤ |η| ≤ 1.3) trigger fake rejection has been improved thanks to the coincidence with muon identification in the hadronic calorimeter. Phase 2 upgrades will emphasise further the reduction of fake rates and improvement of detector resolution to maintain physics efficiency and maximise background rejection. The ATLAS inner tracker [9,10] will be completely replaced with a lighter detector (ITk) extending to higher rapidities. It will be a full silicon-based device to allow the high-precision interception of charged tracks in at least 14 points. The innermost layers will be based on approximately 638 × 10^6 pixels of 25 × 150 μm^2 and 50 × 250 μm^2 (compared to the current 80 × 10^6 pixels of 50 × 400 μm^2). The outer ITk layers will be made of double-sided silicon strip detectors with 74.5 μm spaced strips (at 40 mrad stereo angle), ranging in length from 2.45 cm to 4.9 cm, for a total of ~74 × 10^6 strips. The ITk will be readout at 1 MHz rate. The same RoI approach already introduced in the ATLAS trigger system provides a potential reduction to the amount of information to be processed from the ITk layers: if fast trigger primitives can be identified early enough, these can be used to seed the readout of specific ITk regions at high rate. A first decision can then be taken with this reduced information, allowing the full-ITk readout to be delayed till a later trigger stage. This approach would effectively introduce a new trigger level (Level 0).

The option of a Level 0 readout would split the ATLAS hardware trigger in two stages (Level 0 and Level 1): the Phase 1 decision system will be fed by a new Level 0 decision based on fast calorimetric and muonic primitives. These will identify Level 0 Rols for regional track identification in time for Level 1 decision. The Level 1 Track system will have to fit in ±24 μs total decision latency (L0 accept to Level 1 accept), subdivided in 6 μs for regional ITk readout requests (RRR or R3), 12–15 μs for track identification and reconstruction, and 3–6 μs for data propagation and global Level 1 decision. Current studies are aimed at determining the feasibility and architecture needed to fulfill these constraints.

### 2.1. ITk readout latencies and off-detector processing

The strip tracker readout is based on the ABC130 ASIC, where a double-buffer architecture has been implemented to reflect the two hardware trigger levels. Upon L0 acceptance an RoI map identifies subsets of data from the Level 1 buffer which are readout prior to Level 1 acceptance. Depending on the detector straw size and geometry, multiple ABC130 are linked to a Hybrid Chip Controller (HCC) in a star topology. Detailed simulations [11] (Fig. 1) have shown that through prioritisation of the R3 readouts with respect to Level 1 accept data and the use of a star topology (rather than daisy-chain), even the most occupied ITk strip regions can provide R3 data for 10% of L0 accepts well within 6 μs.

Studies have been performed so far mostly on the implementation of track finding and fitting based on the architecture and ASIC strategy of the Fast TracK project [12]: pattern recognition is based on associative memories, with each location corresponding to a coarse resolution pattern of superstrips (coarser bins of strips) on the ITk layers. Tracks are then fitted with a linear FPGA-based algorithm. The number of associative memory locations needed has been studied by simulating O(100M) single muons in a volume corresponding to about 1/800th of ITK. Preliminary studies based on the use of the strip detector information alone show that O(10^5) patterns is needed for full ITk coverage (requiring 10 ATCA shelves based on FTK hardware projections). Many more details (use of pixel layers, detailed hardware design) are under study and will be defined in the coming months.

### 3. Conclusions

HL-LHC will require a significant redesign of the ATLAS detector and TDAQ system, with improved rejection at early trigger stages to cope with the harsh pile-up conditions. L1Track will provide an essential contribution to this rejection through hardware based track reconstruction. The ATLAS constraints of L1A ≤ 400 kHz and Level 1 Latency ≤ 30 μs make the Level 0/1 approach optimal and the use of RoI-based L1Track possible. The possibility of full Pixel detector readout at 1 MHz would add flexibility, but has not yet been studied. An ITk readout latency of 6 μs seems achievable, and first pattern recognition results, using Strips only, indicate that the FTK concept would work well also for L1Track at the HL-LHC.

### References


**Fig. 1.** Distribution of the simulated full ITk readout latency (colours and numerical values in the plot, in μs) across the ITk strip detector geometry for 1 MHz L0-accept rate [11]. After the optimisation of FIFO sizes, R3 prioritisation and readout topology, all latencies are well below the 20 μs budget for the projected Level 1 rate, and suggest that even full rather than regional processing could be implemented in L1Track. Latency is measured at the 99th percentile in arrival time.