

Optimization of transistor size and operating point for the LVDS driver of the ALICE ITS pixel chip

Author: Solveig Marie Froeen

Supervisors: Thanushan Kugathasan, Walter Snoeys

The ALICE Inner Tracker System (ITS) will be upgraded during Long Shutdown 2. The tracker layers will be equipped with monolithic pixel sensors chips. A Low Voltage Differential Signalling (LVDS) driver is required for the off chip data transmission. A current mode 1.2 Gb/s LVDS driver based on H-bridge scheme has already been implemented and tested. Although the present driver meets the specifications, a decrease of its power consumption is beneficial for the reduction of the material required for the detector powering and cooling.

This report presents the study of a current mode LVDS driver based on H-bridge scheme where the switches are replaced with current sources that can deliver either ON level or OFF level currents. The ON current is the main static power contributor, and its value is set to 4 mA by specifications to have a differential signal of 400 mV over the 100 Ω termination resistor. The second contributor for the static power is the OFF power, which has to be optimized together with the dynamic power. Detailed simulations of the transistor current-voltage characteristics for different transistor sizes are done to find the minimum for the sum of the dynamic and OFF power consumption. From this study transistor sizes and operating voltages are defined for the proposed LVDS driver design.

Low Voltage Differential Signalling Driver specifications

The requirement for the LVDS driver is to transmit a differential signal of 400 mV across a termination resistor of 100 Ω , with a common mode voltage of 1.1 V relative to ground. The differential signal requirement of 400 mV is to allow the receiver to distinguish the signal from the noise.

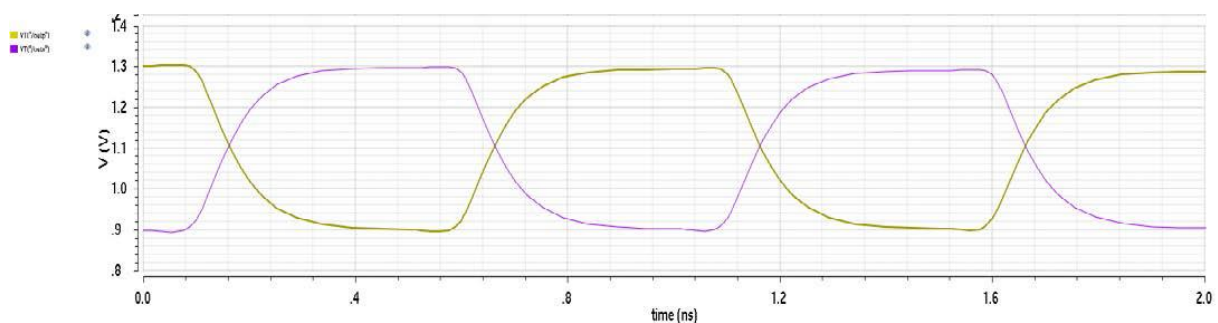


Figure 1 LVDS output signals

Figure 1 shows the differential outputs: V_{OUT+} and V_{OUT-} . The values are reported in Table 2.

The common mode is the mean of the output signals:

$$V_{CM} = \frac{V_{OUT+} + V_{OUT-}}{2}$$

The differential signal is the difference of the output signals:

$$V_d = V_{OUT+} - V_{OUT-}$$

Description of the current design

The driver (Figure 2) is implemented in current mode where the static current is fixed. Four transistors in H-bridge configuration define the direction of the current through the termination resistor (I_R). The value of I_R is set to 4 mA to meet the requirements. The circuit power supplies are $V_{dd} = 1.8$ V and $V_{ss} = 0$ V. Defining I_S as the static current from V_{dd} to V_{ss} , the static power of the driver is:

$$P_{ON} = I_S \cdot V_{dd}$$

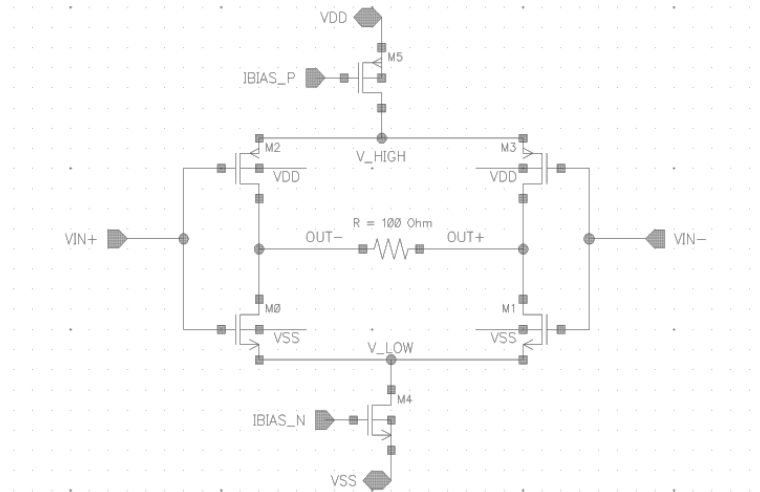


Figure 2 Present LVDS driver

The transistors of the H-bridge (M0, M1, M2, M3) work as switches. Depending on the voltage difference between the gate and the source (V_{gs}), the transistor can be either turned OFF or ON (see Table 1).

The driver has a differential input, with active high (V_{IN+}) and active low (V_{IN-}) signals. The input signals voltage levels are V_{dd} and V_{ss} . V_{IN+} is connected to the gates of M0 and M2, V_{IN-} is connected to the gates of M1 and M3. Internally, M2 and M3 sources are connected to $V_{HIGH} = V_{dd} - V_{sd,M5}$, M0 and M1 sources are connected to $V_{LOW} = V_{ss} + V_{ds,M4}$.

For $V_{IN+} = V_{dd}$ and $V_{IN-} = V_{ss}$ we have $V_{gsM2} \approx 0$, $V_{gsM1} \approx 0$, $V_{gsM3} \approx V_{dd}$, $V_{gsM0} \approx V_{dd}$. Therefore M2 and M1 are OFF, and the current flows through M3, to the termination resistor and down M0. When we invert the input voltage levels the current flows through M2, the opposite way through the termination resistor and down M1.

In the present design the driver static current is defined by two current sources (M5 and M4). The circuit current is fixed by M4, a feedback system sets M5 current to keep the common mode at 1.1V.

M4 and M5 are operating in saturation region, thus reducing the voltage margin needed to keep the H-bridge transistors in saturation region as well. Therefore the four transistors M0, M1, M2 and M3 are working in the triode region.

Transistor operation in triode region vs saturation region

Figure 3 shows the transistor current as a function of V_{ds} for different V_{gs} values. To be in the saturation region we need the source-drain voltage (V_{ds}) to be larger than the saturation voltage (V_{dsat}): the point where V_{ds} go from having a strong influence on I_{ds} to have a weak influence on I_{ds} .

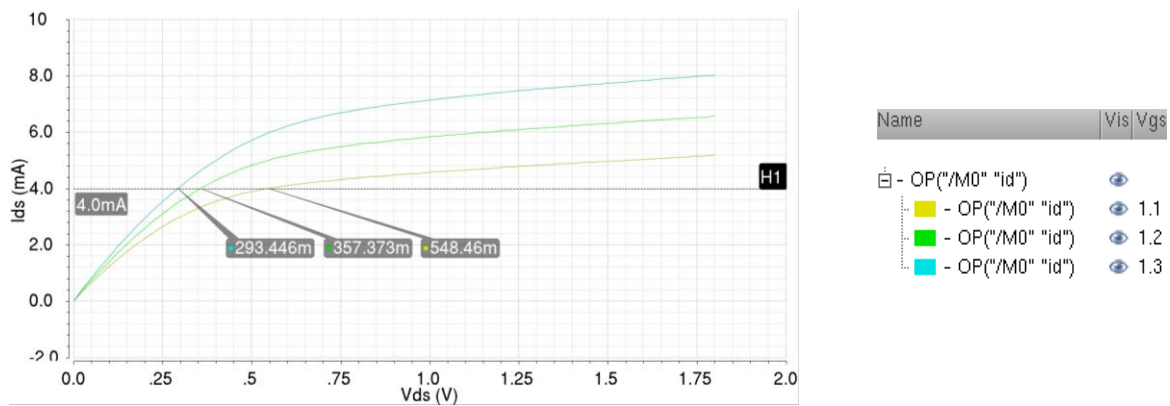


Figure 3 I_{ds} - V_{ds} curve for a NMOS transistor

Moving in to the saturation region (eg. from $V_{ds} = 293$ mV to 548 mV) it is possible to have a larger current with a smaller V_{gs} . The dynamic power is given by $P_d = C_{ox} \cdot L \cdot f \cdot W \cdot \Delta V^2$. Where f is the switching frequency, C_{ox} is the transistor gate capacitance per unit area, L and W are the transistor length and width, and ΔV is the voltage difference between the ON state and OFF states. Therefore, working in saturation region reduces the dynamic power.

Changes in the proposed design

To have more margin to get the H-bridge transistors in saturation region we remove the two transistors working as current sources. Instead we use the H-bridge transistors as current sources. The proposed LVDS driver is shown in Figure 4. In this case M2 and M3 sources are connected to V_{dd} , M0 and M1 sources are connected to V_{ss} . The gate voltages of these transistors have to be set in order to source either I_{ON} or I_{OFF} current (see Table 1).

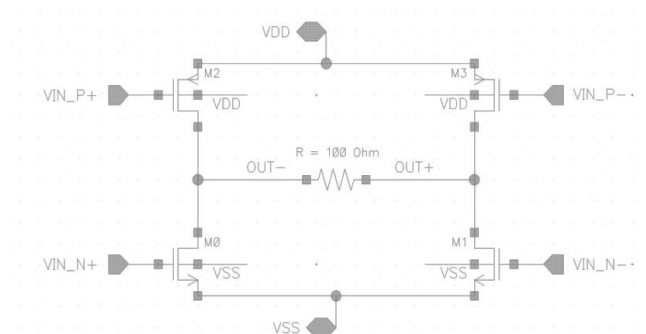


Figure 4 Proposed LVDS driver

Switch (present circuit)			Current source switch (proposed circuit)		
	ON	OFF		ON	OFF
R of the transistor	0	∞	I through the transistor	I_{ON}	I_{OFF}

Table 1 Transistor parameters as a switch and as a current source.

In this configuration we cannot enter the same input voltage for the PMOS transistors (M2 and M3) and the NMOS transistors (M0 and M1) because we have to ensure a current flow of 4 mA. I have been working on optimizing the power consumption of the transistors for these specifications.

	VIN+ [V]		VIN- [V]		OUT logic level	VOUT- [V]	VOUT+ [V]
Present LVDS	0		1.8		0	1.3	0.9
	1.8		0		1	0.9	1.3
Proposed LVDS	VIN_P+	VIN_N+	VIN_P-	VIN_N-			
	VON_P	VOFF_N	VOFF_P	VON_N	0	1.3	0.9
	VOFF_P	VON_N	VON_P	VOFF_N	1	0.9	1.3

Table 2 LVDS logic and voltage levels

Total power consumption analyses

The total power consumption has three contributions: dynamic power, OFF power and ON power: $P_{\text{total}} = P_d + P_{\text{OFF}} + P_{\text{ON}}$

$$= f \cdot C_{\text{ox}} \cdot L \cdot W \cdot \Delta V^2 + I_{\text{OFF}} \cdot (V_{\text{dd}} - V_{\text{ss}}) + I_{\text{ON}} \cdot (V_{\text{dd}} - V_{\text{ss}}) \quad (\text{in our case } V_{\text{ss}} = 0)$$

$$= f \cdot C_{\text{ox}} \cdot L \cdot W \cdot \Delta V^2 + (I_{\text{OFF}} + I_{\text{ON}}) \cdot V_{\text{dd}}$$

The requirement is to have the current through the termination resistor $I_R = I_{\text{ON}} - I_{\text{OFF}} = 4 \text{ mA}$. Assuming to have $I_{\text{ON}} \gg I_{\text{OFF}}$, this translates to $I_{\text{ON}} = 4 \text{ mA}$. Therefore P_{total} has to be reduced by minimizing $P_d + P_{\text{OFF}}$. The optimization is done for $f = 1 \text{ GHz}$. C_{ox} is a technology constant. The transistor length is set to $L = 0.18 \mu\text{m}$ (minimum) to increase the current capability (W/L) and minimize P_d . Therefore the free parameters are W , ΔV^2 and I_{OFF} .

Parameter optimization

Figure 5 shows the current as a function of V_{gs} , for a NMOS in saturation region. From this graph it is possible to define V_{OFF} as the V_{gs} for I_{OFF} and V_{ON} as the V_{gs} for I_{ON} .

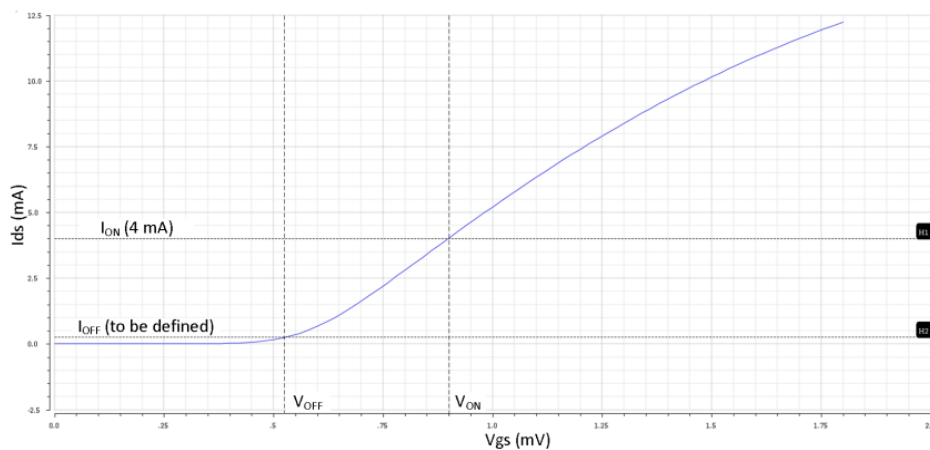


Figure 5 NMOS current as a function of V_{gs} , in saturation region

Figure 6 shows the NMOS current as a function of V_{gs} for different W values. Larger is W smaller is the V_{gs} required to have $I_{\text{ON}} = 4 \text{ mA}$. To optimise the power consumption we need to find a trade off between the width and $\Delta V = V_{\text{ON}} - V_{\text{OFF}}$.

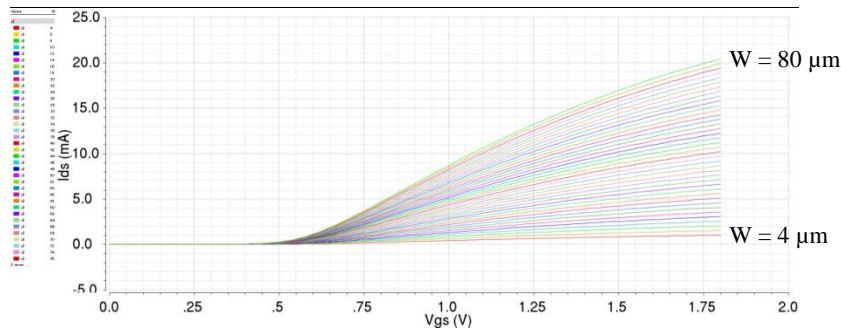


Figure 6 NMOS current as a function of V_{gs} for $W = 4 \mu\text{m}$ to $W = 80 \mu\text{m}$

Figure 7 shows how $W\Delta V^2$, which is proportional to the dynamic power, evolves with W for different I_{OFF} . Each curve has a minimum, therefore it is possible to find a W that minimises the dynamic power for a given I_{OFF} .

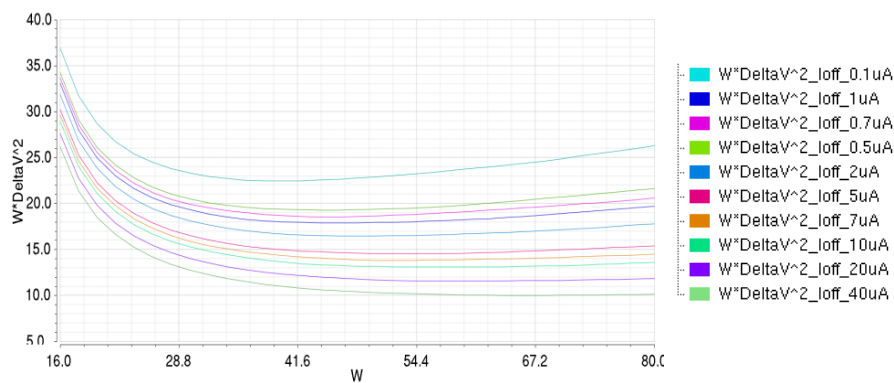


Figure 7 $W\Delta V^2$ as a function of W for different I_{OFF} currents

Table 3 summarises the simulation results to get the W , V_{ON} and V_{OFF} that minimises $P_d + P_{OFF}$ for a PMOS transistor. The optimisation of the NMOS transistor is done in similar way. The minimum for $P_d + P_{OFF}$ is $51.99 \mu\text{W}$, $P_{ON} = 7.2 \text{ mW}$, the total circuit power consumption is $P_{total} = P_d + P_{OFF} + P_{ON} = 7.252 \text{ mW}$.

I_{ON} [mA]	I_{OFF} [μA]	V_{OFF} [V]	V_{ON} [V]	W [μm]	P_{OFF} [μW]	$W\Delta V^2$ [μmV ²]	P_d [μW]	$P_d + P_{OFF}$ [μW]
4	0.5	0.30	1.16	52	0.9	38.87	55.98	56.88
4	0.7	0.31	1.14	54	1.26	37.64	54.21	55.47
4	1.0	0.32	1.13	56	1.8	36.24	52.18	53.98
4	2.0	0.35	1.11	58	3.6	33.61	48.39	51.99
4	5.0	0.39	1.08	62	9.0	30.01	43.21	52.21
4	7.0	0.40	1.06	66	12.6	28.62	41.21	53.81
4	10.0	0.42	1.06	66	18.0	27.14	39.09	57.09

Table 3 Total power consumption calculation.

References

- Texas Instruments, September 2002, “Interface Circuits for TIA/EIA-644 (LVDS)” Technical description of the LVDS standard. Our specifications are slightly different. <http://www.ti.com/lit/an/slla038b/slla038b.pdf>
- The ALICE Collaboration, “Technical Design Report for the Upgrade of the ALICE Inner Tracking System”, 2014 J. Phys. G: Nucl. Part. Phys. 41 [doi:10.1088/0954-3899/41/8/087002](https://doi.org/10.1088/0954-3899/41/8/087002)