Architecture of the upgraded BCM1F Backend Electronics for Beam Conditions and Luminosity measurement - hardware and firmware

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Abstract

The Beam Radiation Instrumentation and Luminosity Project of the CMS experiment, consists of several beam monitoring systems. One system, the upgraded Fast Beams Condition Monitor, is based on 24 single crystal CVD diamonds with a double-pad sensor metallization and a custom designed readout. Signals for real time monitoring are transmitted to the counting room, where they are received and processed by new back-end electronics designed to extract information on LHC collision, beam induced background and activation products. The Slow Control Driver is designed for the front-end electronics configuration and control. The system architecture and the upgrade status will be presented.

The Fast Beam Contition Monitor BCM1F Backend Electronics upgraded, MicroTCA based architecture

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ABSTRACT
The Beam Radiation Instrumentation and Luminosity Project of the CMS experiment, consists of several beam monitoring systems. One system, the upgraded Fast Beams Condition Monitor, is based on 24 single crystal CVD diamonds with a double-pad sensor metallization and a custom designed readout. Signals for real time monitoring are transmitted to the counting room, where they are received and processed by new back-end electronics designed to extract information on LHC collision, beam induced background and activation products. The Slow Control Driver is designed for the front-end electronics configuration and control. The system architecture and the upgrade status will be presented.

Keywords: CMS, BCM1F, Beam Condition Monitor, Luminosity

1. INTRODUCTION
The Large Hadron Collider (LHC)\textsuperscript{1} is a 27 km circumference circular accelerator located at CERN (Geneva, Switzerland). Up until 2013 it has collided beams of protons and lead ions at center of mass energies up to 8 TeV (2.76 TeV per nucleon pair for lead ions) with a peak instantaneous luminosity near $5 \times 10^{33}$ cm\textsuperscript{-2}s\textsuperscript{-1}. For Run II the instantaneous luminosity is foreseen to increase from the previous maximum of $7 \times 10^{33}$ cm\textsuperscript{-2}s\textsuperscript{-1} to around $2 \times 10^{34}$ cm\textsuperscript{-2}s\textsuperscript{-1}. See Ref.\textsuperscript{2}. The Compact Muon Solenoid (CMS)\textsuperscript{3} detector is one of four large detectors situated around the LHC and one of two general-purpose detectors.

Reliable online monitoring of the LHC beam quality in the CMS cavern is important for safe operation of the CMS inner detectors and for optimizing the data taking quality for the experiment. Two essential components are used to assess the quality; the first is measurement of the machine induced background (MIB) particles inside the CMS tracker volume and the second is the luminosity. A measurement of the MIB particles in CMS is essential to determine whether the beam conditions are sufficiently good to switch on the HV of the CMS inner tracking detectors. This measurement needs to be online whenever there is beam in the LHC machine, published in real-time, reliable and sensitive to MIB particles in the presence of a dominating particle flux from collision products at high luminosity, in order to provide a feedback to the tracker control system in real-time. A measurement of the relative online bunch-by-bunch luminosity is needed to optimize the collision rate, thereby maximizing the physics potential to the experiment. A precise measurement of the absolute delivered luminosity by the LHC is important to benchmark the quality of the LHC machine parameters and is used to calculate the dose delivered to various parts of the CMS detector. What is most important is an accurate measurement of the absolute recorded luminosity which is necessary to fully exploit the physics discovery potential of the CMS experiment by allowing accurate normalization measurements of the physics cross sections and hence couplings of the bosons to elementary particles.

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2. ARCHITECTURE OF THE UPGRADED FAST BEAM CONDITION MONITOR

2.1 The Fast Beam Condition Monitor upgrade

The previously installed Fast Beam Conditions Monitor (BCM1F) was successfully operating from 2008 to 2013. Information from 8 diamond sensors had been collected bunch-by-bunch and processed in real time by back-end electronics. BCM1F is able to diagnose fast adverse beam conditions, such as beam losses, that could be harmful for the detector components. The LHC upgrade has several implications for the BCM1F system. During Run I the characteristic instantaneous luminosity ($5 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}$) corresponded to a hit rate of $3.7 \times 10^{6} \text{s}^{-1}$ per sensor ($1.5 \times 10^{7} \text{ cm}^{-2} \text{s}^{-1}$) and a sensor occupancy of 12% as measured. For Run II the instantaneous luminosity is foreseen to increase from the previous maximum of $7 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}$ to around $2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$, corresponding to $7.5 \times 10^{6} \text{s}^{-1}$ per sensor ($3 \times 10^{7} \text{ cm}^{-2} \text{s}^{-1}$) and a sensor occupancy of about $\sim 25\%$.

The upgraded BCM1F detector is one of the monitoring systems of the Beam Radiation Instrumentation and Luminosity Project (BRIL) in the CMS inner detector region. The detector was designed to monitor the flux of particles with a time resolution of a nanosecond. The BCM1F upgrade detector will be mounted inside the pixel volume and will consist of 24 sCVD diamond split sensors that are currently tested to fulfill the requirements of size, of nanosecond time resolution for a fast response, and of radiation hardness. The $5 \text{ mm} \times 5 \text{ mm} \times 0.4 \text{ mm}$ diamond sensors will be mounted $\sim 5 \text{ cm}$ radially from the beam line on two parallel planes located on both sides and 1.83 m away from the CMS interaction point, which is an optimal location for separation of incoming and outgoing particles. Each diamond will be split into two channels by means of a split metallization. It decreases the hit probability of a single sensor, enhancing linearity of the system for high rates. It also makes it more likely that at least one sensor will register a beam halo hits at the incoming beam. The diamonds will be mounted to a new fast transimpedance driver/amplifier, with a peaking time 7 ns and a pulse full width at half maximum (FWHM) of about 8 ns, coupled to an optical driver/amplifier. The radiation-resistant front-end ASIC was developed by AGH in Krakow and is tested in DESY Hamburg electron beam. A newly designed carbon-fiber carriage will hold the PCB carrying the sensors as well as the front-end electronics. Analog signals from the Frontend Electronics will be transmitted to 4 Opto Mother Boards and converted to the optical signals. Fibers will lead signals to the counting room that is placed 80 m from the experimental cavern. Four 4-channels optical receivers of 100 MHz bandwidth will convert them back to analog, then processed by back-end electronics.

The VME based electronics of the previous system is being enhanced to provide a realtime histogramming unit of a resolution 6 ns/bin for initial LHC running. The newly designed MicroTCA based electronics will overtake its function as its reliability will be proven. The new back-end will provide the realtime monitoring of the flux and timing of charged particles originating from the proton-proton collisions and MIB particles. The measurement results will be presented in histograms that will be collected during each run as well as in time when CMS will not collect data. Some amount of a raw data will be collected and sent to the BRIL DAQ for offline analysis. The system will also be in charge of front-end configuration as well as a Beam Pick-up Timing for Experiments (BPTX) signals measurements.

2.2 Requirements for the analog to digital conversion

Two architectures based on different system components are being considered. The main assumption is the possibility to measure peaks of an incoming hit rate 302 MHz for a beam pile-up 50. Overlapping peaks with minimum double hits resolution of 12.5 ns has to be recognised. Digitisation of a peak versus resolution settings was tested as shown in Fig. 1. Values of time and amplitude measurement errors were estimated for the simple peak finding algorithm that does not introduce any noise reduction methods. The digitiser that fits the requirements is FMC125 from 4DSP. It has 4 channels which can work in a 5/2.5/1.25 GS/s sampling rate. Dependably on a type of a FMC connector mounted on a carrier High-pin count (HPC) or Low-pin count (LPC), all 4 channels can be used or only 2 in a latter case. In the second case the mezzanine can be replaced with its 2-channel substitute FMC122 except from the BPTX signal measurement, where the 5 GS/s of the sampling rate will be required. For this purpose a single channel mode of FMC125 can be used, while for the real-time signal measurement the board can be configured into 2 or 4-channel mode. The mezzanine is being tested with CMS GLIB and FC7.
carriers. The board has an internal input AC coupling that limits the bandwidth. Several values of a transformer are being tested for achieving the best result.

2.3 Architecture of the upgraded MicroTCA based BCM1F

The most probable architecture of the system will be based on MicroTCA FMC carriers designed for CMS according to the CMS MicroTCA crate specification. The currently available GLIB boards are being used for the system development, although the board has several limitations and may be replaced by FC7 boards that are designed for CMS. The architecture based on the FC7 with the data flow directions is presented in Fig. 2.

Analog data from 48 detector channels will be digitized by 1.25 GS/s ADC converters of the FMC125 mezzanines mounted on the carriers. Sampling clocks will be synchronized to 40 MHz LHC clock that will be provided through a front panel. Samples will be provided with half of the sampling speed in 8 bit pairs of samples to FPGAs on FMC carriers, where a data processing will be realised. Two types of histograms will be collected during a CMS Lumi Nibble ($2^{12}$ LHC orbits). A minimum 1 orbit of a raw data each Lumi Nibble will be stored to provide an input for the offline statistic processing. During the storage time, without introducing any dead time, a data from a previous Lumi Nibble will be transmitted to AMC13XG that is a specialised MicroTCA Hub (MCH2) designed for CMS. This upgraded AMC13 module provides TTC, DAQ and TTS services to modules installed in a MicroTCA crate. The module will distribute LHC clock that will be used by the BCM1F for synchronization purpose. A basic MicroTCA Hub will be used for a crate management and diagnostics. Data from AMC modules will be transmitted through a backplane and AMC13XG to an external server using 10 Gb IPBus protocol. A server will collect histograms from two MicroTCA crates and send to the BRIL DAQ. Depending on a carrier, one or two AMC modules will be used for BPTX signals measurement. The FMC125 will be configured in single channel, 5 GS/s operating mode and placed in a single or two neighbouring FMC slots. In 1 channel operating mode both LPC or HPC version of the FMC connector can be used, that allows using two GLIB carriers that have single HPC connectors available from the front side as well as a single FC7 carrier that has two LPC connectors. An additional carrier will be used for implementing a Slow Control Driver, that is described in section 4.1.

Several other architectures are considered. One of them is based on an AMC FMC carrier that is developed as a part of Open Hardware Repository (OHWR) project at Warsaw University of Technology. The board has 2 FMC connectors and functionally is similar to the FC7 project. It has many interesting features like compatibility to the White Rabbit synchronisation system developed at CERN that has never been tested in CMS. However, the board does not provide IPBus communication and CMS TTC signals automatic receiving. Except from
providing the given functionality, the BCM1F would like to keep coherent to the other CMS systems, that gives the highest priority to architectures based on modules designed for CMS that will be used by several systems e.g. CMS tracker.

### 3. DATA RATES AND HISTOGRAMS

The presented architecture is designed to process a data collected from the 48 detector channels. Data will be distributed between 12 carrier boards and sampled with a 1.25 GS/s rate. Samples will be transmitted to an FPGA mounted on a carrier board with half of this rate as 16-bit vectors. After buffering and first rough processing, will be processed with an amplitude and time measurement algorithm which is currently developed. The result amplitude value fixed in time in orbit and Lumi Nibble will be presented as two types of histograms: total number of counts in time and total number of counts in amplitude. A train of 50 samples will be marked with a time stamp. A minimal number of bits for providing the necessary timing information is 17 bits for position in orbit. Every 50th sample will be separated with 25 bits containing a data sample and a time stamp. The rest of the samples will be 8 bit or 10 bit for a higher version of the FMC mezzanine. The orbit number will be stored in a separate IPBus register and will not be transmitted with a fast data. In this way for 4 channels (single carrier) a data volume for 1 Lumi Nibble is 1560 kb, that gives a 4 Mb/s rate, a total data production in single microTCA crate (24 channels) is 9.3 Mb per Lumi Nibble and a 24 Mb/s rate. A time domain histogram will be collected during a Lumi Nibble. The time scale will start while the new orbit will be introduced and finish at 89.9 us. Information collected will provide data about an LHC data structure and, what is a unique for BCM1F, about a beam induced background and activation products. The data volume depends on a granularity that will be decided to use. 4-bins per bunch crossing that corresponds to the ability of a VME based system Real-time Histogramming Unit (RHU). For each carrier (4 channels) a data volume is 691 200 b and for a single chassis (24 channels) 4 147 200 b. For improved binning 8 bins/BX a data volume is: 1 382 400 b (4 channels) and 8 294 400 b (24 channels). In contradiction to the RAW data, histogram bins does not require a time stamp; bins will be transmitted continuously including empty bins.
An amplitude histogram will be also collected during a Lumi Nibble. The amplitude resolution will be 8 bits or eventually 10 bits. The base data volume estimation concerns 8 bit resolution. Simulation points that the maximum number of bits for counts is 22 bits. However, the precise number of counts for a noise is unknown and difficult to estimate. After the first runs, when the noise level will be measured, the histogram can be divided into 2 parts: first concerning the registered noise and hit counts and the latter, smallest concerning only hit counts. The results will be continuously monitored and a buffer will be increased if needed. Forseen data volume is 22528 b per board (4 channels) and 135168 b per chassis (24 channels). As mentioned before, bins will be transmitted sequentially.

The Tab. 1 presents the summarized data rates and volumes. An important feature is that we need to store double size of buffers for histogram, but only one of them will be transmitted via backplane during for the single Lumi Nibble. It is possible but not necessary to implement a backup buffer in case of loosing transmission.

<table>
<thead>
<tr>
<th>Data format</th>
<th>4 channels</th>
<th>24 channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw Data</td>
<td>1.560 Mb (4 Mb/s)</td>
<td>9.3 Mb (24 Mb/s)</td>
</tr>
<tr>
<td>Time domain histogram</td>
<td>1.382 Mb</td>
<td>8.294 Mb</td>
</tr>
<tr>
<td>Amplitude histogram</td>
<td>22.528 kb</td>
<td>135.168 kb</td>
</tr>
<tr>
<td>Histograms in total</td>
<td>2.8 Mb (3.8 Mb/s)</td>
<td>16.8 Mb (22.826 Mb/s)</td>
</tr>
<tr>
<td>In total</td>
<td>4.3 Mb (7.8 Mb/s)</td>
<td>25.97 Mb (46.826 Mb/s)</td>
</tr>
</tbody>
</table>

4. CONTROL AND DATA PROCESSING MODULES

4.1 Slow Control Driver

The Slow Control Driver (SCD) is designed for remote setting bias and gain of the linear laser drivers (LLD) of the Digital and Analog Opto Hybrids (D/AOH) being a part of the front-end and optical path. A simplified architecture of the module is presented in Fig. 3. Software is based on the CACTUS environment that was developed at CMS. The user connects to the server, runs a C++ script, then chooses the chip position on a board, bias or gain and the requested value. The software driver generates the command and sends it to the AMC Mother Board using an IPbus protocol. The SCD firmware implemented in the FPGA generates sends the configuration data to a Slow Hub. Data is transmitted through the optical path using SFP transceivers and Digital Opto Hybrid receiver. The EDA-02707-V1 board that was designed in CMS and 8 JDSU transceivers are used. The proper channel of the Slow Hub is activated. The inner part of the frame contains a configuration data coded in to the format acceptable by the Slow Hub. The Hub generates 625 kHz clock and decode data into an I2C message for an LLD mounted on a selected Analog Opto Hybrid mezzanine. One of four addressable registers can be chosen. Registers 0 to 3 allow the bias setting, whereas register 4 allows the gain setting for three channels. The implementation of the SCD contains multi-level state machines, that allows easy adaptation to the given hardware structure. E.g. testing boards that are used contain a Slow Hub Adapter, that needs an additional configuration. Ultimately, the SCD will communicate directly with the Slow Hub chip that is mounted on the C-shape board.

4.2 Data processing module

A very important part of the system that is being developed is a data processing module. Incoming data will be sampled by 1.25 GS/s ADCs on the FMC125 or optionally FMC122 mezzanine by 4DSP, mounted on a AMC FMC Carrier (AFC) FC7 (Xilinx Artix-7 200T FFG1156 FPGA). Limited resources, dead time free operation and a very high volume of a data will limit possibility of the complex algorithm implementation. The algorithm has to provide reliable amplitude and time measurement. Results will be collected in histograms and sent to

LN - Lumi Nibble, 2^{12} Orbits, 368.23 ms
the local BRIL DAQ. A small amount of RAW data called spy data will be transmitted to the server for offline processing and an efficiency measurement of the algorithm. Two simple algorithms are currently being analysed: a peak finding and a deconvolution. They are being tested with data measured in different conditions. The peak finding (PF) is the naive algorithm that can be easily implemented. It can provide fast peak recognising on the basis of several consecutive samples. The problem is to define the saturation state and the high sensitivity to noise of the algorithm. It is possible to distinguish between the overlapping samples with 6 ns spacing. However, the algorithm is very sensitive to noise and pulse saturation. Knowledge of the exact signal shape is not crucial. For extracting the highest sample and decreasing an influence of the noise filtering can be implemented. In hardware implementation, the incoming signal will be smooth by the optical receiver of a 100 MHz bandwidth. The deconvolution algorithm provides reliable information about a peak occurrence. The main difficulty is to find the mathematical model of the peak that is close enough to real signal shape. An overlapping pulse that can occur can have a significant influence on the result. Separation of these pulses is very important in terms of MIB hits rejection. This algorithm has a low resistance for anomalies such as saturated peaks or unknown noise character.

These and some other algorithms will be tested on the simulation with a mathematic model and measured pulses to assess the possibility of its usage for online and offline analysis. On the basis of these studies, the novel algorithm will be provided for a high reliable signal measurement particular for the designed system. The additional function of the algorithm that will be implemented is a baseline measurement that will be done during the last 50 ns of the abort gap and repeated every orbit. Averaged value $A_{ref}(\text{baseline})$ will be taken into account. There is a possibility of $A_{ref}(\text{dynamic})$ measurement during collisions. Amplitude of pulses $A_{adc}$ will be corrected with the value of baseline $A_{ref}(\text{baseline}) - A_{ref}(\text{dynamic})$ as shown in Fig. 4.
5. SUMMARY

The Beam Condition Monitoring (BCM1F) system is a part of the CMS Beam Condition Radiation and Luminosity Project (BRIL). The detector that had been successfully operated after the installation in 2008 to the shutdown in 2013. Currently the detector is being developed following the upgrade of LHC to a collision energy of up to 14 TeV, higher luminosity and 25 ns bunch spacing after 2015. The main challenge for the BCM1F is to provide the realiable measurement of the Machine Induced Background (MIB) inside the CMS tracker volume and the second is the luminosity measurement. The newly designed front-end consist on 24 single crystal CVD diamond sensors positioned at a distance of $\pm 1.8\,m$ from the interaction point, divided into 48 channels. The amplyfing and shaping ASIC provided for this purpose is able to produce the pulse of a different amplitude and about 8 ns FWHM, constant for a different hit energies. The BCM1F back-end electronics are designed to receive signals from the front-end electronics via 48 optical channels. Two separated architectures with different capabilities are being developed in parallel. The first VME based is an upgraded architecture of the previously working system. It will be the base system until the reliability of the newly designed system will be confirmed. The second MicroTCA based system is being developed to improve the time and amplitude measurement resolution. Architecture of the system follows CMS recommendation and introduces some custom solutions that will allow fast signals measurement and accurate luminosity measurement. The data processing algorithm is being designed to be able to recognize signals from the detectors with a minimum spacing of less than 12 ns. That value corresponds to the maximum overlap of two pulses that can be recognized as separate by the ASIC. The methods of the amplitude and time measurement are tested with the use of the real signals as well as with the use of a mathematic model. In the real system 1.25 GS/s of the incoming data from 4 channels must be analyzed without introducing any dead time. The possibility of implementation of the algorithm is limited by the available FPGA resources. The histogramming modules and buffers for raw data will be implemented in the block RAM of the FPGA, hence the more complex algorithms can be used only for offline analysis. The system elements are being tested for system compatibility and a possibility of usage in the real system. The algorithm for peak recognition is developed on the basis of previous BCM1F experience and current front-end measurements and simulations. The basic functionality will be provided before 2015, system firmware and software will be developed according to the first commissionning results.

Figure 4. Architecture and the data flow in the upgraded MicroTCA based BCM1F system

\[ A_{max} = A_{adc} - [A_{ref}(baseline) - A_{ref}(dynamic)] \]
REFERENCES


