Pixel detector:
4 Layer precision tracking detector with a resolution of ~10 μm in Φ coordinates and ~115 μm in z. Total of 2024 Modules for a grand total of 92 Million pixels.

Upgrade actions & motivation:
Readout bandwidth saturation is foreseen for Layer 2 in 2016 and Layer 1 from 2017 onwards given the expected luminosity.
- Replaced Pixel ROD/BOC by IBL cards while doubling the bandwidth.
- Profit from IBL operational experience from 2015 using same core firmware and software.
- Same IBL hardware, except the new receiver plugins (Rx) that had to be re-designed.
- IBL software features offer more flexibility for operation and recovery.

Rx Plugins:
- Working with non return to zero signals up to 160 MHz.
- Operation for L2 and L1 possible at 40 or 80MHz.
- SNAP 12 based plugin.
- Threshold adjustment on per channel basis.
- Excellent operating range as can be seen on Figure 1.
- Aging test at 80°C 80% relative humidity showed a life expectancy of more than 10 years under normal condition of 25°C and 20% relative humidity.

Installation done:
- Re-placement of new hardware was completed in January.
- Total of two crates, 32 couples BOC/ROD
- Commissioning the new hardware with the detector was completed and satisfactory.
- All testing performed showed no errors in the recabling procedure.
- New FTK Fibers routing allowing for more flexibility in case of intervention.
- Layer 1 upgrade should take place at the end of 2016.

Pixel DAQ:
The pixel modules ship back data optically via "optoboards". The Back-Of-Crate (BOC) receive and convert signals for the Read-Out-Driver (ROD). The ROD is the main board, taking care of: data formatting and monitoring, issuing host command and create and send Front-Ends commands. The Fit Server takes care of calibration data processing. A Single Board Computer (SBC) controls the ROD-BOC cards. The Time, trigger and control (TTC) provides through TTC Interface Module (TIM) triggers to ship data back to the higher level read-out (ROS).

Pixel Software:
- Run Controller coordinate all concurrent processes.
- Actions are started by the host and handled by Action Servers on the Single Board Computer (SBC).
- Processes threatened in parallel via Inter Process Communication(IPC).
- The coordination via VME is handled by the Crate Broker.
- Adjustments needed to accommodate the differences between the different readout procedures for the different Front-Ends of the Pixel Detector.